DIGITAL NOISE EMULATOR FOR CHARACTERIZATION OF PHASE-LOCKED-LOOP SYSTEMS EXPOSED TO SUBSTRATE NOISE

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Abstract

There are more and more System-on-a-Chip (SoC) products available these days. However, in SoC applications it is always a challenge to integrate sensitive components with noisy digital blocks on the same chip. The results of our research indicate there are several digital parameters significant to substrate crosstalk. Based on the study, we propose a digital block to characterize analog blocks, and use a synthesized PLL as the test vehicle to verify the proposal.

This research first reviews measurements from an IEEE 802.11a wireless LAN base-band/MAC processor. Results confirm that there are dominant components of digital switching noise spectra, predetermined by the architecture. Based on this observation and supporting work at Stanford, a new low-complexity Digital Noise Emulator (DNE) is presented which emulates global digital signatures of complicated digital systems. The DNE can generate both deterministic and random signals, and inject different amounts of digital noise into the substrate for further studies.

The work also covers measurement results from a test chip including a DNE and ring-oscillator based PLL. The DNE test-chip was fabricated using a TSMC 0.18μm CL018G technology. Measurement results reveal that there are several digital parameters, including phase and frequency, important to PLL performance. By properly controlling the phase of digital inputs with respect to the PLL reference clock, improvements up to 71% reduction in jitter standard deviation from the worst case relative to best case can be observed. In addition, the measurement data at representative DNE operating frequencies are presented. Experiment results also confirm that deterministic and random noise will have different impact on performance.

Finally, it is demonstrated that the DNE can be used for noise cancellation to improve system performance. By activating a DNE, an impact to the target PLL caused by a second noise source is minimized. A 50% reduction in jitter standard deviation was obtained in the case of canceling deterministic noise.

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Chapter 1

Introduction

1.1 System-on-a-Chip (SoC)

As the semiconductor industry has grown over the past three decades, scaling in transistor size is driven by the goal of providing better device performance at lower production cost. As predicted in the 2003 International Technology Roadmap for Semiconductors (ITRS) [1], the physical gate length for low-power logic chips will decrease from 53 nm in year 2004 to 18 nm in year 2012, which implies more transistors can be fitted to a single chip. In the future, this increasing functionality on a single chip will embrace applications provided by multi-chip systems today.

1.1.1 Typical Communication Systems

To elaborate on some of the system integration issues implied by the evolution of SoC, a typical communication system [2] is shown in Figure 1-1. In practice, these systems are currently implemented by chipset solutions. When the system is operated in the receiving mode, the signal is first collected by the antenna, passed to a low noise amplifier (LNA) to detect the incoming signals on the selected channel, and down-converted by a mixer to its base-band frequency. The retrieved signal is then fed to an auto-gain-control (AGC) amplifier to adjust the signal amplitude, and then sent through an anti-alias filter (AA) to reject unwanted spectra. The output of the AA is converted from an analog waveform to a digital stream by an analog-digital converter (ADC). The

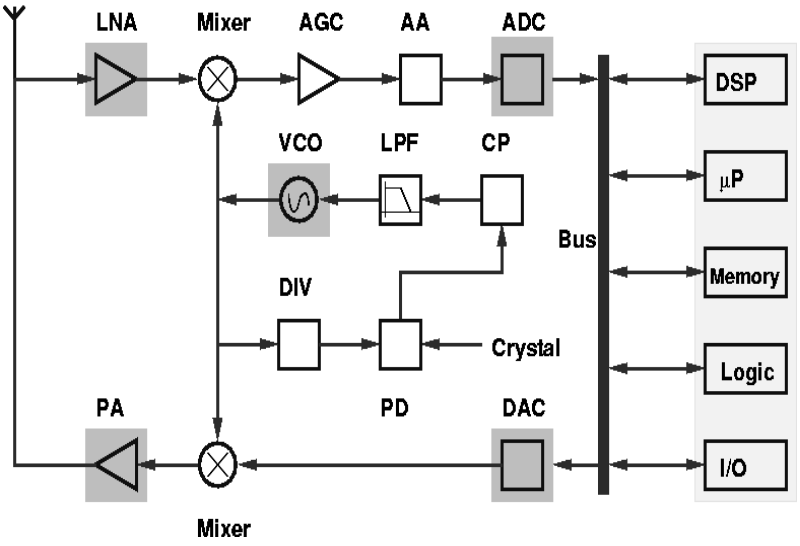


Figure 1-1 Block diagram of a typical communication system.

digital stream is dispatched accordingly to different digital blocks, including memory, logic blocks, I/Os, microprocessor (μP), and digital signal processing (DSP) core. The transmit (reverse) path of the system starts from the digital blocks. The digital stream is converted to an analog waveform using a digital-to-analog converter (DAC). The output of the DAC is up-converted to a signal at the radio frequency assigned by protocols. The power amplifier (PA) takes the signal and transmits the amplified signal out through the antenna. As a part of the system, a Phase-Locked-Loop (PLL) is connected to the two mixers to remove/insert carriers. The PLL consists of a voltage-controlled-oscillator (VCO), a divider (DIV), a phase detector (PD), a charge-pump (CP) and a low-pass-filter (LPF). The details of the PLL architecture will be reviewed in Chapter 3.

1.1.2 SoC Applications

The building blocks listed above are common in most communication systems. The concept of System-on-a-Chip (SoC) is to integrate these blocks on a single chip. The semiconductor industry works hard toward this goal, since SoC solutions hold promise in reducing the number of large output buffers, lengths of connections between chips, and cost of packaging and fabrication, which in turn leads to improved performance and

Company	Date	Application	PA	LNA	VCO	ADC DAC	µP DSP	Mem.
Alcatel	'01	Bluetooth	X	X	X	X	X	X
Lucent	'01	GSM CSP				X	X	
Alcatel	'01	GSM BTS			X	X	X	X
Conexant	'02	GSM/GPRS		X	X	X	X	
Atheros	'02	IEEE802.11a	X	X	X			
Atheros	'02	IEEE802.11a			X	X	X	
Toshiba	'03	IEEE802.11a			X	X	X	X
AMD	'03	IEEE802.11b	X	X	X	X		

Table 1-1 Recent SoC applications announced at ISSCC.

reduced cost. Of course, as technology evolves, higher operating frequencies, lower supply voltages, higher transistor density, and integration of different sub-systems on a single chip will complicate signal integrity issues because of cross-talk between the blocks. Since the driving force for technology innovation is primarily the cost, it is inevitably a trade-off between how many resources should be allocated in the design and how much benefit can be achieved in realizing SoC applications. This can explain why in many SoC applications sensitive analog blocks, such as PAs and LNAs, are not integrated.

To overcome this barrier, novel approaches to solve signal integrity problems are gaining attention as advocated in ITRS documents and research priorities [3] proposed by the Semiconductor Research Corporation (SRC). Therefore, characteristics of noise and efficient noise suppression techniques should be studied more extensively in order to support future high-performance SoC designs.

Table 1-1 shows representative SoC applications announced at the International Solid-State Circuit Conference (ISSCC) over the past three years [4-11]. As indicated in the table, the Bluetooth solution provided by Alcatel [4] has integrated most analog/mixed

signal blocks with DSP core and memory. For the Bluetooth specification, the PA performance is not as tightly constrained as for the other applications. However, in GSM and IEEE 802.11 cases, the RF and base-band digital blocks are usually implemented separately. There are reports (for example, [5][7]) mentioning that extra effort must be applied to avoid signal integrity issues when integrating sensitive analog/mixed-signal circuits with noisy digital systems. They confirm that signal integrity is one of the limiting factors of SoC performance.

1.1.3 Reusable Intellectual Property (IP) Blocks

When a system is built using multiple chips at the board level, the chips can be selected from different providers. In addition, a chip used in one system can be reused in other different systems. By doing so, it gives system designers more flexibility as long as those chips can communicate with pre-defined protocols, thus saving design time and cost. A similar concept could be applied to SoC applications. The building blocks, for example, PLL and ADCs, can be designed in different companies, and integrated on to the same chip, as long as signal integrity issues can be avoided/solved. The creation and reuse of portable IP blocks is a promising avenue to expand the SoC markets.

However, integrating different blocks on a single chip is more difficult than building systems on a board (or boards); coupling between functional blocks becomes more significant as distances between the blocks are reduced. In addition, due to area limitations on the chip, matching components cannot be as easily implemented compared to board level integration.

In SoC applications, one of the most significant problems comes from the cross-talk between noisy digital blocks and sensitive analog/mixed-signal blocks. The two major types of digital switching noise (DSN) are the noise coupled via the substrate and power grids. Although their propagation paths are different, the noise content can be highly correlated due to the direct connection between power grids and the substrate through metal contacts. The impact of power grid noise can be reduced using separate supplies for the analog and digital blocks, including the use of decoupling capacitors. However,

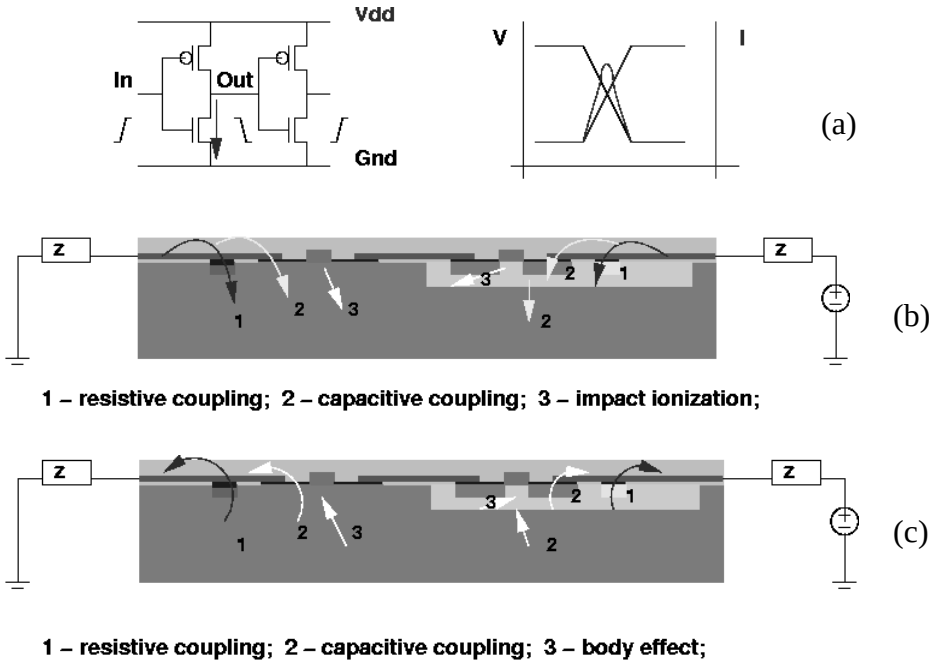


Figure 1-2 (a) Inverters and DSN, (b) DSN coupled from NMOS and PMOS, (b) DSN coupled to NMOS and PMOS.

DSN can still propagate across the electrically connected substrate, and affect analog/mixed-signal blocks.

Therefore, the focus of this work will be on how to model DSN in a monolithic substrate, and how to use the model to reduce the impacts from DSN in possible SoC applications.

1.2 Digital Switching Noise

Digital switching noise is generated at rising and falling edges of signals. Figure 1-2(a) shows an example with inverters. When a signal rises from low to high at an input node, the NMOS turns on, and current starts to flow through the transistor. Meanwhile, the voltage at the input of the second stage begins to decrease. Since the ground wire is not perfect, voltage fluctuations can be observed on the ground wire due to resistance-induced voltage drops, or inductive ringing. As illustrated in Figure 1-2(b), the noise

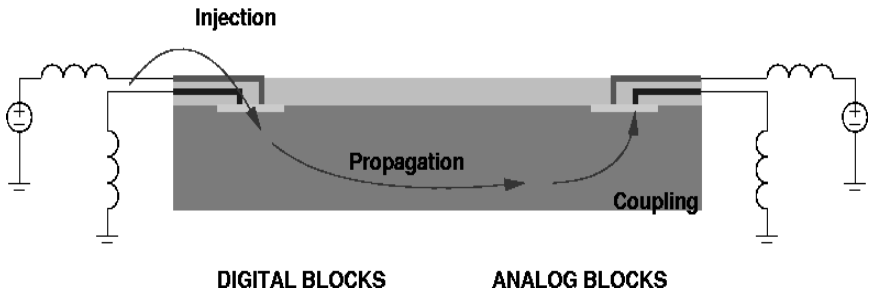


Figure 1-3 Three stages in the substrate noise problems.

current will couple to the substrate through three major mechanisms: (1) resistive coupling through substrate contacts, (2) capacitive coupling via source/drain junctions or the dielectric beneath the interconnects, and (3) current-induced impact ionization. Noise in the substrate will impact sensitive devices based on three different mechanisms as suggested in Figure 1-2(c): (1) resistive coupling through substrate contacts, (2) capacitive coupling through drain/source junctions, and (3) the body effect to other devices. The impact on PMOS device is typically smaller at low frequencies, because of the reverse biased junctions between the N-wells and the P-substrate.

In general, the impact of substrate DSN can be divided into three stages as shown in Figure 1-3: (1) noise injection from digital blocks into the substrate, (2) noise propagation in the substrate, and (3) noise coupling from the substrate to analog/mixed signal blocks. In this work, noise injection will be discussed in Chapters 2 and 3; noise propagation will be investigated in Chapter 7; Chapters 4 to 6 will focus on the measurement results and discussion of issues related to noise coupling.

It should be mentioned that the DSN is different from fundamental device noise, which includes: thermal noise, popcorn noise, shot noise and 1/f noise. A summary about device level noise and its impact on circuit performance can be found in [12][13]. In this research, device noise is not emphasized because its magnitude can be orders smaller than DSN as suggested by Verghese in [14].

1.3 Previous Work in Substrate Noise

There has been extensive research in the field of substrate-coupled noise. Previous work can be further categorized into six representative fields: (1) to investigate different substrate types with CMOS, BiCMOS, or SOI; and their efficiency in noise isolation [15-20], (2) to propose substrate models using meshes, Green's functions, or other order reduction techniques [22][23][27-32], (3) to explore noise suppression techniques using guard rings or other active circuits [33-36], (4) to design substrate noise sensors [21][41-45], (5) to model noise behavior and implement simulation tools [47-59], and (6) to study how analog/mixed-signal systems, such as Σ-Δ modulators and LNAs, react to substrate noise [21][40][41][61-67]. The above list of substrate noise research is not exhaustive. In this section, a brief summary of relevant previous work is presented.

1.3.1 Different Substrate Types

There are various types of substrates. For very-large-scaled-integrated-circuit applications, silicon substrates are mostly used. With different doping profiles, there are three major types of silicon substrates for CMOS technologies: (1) lightly doped (p-) bulk substrates, (2) heavily doped (p+) substrates with p- epitaxial layers on top, and (3) silicon-on-insulator (SOI) technology.

Aragonès [15] demonstrated that a p- wafer has better noise isolation characteristics than a p+ wafer. However, Merrill [16] suggested that the non-epi p- substrates have worse latch-up properties for many mixed mode circuit applications, and thicker p- epitaxial layers will have better noise isolation but worse latch-up properties. Joardar [17][18] examined noise isolation in different types of substrates; the results indicated that SOI has better properties than p- substrates, and triple-well technology could be equal to or better than standard SOI with lower fabrication costs. Of course, isolation properties degrade as frequency increases, because either the oxide or reverse-biased N-well junctions becomes conductive at high frequencies. Raskin [19] argued that high-resistivity SOI gives better performance than deep N-well technology up to frequencies in the 10 GHz range, though the difference becomes smaller when operating frequencies

approach 100 GHz. These examples show that noise attenuation in substrates is highly dependent on the technology selected and operating frequency used.

In BiCMOS applications, Casalta [20] conducted research showing that the common-collector (CC) configuration is quieter and more robust than common-emitter (CE) case. However, bipolar devices inject larger amounts of noise into the substrate when compared to CMOS implementations.

1.3.2 Substrate Models

In Su's pioneering work [21], the p+ silicon bulk is treated as a single node, and the p- epitaxial layer, because of high resistivity in the region, is modeled with spreading resistors. In general, there are two typical approaches to extract substrate impedance in p- regions: one type uses a distributed RC (or R) format in [22][23], and the other uses a boundary element (numerical) approach as demonstrated in [27-32].

The distributed (RC) model will be discussed again in Chapter 7. It is basically built from Maxwell equations using a spatial discretization method (Kumashiro [22], and Verghese [23]). These model equations can be solved either using circuit simulators like HSpice [24] and Spectre [25], or adapting the Asymptotic Waveform Evaluation (AWE) (Pillage [26]) techniques as demonstrated in [23]. The 3D mesh that is generated can be reduced using Voronoi Tessellation (Wemple [27]) and Congruence Transformation method (Kerns [28]).

Boundary element methods consider only the external nodes connected to devices or contacts using Green's Functions (Gharpurey [29], and Costa [30]). Device simulation and curve fitting techniques are used in Samavedam's work [31], and an improvement is proposed using a near/far field model (Lan [22]).

1.3.3 Noise Suppression and Noise-Aware Designs

Noise suppression can be achieved with either passive or active components. In passive suppression cases, the technique includes guard rings [21], Faraday cage (Wu [33]), or oxide trenches shown in Joardar's simulation [17][18]. For active noise

cancellation approaches, active guard rings (Makie-Fukuda [34] and Agung [35]) and feedback cancellation loop (Peng [36]) are proposed.

Guard ring structures are usually implemented with high doping concentration regions connected to dedicated ground/Vdd to provide low-resistivity paths for substrate noise. The Faraday cage method is implemented using a ring of grounded vias surrounding noisy and sensitive blocks. The concept of using active guard rings is to collect substrate noise with guard rings, and inject a negative replica to cancel the noise. The discrete time feedback loop first senses substrate noise; the noise is passed to a filter, and arrays of digital inverters are used to cancel the noise.

Niknejad [37] presented a spiral inductor design using a Green's function model for substrate coupling. Allstot [38] suggested fold-source-coupled logic to reduce digital switching noise compared to traditional CMOS design. Blalack [39] proposed staggered digital switching to reduce in-band substrate noise. However, as pointed out by Xu [40], the staggered technique only reshapes spectra but does not reduce total noise power, and noise reduction in the time domain does not necessarily imply in-band noise has been suppressed.

1.3.4 Substrate Noise Sensors

To monitor noise in substrates, various substrate noise sensors have been proposed. The easiest substrate sensor is implemented by a single NMOS device [21]. The sensing mechanisms are capacitive coupling and body effects of the NMOS transistor. Details of this design approach will be re-visited in Chapter 2. A more advanced substrate sensor is proposed by Franca-Neto [41] using Focused Ion Beam from the back of the die to cut and isolate the sensor from the rest of circuit to improve its accuracy. Van Heijningen [42] suggested a differential amplifier implemented in NMOS technology, and measurement results using this design approach are presented in Rolain's work [43]. Makie-Fukuda proposed a chopper-type voltage comparator and its modification to sense substrate noise [44][45]. The measurement results collected from Makie-Fukuda's sensors are discussed in detail in [46].

1.3.5 Noise Behavior and Simulation Tools

The results from Makie-Fukuda [44] indicated that substrate noise is closely related to rising and falling edges of digital signals. Briaire [47] had similar results and further concluded that noise on power grids is the dominant source of substrate noise. Nagata discussed the effects of power-supply parasitic components on substrate noise generation [48]. Xu [41] derived equations to express noise spectra in the substrate; periodic digital signals will induce discrete components in the noise spectra, while stochastic signals are the source for the continuous spectra observed.

Given the close relationship between the power grid and substrate noise, the Matsushita EMI noise analysis [49] and gate level simulation tool [50] could be applicable to substrate analysis with minor modification. Detailed device simulation to model a single noise injection and link the result to event-driven logic simulation is proposed by Miliozzi [51]. Zanella [52] ran multiple Spice simulations and used polynomial fitting to construct substrate noise patterns caused by different digital libraries. A high-level simulation of substrate noise is demonstrated by van Heijningen using a Spice substrate model with a VHDL cell library [53]. Stanisic [54] implemented software to simulate substrate coupling effects to power distribution synthesis. Clement's tool [55] is capable of plotting noise voltage contours on chip surfaces. Miliozzi [56] also demonstrated a VCO design, which is optimized for power and performance; the design includes substrate noise analysis using a local noise generator model. Mitra proposed a substrate–aware mixed-signal macrocell placement tool, assuming that the noise is at a single frequency [57]; later a modified version considering effective (root-mean-square) wide-band noise was discussed in [58]. Charbon [59] proposed a sensitivity analysis of the substrate to assess effects due to design modifications. As to commercial tools for substrate noise analysis, Cadence [60] provides a package named Substrate Noise Analyst, which is a combined set of two tools, SeismIC and Substrate Storm. SeismIC identifies significant noise injectors to the substrate; Substrate Storm models parasitic based on substrate doping profiles. Substrate Noise Analyst then generates netlists, containing substrate networks and current (noise) sources, for further

Spice simulations. However, the functions of guard ring placement and place-and-route under DSN are not fully automatic in the Cadence tool yet.

1.3.6 Circuit Performance under Substrate Noise

Circuit performance degradation due to substrate noise has drawn lots of attention in the past. Representative simulation approaches include Heydari's [61] work on Σ-Δ modulator, and Welch's simulation of PLLs [62].

In addition, test chips have also been fabricated and measured. Su [21] used an on-chip ring oscillator as the noise source and measured substrate noise using an NMOS transistor. Blalack [39] chose a shift register to generate digital noise, and studied how substrate noise impacts a Σ-Δ modulator in terms of SNR and SNDR. Xu [40] analyzed how an LNA is impacted by substrate noise. Larsson [63] gave a detailed survey about PLL jitter impacted by power grid/substrate noise under different power supply configurations. Distortion of the output waveform of an OPAMP due to substrate noise is discussed in Catrysse's work [64]. An 86 K-gate ASIC chip and a 12-bit I/Q up/down converter are implemented and investigated by van Heijningen in [65][66]. Nagata used a ripple-adder and shift registers [48], and a transition-controllable noise source [67] to investigate noise parameters, instead.

This project measures PLL performance under the influence of injected substrate noise. Instead of focusing on power grid configurations, this research studies jitter characteristics under different noise patterns. The parameters of the noise patterns include different frequencies, phase information, signal amplitude and switching activity level.

1.3.7 Related Noise Work

The related work is not limited to substrate noise. As mentioned, power grid noise is closely related to substrate noise. Larsson gave detailed discussion on power supply issues in [68][69], and proposed several power grid noise suppression techniques as well as robust circuit design styles. These techniques can as well reduce the impact of substrate noise as suggested by Iwata [70], which include adapting: (1) decoupling capacitance, (2) guard ring structures, (3) differential signaling, and (4) reducing

interconnect inductances. A design of on-chip decoupling using RLC components is discussed in Ingel's work [71].

In terms of high-level analysis, Hull [72] first gave a systematic approach to noise analysis in mixers. Roychowdhury [73] presented a technique to analyze large RF circuits under multi-tone noise. Razavi [74] has given a detailed review on phase noise in CMOS oscillators. Hajimiri [75] proposed the Impulse Sensitivity Function (ISF) method to analyze the impact of noise on VCOs. By integrating Perrott's C++ simulation tool [76] with the ISF approach, Kim [77] presented a system-level substrate noise analysis of VCOs.

Demir presented a series of papers regarding digital switching noise. A time-domain noise simulation for nonlinear dynamic circuits with arbitrary excitations are proposed in [78] based on the theory of stochastic dynamic systems. Demir [79] also argued that there should be two types of perturbations, deterministic and random, to model noise inputs. Later in [80], Demir analyzed phase noise and timing jitter in oscillators. One major difference between Demir and Hajimiri's approach about VCO is that Demir emphasized the non-linearity but Hajimiri assumed the system is linear but time variant (LTV).

1.4 Outline of Dissertation

Chapter 2 discusses components of digital noise spectra, and proposes a general-purpose digital block to emulate various digital spectra. The DSN measured from 2.5 V power grids provided by Atheros Communication Inc. is analyzed. The data led to a conclusion that digital spectra are closely related to system architectures. The IEEE 802.11a standard is also discussed to support the argument. After identifying typical DSN spectra, a low-complexity Digital Noise Emulator (DNE) is proposed to model digital systems at the behavior level. Discussion of the substrate sensor design and DSN generated by the DNE completes Chapter 2.

In Chapter 3, the background information of the test chip is introduced. The test chip includes a synthesized PLL provided by Barcelona Design Inc. and a Stanford designed DNE. The test chip can be used to demonstrate how different substrate noise parameters impact the PLL performance. Deterministic jitter, cumulative jitter and other performance parameters are discussed. Since noise phase is an important factor in analysis, a 3D plot (histogram versus phase) is first proposed in this chapter. The 3D plots will be used extensively in the following chapters.

Chapter 4 shows the measurement results from the test chip. PLL performance, under different noise frequency, phase and amplitude, are measured and compared. The results suggest that deterministic noise and stochastic noise will impact PLL differently. The collected data provides the necessary information for modeling work discussed in Chapter 5.

In Chapter 5, the formalism to calculate splitting factors and numbers of sub-cycles are introduced. Based on the theory and observations, data in any 2D histogram can be modeled by a combination of simple Gaussian curves. The model demonstrates its advantage in predicting system performance under different noise conditions. The approach is especially helpful for reusable IP designers to determine if the IP blocks are suitable for their application.

The DNE is not only useful for noise generation, but also can be applied for canceling deterministic noise. In Chapter 6, the concept is verified by experiment. The impact on PLLs from a noise coupled from a trace can be reduced when the DNE is activated. A mathematical model is included to support this methodology. Later in the chapter, the relationship between power grid noise and substrate noise is presented. This is the supplementary material needed to validate the argument that power grid noise and substrate noise are closely related to each other.

Chapter 7 further discusses substrate models and signal integrity issues. As operating frequency goes into the range of several tens of GHz in the future, quasi-static assumptions should be revised. A non-quasi-static substrate model is proposed to

account for magnetic coupling. The inductance issue and electromagnetic coupling in substrates are discussed as well in the latter part of Chapter 7.

In Chapter 8, recommendations for future studies are discussed, and the dissertation concludes with a summary of this work.

Chapter 2

Digital Noise Spectra and Digital Noise Emulator

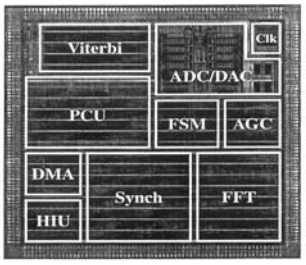
2.1 Introduction

In this chapter, the power grid noise spectra in an IEEE 802.11a Base-band/MAC processor will be first explored. As it will be shown later in Chapter 6, the spectra of the power grid noise and the substrate noise should have the same noise components. The measurement results show that noise spectra depend strongly on system architectures. Therefore, a low-complexity digital noise emulator is proposed as a means to efficiently model digital systems.

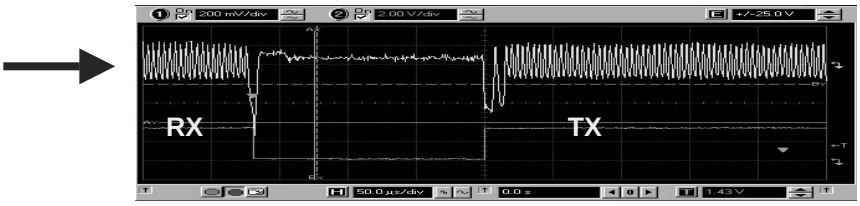
2.2 Digital Noise Spectra

2.2.1 IEEE 802.11a Base-band/MAC Processor

Figure 2-1(a) shows the micrograph of the IEEE 802.11a [2] base-band/MAC processor by Atheros Communication Inc., from which digital noise on the 2.5 V power grid was measured. The detailed information about the chip can be found in [9]. The processor and a separate RF IC [8] provide a chipset solution to create an 802.11a



(a)



(b)

Figure 2-1 (a) Micrograph of Atheros' IEEE 802.11a Wireless LAN base-band/MAC processor (courtesy by Atheros Communication Inc.), (b) current waveform on the 2.5 V power grid.

Block	CLK	DAC	ADC	FFT	AGC	SYNC	HIU	Others
Freq (MHz)	40	160	80	80 160	40/80	40 80	33 (3.3 V)	40

Table 2-1 Clock frequencies in major digital blocks (802.11a).

system. The staff at Atheros Communication Inc. completed the measurement at their site and provided the data to Stanford University.

The experimental results provided data concerning the spectrum of digital switching noise on the power grid of the chip. The time domain noise waveform on the 2.5 V grid is shown in Figure 2-1(b), in which RX stands for receiving mode, and TX stands for transmitting mode.

Before looking at the noise spectra, the clock frequencies in the major digital blocks are first listed in Table 2-1. Except for the HIU block, which is connected to the 3.3 V

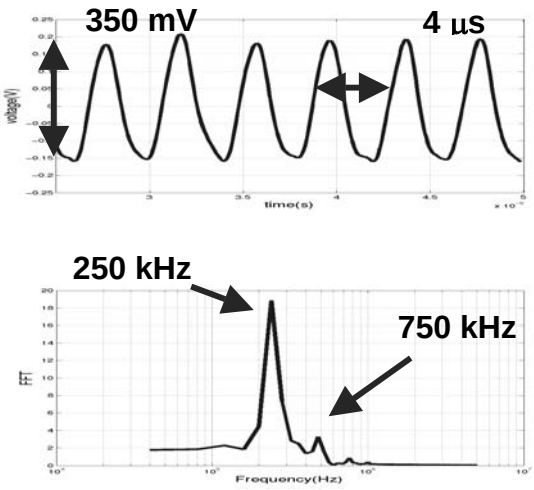


Figure 2-2 (a) Enlarged version of the TX portion shown in Figure 2-1(b), (b) FFT of Figure 2-2(a), largest peak at 250 kHz.

net, all the blocks are clocked at 40 MHz and its higher harmonics, 80 MHz and 160 MHz. At first glance, the peak noise frequencies should be found at these specific locations. However, this is not the case.

Figure 2-2(a) shows the enlarged version of the noise waveform in the TX mode, and Figure 2-2(b) is the FFT result of Figure 2-2(a). It is clearly seen from the figure that the largest noise component is neither the clock fed into the chip nor its higher harmonics. Instead, it is the symbol rate of the system. Therefore, it can be argued that the digital noise spectra strongly depends on system architecture, or the standards used in applications; DSN is not necessarily dominated by the input clocks.

To further elaborate the argument, using the IEEE 802.11a as an example, the data stream at the output buffers is shown Figure 2-3(a). The architecture is called orthogonal frequency division modulation (OFDM). In the TX mode, the input digital data is first fed into the convolutional encoder block (FEC) as shown in Figure 2-3(b). According to the protocol, those encoded bits will be interleaved within the length of a symbol. Then the data are mapped using either BPSK, QPSK, 16-QAM, or 64-QAM [81] and sent out in 48 parallel complex number streams. In the next three digital stages, Inverse Fast Fourier Transform (IFFT), Guard Interval (GI) Insertion, and Waveform Shaping blocks,

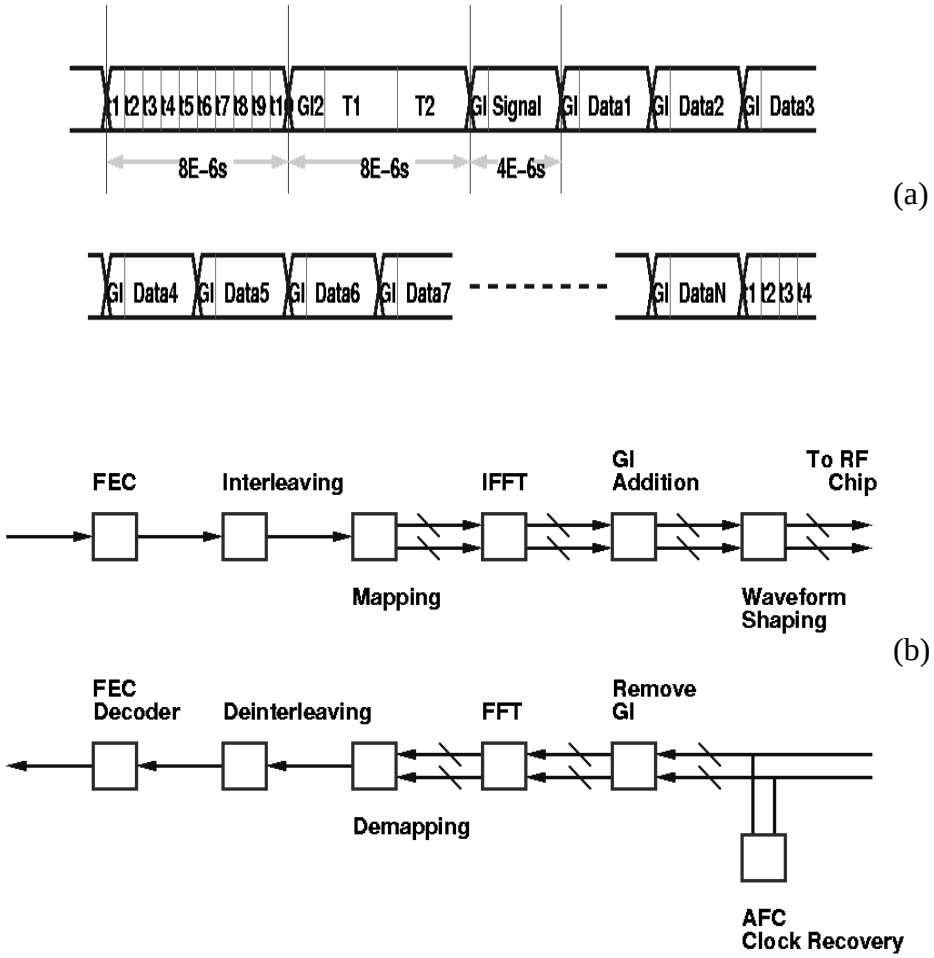


Figure 2-3 (a) Data stream of IEEE 802.11a signal at the base-band/MAC processor chip edge, (b) the architecture of the OFDM system.

digital data are calculated, added, shaped, and then sent to DAC in the cycles of the symbol interval, 4 μs (250 kHz, not every transistor changes its state as frequent as the clocks listed in Table 2-1). These digital blocks consume about 72% of total power (219 mW out of 301 mW). This explains why the 250 kHz component is the most significant digital noise measured on the power grids, and, theoretically, in the substrate as well. Therefore, in terms of behavior modeling, the spectrum and time domain waveform of this base-band chip can be approximated by:

Frequency domain: $A \cdot \delta(250 \cdot 10^3) + B \cdot \delta(750 \cdot 10^3) + S(f)$,

Application	Effective Symbol (T)	Guard Interval Factor (f)
DVB-T (2K, 8K)	224, 896 μs	1/4 1/8 1/16 1/32
ISDB-T (M1, 2, 3)	252, 5004, 1008 μs	1/4 1/8 1/16 1/32
802.11a	3.2 μs	1/4
802.16	22.4, 32, 36.57, 44.8, 64, 73.14, 128 μs	1/8 1/16 (1/32)

Table 2-2 Symbol rates of representative OFDM systems.

Time domain: $C\cos(2\pi \cdot 250 \cdot 10^3 \cdot t + \psi_1) + D\cos(2\pi \cdot 750 \cdot 10^3 \cdot t + \psi_2) + s(t)$,

where *S(f)* is the noise floor, and *s(t)* is a random process.

In Atheros' case, the base-band modules are not integrated with the RF blocks. However, the low-complexity behavior model can always replace complicated digital systems, and speed up interactive signal integrity simulations to check if single-chip solution is feasible. Latter in this chapter, the concept based on this result will be proposed and discussed in detail.

2.2.2 Other OFDM Applications

In addition to IEEE 802.11a, there are several other standards using OFDM technologies. OFDM is mostly applied in the applications where multi-path reflection inter-symbol-interference (ISI) is a concern. These communication protocols include European Terrestrial Digital Video Broadcasting (DVB-T) systems, Japanese Terrestrial Integrated Services Digital Broadcasting (ISDB-T) systems, IEEE 802.16 Metropolitan Access Network, and possible 4G-CDMA applications [82-84]. Since they all have similar architectures in the base-band modules, the most significant digital noise generated could be the component at one-over-the-symbol-rate, as found and discussed in this chapter. Table 2-2 lists the symbol rates of representative OFDM systems.

2.2.3 Spectra in General

From the above discussion, once the system architecture is selected, the shape and content of the spectra are roughly determined. A reduced-order model of complicated systems, using only a few key parameters, is especially helpful in cases of developing system level simulation models. Because of computational issues, it is not practical to include designs at the detailed transistor level. In the next few sections, key DSN model parameters will be discussed. Based on this model, a general-purpose digital noise emulator (DNE) will be proposed. The advantage of using the DNE is the controllability of spectral content. The DNE can help to identify different responses caused by specific noise parameters efficiently. Implementing the DNE in software help designers to perform signal integrity checks with acceptable computational resources. A hardware realization helps to characterize the robustness of IP designs under different noise conditions before introducing the IPs to market or in evaluating issues related to SoC integration.

2.2.4 Key Parameters of Digital Switching Noise

Different digital blocks have different spectral noise signatures [52]. From the inverse Fast Fourier Transform (IFFT), discrete components in the frequency domain correspond to periodic digital switching noise in the time domain, and continuous spectra are the result of stochastic signals.

Therefore, the digital switching noise, $N(t)$, either in the substrate or on power grid lines, should be described as a sum of deterministic, $d(t)$, and stochastic components, $s(t)$.

$$N(t) = d(t) + s(t)$$

$$= \sum_{i=1}^{K} \alpha_i \cos(2\pi \cdot f_i \cdot t + \theta_i) + s(t)$$

where α, f and θ, are the amplitude, frequency and phase of the deterministic signals, using Cosine transforms. Frequency and timing of digital clocks, digital switching activities, and the number of transistors in digital blocks are the parameters which will affect the values of α, f, θ, $s(t)$, and, therefore, the performance of analog/mixed-signal

systems. To investigate how the system responds to these digital variables, a DNE is proposed in the next section for behavior-level modeling.

For example, in the case of an IEEE 802.11a base-band/MAC processor, the system architecture and measurement data both indicate that the largest component of digital switching noise is at the symbol rate, 250 kHz. For behavior level simulations, the complicated system can be replaced by a low-complexity DNE, generating a single-tone noise at 250 KHz with added random noise to enhance simulation accuracy. Since the significant components of the digital noise spectra are always application and architecture dependent, the concept of using the DNE is applicable to a variety of digital designs.

2.3 Digital Noise Emulator

2.3.1 Architecture

The DNE consists of four major blocks: (1) a deterministic signal generator (CLK), (2) a frequency divider (DIV), (3) a pseudo random noise generator (PRNG), and (4) several noise injection devices (NID). The CLK and DIV are used to generate dual-tone deterministic noise; the stochastic behavior *s(t),* is emulated by the PRNG; the NIDs, controlling amplitudes α, are implemented using junction capacitances in different sizes. The detailed architecture (dual-tone) is shown in Figure 2-4. Off-chip clocking is recommended because it provides flexibility in selecting clock characteristics, such as frequency (f), phase (θ) and duty cycle. Extending this architecture for multi-tone cases is straightforward. In practice, more than one DNE can be implemented to emulate more complicated system effects. However, it is a trade-off between completeness and complexity.

In short, a standard procedure to characterize noise impact as follows:

(1) Estimate digital noise spectra based on the architecture and previous experience, i.e. estimate the variables, α, f and $s(t)$, in $\sum_{i=1}^{K} \alpha_i \cos(2\pi \cdot f_i \cdot t + \theta_i) + s(t)$.

(2) Use a DNE to emulate the estimated spectra for system-level analysis.

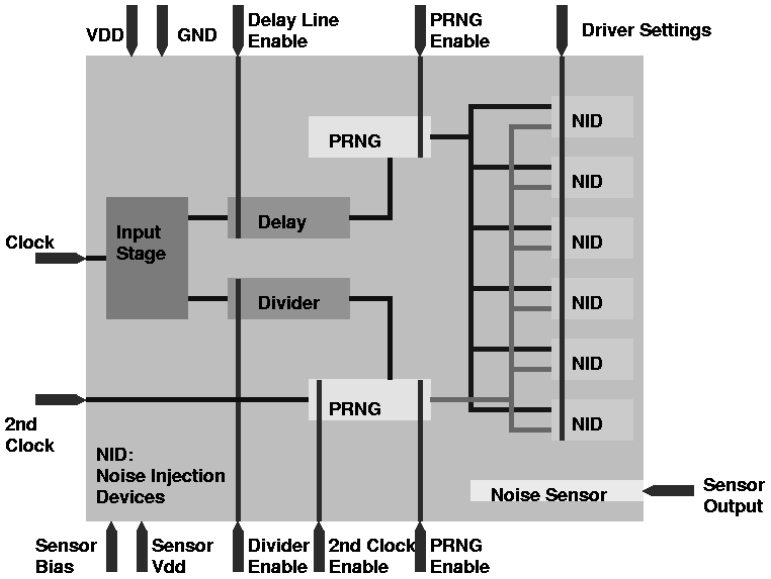


Figure 2-4 Architecture of Digital Noise Emulator (DNE).

Su(’93)	on-chip oscillator w/ fixed loading
Blalack(’97)	off-chip clock w/ variable loading
Xu(’01)	off-chip clock/on-chip oscillator w/ variable loading
Larsson(’01)	off-chip clock w/ on-chip random logic, fixed loading

Table 2-3 Summary of previous noise emulator designs.

2.3.2 Comparison to Previous Work

As discussed in Chapter 1, several previous efforts have investigated how systems react when exposed to substrate noise. The digital noise sources used are different for each case. Some of them use real circuit blocks, and some adopt the concept of noise emulators, which have the above-mentioned advantages of controllability in noise shaping. The proposed emulator can generate a variety of digital switching noise. By properly setting transistor status in the control logic, the impact coming from different noise parameters can be isolated and studied in detail.

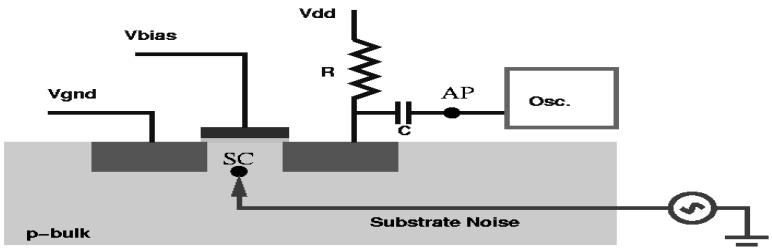


Figure 2-5 Sensor configuration.

Table 2-3 summarizes the differences between selected emulator designs. The major differences between the DNE proposed in this work and others include: (1) variable loading capacitors with both deterministic and random noise features, (2) a divider to emulate dual-tone signals.

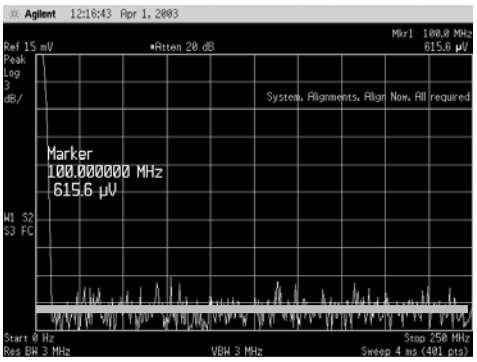
2.4 Substrate Noise Sensor

2.4.1 Sensor Designs

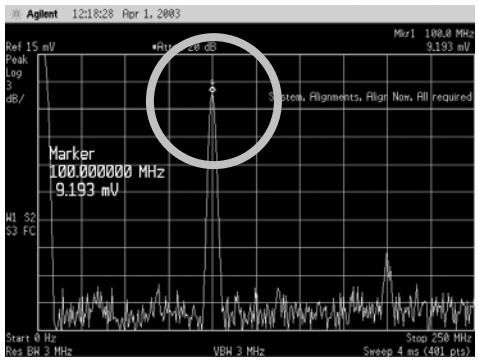
The sensor used in the design is a single NMOS transistor shown in Figure 2-5. Noise is detected using the back-gate (substrate) concept. The sensor has a separate ground pin connected to the source node to provide a better reference. The gate voltage is set to 0.6 V, and the drain is connected to a dedicated power supply through a 1 kΩ resistor. A bypass capacitor is used to filter out the DC component at the node AP. Based on HSpice simulations, if an active probe with high impedance is connected to AP, the gain between the node AP and the node SC in the substrate is about 0.5. The bandwidth is more than 1 GHz, and is limited by the active probe used.

This simple design is selected because of the trade-off between several factors. More complicated sensor designs may grant better gain with reasonable bandwidth. Some previous work in sensor designs is discussed in Chapter 1, and won't be repeated here.

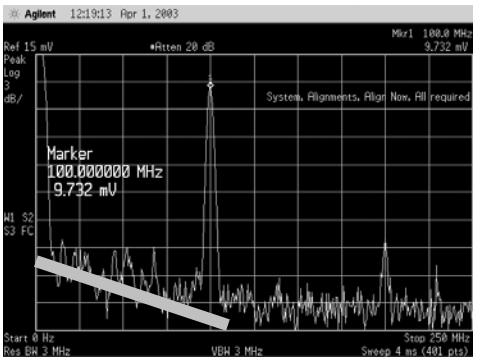
(a)



(b)



(c)



(d)

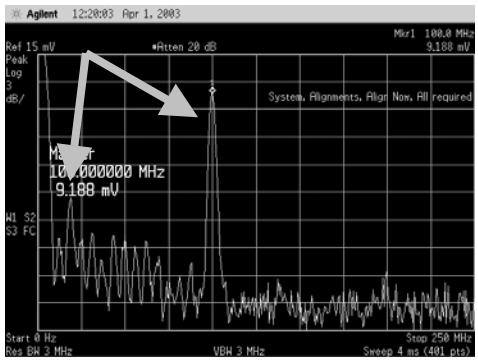


Figure 2-6 Noise outputs from Spectrum Analyzer: (a) noise-free, (b) a 100 MHz deterministic noise, (c) a 100 MHz deterministic noise with other random noise components, (d) a dual-tone case, 6.25 MHz locked with 100 MHz.

2.4.2 Emulated Noise Spectra

Figure 2-6 shows measured noise spectra. An active probe is attached to the coupling capacitor (node AP in Figure 2-5), and connected to a Tektronix 1103 Tekprobe Power Supply at the other end. The Tekprobe Power Supply sends the signal to an Agilent E4407B Spectrum Analyzer through a BNC cable.

Figure 2-6(a) shows the case without any digital noise. After activating the DNE, which generates a 100 MHz deterministic noise, a 9.193 mV peak is measured at the exact location of the spectrum (Figure 2-6(b)). When the PRNG block is also activated, the noise floor rises with additional small random peaks at various locations (Figure 2-6(c)). Figure 2-6(d) demonstrates a dual-tone case, where the divider block is on and

locked to a 100 MHz deterministic noise. Because the divider is at the ratio of one-to-sixteen, deterministic noise at 6.25 MHz and the higher harmonics can be clearly observed. Since the gain of the sensor and the probe are 0.5 and 0.2 respectively, the noise amplitudes shown in Figure 2-6 are ten times smaller than their actual values, which means the 9 mV measured peak corresponds to 90 mV in the substrate.

2.5 Summary

This chapter first shows a digital noise waveform measured from an IEEE 802.11a wireless LAN base-band/MAC processor (provided by Atheros Communications Inc.). The largest noise component is at the symbol rate of the system, 250 kHz, which can be explained by understanding the system architecture. Since the significant noise behavior is architecture dependent, a low-complexity DNE is proposed to substitute for a more complicated digital block, and it is parameterized based on key noise parameters.

Chapter 3

Test Chip Background Information

3.1 Introduction

A test chip was designed and fabricated to investigate how different substrate noise patterns impact system performance. The chip consists of two major blocks, a synthesized PLL and a DNE. The DNE architecture has been discussed in Chapter 2. In Chapter 3, the building blocks of PLLs will first be reviewed, followed by discussion of the test board and measurement setup. Since jitter is one of the prime indicators of PLL performance, the fundamentals of jitter characteristics will be discussed. Measurement samples from the spectrum analyzer will also be considered in the latter part of this chapter.

3.2 Test Chip

The hardware implementation of the DNE was fabricated next to a 200 MHz PLL using the TSMC 0.18 μm 1P6M 1.8 V/3.3 V Logic/Generic technology. Figure 3-1 shows a micrograph of the test chip. The die size is 1500 μm by 1900 μm (with DNE 1000 μm by 500 μm), and it is packaged in a 68-pin QFP. The PLL was synthesized using the Miró^{TM} CGS18T PLL Engine [85] provided by Barcelona Design Inc. The PLL core is a ring-typed VCO. In the DNE design, without losing generality, the Delay

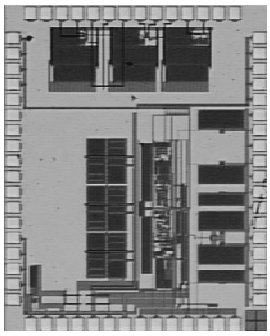


Figure 3-1 Micrograph of the test chip.

block and second Clock input option is removed from the architecture proposed in Figure 2-4 because of area and pin constrains in the final tape-out. The impact of DNE location relative to the PLL is less significant in this case because the substrate is epi-type (on a heavily doped substrate), and it is reasonable to treat the entire substrate as a single grounded node.

3.2.1 PLL Block

The high-level block diagram of the synthesized PLL (provided by Barcelona Design Inc.) is shown in Figure 3-2. The reference clock at 20 MHz is provided by an off-chip crystal. The phase detector block determines the phase difference between the reference clock and internal feedback clock, and generates UP and DOWN sequences of pulses to control the charge pump. The charge pump will either charge or discharge the parasitic capacitor at its output node according to the pulse signals. If the voltage of the node increases, the operating frequency of the VCO increases, and vice versa. The loop filter inserted between the charge pump and the VCO filters out the undesired interfering signals generated by the phase detector. The output of the loop filter controls the voltage bias of the ring-type VCO running at 400 MHz. Since there are two distinct peaks observed in the VCO output jitter plot from simulations, a divide-by-two divider is inserted to select every other VCO clock rising edge to provide an accurate 50% duty cycle. Therefore, the PLL output frequency is at 200 MHz. In the feedback loop, a divide-by-ten divider is implemented to bring the loop signal from 200 MHz to 20 MHz.

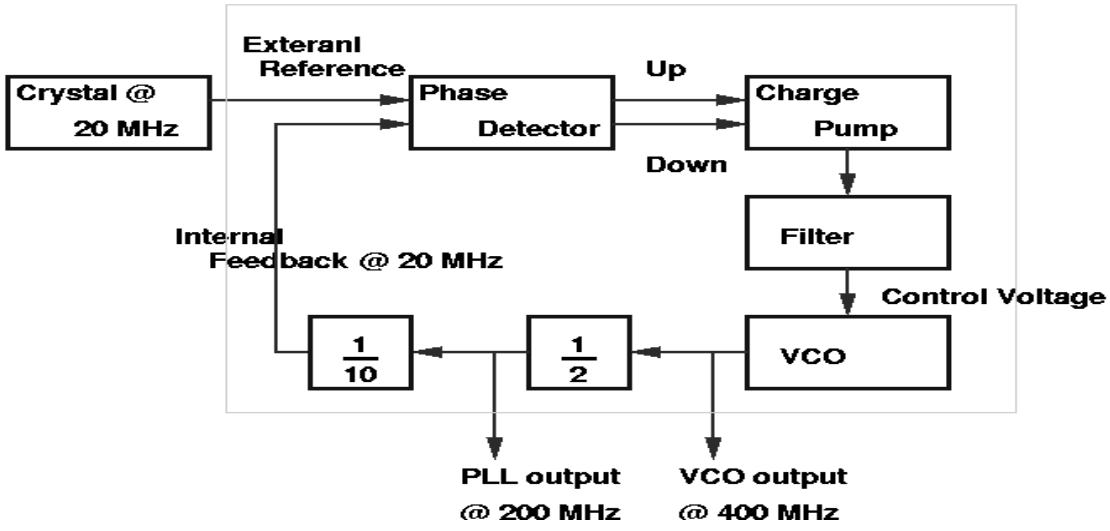


Figure 3-2 Block diagram of the synthesized PLL.

The phase detector compares the feedback signal with the reference clock, which completes the loop. If the denominator of the divider block is set to a different number over a reasonable range, the PLL output frequency will change accordingly. For example, it the number is set to 8 instead of 10, the output frequency will be reduced to 160 MHz. When operating at 200 MHz, the PLL core consumes 2.45 mW at 1.8 V.

The phase detector basically employs conventional sequential logic design as suggested in [86]. Since it is a digital block, it is normally more robust to substrate noise. In general, the VCO and charge pump are the most sensitive blocks to substrate noise in a PLL. The low-pass-filter in the loop is less sensitive to digital noise; however, since the output of the loop filter is directly connected to the control node of the VCO, even a small variation in the block itself will cause a large impact on the VCO as reported by Kim [62]. The VCO is designed in a three-stage delay line structure. The area of the PLL core is about 900 μm by 300 μm in this design.

The divide-by-ten circuit in the loop is implemented with a ripple-type divider. Because of its digital nature, it is also a possible noise generator to system performance. Therefore, if area permits in future implementations, guard rings should be implemented around the divider to reduce substrate noise injection. In addition, placing guard ring

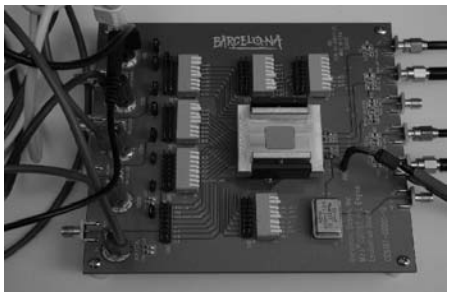


Figure 3-3 Test board provided by Barcelona Design Inc.

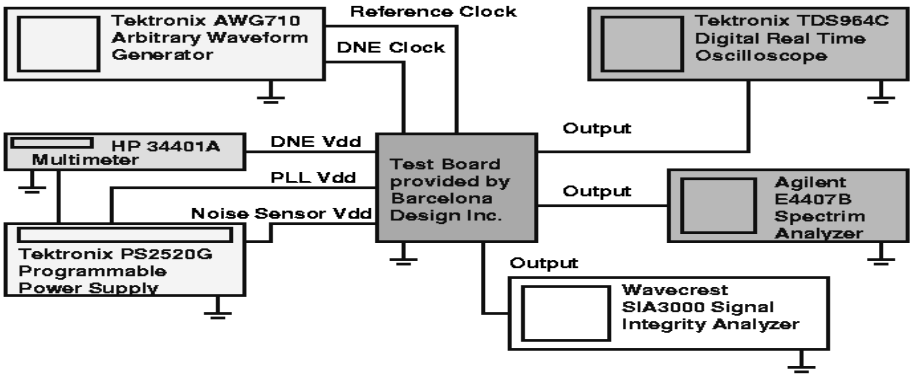


Figure 3-4 Measurement setup.

structures to surround sensitive circuit blocks is also recommended to reduce noise coupling.

3.2.2 Test Board and Measurement Setup

The test board, shown in Figure 3-3, has six layers with dedicated power supplies for the DNE, PLL I/O, PLL Analog, and PLL Digital. Each supply has a 3300 pF decoupling capacitance attached to it. The measurement setup is depicted in Figure 3-4. The reference clock to the PLL and the input clock of the DNE are generated by the Tektronix AWG710 Arbitrary Waveform Generator. The PLL output is connected to a Wavecrest SIA3000 Signal Integrity Analyzer [87] to measure the histograms of the PLL clock cycle, which are chosen as the primary discussion vehicle for illustrating the impact

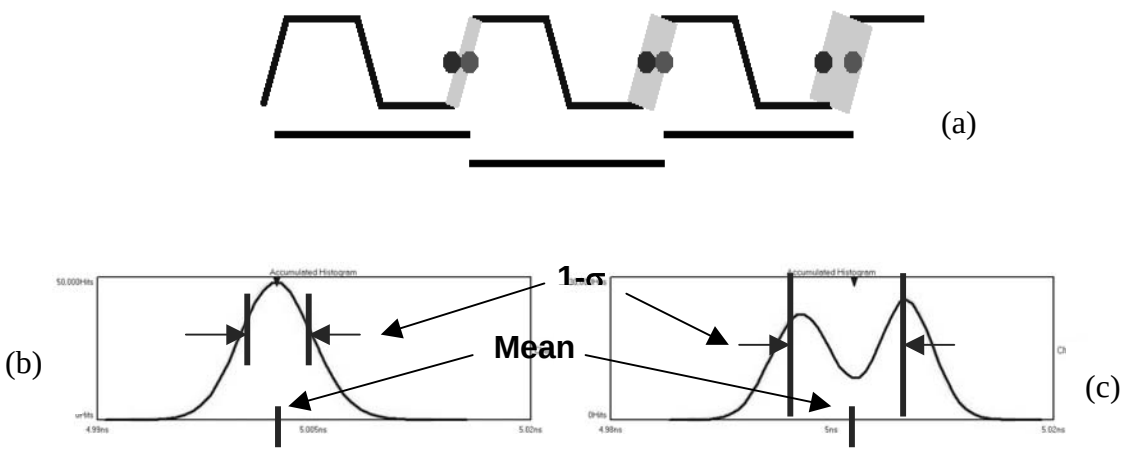


Figure 3-5 (a) Cycle-time varies because of noise, (b) typical histogram, single Gaussian curve, (c) typical histogram, summation of two Gaussian curves.

from substrate-coupled noise. The output is also connected to an Agilent E4407B Spectrum Analyzer and Tektronix TDS TDS964 Digital Real Time Oscilloscope to monitor output spectra and time domain waveforms, respectively. Target systems are not limited to PLLs. ADCs, DACs, PAs, and LNAs can as well be characterized using the methodology proposed. Of course, different analog/mixed signal systems have different figures of merit. For example, in ADC designs [39], signal-to-noise-and-distortion ratio (SNDR) should be used, as suggested in [88].

3.3 Jitter Fundamentals

3.3.1 Periodic Jitter

If a PLL is operating under ideal conditions, the length of each cycle, from a rising edge to its next rising edge, is constant. The histogram, which plots the numbers of hits versus cycle times over a long period, has only one single spike at the exact time spot. However, in practical circuits, device noise as well as digital switching noise will make the position of clock rising edges fluctuate within a certain range as shown in Figure 3-

5(a). Therefore, the shape of the histograms will no longer be a single spike. It can be either a Gaussian curve because of the nature of the pure random noise, Figure 3-5(b), or a summation of Gaussian curves caused by complicated digital switching activities, Figure 3-5(c). If a PLL is in lock and functioning correctly, the mean of the histogram should not change dramatically between cases. However, the standard deviation of the histogram, 1-σ jitter, could be very different from one case to another. In the following chapters, the differences between the histograms will be listed and compared.

3.3.2 Cumulative Jitter

In addition to periodic jitter, cumulative jitter is also an important indicator of the PLL performance. Procedures to obtain cumulative jitter are illustrated in Figure 3-6.

A sequence of the clock is first generated in Figure 3-6(a), which can have more than thousands of cycles. At first, one randomly picks a cycle and measures its cycle length, t_1. Then repeat the procedure for a total of n times, and record t_2, t_3,…t_n. The standard deviation σ_1, associated with these t_is can be obtained. As the second step, one randomly picks two consecutive cycles and measures the total length of the two cycles, s_1, and repeats n times. By the same token, the standard deviation σ_2, can be calculated. The same procedure is applied to three cycles, four cycles, and up to several hundred cycles. In that case, a result similar to Figure 3-6(b) can be plotted. The figure shows cumulative jitter measured under the DSN-free condition.

When the cycle numbers are small, the values of standard deviation increase steadily. Because the limitation of PLL bandwidth, jitter will accumulate up to a certain number of periods before the PLL reacts to the noise. Beyond this point, the standard deviation will fluctuate around a fixed number. The period of the fluctuation is closely related to the noise frequency. For example, if the noise is at the half (one-third) frequency of the PLL output, cumulative jitter is in the period of two (three) cycles. More detailed discussion and examples of cumulative jitter will be revisited in the next chapter. As additional information, the bandwidth is about 2 MHz, one tenth of the reference clock, in this PLL design.

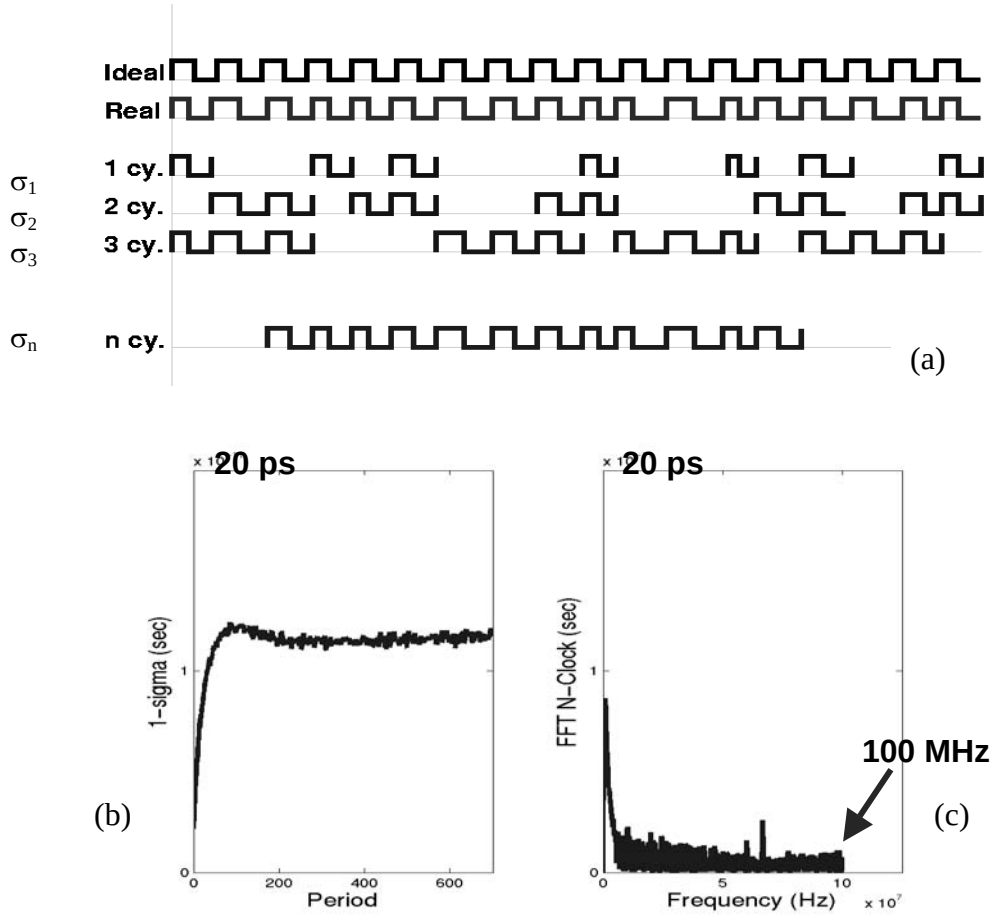


Figure 3-6 Cumulative jitter: (a) collect standard deviations of different cycle lengths, (b) standard deviations versus periods, (c) FFT of (b).

Figure 3-6(c) shows the FFT result of Figure 3-6(b). The large peak in the lower frequency range comes from the slow-rising edge in Figure 3-6(b). The small peak at 67 MHz comes from the 6.7 MHz noise embedded in the reference clock, multiplied by 10 because of the system loop.

As will be demonstrated in the next chapter, the FFT plots provide the "high frequency modulation" information between the clock output and noise. The upper bound of the frequency axis is set at the Nyquist rate of the PLL output frequency, which is 100 MHz in this case.

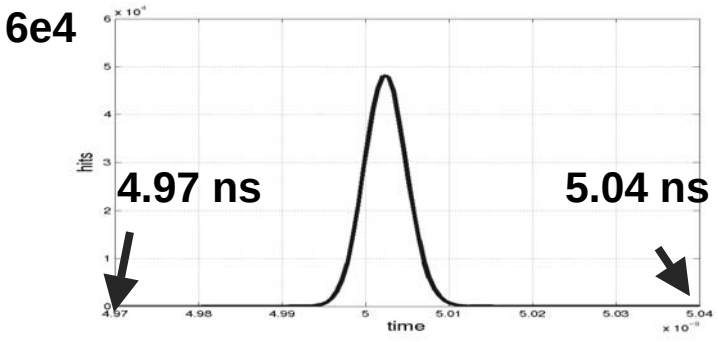


Figure 3-7 Histogram of clock cycle time.

Mean	**5.0024 ns**
Standard Deviation	**2.5266 ps**
Peak-Peak	**23.79 ps**
Skewness (*s*)	**0.07**
Kurtosis (*k*)	**3.02**

Table 3-1 Statistic results of the distribution shown in Figure 3-7.

3.4 Measurement Result w/o DSN

Figure 3-7 shows the histogram of the cycle lengths under a DSN-free condition. The histogram contains data measured in 500,000 cycles (hits). As listed in Table 3-1, the mean of the distribution is 5.0024 ns (targeting 5 ns). The standard deviation is 2.5266 ps. The peak-to-peak jitter is 23.79 ps.

The histogram has a bell-shape at first glance. To determine if it is suitable to use a single Gaussian distribution to describe the histogram, which will be an important assumption in Chapter 5, the skewness and kurtosis should be further calculated.

By definition, given *X* is a set of cycle lengths measured, $X = \{x_1, x_2, \cdots x_n\}$. The mean (*m*), standard deviation (σ), skewness (*s*), and kurtosis (*k*) of the data set are defined as follows:

Given $\mu_j = EX^j = \frac{1}{n}\sum_{i=1}^{n} {x_n}^j$,

mean, $m = \mu_1$,

standard deviation, $\sigma = \sqrt{\mu_2 - m^2}$,

skewness, $s = \frac{\mu_3}{{\mu_2}^{3/2}}$,

kurtosis, $k = \frac{\mu_4}{{\mu_2}^2}$.

The objectives in calculating the mean and standard deviation are obvious. Skewness is a measure of the asymmetry in distortion. In the cases similar to a Gaussian distribution, the histogram is symmetric, and skewness should be very close to 0. Kurtosis is defined as the tail-weight of the data. If *k* = 3, it is called mesokurtic and matched to the Gaussian distribution. The numbers in Table 3-1 show that *s* is 0.07, and *k* equals to 3.02. The results confirm that the system can be modeled as a Gaussian curve. Once noise is added, the variations on the model will be derived based on this observation. Jitter behavior, influenced by the impact of substrate noise, will be examined later in detail.

3.5 3-D Histogram Plot

In the following chapters, 3D histogram plots are used extensively. The 3D histogram is a collection of jitter histograms shown as Figures 3-5(b), (c), or other variations, which will be referred as 2D cross-sections in the later chapters. Figure 3-8 shows a 3D

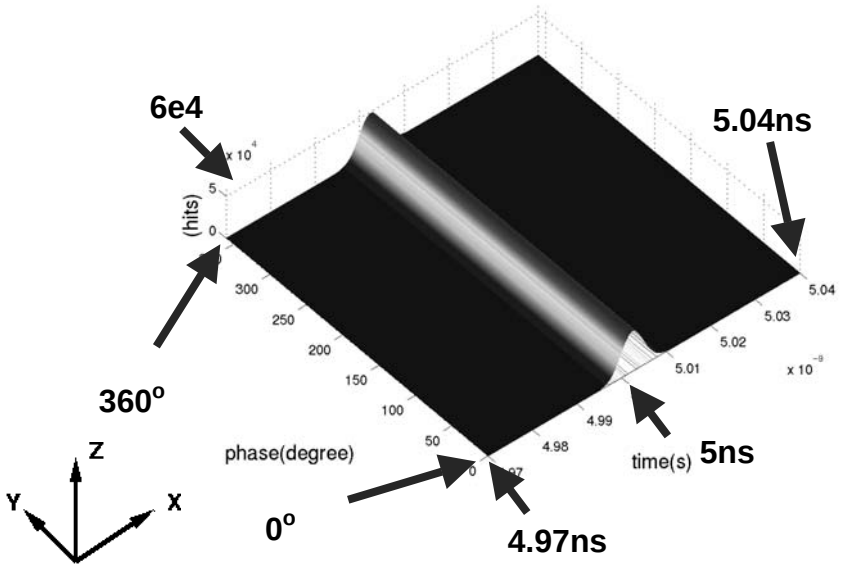


Figure 3-8 3D histogram-versus-phase plot, device noise only, no additional digital noise added.

histogram as an example. Since there is always device noise embedded, Gaussian shapes are observed even though there is no digital switching noise added.

As will be demonstrated in the following chapters, the phase differences between the PLL output and the digital clock would be significant to jitter characteristics. This is why the collection of 2D cross-sections at difference phases is valuable information and therefore plotted. 2D cross-sections are on the X-Z plane (hits versus time), and the phase is the variable of the Y-axis.

3.6 Outputs from Spectrum Analyzer

Before moving to the next chapter, typical outputs from the spectrum analyzer are shown. Figure 3-9(a) shows the DSN-free case, where the highest peak is at 200 MHz as expected, and the smaller peaks at $200 \pm 20n$ MHz ($n \in N$) come from the feed-through of the reference clock at 20 MHz. Figure 3-9(b) shows the case where the PLL is

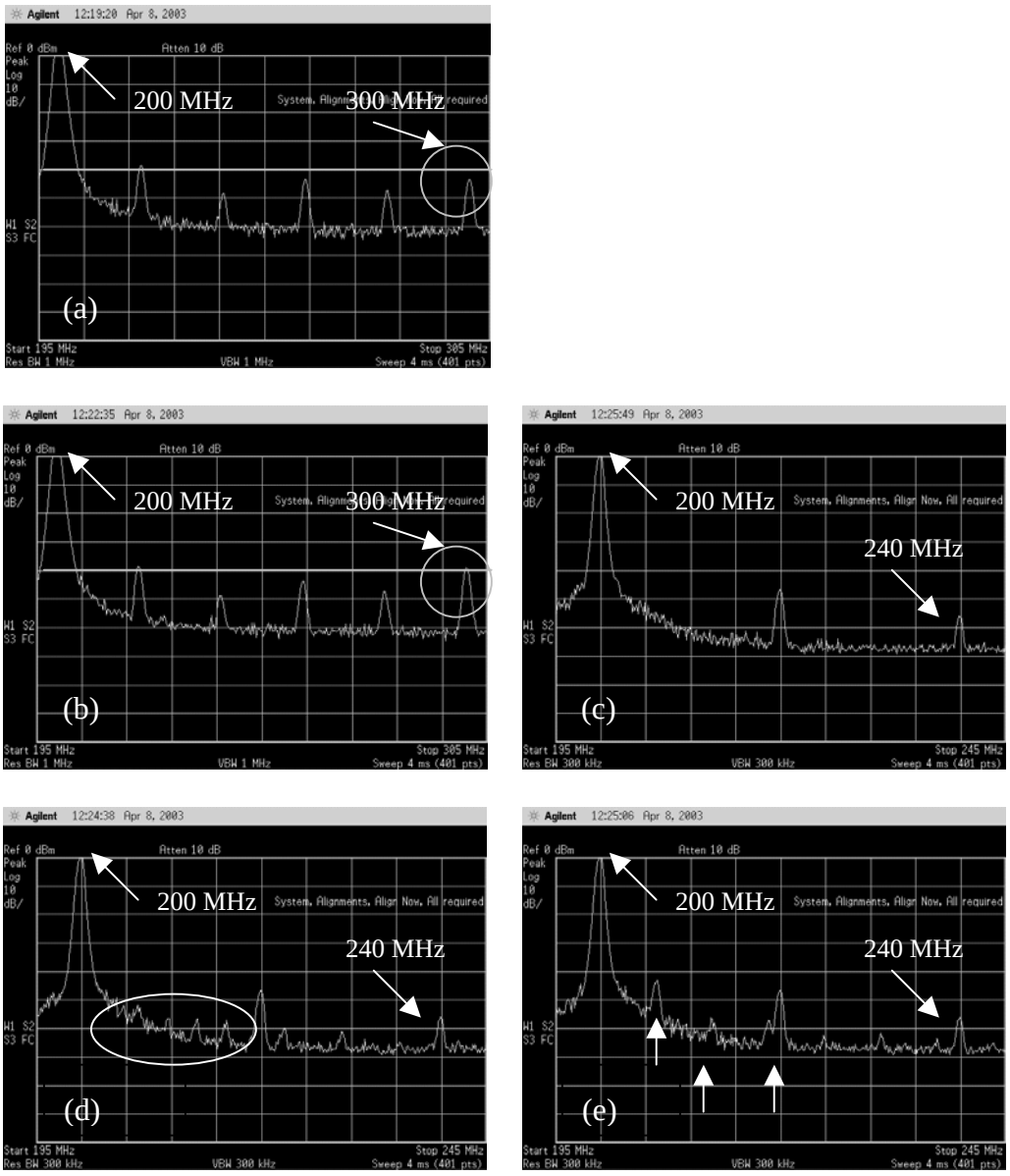


Figure 3-9 PLL output spectra: (a) noise free, (b) deterministic noise at 100 MHz, (c) enlarged version of (b), (d) random noise injected, (e) divider on.

impacted by a 100 MHz deterministic noise. Since the system is linear time-variant, the 100 MHz noise will bring effects at 300 MHz.

Figure 3-9(c) is an enlarged version of Figure 3-9(b). When compared to Figure 3-9(c), the extra peaks in Figure 3-9(d) are caused by stochastic noise generated from the

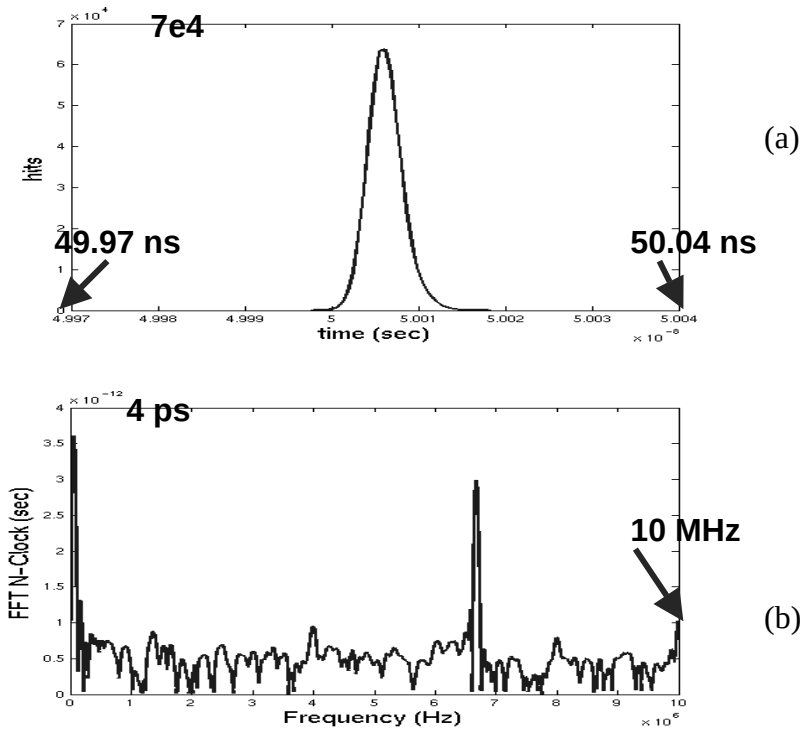


Figure 3-10 (a) Periodic jitter of the reference clock, (b) FFT of cumulative jitter.

PRNG. The additional peaks in Figure 3-9(e) (compared to Figure 3-9(c)) come from the one-divided-by-sixteen divider, the locations of the peaks are at $200 \pm 6.25n$ MHz ($n \in N \cup \{0\}$). The 6.25 MHz peak is one-sixteenth of 100 MHz. The differences in frequencies are clear among these cases. However, phase differences are not as clear from the spectrum plots. Therefore, the 3D histograms proposed in Section 3-5 should be used when phase impact is of interest.

3.7 Reference Clock Characteristics

The characteristics of the reference clock is important to PLL performance, and good board-level design can result in better reference clocks, in turn giving better system performance. As discussed above, the reference clock is modulated to the PLL output because of clock feed-through. Figure 3-10(a) shows the periodic jitter histogram of the

reference clock used in this research. The mean and standard deviation are 50.01 ns and 2.014 ps, respectively. In Figure 3-10(b), an embedded 6.7 MHz noise is observed, which explains why there is a small 67 MHz peak, measured at the output node of the PLL, even though there is no external digital noise input.

3.8 Summary

The test chip includes a synthesized PLL provided by Barcelona Design and a DNE is fabricated through TSMC. The detailed information of the test chip and the background knowledge of PLL jitter are discussed. The design of the test board and arrangement of test equipments are also included. Representative noise waveforms are demonstrated. At the end of the chapter, a 3D histogram plot (histogram versus phase) is first proposed. 3D histogram plots, which can demonstrate the impact of phase, are used extensively in the later part of this work.

Chapter 4

PLL Exposed to Substrate Noise

4.1 Key Parameters Revisited

Frequency and timing of digital clocks, digital switching activities, and number of transistors in digital blocks are key behavior-level parameters needed to model switching noise generated by complicated digital systems. This chapter elaborates on how these parameters impact the performance of a synthesized PLL, based on measured results. As mentioned in the previous chapters, this modeling approach is not limited to PLL applications.

Figure 4-1 again shows a 3D-histogram-versus-phase plot, which presents the case without any influence from digital switching noise in the substrate. Any 2D cross-section on the X-Z plane (hits versus time) represents a jitter histogram that is measured at a specific phase. Because there is no noise impact, the histogram is Gaussian in shape. The collection of 2D-cross-section plots in the Y (phase) direction results in the 3D plot, which will be extensively used in this chapter. In all 3D figures, unless specified otherwise, all dimensions are kept constant for comparison purposes. The X-axis is chosen to be between 4.97 ns to 5.04 ns. The range of the Y-axis is from 0^o to 360^o. The Z-axis is from 0 to 60000 hits. Again, the “phase” being plotted is the phase difference between the DNE clock and the PLL reference clock.

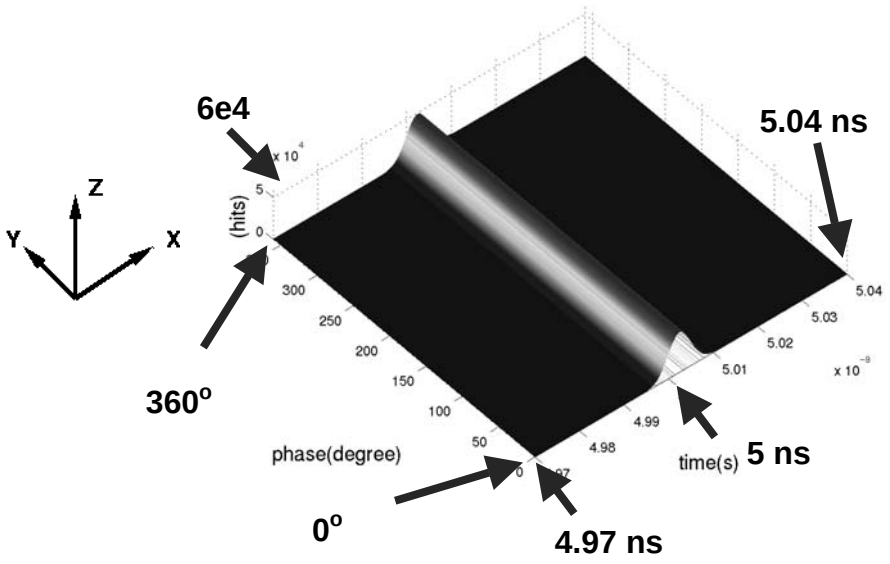


Figure 4-1 Histogram versus phase plot showing no noise impact.

4.2 Periodic Jitter

4.2.1 Phase Impact

The experiments start by injecting deterministic noise at 100 MHz while setting the coupling capacitance of the DNE at 40 pF. The measurement data in Figure 4-2 shows how the histogram varies as the phase changes. Except for some special cases, most of the 2D cross-section plots in the X-Z plane are no longer represented by a single Gaussian curve. Instead, they look more like a combination of two Gaussian curves. In addition, there are two sub-cycles in the Y direction.

The relative positions of rising edges between the DNE clock and the PLL reference clock are the cause of this two-sub-cycle behavior. At the rising and falling of the deterministic clock edges, the DNE injects current into the substrate. If these transients align with the PLL clock edges, the PLL performance will be the worst. When shifting the edge positions of the deterministic noise from 0^o to 360^o, the phase (θ) relative to PLL goes through two complete cycles as shown in Figure 4-3. By properly controlling θ, a

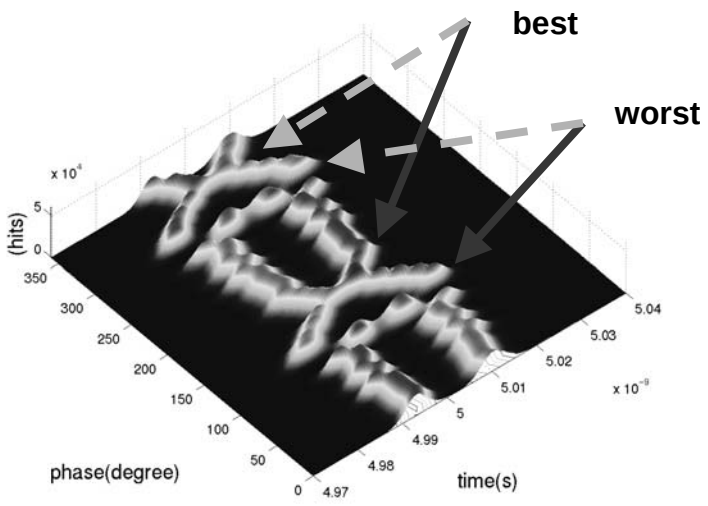


Figure 4-2 3D histogram plot with noise at 100 MHz, and coupling capacitance NID = 40pF (deterministic).

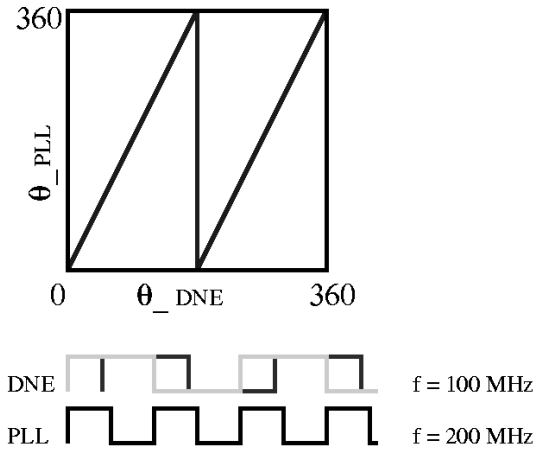


Figure 4-3 Relative phase between the DNE clock and the PLL reference clock.

71% improvement in jitter standard deviation from the worst case (14.394 ps) relative to best case (4.042 ps) is observed.

4.2.2 Coupling Capacitance

In Figure 4-4, the coupling capacitance is reduced from 40 pF to 20 pF. The signal is still purely deterministic at 100 MHz. When compared to Figure 4-2, the locations of the

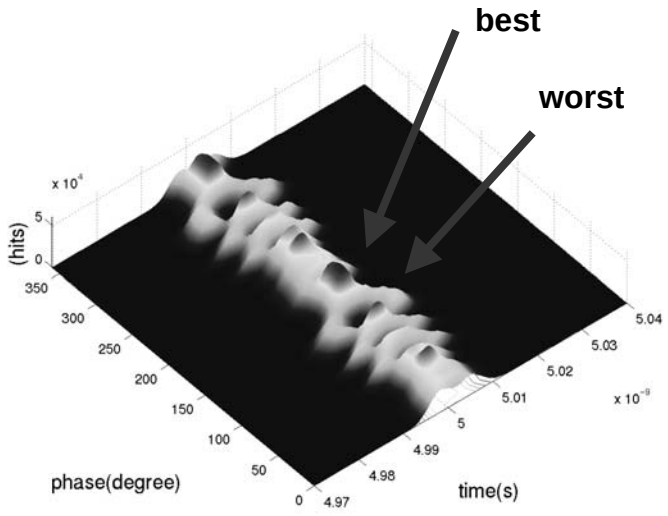


Figure 4-4 3D histogram plot with noise at 100 MHz, and coupling capacitance NID = 20 pF (deterministic).

best and worst cases remain the same, and two sub-cycles are also observed. However, the distance between the peaks decreases. This is because the substrate noise current injected into the substrate is proportional to the number of active transistors. For each specific phase, the smaller the substrate current, the smaller the impact will be. Therefore, smaller numbers of standard deviation could be observed in this case. According to the measurement results, the worst case is 7.23 ps, and the best case is 2.535 ps. Assuming the system is linear, applying interpolation and (or) extrapolation techniques to the measurement results, the system performance can be estimated. Details for interpolating the data will be discussed in the next chapter.

4.2.3 Switching Activities

In Figure 4-5, 40 pF of the noise-injection-device (NID) signal is divided into two parts, 20 pF is dedicated to deterministic noise coupling, and the other 20 pF is used to inject random noise into the substrate. Although the total coupling capacitance values in Figure 4-2 and Figure 4-5 are the same, system performance is very different for the two cases. This is because deterministic noise moves the peaks, while random noise makes the distribution wider. The larger the stochastic behavior, the lower the height of the

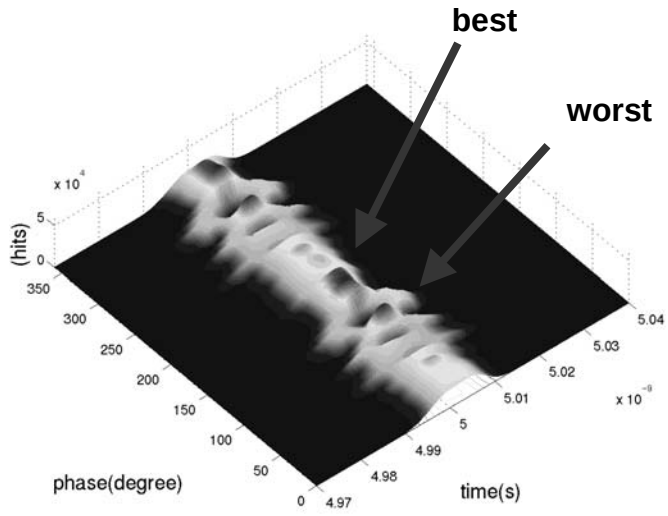


Figure 4-5 3D histogram with deterministic noise at 100 MHz, and coupling capacitance NID = 20pF (deterministic) + 20 pF (stochastic).

peak becomes, and the larger the standard deviation of the distribution. As expected, the locations of the best and worst cases are the same as the previous two cases. The standard deviation numbers of the best and worst cases are 3.106 ps and 7.379 ps, respectively.

4.2.4 Divider Output

Figure 4-6 shows the PLL performance under a multi-tone noise scenario. The NID is 40 pF in total. Half of the NID, 20 pF, is clocked at 100 MHz, and the other half is clocked and locked at 6.25 MHz (one-sixteenth of the 100 MHz clock, generated by a divider). Although the deterministic noise component will cause peak-splitting behavior in the jitter histograms, the impact is not significant in this case. This is because the divider number (sixteen) is large, and only one rising edge out of every thirty-two PLL edges will be impacted by the noise generated from the divider (F_{PLL}/F_{DNE_DIV} = 200 MHz/6.25 MHz=32). Therefore, the result in Figure 4-6 looks similar to the case shown in Figure 4-4. If the divider number decreases, the impact observed in 3D histograms will be more prominent. The standard deviation numbers of the best and the worst cases are 2.843 ps and 7.209 ps, respectively.

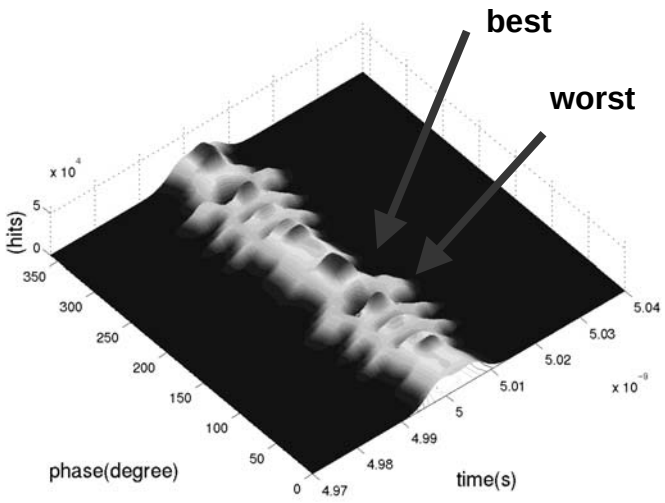


Figure 4-6 3D histogram with deterministic noise at dual frequencies, (100 MHz, and 6.25 MHz), and coupling capacitance NID = 20pF (100 MHz deterministic) + 20 pF (6.25 MHz deterministic).

4.2.5 Edge Sensitivity

As previously mentioned, the impact is closely related to the edges of noise waveforms. This section further elaborates on this argument. Figures 4-7(a) and (b) show the 2D (X-Y plane) projections of 3D histograms. The X-axis is phase in degrees, and the Y-axis is time in seconds. Clock duty cycles are set to 50% and 45% in Figures 4-7(a) and (b), respectively. By comparing the two figures, the worst case moves 18^o (i.e. 5% of 360^o) as indicated. This again confirms that the PLL output is sensitive to the DNE clock edges.

4.2.6 Phase Impact at 40 MHz

In all the results demonstrated so far, the fundamental DNE clock frequency is 100 MHz, and there are two sub-cycles observed in 3D histograms. In this section, the DNE operates at 40 MHz. Figure 4-8(a) shows the relative phase plot between the DNE clock (40 MHz) and PLL output (200 MHz). When shifting the edge positions of the DNE clock from 0^o to 360^o, the phase relative to the PLL goes through five complete cycles.

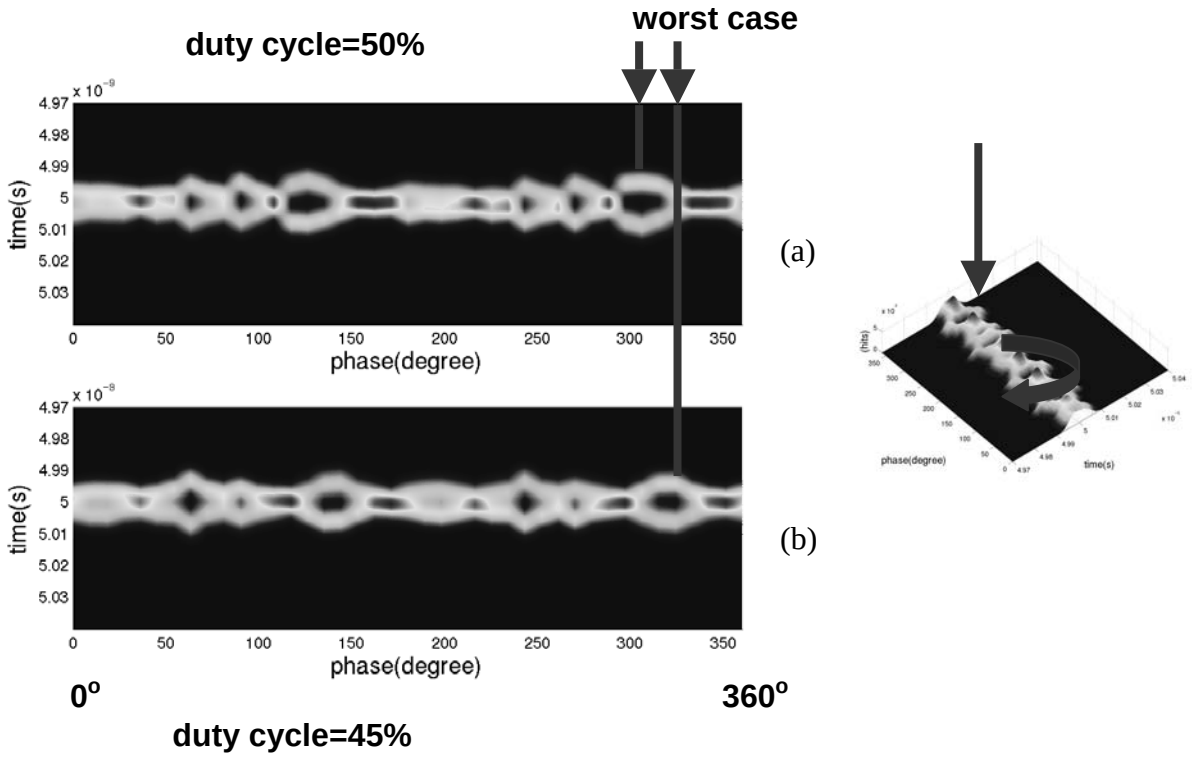


Figure 4-7 2D projection of 3D histogram: (a) clock duty cycle = 50%, (b) clock duty cycle = 45%.

This fact explains why there are five sub-cycles in the 3D histogram (Figure 4-8(b), with NID = 20 pF and deterministic noise at 40 MHz). The frequency behavior (at 40MHz) is in a category defined as sub-harmonic frequencies of the PLL output frequency (200 MHz) at a ratio of 5, reflecting the ratio between the PLL and DNE frequencies. The definition and number of the categories will be discussed in detail in the next chapter.

Figure 4-8(c) is the side-view (Z elevation) of Figure 4-8(b), from which 5 sub-cycles can be clearly observed. Figure 4-8(d) is the front-view (Z elevation) of Figure 4-8(b). It shows that the 2D cross-section of the 3D histogram can no longer be modeled using either a single or two Gaussian curves. In fact, as many as five Gaussian curves are needed for this case. In addition, the standard deviation numbers for the best and the worst cases are 3.428 ps and 6.845 ps, respectively.

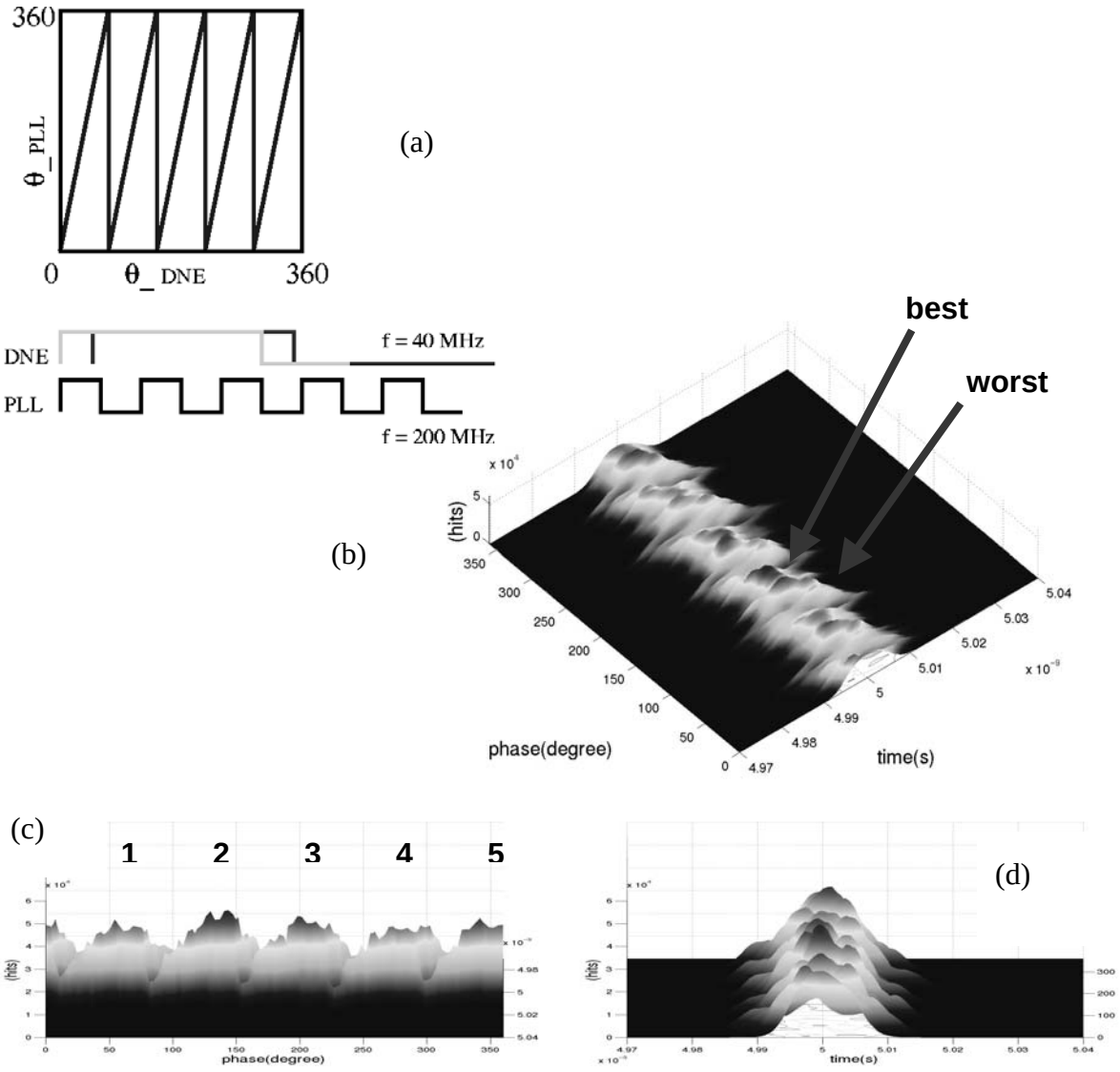


Figure 4-8 (a) Relative phase between the DNE and PLL clocks, (b) 3D histogram, with NID = 20 pF (deterministic, 40 MHz), (c) side view, (d) front view.

4.2.7 Phase Impact at 160 MHz

Figure 4-9(a) shows the relative phase plot between the DNE clock (160 MHz) and PLL output (200 MHz). Although there are also five sub-cycles in one DNE cycle, there are four lines in each sub-cycle. The four lines correspond to four consecutive rising edges of the DNE clocks, because their relative positions to the PLL clock rising edges

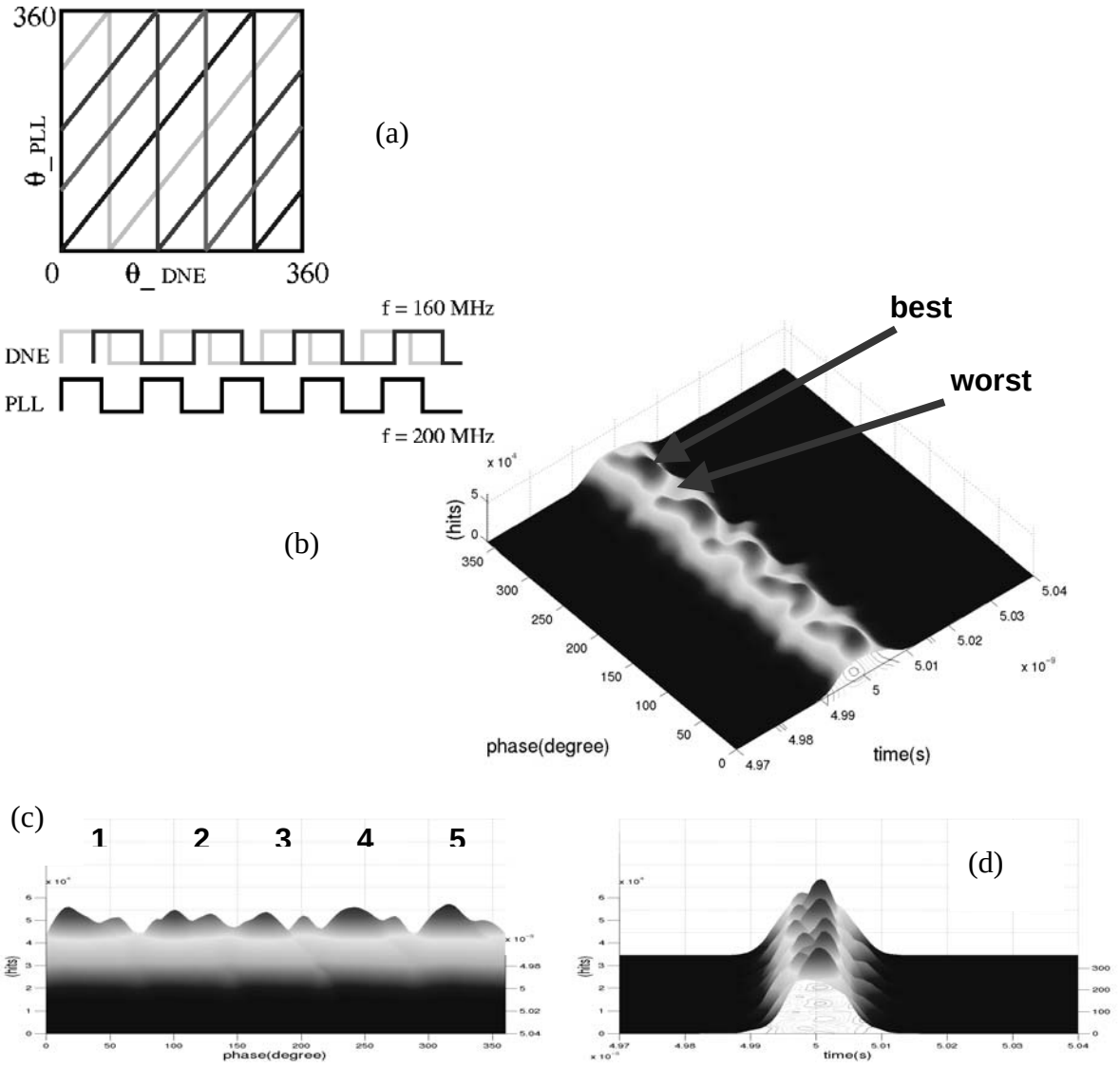


Figure 4-9 (a) Relative phase between the DNE and PLL clocks, (b) 3D histogram with NID = 20 pF (deterministic, 160 MHz), (c) side view, (d) front view.

are different. (In the 40 MHz case, all the consecutive DNE rising edges have the same relative positions, referenced to the PLL clock).

This frequency behavior (at 160 MHz) is in the category defined (in Chapter 5) as ultra-sub-harmonic frequencies of the PLL output frequency (200 MHz). The ratio between PLL and DNE clocks is 5/4. The standard deviation numbers of the best and

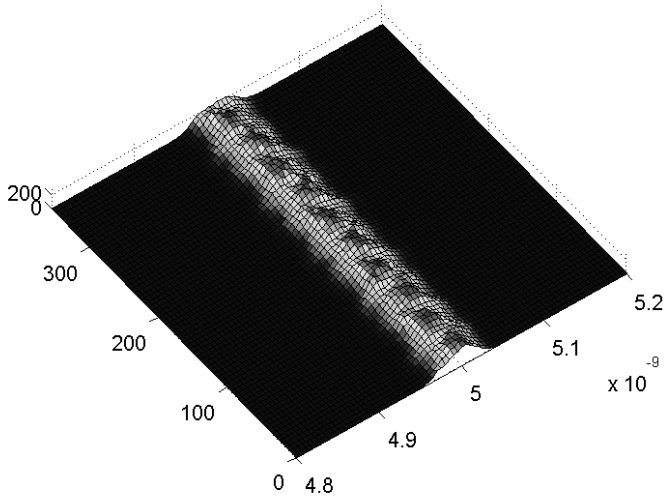


Figure 4-10 Simulation result from Verilog-A HDL, with deterministic noise at 160 MHz. (Courtesy by Jae Wook Kim).

worst cases are 3.341 ps and 4.887 ps, respectively. The 3D plot, side and front (Z elevation) views are plotted in Figures 4-9(b), (c) and (d) for reference.

4.2.8 Software Simulation

In addition to the hardware realization, a software version of the DNE [77] is implemented in Verilog-A HDL for comparison purposes. Detailed substrate network and power grid parasitic are implemented with the PLL being studied. By using the impulse sensitivity function (ISF) technique [75], the simulation results can be obtained within several tens of minutes, while it is difficult to obtain any result from transistor level simulators, for example Spectre and HSpice, in which the different time constants between the VCO and the divider output nodes in PLL systems make the simulation converge slowly.

One representative result is shown in Figure 4-10, simulating the performance of the PLL exposed to a 160 MHz deterministic noise source. It shows good consistency when compared to Figure 4-9(b).

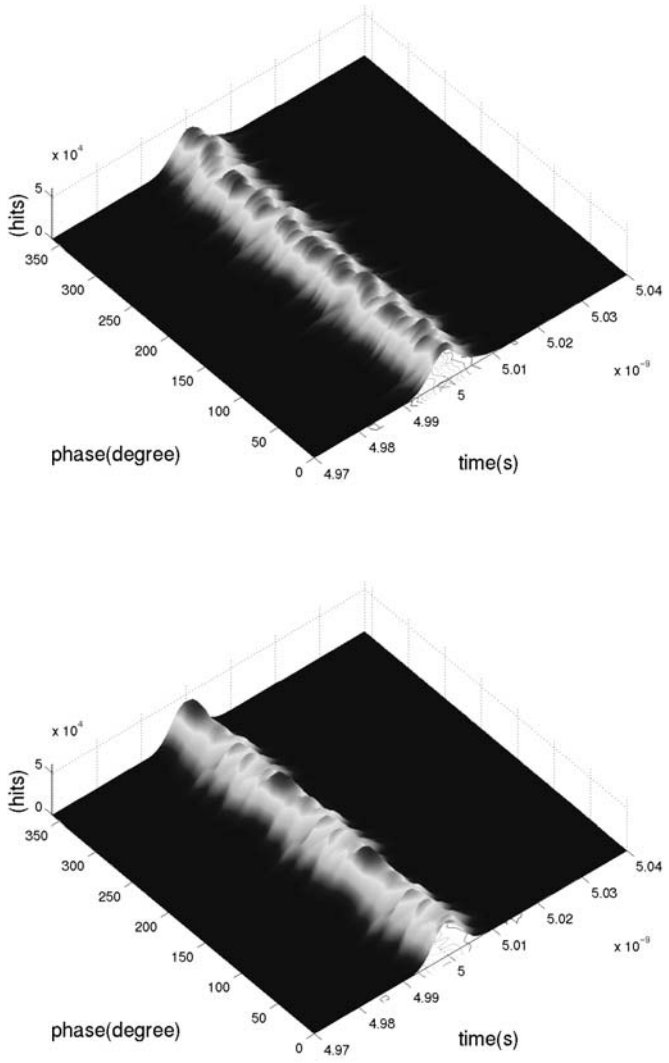


Figure 4-11 3D histogram, with coupling capacitance NID = 20 pF (deterministic): (a) clocked at 20 MHz, (b) clocked at 67 MHz.

4.2.9 Phase Impact at 20, 67, and 133 MHz

From the previous discussion, there are at least two categories of deterministic noise: sub-harmonic and ultra-sub-harmonic. As what will be discussed in the next chapter, there are two other categories, ultra-harmonic and a-harmonic. The latter two cases are not of concern in applications discussed here, since the PLL should be the highest-speed block to provide digital clocks.

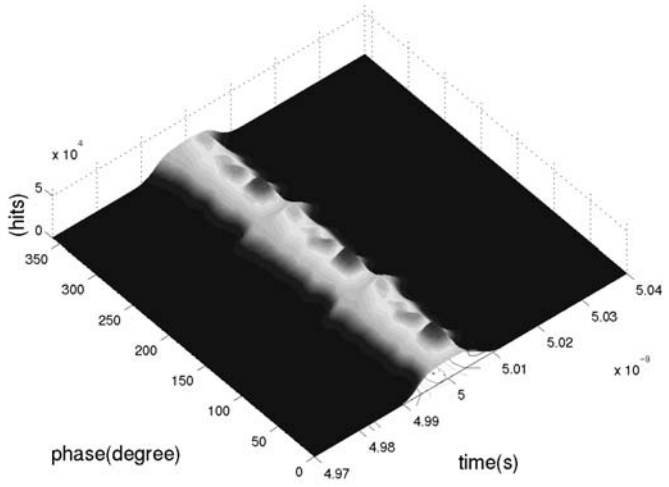


Figure 4-11 3D histogram, with coupling capacitance NID = 20 pF (deterministic): (c) clocked at 133 MHz.

To further explore the first two categories, other deterministic noise conditions that can be generated by the DNE were tested. Figures 4-11(a), (b), and (c) show the results of 20 MHz, 67 MHz, and 133 MHz deterministic cases with an injector value of NID = 20pF. As previously discussed, the numbers of the sub-cycles observed are 10, 3, and 3, respectively. The standard deviation numbers of the best cases are 3.103 ps (20 MHz), 2.446 ps (67 MHz), and 2.414 ps (133 MHz). The standard deviation numbers of the worst cases are 4.761 ps (20 MHz), 4.463 ps (67 MHz), and 4.487 ps (133 MHz).

4.2.10 Frequency Impact

After investigating the phase impact at different frequencies, this section compares two main characteristics of the PLL performance over frequency. The first parameter, σ_{max}, is the largest standard deviation jitter measured over all phase conditions at a specific frequency. The second parameter, p-p, is the largest peak-to-peak jitter observed. Figure 4-12(a) shows the value for σ_{max}, at representative frequencies selected; the results are compared to the case without any digital noise, 2.51 ps. Over frequency, the 40 MHz and 100 MHz cases are relatively worse. They are twice the frequency of the reference clock,

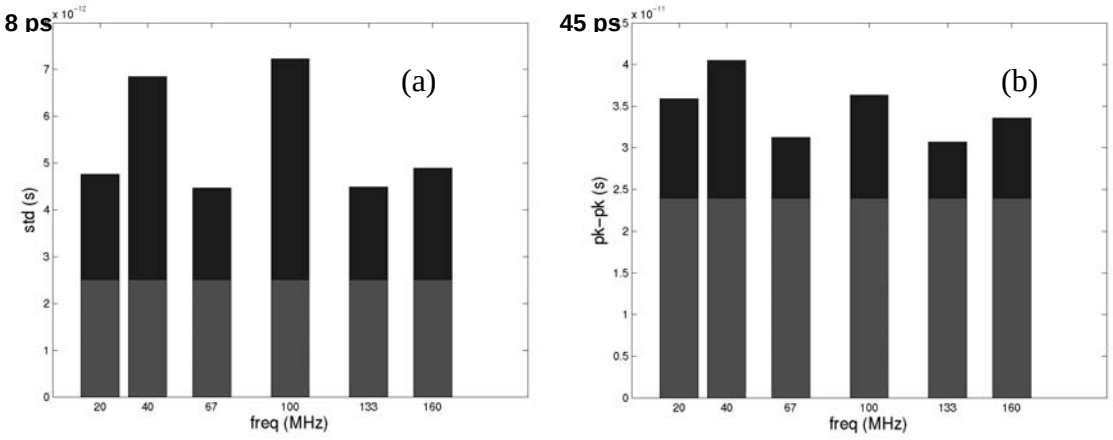


Figure 4-12 Characteristics of the jitters at different frequencies: (a) standard deviation numbers of the worst cases, (b) peak-to-peak numbers of the worst cases.

20 MHz, and half the frequency of the PLL output, 100 MHz. Figure 4-12(b) plots the peak-peak values, at the same frequencies selected in Figure 4-12(a). It shows that 67 MHz and 133 MHz give relatively smaller peak-to-peak jitters.

If the divider number in the feedback loop is changed from 10 to 8, the PLL output will become 160 MHz as discussed in Chapter 3. Though the measurement data of the 160 MHz case are not as complete as at 200 MHz, deterministic noise at 40 MHz and 80 MHz, which are twice the reference clock and half the output frequency, show generally worse PLL performance. The results are consistent with the data collected and shown in Figure 4-12(a).

4.2.11 DC Impact and Node Sensitivity

Figure 4-13(a) shows how the PLL functions at different DC biases. The DNE is not active, but the supply voltage changes from 1.6 V to 2.0 V. Histograms basically maintain the Gaussian shape, with improved performance at higher biasing voltages. From this experiment, it shows that DC shifts do not impact the system as much as AC (transient) substrate noise does.

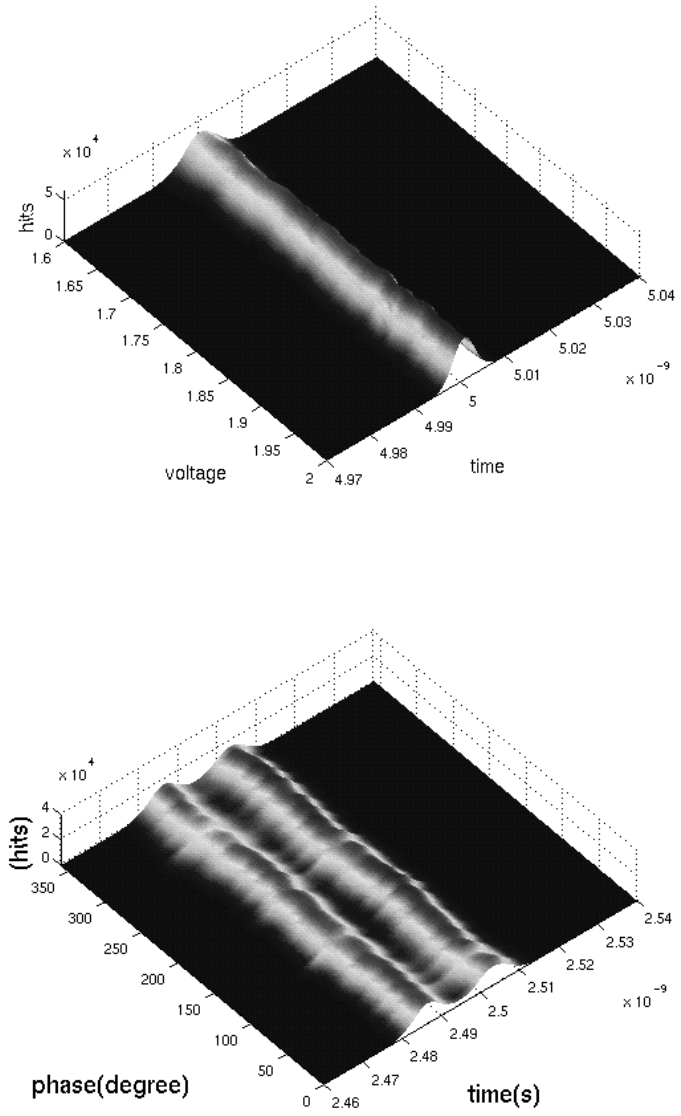


Figure 4-13 (a) Supply voltage versus histograms, (b) 3D histogram at VCO output, with coupling capacitance NID = 20pF (deterministic, 100 MHz).

Figure 4-13(b) shows the 3D histogram plotted at the VCO node, with the coupling capacitance set to 20 pF, and the deterministic noise at 100 MHz. It generates very different results from the one of the PLL output node even with identical digital noise environment (refer to Figure 4-4). Even though the noise amplitude is almost the same

everywhere on the chip because of the epi-technology adopted in this design, the sensitivity to substrate noise is different in different nodes, and circuit design styles can definitely affect the results.

4.3 Cumulative Jitter

4.3.1 Various Settings

Figure 4-14 shows cumulative "jitter versus span" for different settings at the same phase with respect to the DSN-free condition. Figure 4-14(a) is the impact from a pure 100 MHz noise source with NID = 20 pF. The minimum and maximum values of the standard deviation jitter over the span between 1 and 700 PLL cycles are 2.893 ps and 12.929 ps, respectively. Figure 4-14(e) shows the enlarged version of Figure 4-14(a) in the range between 300 and 330 PLL cycles. There are a total of 15 noise-induced cycles, from which high frequency modulation behavior (a 100 MHz noise source modulates with the 200 MHz output) can be observed.

Figure 4-14(b) illustrates the case where both deterministic noise (NID = 20 pF, 100 MHz) and stochastic noise (NID = 20 pF) are injected into the substrate. The minimum and maximum values of the standard deviation jitters are 4.246 ps and 13.25 ps. Figure 4-14(f) shows that additional stochastic noise makes the result in the enlarged region a-periodic.

Figure 4-14(c) plots the data measured from the case where there are two deterministic noise sources at 100 MHz (NID = 20 pF) and 6.25 MHz (NID = 20 pF). The minimum and maximum values of the standard deviation jitter are 3.71 ps and 16.319 ps in this case. The larger jitter partly comes from the divider block, which also injects noise into the substrate because of its intrinsically digital nature. The enlarged version, Figure 4-14(g), shows that there is one noise-induced cycle in the range between 300 and 332 PLL cycles (200 MHz/ 6.25 MHz = 32).

Figure 4-14(d) shows cumulative jitter collected from the PLL output with a 100 MHz deterministic noise source and NID = 40 pF. The minimum and maximum values of the

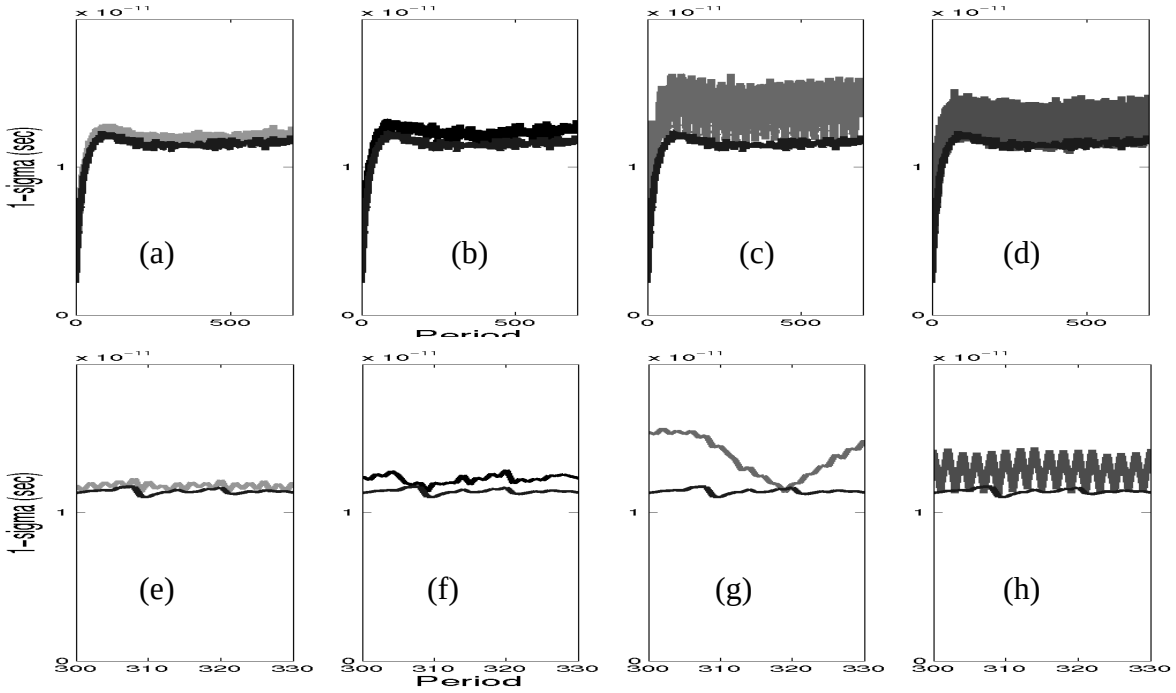


Figure 4-14 Cumulative jitter: (a) NID = 20 pF (deterministic 100 MHz), (b) NID = 20 pF (deterministic 100 MHz) + 20 pF (stochastic), (c) NID = 20 pF (deterministic 100 MHz) + 20 pF (deterministic 6.25 MHz), (d) NID = 40 pF (deterministic 100 MHz), (e) enlarged version of (a), (f) enlarged version of (b), (g) enlarged version of (c), (h) enlarged version of (d).

standard deviation jitter are 2.874 ps and 15.763 ps. As expected, a total of 15 cycles can be observed in Figure 4-14(h). Because the noise amplitude is twice as large (40 pF/ 20 pF = 2), the variance of the standard deviation jitter is larger in Figure 4-14(h) than the one in Figure 4-14(e).

4.3.2 FFT Results

Figures 4-15(a), (b), (c), and (d) are the FFT results of Figures 4-14(a), (b), (c), and (d), respectively. In all four figures, a frequency component at 100 MHz can be observed. Random noise raises the noise floor of the FFT plots, as shown in Figure 4-15(b). A 6.25 MHz peak (14.2 ps) can be spotted in Figure 4-15(c), because the one-

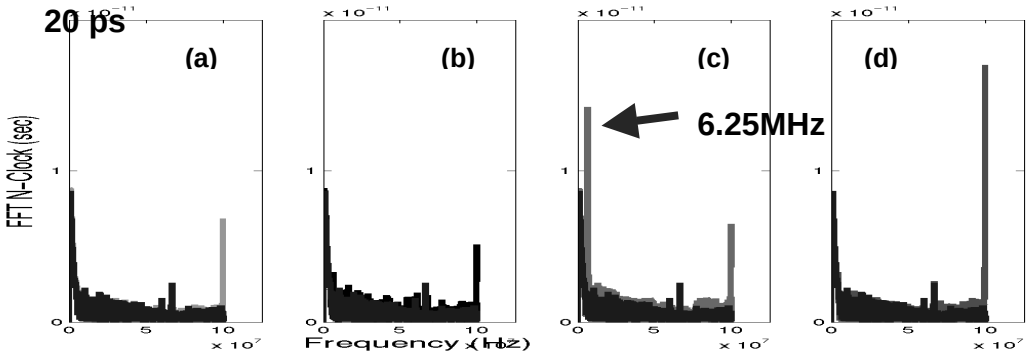


Figure 4-15 N-CLK FFT: (a) NID = 20 pF (deterministic 100 MHz), (b) NID = 20 pF (deterministic 100 MHz) + 20 pF (stochastic), (c) NID = 20 pF (deterministic 100 MHz) + 20 pF (deterministic 6.25 MHz), (d) NID = 40 pF (deterministic 100 MHz).

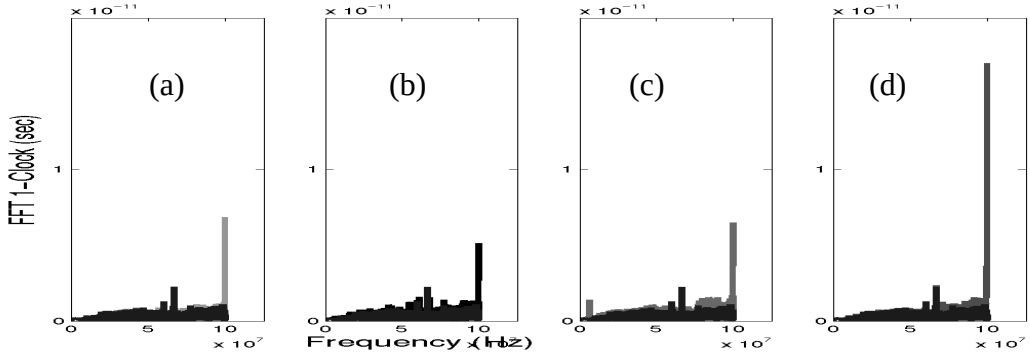


Figure 4-16 1-CLK FFT: (a) NID = 20 pF (deterministic 100 MHz), (b) NID = 20 pF (deterministic 100 MHz) + 20 pF (stochastic), (c) NID = 20 pF (deterministic 100 MHz) + 20 pF (deterministic 6.25 MHz), (d) NID = 40 pF (deterministic 100 MHz).

divided-by-sixteen divider is active. Figure 4-15(d) gives a larger peak at 100 MHz, since the NID = 40 pF is set to double the size of the NID that was used to plot Figure 4-15(a). The 100 MHz components in these four cases are 6.9 ps, 5.1 ps, 6.5 ps, and 17 ps, respectively.

As discussed in Chapter 3, the large low frequency component at around 600 KHz comes from the slope measured in the low clock cycle region seen in Figures 4-15(a), (b), (c), and (d). Figures 4-16(a), (b), (c), and (d) are obtained by normalizing the results of

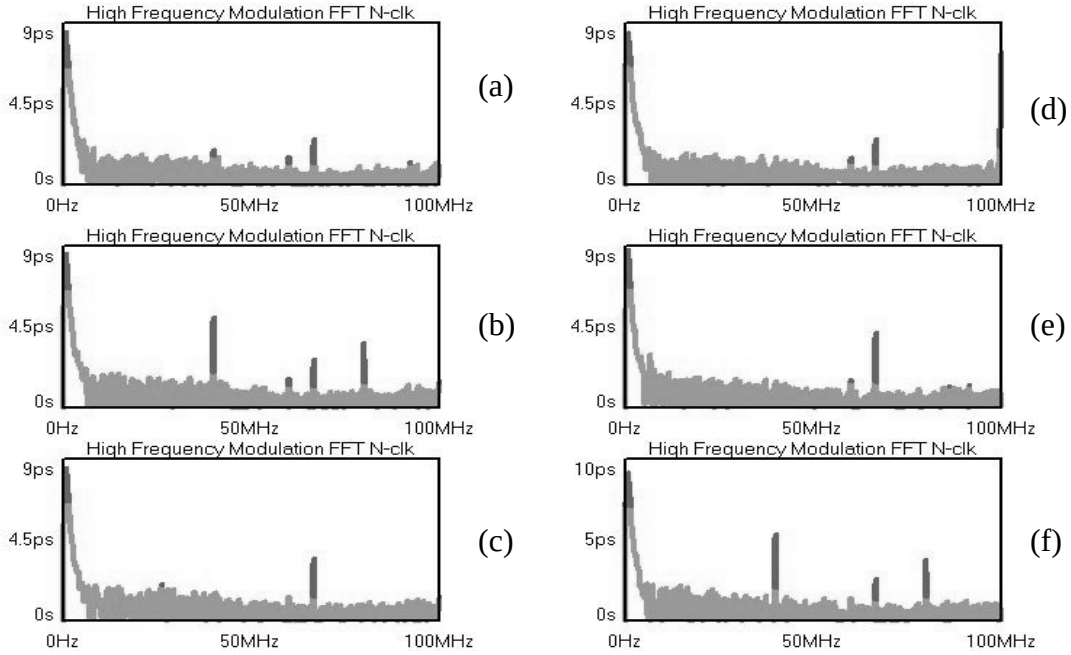


Figure 4-17 N-CLK FFT: (a) DSN free, (b) 40 MHz,
(c) 67 MHz, (d) 100 MHz, (e) 133 MHz, (f) 160 MHz.

N-CLK FFT in Figures 4-15(a), (b), (c), and (d) to 1-CLK FFT. The results imply that even the impact caused by the 6.25 MHz component is large within N clock cycles. The impact is not as significant as for the case caused by higher frequency components, since it does not impact as often. However, it is important to notice that these low frequency components coming from digital switching are still above the bandwidth of the PLL. For the device noise lower than the PLL bandwidth, the spectra will enter the loop and impact the system performance significantly.

Figure 4-17 shows the N-CLK FFT of cumulative jitters at different frequencies. Figure 4-17(a) is the plot of the DSN free case. The peaks at 40 MHz, 60 MHz, and 67 MHz are not coming from the digital noise but directly being fed from the reference clock as discussed in Chapter 3. Figure 4-17(b) shows the case with deterministic noise at 40 MHz, from which a 40 MHz peak and its harmonic, 80 MHz, can be observed. Figures 4-17(c) and (d), the sub-harmonic cases, confirm that the digital noise at 67 MHz and 100 MHz are modulated to enter the cumulative jitter. For the ultra-sub-harmonic

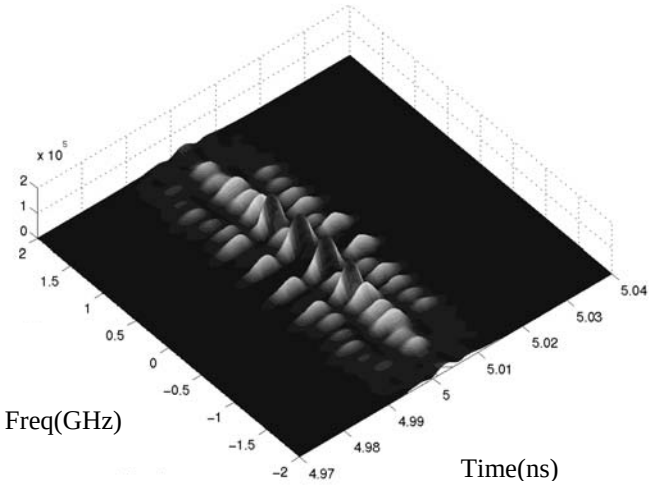


Figure 4-18 FFT of 3D histogram in phase direction (NID = 20 pF, deterministic noise at 100 MHz).

noise components at 133 MHz and 160 MHz, because of the characteristics of FFT, the frequency folding phenomena are observed in Figures 4-17(e) and (f), where the peaks are at 67 MHz and 40 MHz, respectively.

4.4 Post-Processing of Periodic Jitter Plots

This section shows two post-processing figures of the data, based on the 3D histograms of the periodic jitter. The figures, especially the negative gradient plots, provide useful information for developing possible noise cancellation scheme, which will be discussed in detail in Chapter 6.

4.4.1 FFT Plot

Figure 4-18 gives the FFT of the 3D histogram (NID = 20 pF, deterministic noise at 100 MHz, refer to Figure 4-4) in the phase direction. Peaks at 200 MHz and 600 MHz (the third harmonic) can be observed. It again supports the premise that the 3D histogram, plotted in a complete digital noise cycle, contains sufficient information to analyze the problem. The argument is valid for the cases that the digital frequencies are

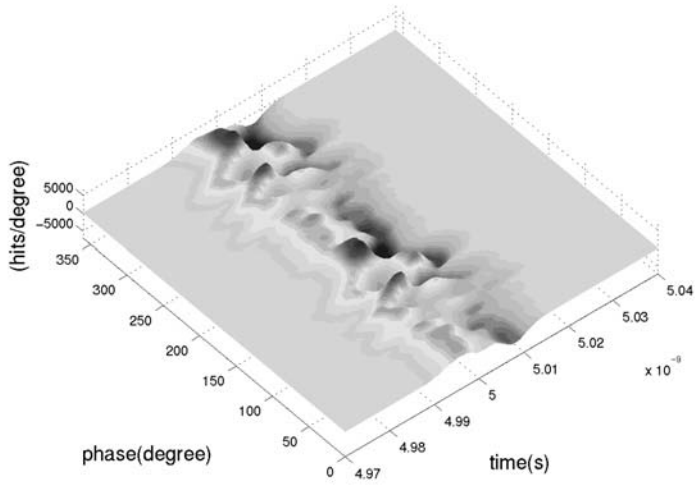


Figure 4-19 Gradient in time direction of 3D histogram (NID = 20 pF, deterministic noise at 100 MHz).

lower than the PLL output frequency. If ultra-harmonic cases are of interest, which are beyond the scope of this research and rarely seen, the 3D histogram should be plotted in a complete PLL cycle to include the necessary information.

4.4.2 Gradient Plots

Figure 4-19 shows the gradient in the time direction of Figure 4-4. The points where the gradient goes from positive to negative are the locations of peaks. Figure 4-20 is the negative gradient in the phase direction of Figure 4-4. The peaks in Figure 4-20 imply that the performance deteriorates quickly in this region. The operating points should be properly selected to avoid those regions, because of sensitivity issues.

4.5 Summary

Chapter 4 shows the measurement results from the test chip. The plots illustrate how the PLL reacts to the substrate noise under different noise conditions at different phases. The 3D histograms under different key noise parameters, including frequency, phase,

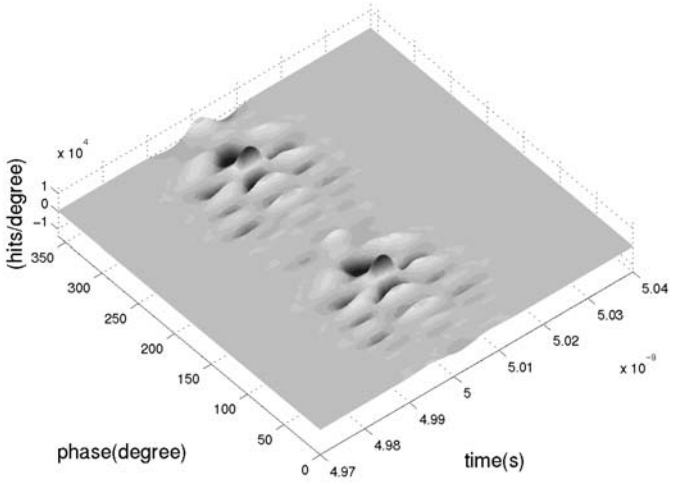


Figure 4-20 Negative gradient in phase direction of 3D histogram (NID = 20 pF, deterministic noise at 100 MHz).

coupling capacitance, and randomness of the injected noise waveform, are presented. The result also confirms that most significant impact of noise happens at the noise rising/falling edges. The measurement results include both periodic and cumulative jitters. By properly controlling the phase of the digital inputs with respect to the PLL reference clock, a 71% improvement in jitter standard deviation from the worst case relative to best case was observed from the measured results.

Chapter 5

Modeling the Impact of the Substrate

5.1 Introduction

The 3D histograms in Chapter 4 show that different types of substrate noise will give different characteristics of the PLL system. In this chapter, the details of the 3D histograms will be reviewed, followed by models and an algorithm to predict the PLL performance. The approach will be helpful in analyzing signal integrity of systems exposed to digital noise. A look-up table approach is proposed to record the necessary variables to describe the 3D histograms in a compact format.

5.2 Frequency and Phase Impact

Using a PLL as the system-under-test, Figure 5-1 depicts the possible waveforms of three important physical quantities in the noise experiments. The quantities are the PLL output voltage, digital input voltage, and current in the substrate. As previously discussed, at the rising and falling edges of digital clocks, digital blocks will inject current into the substrate, thereby, changing the performance of the PLL. For a given

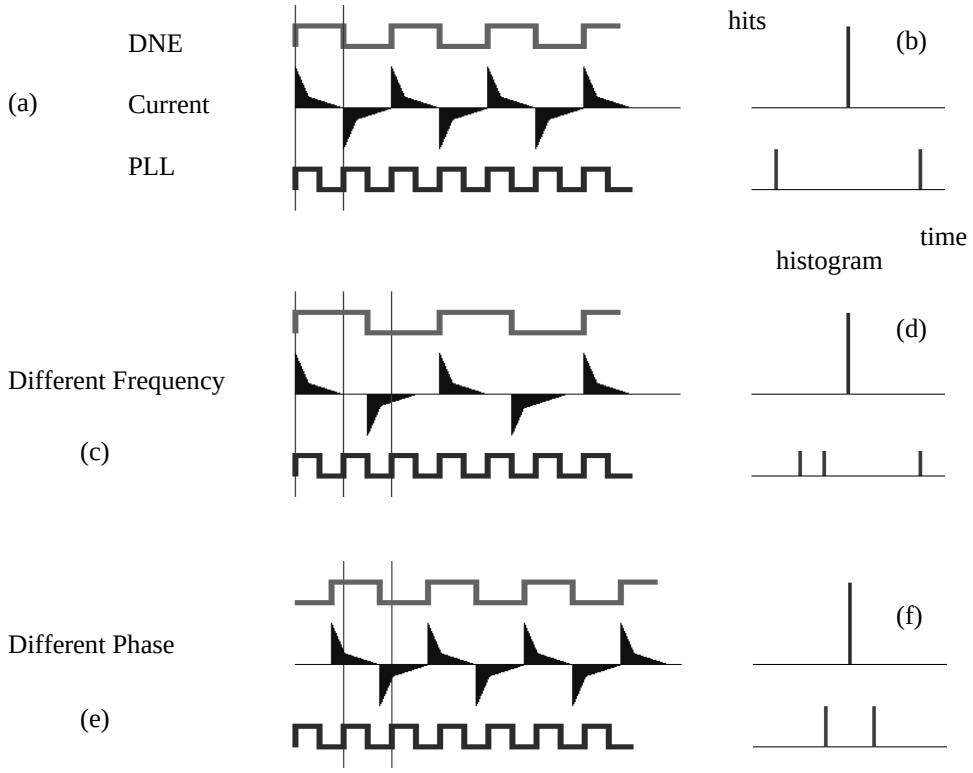


Figure 5-1 (a) Waveforms: digital clock (voltage), current in the substrate, and PLL output (voltage), (b) single peak splits into two because of dual-mode impact, (c) waveforms with digital clock at a lower frequency, (d) single peak splits into three peaks, (e) waveforms with digital clock at different phase, (f) new peaks are at different locations from (b) because of phase differences.

noise frequency (half PLL output frequency in this example) at a specific phase, the two consecutive PLL outputs will be impacted differently (Figure 5-1(a)). The waveform of noise current repeats every two cycles, thus causes the PLL output to have two different cycle lengths. As a result, the single peak (ideal case) in the histogram splits into two smaller symmetric peaks (dual mode, splitting factor = 2), Figure 5-1(b). Because the splitting factor also comes from relative phases between the PLL output and digital clock, the splitting factor equals the number of sub-cycles observed in the 3D histograms.

Figure 5-1(c) shows the waveforms similar to Figure 5-1(a), but the digital clock is at a different frequency. The substrate current measured at each PLL rising edge corresponds

to three different cases, and each case repeats every three PLL cycles. This explains why the single peak of the DSN-free case splits into three asymmetric but equally high peaks (splitting factor = 3) in the histogram as shown in Figure 5-1(d).

Figure 5-1(e) is obtained by shifting relative phase between the digital clock and the PLL output. The noise condition repeats every two cycles as discussed in Figures 5-1(a) and (b), however, the substrate current measured at the rising edges of the PLL output are different between the two cases because of phase differences. Therefore, the positions of the peaks in Figure 5-1(f) should be different from the ones in Figure 5-1(b).

Based on the measurement results in Chapter 4 and the above discussion, the number of sub-cycles in the 3D histograms and the shape of their 2D cross-sections are highly dependent on the relationships between the digital noise frequency, F_{CLK}, and the PLL output frequencies, F_{PLL}. This relationship can be classified using the equations:

$$m \cdot F_{CLK} = n \cdot F_{PLL}.$$

where:

(1) F_{CLK} is sub-harmonic of F_{PLL}: $m \in N, n = 1$,

(2) F_{CLK} is ultra-sub-harmonic of F_{PLL}: $m, n \in N - \{1\}$,

(3) F_{CLK} is ultra-harmonic of F_{PLL}: $m = 1, n \in N - \{1\}$,

(4) others: $\frac{n}{m} \notin Q$.

In practice, the in-band noise to analog/mixed signal blocks is always the fundamental or higher harmonics of the digital frequency ($m \geq n$). Therefore, cases (1) and (2) are examined in more detail here. Figures 5-2(a) and (b) show the phase relations between PLL output and digital clocks in two sub-harmonic cases (PLL 200 MHz, noise 100 MHz in (a), 66.7 MHz in (b)). The number of splitting factors and the sub-cycles in sub-harmonic cases are defined as the ratio between PLL and noise frequency. As the phase of the deterministic noise varies from 0 to 2π, there are cycles with respect to the digital

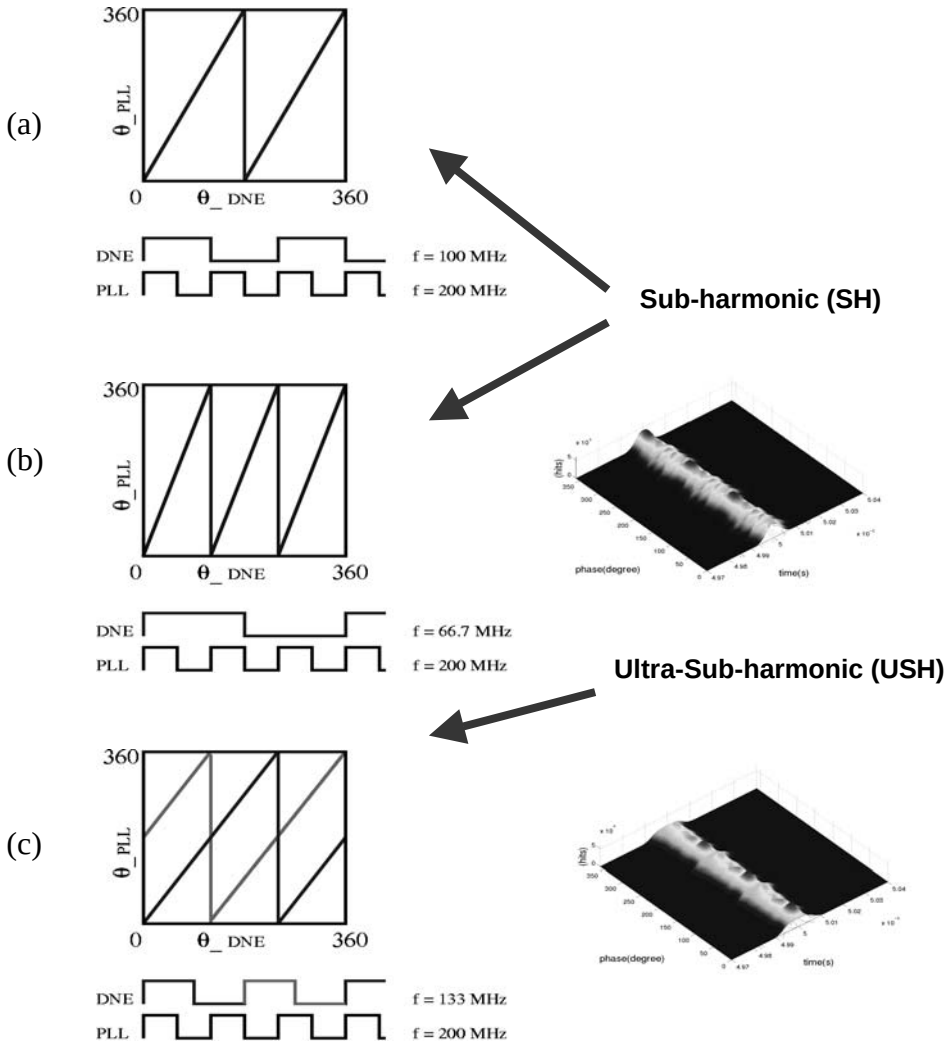


Figure 5-2 Relative phase between PLL output, and digital noise, (a) sub-harmonic, F_{PLL} = 200 MHz, F_{CLK} = 100 MHz, (b) sub-harmonic, F_{PLL} = 200 MHz, F_{CLK} = 66.7 MHz, (c) ultra-sub-harmonic, F_{PLL} = 200 MHz, F_{CLK} = 133 MHz.

phase variation (2 cycles in 100 MHz case and 3 cycles in 66.7 MHz case, with saw-tooth shapes).

Figure 5-2(c) depicts the case for ultra-sub-harmonics (digital noise at 160 MHz). The splitting number in ultra-sub-harmonics is defined as the numerator of the ratio between PLL and noise frequencies. The phase plot depicting the phase relations between the PLL and the noise shows that there are three sub-cycles when digital clock phase varies from 0 to 2π.

Freq	m	n	K	Class
200	1	1	1	SH
100	2	1	2	SH
66.67	3	1	3	SH
50	4	1	4	SH
40	5	1	5	SH
160	5	4	5	USH
133.3	3	2	3	USH
80	5	2	5	USH
7^.5			1	O

Table 5-1 A summary of numbers, m, n, and K, at representative noise frequencies (PLL 200 MHz).

To have additional examples, with the PLL operating at 200 MHz and noise running at 50 MHz and 150 MHz, the number of splitting factors and sub-cycles equals 4 for both cases. The splitting numbers, K, determine the shape of clock histograms. In chip realizations, since there are stochastic perturbations, the K sharp peaks in Figure 5-1 will expand into K bell-shaped groups. In some cases, the distributions will merge and appear as a smaller number of groups. Nevertheless, at most K groups can be observed.

Table 5-1 gives a summary of the numbers, m, n, and K, at some representative noise frequencies. If the ratio between F_{PLL} and F_{CLK} is not rational, the result is similar to the purely stochastic case; therefore, the splitting factor is defined as 1, which means that the histogram can be modeled using a single bell-shaped curve.

Splitting factors can also be observed in trajectory plots. As suggested by dynamic system theories [89-91], a PLL system can be expressed as:

$$\dot{x}(t) = A(x,t) + B(x,t)u(t),$$

where x is a vector containing state variables. Figure 5-3(a) shows a typical trajectory plot of the state variables, x_1, x_2,…x_n. The number of state variables of the system

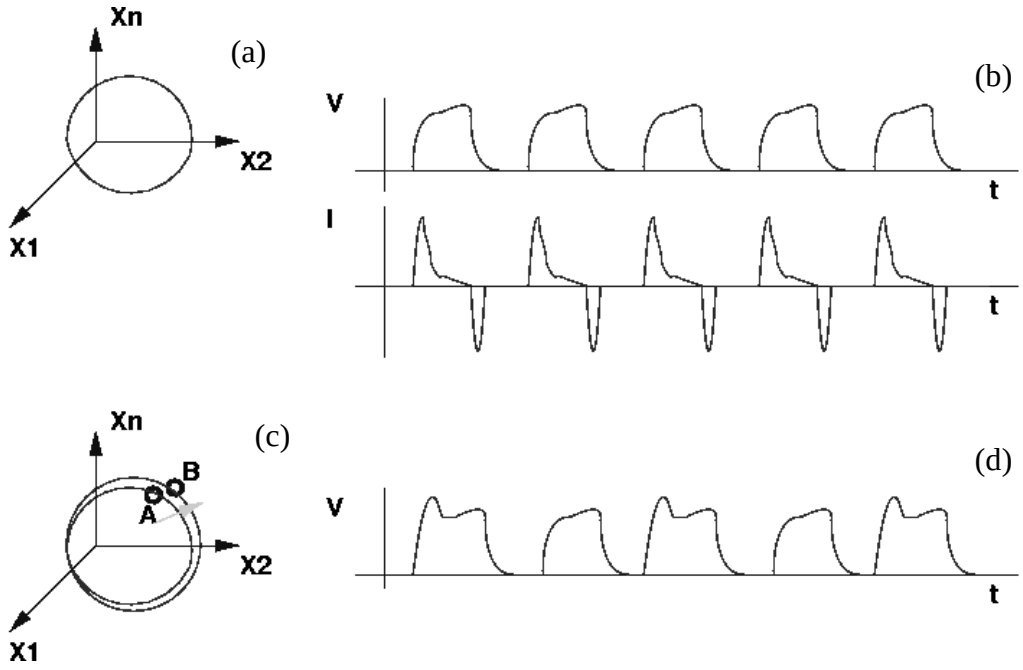


Figure 5-3 (a) A typical PLL trajectory plot w/o DSN impact, (b) typical voltage and current waveforms measured at output nodes w/o DSN impact, (c) possible PLL trajectory plot under DSN impact, (d) possible voltage waveform measured at the output node.

determines the dimension of the trajectory plots. For an ideal PLL, the trajectory will be a closed loop repeating every clock cycle. The state variables can be either voltage across a capacitor or current flowing through an inductor. Figure 5-3(b) gives an example of voltage and current waveforms measured at the output node if there is no DSN.

For sub-harmonic and ultra-sub-harmonic cases discussed above, the cycle-lengths will be observed at K distinct values, and repeat every K cycles. This causes loop-splitting behavior in trajectory plots. Figure 5-3(c) depicts the K=2 case. The point in Figure 5-3(a) will be split into two points, A and B, in Figure 5-3(c). A possible voltage waveform at the output node is plotted in Figure 5-3(d) for sub-harmonic case K=2. The output is impacted by DSN in a period of two cycles.

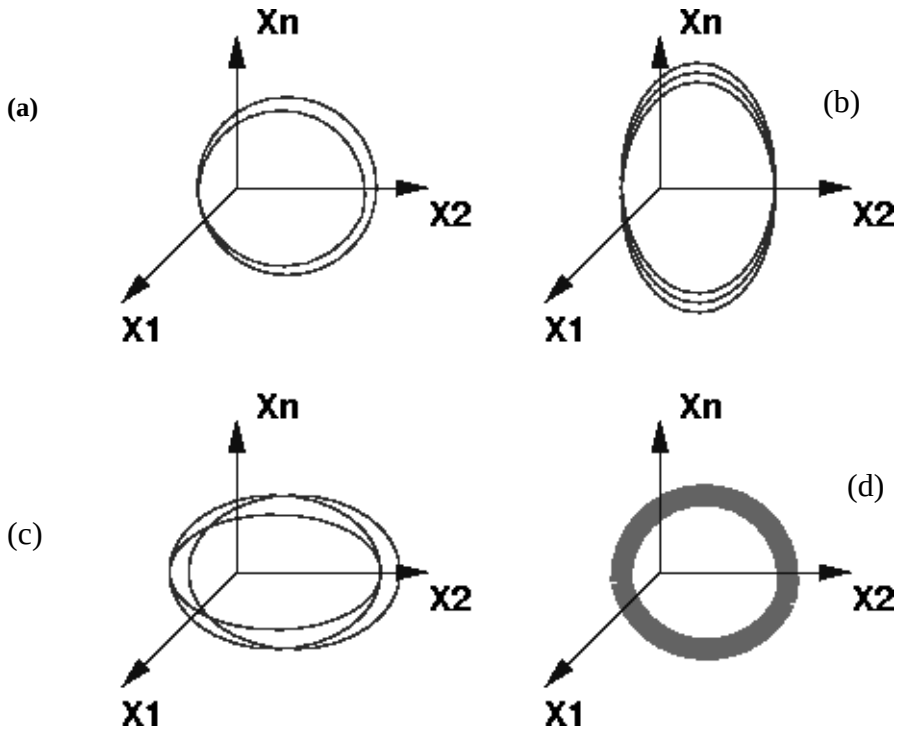


Figure 5-4 Different trajectory plots: (a) ideal PLL, (b) splitting factor K=2, (c) splitting factor K=3, (d) embedded with random noise.

Figure 5-3(c) is re-plotted in Figure 5-4(a). If the PLL is operating at 200 MHz, the two sub-loops in Figures 5-4(a) indicate that there exists a periodic noise at 100 MHz. In Figure 5-4(b) and (c), though the number of sub-loops are both three, the exact positions of sub-loops may be very different because of differences in the phases and frequencies (either could be 67 MHz or 133 MHz in these two cases).

If random noise is added to the PLL system, and assuming the perturbation is small, the trajectory plot can still be similar to the plot shown in Figure 5-4(d). The trajectories may be broadened from a narrow line to a wide band. The trace of state variables deviates from the original track, and the distance and direction changes because of the uncertainty inherent in random noise. Therefore, it is more difficult to reduce the effects from random noise. The impact caused by deterministic noise is easier to offset by introducing a correlated noise to “push” the state variables back to their original position. The technique will be discussed in the next chapter.

5.3 Data Format and Types of Models

It has been demonstrated that 3D jitter histograms provide insight into signal integrity issues of the PLL system under specific conditions, for example, in a certain switching activity pattern with a fixed coupling device size. It will be very helpful if the system performance at some other noise conditions can be estimated. Consequently, there should be a systematic way to record pre-selected data sets, and use them to predict system performance.

The raw data of jitter histograms are in a two-column format obtained directly from the output port of the SIA-3000 Signal Integrity Analyzer. The first column is the time step of the histogram, and the second one records the number of hits accumulated at each time stamp. Since the PLL is operating at 200 MHz, all the data measured are distributed within the range between 4.97 ns and 5.03 ns. The time step is about 0.6 ps, which means even a single histogram, a 2D cross-section, contains a huge amount of data, not mentioning that the 3D histogram contains several tens of these 2D cross-sections.

These data can be saved for reference in its original data format, since the price of available storage devices is relatively cheap. However, these raw data cannot provide any additional information if the noise conditions are different from the data sets saved. Therefore, either a parametric or non-parametric model, based on the measurement data, should be formulated to characterize the PLL performance under different noise conditions. The model will be especially helpful to analog/mixed signal IP providers to describe the robustness of their products.

Since the target analog/mixed signal system and the noise sources are both very complicated, it is difficult to get an analytical formula using a relatively few parameters to describe system behaviors. Therefore, analytical models are less favorable in this case. Using statistical models to fit the measurement data, and correlating the coefficients of the basis with key parameters seems to be the most efficient approach to analyze the system. The details of the statistical models will be discussed in the next section and the result is compared to the data measured.

5.4 Statistical Model

The most commonly adapted method to fit curves is the Least Square Fitting Method. Given one of the original data sets is $H_m(t_i, h_i)$, where t_i is the elements in time, and h_i is the correspondent element in the number of hits, the method is to find a representation $R_m(t) = \sum_{j=1}^{K} C_{mj}\phi_j(t)$, to minimize $\sum_{i=1}^{N}[h_i - \sum_{j=1}^{K} C_{mj}\phi_j(t_i)]^2$. The $\phi_1(t)$, $\phi_2(t)\ldots\phi_K(t)$ are the basis of the expansion, and the C_{mj}s are the coefficients of the basis.

For different data sets using the same basis, there will be different C_{mj}s. If there are L jitter histograms measured, an $L \times K$ matrix, *Coef*, can be obtained, where:

$$Coef = \begin{bmatrix} C_{11} & C_{12} & \cdots & C_{1K} \\ C_{21} & C_{22} & \cdots & C_{2K} \\ \vdots & \vdots & \ddots & \vdots \\ C_{L1} & C_{L2} & \cdots & C_{LK} \end{bmatrix}.$$

By using linear regression to correlate the *Coef* and noise condition parameters, such as frequency, amplitude and phase, a non-parametric model to estimate the system performance under different noise conditions can be constructed. The approach is documented in many numerical analysis and statistical books (for example, [92]). The only two issues left are what kind of basis should be used, and what is the proper dimension of the basis set.

The typical choices for basis set include Fourier series, polynomial basis, or B-spline. Because of the shapes of the measurement data, the bell-shape B-spline is a good candidate at first glance. A packaged tool, R [93], can be used to calculate the coefficients of the B-spline basis. For the cases with high splitting factors and number of sub-cycles, the B-spline approach generates stable results. However, for the low splitting factor cases, the parameters to model histograms can be reduced by using a Gaussian approximation. The details of this approach are discussed below.

From Section 5-2, the histograms can be treated as a summation of several Gaussian curves, which implies a jitter histogram (2D cross-section) can be described by recording

only the mean, variance, and the amplitude of the Gaussian curves. From the previous discussion, because of the device noise and digital switching noise, each peak observed in Section 5-2 corresponds to a Gaussian curve. Therefore, the number of curves equals the splitting factor corresponding to the noise frequency. However, in certain cases, the peaks are close to each other, and several Gaussian curves will merge into one and hence can be modeled by a single Gaussian curve. In these cases, the number needed is smaller than the splitting factor, and they become degenerate cases. Consequently, if deterministic digital noise is applied, the jitter histogram can be modeled as:

$H(t) = \sum_{i=1}^{K} \alpha_i \exp(-(t-\mu_i)^2/(2\sigma_i^2))$, where K is the splitting factor.

This statistical model will be discussed in detail shortly. A predicted 100 MHz result will be compared to the data measured.

5.5 100 MHz Example

5.5.1 Formulation

Given noise is at 100MHz, the splitting factor is 2. The equation to model a 2D cross-section (jitter histogram) can be expressed as:

$\hat{H}(t) = \alpha_1 \exp(-(t-\mu_1)^2/(2\sigma_1^2)) + \alpha_2 \exp(-(t-\mu_2)^2/(2\sigma_2^2))$.

Since the stochastic noise comes from the same source in these cases, the two curves should have the same shape. Therefore, the amplitudes, α_1 and α_2, can be replaced by a single number, α. This observation applies to σ_1 and σ_2 as well. And the equation is further reduced:

$\tilde{H}(t) = \alpha[\exp(-(t-\mu_1)^2/(2\sigma^2)) + \exp(-(t-\mu_2)^2/(2\sigma^2))]$.

Figure 5-5 shows the peak locations of Gaussian curves extracted from a 3D histogram, with coupling capacitance NID = 40 pF, and deterministic noise at 100 MHz.

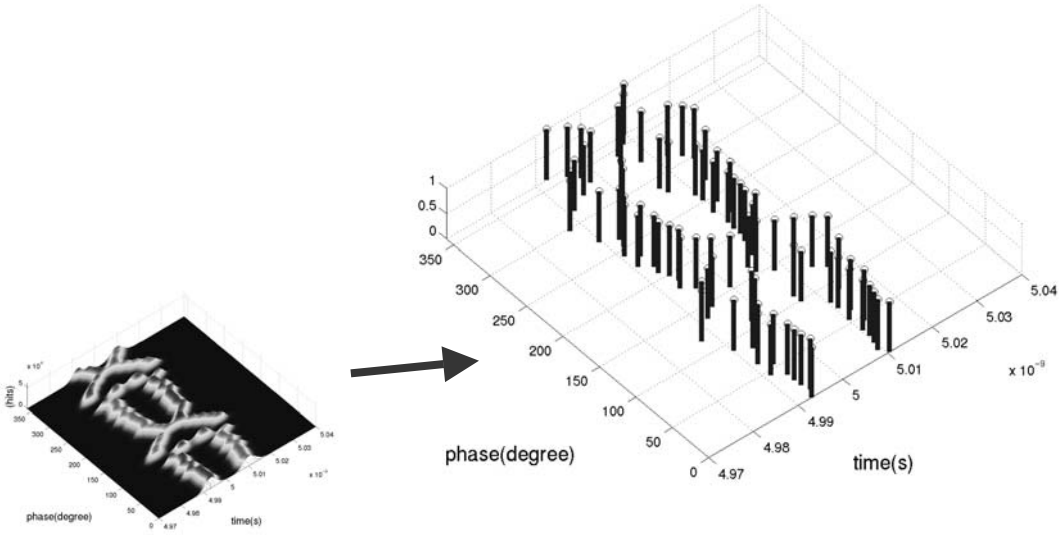


Figure 5-5 Peaks of Gaussian curves extracted from the 3D histogram, with NID = 40 pF, deterministic noise at 100 MHz.

It is clear that the number of sub-cycles is 2, which is expected to be same as the splitting factor.

By the same token, if the splitting factor is 5 (digital noise at 40 MHz or 160 MHz), as many as five Gaussian curves should be used to extract the parameters to maintain accuracy, and 5 sub-cycles can be observed. Simulation results using Verilog-A HDL [77] confirms the argument.

The Gaussian basis approach has greatly reduced the data needed to reconstruct 2D cross-sections. However, the resolution along the phase axis strongly depends on the number of 2D cross-sections available. It is a trade-off between accuracy and efficiency. In all 3D histograms demonstrated, the phase resolution is kept as fine as possible. The coarsest plot is the one of 160 MHz noise, and the resolution is 14.4^{o}. For the 100 MHz case, the resolution is 9^{o}. An interpolation method is used to provide smooth surfaces and interim data between phases measured.

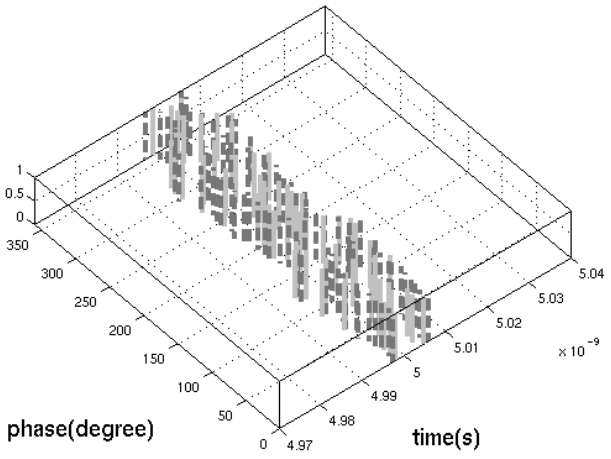


Figure 5-6 Peak locations predicted by scaling (dash line) and compared to the measurement data (solid line).

5.5.2 Linear System Model

As mentioned at the beginning of this section, the goal of the statistical model is to eventually predict the system performance at different noise conditions under which no measurement data are available due to constraints in time and cost. Assuming the system is linear, a regression method bridging α, μ and σ, with design parameters of digital blocks is complete but not necessary.

Based on the measurement results, it is found that the model prediction for different coupling capacitance values in the same digital switching pattern can be obtained by scaling the distance between μ_1 and μ_2 extracted. For example, if all the conditions in Figure 5-3 are kept unchanged except reducing the NID from 40 pF, to 20 pF, the predicted peak locations are re-scaled (assuming $\mu_1 \le \mu_2$):

$$\mu_1 \to \frac{3\mu_1 + \mu_2}{4},$$

$$\mu_2 \to \frac{\mu_1 + 3\mu_2}{4}.$$

NID=x	Freq 1	Freq 2	….	Freq M
Phase 1	$(\mu,\alpha,\sigma)_{11}$	$(\mu,\alpha,\sigma)_{12}$	….	$(\mu,\alpha,\sigma)_{1M}$
Phase 2	$(\mu,\alpha,\sigma)_{21}$	$(\mu,\alpha,\sigma)_{22}$	….	$(\mu,\alpha,\sigma)_{2M}$
:	:	:	:	:
:	:	:	:	:
Phase N	$(\mu,\alpha,\sigma)_{N1}$	$(\mu,\alpha,\sigma)_{N2}$	….	$(\mu,\alpha,\sigma)_{NM}$

Table 5-2 Look-up table for jitter prediction.

The measurement results are also plotted on Figure 5-6 for reference. It seems that differences are small, which implies the approach is feasible in the region discussed. Of course, the algorithm is only valid where linearity can be assured to retain accuracy. But the interpolation method can be used to increase the confidence level. For example, with both data sets in NID = 40 pF and 80 pF cases, the result of 60 pF case could be more accurate from interpolation than the merely scaling the distance in 40 pF case by 1.5 times.

5.5.3 Table Format

For each 2D cross-section at a specific phase and noise condition, α, μ, and σ are the three vectors containing information to reconstruct the histogram. The number of the elements in each vector equals the defined splitting factors. These three vectors consist of a unique element recorded in the look-up table, Table 5-2.

To re-build a 3D histogram, a data set including all elements in a specific column in the look-up table should be used. Since there are M columns in this example, the 3D histograms in M different frequencies can be reconstructed from this look-up table. If the linear assumption is valid, a look-up table can provide the jitter characteristics of any selection of deterministic NID values, at any phase of interest, at these pre-selected M frequencies.

In most cases, the elements of α and σ are identical throughout the entire look-up, since device noise effects are exactly the same across all peaks. In addition, because there are K sub-cycles in each 3D histogram, the elements in each column have the periodic properties with K periods.

If stochastic digital signals are injected into the substrate in addition to the deterministic digital noise, the value of σ in the look-up table should be carefully revised, because the variances of Gaussian curves are larger when compared to the original cases.

5.5.4 Reconstruction

Figure 5-7 shows two 3D histograms, where both of them are under the conditions with deterministic noise at 100 MHz, and coupling capacitance NID = 20pF (deterministic) + 20 pF (stochastic). Figure 5-7(a) is from measurement, and Figure 5-7(b) is predicted result using the model proposed.

The reconstruction process starts with a look-up table recording the peak positions showing in Figure 5-5, in which NID is 40 pF with pure deterministic switching patterns. Assuming linear noise impact, new peak locations in the case of the 20 pF pure deterministic switching pattern are shown in Figure 5-6. By adding an extra 20 pF coupling capacitance with stochastic switching patterns, the σ is modified from the extracted value in Figure 5-5, 2.5 ps, to a larger σ value, 4.0 ps. The results in Figures 5-7(a) and (b) show good consistency with each other.

5.6 Summary

Frequencies of deterministic noise can be assigned to one of the four difference classes: sub-harmonic, ultra-harmonic, ultra-sub-harmonic, and none-of-above. Each category has different characteristics of splitting factors and sub-cycles numbers. The number corresponds to the number of Gaussian curves required to model a 2D histogram. The extracted parameters associated to the Gaussian curves are recorded as the elements

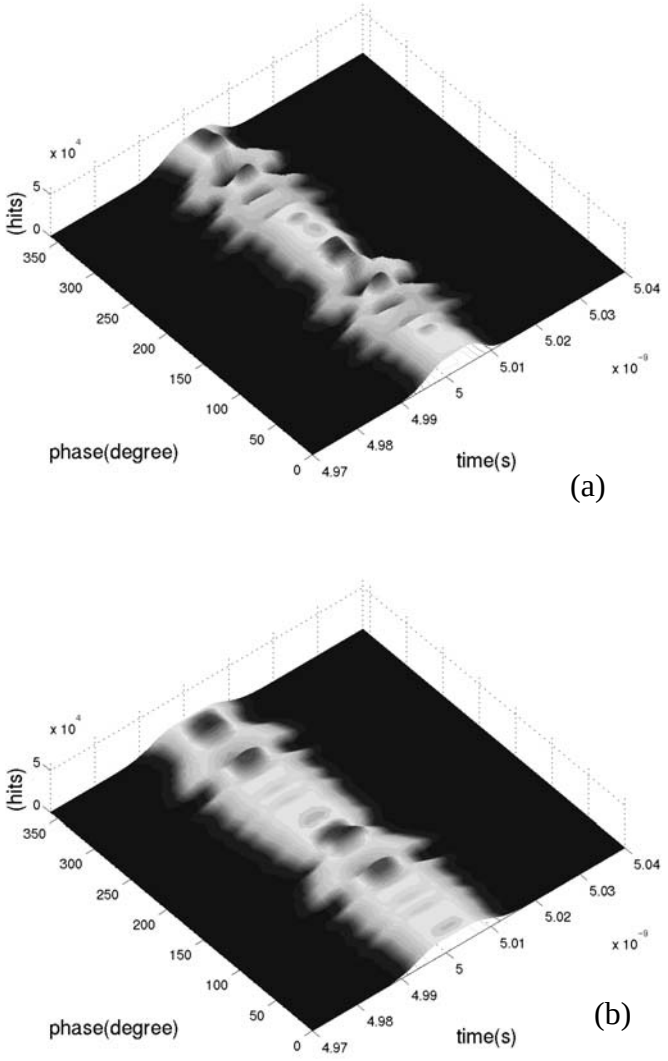


Figure 5-7 3D histogram, with deterministic noise at 100 MHz, and coupling capacitance NID = 20pF (deterministic) + 20 pF (stochastic), (a) measurement data, (b) predicted data.

of a look-up table, which is very useful to predict jitter under different noise conditions using an interpolation method (or less accurate extrapolation method).

Chapter 6

Noise Cancellation

6.1 Introduction

The DNE can be used not only to benchmark system performance but also to partially cancel deterministic noise coupled from other sources. The concept will be especially useful in SoC applications if significant frequency components in digital noise spectra can be cancelled (for example, 250 kHz in IEEE802.11a). In Chapter 6, a mathematical model is presented and followed by experimental results using a PLL as the test vehicle.

6.2 Mathematical Model

In the first configuration shown in Figure 6-1(a), with DNE off, a deterministic clock is injected to a trace on the test board and coupled to the targeted PLL. From dynamic system theory [89-91], the system can be expressed as $\dot{x}(t) = A(x,t) + B(x,t)u(t)$ in general. Given that the PLL can be modeled as a time-variant linear system, the equation can be rewritten as:

$$\dot{x}(t) = A(t)x(t) + \begin{bmatrix} B_{11}(t) \\ B_{21}(t) \\ \vdots \\ B_{n1}(t) \end{bmatrix} u(t) = A(t)x(t) + B(t) \begin{bmatrix} u(t) \\ 0 \\ \vdots \\ 0 \end{bmatrix}$$

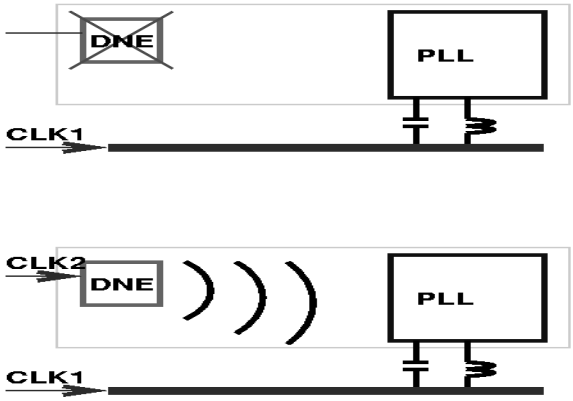


Figure 6-1 (a) Noise injected from a trace, (b) activate DNE to suppress the noise.

where transition matrix, *A(t)*, distribution matrix, *B(t)*, state vector, *x(t)*, and the noise coupled from the trace, *u(t)*, can be expressed as:

$$A(t)=\begin{bmatrix} A_{11}(t) & A_{12}(t) & \cdots & A_{1n}(t) \\ A_{21}(t) & A_{22}(t) & \cdots & A_{2n}(t) \\ \vdots & \vdots & \ddots & \vdots \\ A_{n1}(t) & A_{n2}(t) & \cdots & A_{nn}(t) \end{bmatrix}$$

$$B(t)=\begin{bmatrix} B_{11}(t) & B_{12}(t) & \cdots & B_{1m}(t) \\ B_{21}(t) & B_{22}(t) & \cdots & B_{2m}(t) \\ \vdots & \vdots & \ddots & \vdots \\ B_{n1}(t) & B_{n2}(t) & \cdots & B_{nm}(t) \end{bmatrix},$$

$$x(t)=\begin{bmatrix} x_1(t) \\ x_2(t) \\ \vdots \\ x_n(t) \end{bmatrix},$$

and $u(t)=\sum_{i=1}^{K}\alpha_i\cos(2\pi\cdot f_i\cdot t+\theta_i)+s(t)$, respectively. The elements in the state vector are physical quantities, for example, either voltage across a capacitor or current flowing through an inductance.

In the second configuration, Figure 6-1(b), by activating the DNE, extra noise is coupled through the substrate. In general, if there are (m-1) DNEs, the system equations can be revised as following:

$$\dot{x}(t) = A(t)x(t) + B(t)\begin{bmatrix} u(t) \\ u_{dne\_1}(t) \\ \vdots \\ u_{dne\_(m-1)}(t) \end{bmatrix}.$$

The optimization problem is to minimize the largest noise impact:

$$\min\{\max\{\left\| B_{j1}(t)u(t) + \sum_{k=2}^{m} B_{jk}(t)u_{den\_(k-1)}(t) \right\|\}\}.$$

Given the PLL is a periodic time varying system,

$$B_{jl}(t) = \sum_{l=1}^{K} \beta_{jl}(t)\cos(2\pi \cdot f_l \cdot t + \theta_l).$$

With no random logic in the DNE, the noise spectra generated can be approximated by:

$$u_{den\_h}(t) = \sum_{m=1}^{K} \gamma_m(t)\cos(2\pi \cdot f_m \cdot t + \theta_m).$$

The goal (in deterministic part) can be written as:

$$\min\{\max\{\left\| \sum_{p=1}^{K}\sum_{q=1}^{K} \kappa_{pq}(t)\cos(2\pi \cdot (f_p \pm f_q) \cdot t + \theta_{pq}) \right\|\}\}.$$

From the above equation, in the case of a 200 MHz PLL, with reference clock at 20 MHz and noise at 100 MHz, the major components in the output spectrum are 200 MHz, 200±20n MHz, 200±100n MHz, where n is an integer.

6.3 Experimental Results

In our experiment, *u(t)* is a 100 MHz square wave. Consequently, by properly adjusting the phase and the magnitude of the noise generated by a DNE at 100 MHz, the

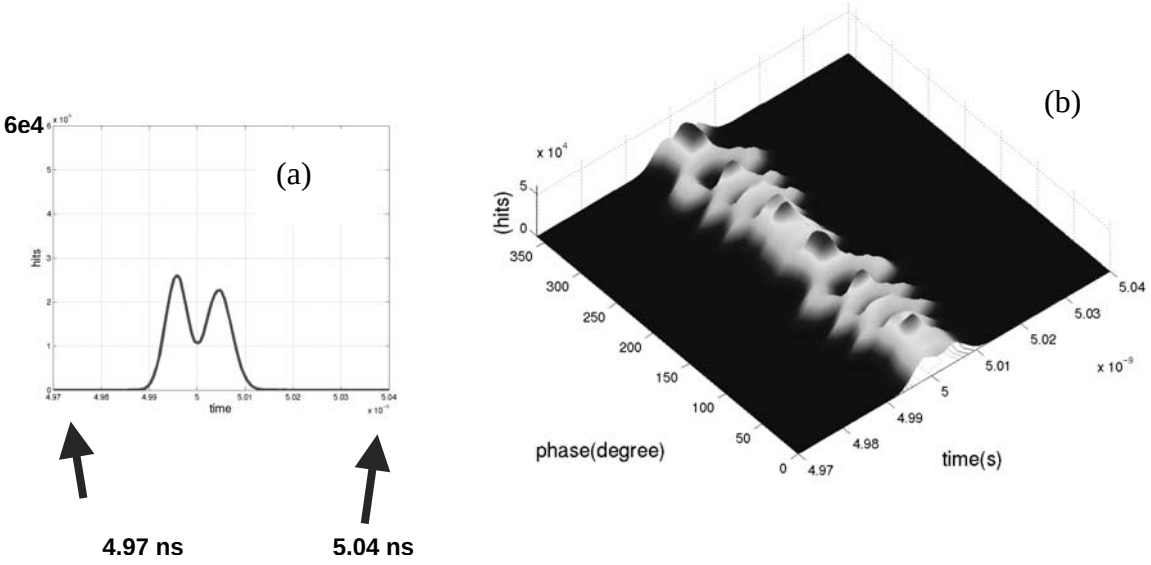


Figure 6-2 (a) Worst case with noise coupled from the trace, (b) 3D histogram, DNE at 100 MHz (with NID = 20 pF, deterministic).

optimal point can be achieved without great difficulty. In the first configuration, the worst case of the standard deviation is 5.068 ps (θ=45^o) as shown in Figure 6-2(a). In the second configuration, the phase of CLK1 is fixed at 45^o, and the phase of CLK2 is varied. The 3D plot of the activated DNE is plotted in Figure 6-2(b). As shown in Figure 6-3(a), when the phase difference between CLK2 and the PLL reference clock is in the range between –90^o and 90^o, the performance is worse. However, in the region between 90^o and 270^o, the performance is improved.

In the best case, the standard deviation is reduced from 5.068 ps to 2.501 ps, which represents a 50% improvement when compared to the case operating without the DNE in active, Figure 6-3(b). The impact caused by the deterministic noise (two peaks) is suppressed and peaks are merged, owing to the signal injection by the DNE. Figure 6-4 shows the negative gradient of Figure 6-3(a) in the direction of phase. From Figure 6-4, between 180^o and 270^o, the negative gradient is small, which implies that even when the operating point of DNE deviates from the designated point, the effectiveness of noise cancellation will not degrade too quickly because of the wide margin (90^o). Therefore, the feasibility of applying a noise cancellation technique has been demonstrated.

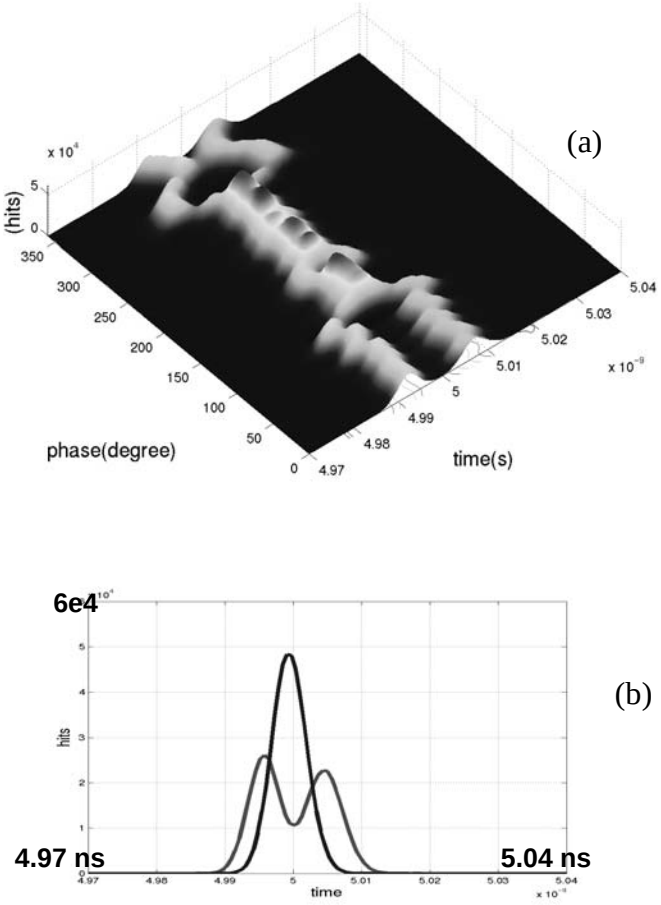


Figure 6-3 (a) 3D histogram with DNE activated; (b) comparison between the results before activating DNE and the best result obtained.

In practical digital design cases, *u(t)* could be much more complicated than the experiment demonstrated here. However, once the key deterministic components are identified, the techniques proposed in this section can be used to reasonably reduce the noise impact. It should be mentioned that this approach is less likely to be applicable for canceling stochastic noise. Namely, generation of a stochastic signal that is highly correlated to the existing random noise is not as easy as it is for the deterministic counterpart. The goal (in random part) is:

$$\min\{\max\{\left\| B_{j1}(t)s(t) + \sum_{k=2}^{m} B_{jk}(t)s_{den\_(k-1)}(t) \right\|\}\}.$$

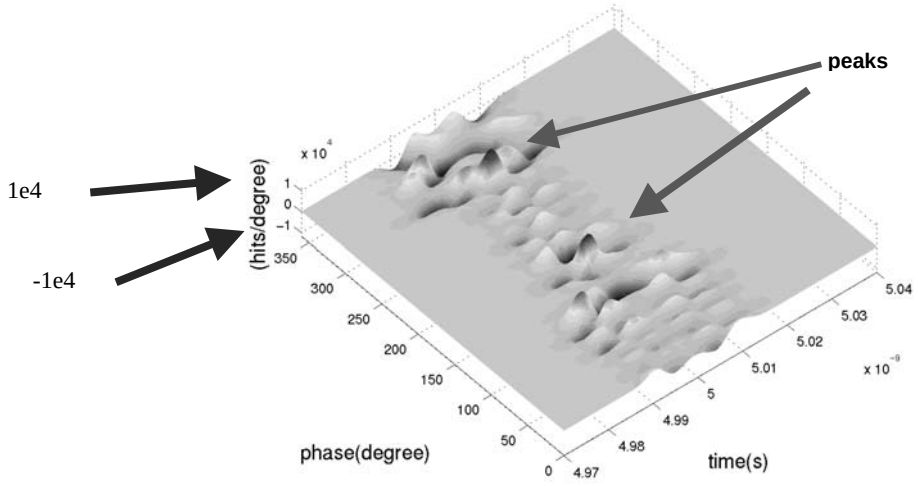


Figure 6-4 Negative gradient plot of Figure 6-3(a).

From the equation, it is clear that the results can be either constructive or destructive for random noise. In the case where random noise is dominant, more complicated cancellation systems using feedback loops and DSP techniques should be considered [34-36].

6.4 Substrate Noise and Power Grid Noise

The elements of the noise array, u(t), are not limited to substrate noise. Any power grid noise can be linearly transformed into its correspondent substrate noise, because these two types of noise are in fact connected through metal contacts. A circuit model shown in Figure 6-5 will be helpful to further elaborate this argument. The physical meanings of the components are listed as follows.

An inverter, power grids, and substrate network are included in this noise injection model. The supply and ground nets are modeled with two lumped RLGC blocks. The components associated with the power grids are: (1) line resistance, Rgnd and Rvdd, (2) line inductances, Lgnd and Lvdd, (3) capacitance between power lines and substrate,

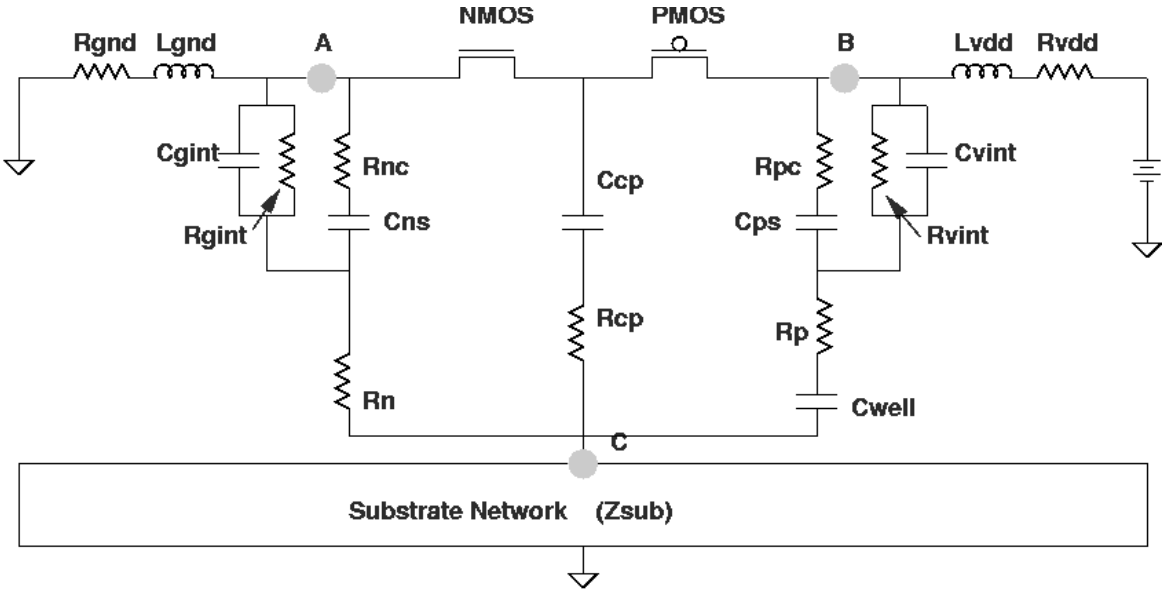


Figure 6-5 Noise injection model with circuit elements.

Cgint and Cvint, and (4) conductance between power lines and substrate, 1/Rgint and 1/Rvint. The substrate network is left as a black box, Zsub, and its characteristics depend solely on process technologies. Varied from one technology to another, the node C can be either at the boundary between bulk and epitaxial layer (epi-technology), at the boundary between silicon and SiO_2 (SOI), or a selected reference node (bulk-CMOS).

The load capacitance of the inverter is defined as Ccp, while Rcp is the substrate resistance between the surface node and the substrate node C. Rn is the resistance between the NMOS source node and the substrate node C. Rp is the resistance under the PMOS source node in the N-well region. Cwell is the junction capacitance of the N-well. Rnc and Rpc are the substrate contact resistances of the NMOS and PMOS. Cns and Cps are the source capacitances of the NMOS and PMOS. Node A and B are the two points where the transistors are connected to the power grids.

When the input to the inverter changes from high to low, the NMOS is off, and the equivalent substrate resistance between node C and ground, Z_{sub_HL} can be expressed as:

$$Z_{sub\_HL} = Z_{sub} \parallel (R_n + ((\frac{1}{sC_{ns}} + R_{nc}) \parallel R_{gint} \parallel \frac{1}{sC_{gint}}) + sL_{gnd} + R_{gnd}) .$$

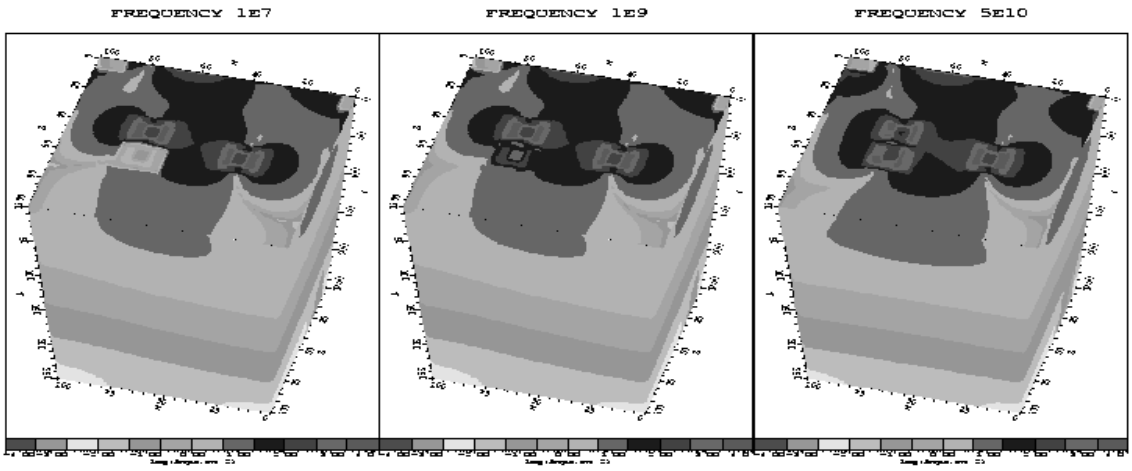
The impedance between node C and A, Z_{AC}, is:

$$Z_{AC} = (R_n + ((\frac{1}{sC_{ns}} + R_{nc}) \parallel R_{gint} \parallel \frac{1}{sC_{gint}})) .$$

If the operating frequency is relatively low, capacitances can be treated as open circuits, Z_{AC} can be simplified into $Z_{AC} = (R_n + (R_{nc} \parallel R_{gint}))$, and the major injection paths are through substrate contacts. If the operating frequency is high, Z_{AC} can be expressed as $Z_{AC} = R_n$, and capacitive coupling is treated as short circuits and they are the major paths for noise injection. For the intermediate frequencies, these two mechanisms are comparable to each other. Nevertheless, in all cases, the relation remains linear between the noise waveforms measured at either node A or C.

Similar results can be obtained for the cases when PMOS is off. The only difference is that there is a junction capacitance, Cwell, connected to Rp. In the low frequency range, because Cwell is open, the PMOS injects less noise into the substrate because of the presence of Cwell. The same reason explains why PMOS is more robust if substrate noise frequencies are low.

Figure 6-6 shows the effects of junction capacitance from a simplified structure using the device simulator, DAVINCI. The structure contains one p+ contact as an aggressor, and a pair of p+ and n+ contacts sitting symmetrically as victims on top of a p-type substrate. An AC noise signal is injected into the substrate through the aggressor. Because of the junction capacitance, current flowing through the n+ and p+ contacts are very different and are frequency dependent. For the cases at 10 MHz, most AC current is flowing to the p+ contact. Current through n+ contact increases its magnitude as frequency increases. According to the simulation results, there is no significant difference between p+ and n+ contacts when the frequency is beyond 50 GHz. Of course, the noise contour also depends on the layout geometry and doping concentration in the substrate.



(a) (b) (c)

Figure 6-6 Current contours at different noise frequencies, (a) 10 MHz, (b) 1 GHz, (c) 50 GHz.

6.5 Summary

The DNE block can be also used for noise cancellation to improve PLL performance in the presence of deterministic noise. In the experiment demonstrated in this chapter, a 50% reduction in jitter standard deviation was obtained after activating the DNE. Mathematical explanations are also included to gain more insight into digital switching noise and this noise cancellation approach. The noise sources can be either substrate noise or power grid noise in the noise cancellation model. These two noise sources are connected through metal substrate contacts, and correlated to each other.

Chapter 7

Substrate and Line Models

7.1 Introduction

In the previous chapters, the impact of substrate noise has been demonstrated. Since an epi-type substrate is used for the test chip, in the range of operation the entire substrate bulk can be treated as a single node. However, this single node assumption is not necessarily valid for other types of substrates, such as high-resistivity bulk and SOI wafers, because there are known potential differences in these substrates. In these cases, more complicated substrate models are needed. In addition, as operating frequencies increase, the quasi-static assumption is no longer valid, and magnetic coupling should be considered as well. In this chapter, different substrate models will be discussed, including a non-quasi-static model.

As discussed in the previous chapter, line inductance will also shape the spectra of substrate noise. Similar to the substrate cases, lumped models are no longer valid for power/signal lines when operating at high frequencies. However, the inductance values in the distributed model are difficult to extract because of the ambiguous return paths. In the second part of this chapter, the inductance effects and electromagnetic coupling to the substrate are discussed.

7.2 Substrate Models

7.2.1 Single Node Model

If there are no severe signal integrity concerns, primarily at low frequencies, the substrate can be treated as a perfect ground node. For the epi-type wafer case, the bulk can be modeled as a single node because of low resistivity in the bulk regions, but additional resistance effects in the epi layer should be modeled. This type of model is not suitable for either the non-epi-bulk substrate or SOI case.

7.2.2 Fully-Connected Compact Model

As an improvement to the single-node model, the compact model treats the digital blocks and analog blocks as aggressors and victims. A two-port equivalent circuit block is used to model an aggressor-victim pair. If there are N aggressors and M victims, there will be a total of N by M two-port circuits. The two-port circuit can be obtained from fitting the results of device simulations using lumped circuit elements. It can be either as simple as a π-model, or a robust wide-band model as proposed in [94].

7.2.3 Locally Fully-Connected Model

To reduce the order of the fully-connected model, a localized version of model is proposed in [32]. It suggests using fully-connected elements, but removing far-apart aggressor-victim pairs with weak interactions. By doing so, a sparse impedance (admittance) matrix can be obtained.

In the case that the number of the aggressor-victim pairs is small, a compact model formulation is a good choice. On the contrary, when the number of pairs is large, the distributed model is a better choice. This is because the complexity of compact model will grow in the order of N^2, where N is the number of sensitive nodes. Besides, the extraction process of the fully-connected model can be time-consuming because device simulation is relatively slow. Traditionally, even minor changes in the layout can require running device simulation again to extract the model parameters.

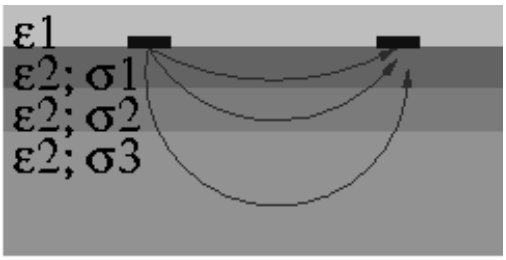


Figure 7-1 Substrate in a layered structure.

7.2.4 Distributed Model

Most commercial packages (for example, [60]) model the substrate using a distributed network, as discussed in this section, to speed up simulations. The substrate can be treated as a layered structure with different permittivities and conductivities shown in Figure 7-1. The noise propagation in the substrate follows Maxwell's equations. In a specific layer with permittivity ε and conductivity σ, Ampère's law should be written as:

$$\nabla \times \vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t} = \sigma \vec{E} + \varepsilon \frac{\partial \vec{E}}{\partial t} = (\sigma + \varepsilon \frac{\partial}{\partial t})\vec{E}\,.$$

From the null identity, divergence theorem, and using box integration [22][23] (assuming the box is in the dimension of w_{ij}, h_{ij}, and l_{ij}), the equation can be expressed as:

$$0 = (\sigma + \varepsilon \frac{\partial}{\partial t}) \oiint \vec{E} \cdot dS = (\sigma + \varepsilon \frac{\partial}{\partial t}) \sum_{j=1}^{6} E_{ij} (w_{ij} h_{ij})\,.$$

If the quasi-static condition is assumed, $\vec{E} = -\nabla V$, ($E_{ij} = \frac{V_i - V_j}{l_{ij}}$), the above equation is in the form of:

$$0 = \sum_{j=1}^{6} [\sigma (\frac{w_{ij} h_{ij}}{l_{ij}})(V_i - V_j) + \varepsilon (\frac{w_{ij} h_{ij}}{l_{ij}}) \frac{\partial}{\partial t}(V_i - V_j)]\,,$$

which means that if we define:

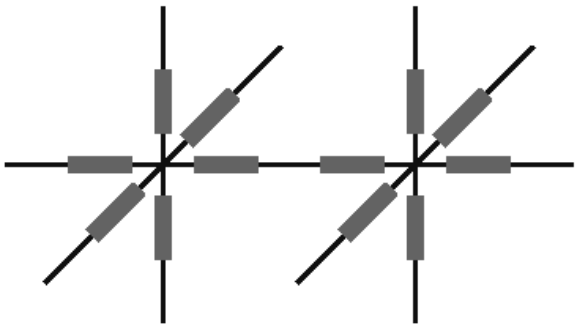


Figure 7-2 Quasi-static substrate network model.

$R_{ij} = \frac{l_{ij}}{\sigma(w_{ij} h_{ij})}$ and $C_{ij} = \varepsilon(\frac{w_{ij} h_{ij}}{l_{ij}})$, a single substrate can be modeled as concatenation of several six-branch modules as shown in Figure 7-2. Each branch has a resistance, R_{ij}, and a capacitance, C_{ij}, connected in parallel.

This extraction process is repeated in different layers to build the entire network. Therefore, the distributed substrate network is actually an RC network. If the operating frequency is low, the capacitance effect will be small. The network can be further reduced into a purely resistive network. The thickness of the layer should not exceed a reasonable value to make the box-integral assumption valid. The details of the distributed model and using the Asymptotic Waveform Evaluation to solve this RC network have been discussed extensively in the Carnegie Mellon University work [23]. This distributed model can be applied to different technologies, including SOI.

7.2.5 Non-Quasi-Static Distributed Model

As operating frequency increases, the quasi-static assumption is no longer valid. Therefore, the equation $\vec{E} = -\nabla V$, should be revised to include the non-quasi-static condition:

$$\vec{E} = -\nabla V - \frac{\partial A}{\partial t}.$$

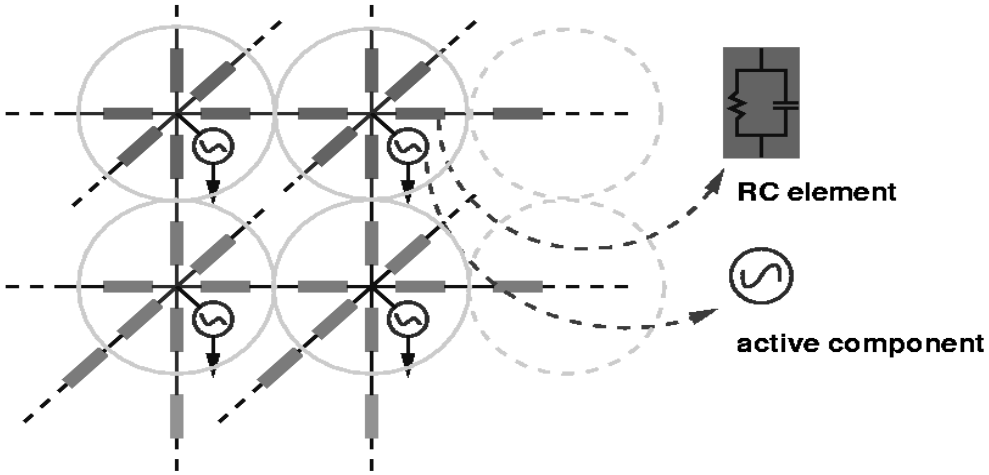


Figure 7-3 Non-quasi-static substrate network model.

When solving the equation, $0 = (\sigma + \varepsilon \frac{\partial}{\partial t}) \oiint \vec{E} \cdot d\vec{S}$, an extra term caused by the magnetic potential, *A*, should be included using the Lorentz condition for lossy dielectrics:

$$\nabla \cdot A + \mu(\sigma + \varepsilon \frac{\partial}{\partial t})V = 0 .$$

Therefore, the node equation becomes:

$$0 = \sum_{j=1}^{6} [\sigma(\frac{w_{ij} h_{ij}}{l_{ij}})(V_i - V_j) + \varepsilon(\frac{w_{ij} h_{ij}}{l_{ij}}) \frac{\partial}{\partial t}(V_i - V_j)] + GV_i ,$$

where $GV_i = (w_{ij} h_{ij} l_{ij}) \mu(\sigma + \varepsilon \frac{\partial}{\partial t})^2 \frac{\partial}{\partial t} V_i$.

An additional active element, a voltage controlled current source, should be attached to the original RC network to account for the non-quasi-static condition as shown in Figure 7-3.

If the potential varies as a sinusoidal signal at the frequency ω, the active element can be replaced by connecting a negative resistance, $\hat{R}$, in parallel with a capacitance, $\hat{C}$, to ground:

$$G = \frac{1}{\hat{R}} + j\omega\hat{C} = (w_{ij}h_{ij}l_{ij})[-2\omega^2\mu\sigma\varepsilon + (j\omega\mu(\sigma^2 - \omega^2\varepsilon^2))],$$

where $\hat{R} = \dfrac{1}{-2\omega^2\mu\sigma\varepsilon(w_{ij}h_{ij}l_{ij})}$, and $\hat{C} = (w_{ij}h_{ij}l_{ij})[\mu(\sigma^2 - \omega^2\varepsilon^2)]$.

A model using a similar concept but solved by constructing magnetic potential network can be found in [95].

7.3 Inductance Effects

The techniques to reduce power grid noise can also suppress noise in the substrate. These techniques, as previously discussed, include adopting: (1) decoupling capacitance, (2) guard ring structures, (3) differential signaling, and (4) reducing interconnect inductance.

In order to reduce interconnect inductance, good line models are necessary. Similar to the substrate models, when operating frequency increases, the lumped circuit model can no longer describe the power grids and long signal lines on chip properly. Compared to power grids and signal lines, substrates represent simple layered structures; therefore distributed models can be obtained once doping profiles are given. Distributed line models have been thoroughly discussed in [96]. However, though self-inductances of the transmission line model are easy to calculate, mutual-inductances between wires are difficult to estimate without knowing the exact current return paths.

There are extensive efforts at investigating how to extract parasitic inductances (for example, [97][98]). In Appendix A, a fast technique for estimating the bounds of on-chip wire inductance without detailed extraction is discussed. Qi [99] at Stanford University proposed an accurate method to extract the impedance of bond wires. By including good

substrate and line models, the signal integrity simulation can be more accurate in the high frequency ranges.

7.4 Electromagnetic Substrate Noise

Electromagnetic substrate noise also comes into the picture as the operating frequency increases. The term electromagnetic is used to distinguish the noise type from the electrical substrate noise discussed in the previous chapters. For electrical type noise, electrons are injected into or driven from the substrate through substrate contacts and active devices. Electromagnetic substrate noise is coupled into substrate via metal-insulator-semiconductor (MIS) interconnect structures.

Although it is difficult to tell noise types between electrical and electromagnetic noise from circuit-level jitter histograms, it is still worthwhile to distinguish them for modeling purposes if the operating frequency becomes higher than several GHz. The topic is beyond the scope of this project, because the operating frequency is only several hundred MHz for the circuits considered here. The interested reader should refer to Wang, who gives a detailed discussion on electromagnetic substrate coupling [100].

7.5 Summary

Chapter 7 reviews different existing quasi-static substrate models. As operating frequency increases, because of magnetic coupling effects, quasi-static models should be replaced with the proposed non-quasi-static model.

Reducing inductive ringing on power grids also helps to suppress noise in the substrate. The summary of inductance modeling and electromagnetic coupling are included as references.

Chapter 8

Conclusion

8.1 Recommendation for Future Research

A synthesized ring-type-VCO-based PLL is chosen as the test vehicle for noise coupling studies in this work. The PLL can be replaced with ADC, DAC, LAN, PA, or other sensitive analog/mixed signal blocks to investigate how these systems operate when exposed to substrate noise. The figures of merit (FoM) of different analog blocks will be different, and FoMs are not limited to periodic or cumulative jitter effects. For example, signal-to-noise-ratio (SNR) and signal-to-noise-and-distortion ratio (SNDR) are the two performance parameters mostly quoted for ADC designs. The suggested FoMs of typical mixed-signal designs can be found in [88]. Nevertheless, the characterization procedures proposed in this work can be applied to other analog/mixed-signal systems. A second-generation test chip with pipeline ADC and DNE block is currently being fabricated to explore these noise-coupling effects [77].

Standard silicon CMOS technology on epi-type wafers was selected for the first "PLL + DNE" test chip. To compare differences between technologies, SOI, SiGe, and non-epi-substrate can be used as alternative substrates. In theory, SOI should be more robust when compared to other technologies as shown in [19]. Nevertheless, it would be interesting to investigate the issue again using more complicated circuit blocks rather than simple coplanar test structures. Casalta [20] compared the CC and CE configurations in a BiCMOS technology. Further exploration on SiGe-BiCMOS

substrates may bring more interesting results. A third generation test chip using the IBM 7HP SiGe-BiCMOS has recently been designed and is being fabricated. Since non-epi-substrate cannot be modeled as a single node, to correlate circuit performance with aggressor locations on non-epi-substrate would be a valuable avenue for further study.

Guard ring structures can be used to reduce the impact of substrate noise. Instead of randomly including guard rings for all circuit blocks, there should be a systematic approach to address this issue. Circuit performance with and without guard ring structures should be compared quantitatively, and the results should be correlated to the geometries and locations of guard rings either analytically or statistically. Deep oxide isolation trenches as well as guard rings could be interesting topics for further study. The guard rings can be placed at various locations, with different geometries, to study guidelines for using guard rings in terms of how they influence performance and efficiency. The results could be helpful to determine if guard rings should be added near the digital noise sources to control noise injection or put next to sensitive analog/mixed blocks in order to block noise locally.

Noise cancellation is an important topic for further study. In the demonstrations presented here, a DNE is used to cancel noise coupled from a metal trace. To further elaborate on the concept, a test chip with multiple DNEs should first be prepared. In addition, it would be a useful demonstration to include practical digital blocks on the test chip as well, for example, a digital signal processor. The ultimate goal would be to cancel digital noise generated by the digital signal processor by introducing noise components generated from the DNEs. The results could be very supportive to the experimental results demonstrated in Chapter 6. Of course, further exploration of noise cancellation systems based on active guard rings [34][35], and the structure proposed by Peng at MIT [36], are also possible directions for further research.

Full wave substrate modeling may gain increased importance as the operating frequency increases. Synthesizable compact models for substrates seem promising for layout planning and verification. A software tool based on this approach would be useful. CPU time in simulations is one of the critical factors to designers in determining

if any interactive check of signal integrity needs to be included in design flows. A good behavior level simulator for noise analysis can help designers in the beginning stages of design, and it deserves more attention.

Substrate noise is closely related to power grid noise, because of the direct coupling through substrate contacts. If power grid noise can be suppressed, it will reduce the noise in the substrate as well. Therefore, it will be important to be able to assess line inductance values accurately and efficiently. System-in-a-Package only solves parts of the signal integrity problem by stopping direct coupling through the substrate. However, the coupling between inter-chip connections still exists. Digital noise can be coupled from one wire to another, and signals can be injected into the substrate via either substrate/N-well contacts or capacitive coupling between lines and substrates. Therefore, packaging and circuit board design styles should be emphasized as well.

8.2 Conclusion

Increased understanding of signal integrity issues caused by substrate noise is the prime theme and motivation of this work. Having insight into the problem will definitely contribute to further SoC research and development. This work has been focused on substrate noise modeling and noise impacts to system performance.

This work starts with the literature review of previous research in this field. Chapter 2 shows results of digital noise measured from an IEEE 802.11a wireless LAN base-band/MAC processor provided by Atheros Communications Inc. The largest noise component is at the symbol rate of the system, 250 kHz, and is explained by reviewing the system architecture. Since the significant noise behavior is architecture dependent, a low-complexity DNE is proposed to substitute for more complicated digital blocks in behavior-level modeling, based on key noise parameters. The DNE can be implemented either in hardware or software to investigate DSN impact on analog/mixed signal systems.

A test chip including a synthesized PLL provided by Barcelona Design and a DNE is fabricated through TSMC. The detailed information of the test chip and the background knowledge of PLL jitter are discussed in Chapter 3. The design of test board and arrangement of test equipment are also included. Representative noise waveforms are demonstrated. At the end of the chapter, a 3D histogram plot (histogram versus phase) is demonstrated, which can quantify the phase impact of correlated noise on PLL performance.

Chapter 4 shows the measurement results from the test chip. The plots illustrate how the PLL reacts to the substrate noise under different noise conditions with different phase. 3D histograms under different key noise parameters, including frequency, phase, coupling capacitance, and randomness of the noise waveform, are presented. The results confirm that the most significant impact occurs at the rising/falling edges of the noise signals. The measurement results show both periodic and cumulative jitter. By properly controlling the phase of digital inputs with respect to the PLL reference clock, a 71% improvement in the jitter standard deviation from the worst case, relative to best case, was observed.

Frequencies of deterministic noise can be assigned to one of the four different classes. Each category has different characteristics of splitting factors and sub-cycles numbers. In Chapter 5, a statistical model is proposed to record jitter information in the form of a summation of Gaussian curves. The model greatly reduces the order of the data that needs to be stored. Jitter characteristics under different noise conditions can be predicted using interpolation or extrapolation methods to process the parameters in the statistical model.

The DNE can be also used for noise cancellation to improve PLL performance in the presence of deterministic noise. In the experiment demonstrated in Chapter 6, a 50% reduction in jitter standard deviation was obtained after activating the DNE. Mathematical explanations are also included to increase insight into digital switching noise and the noise cancellation approach discussed in this work.

Chapter 7 first reviews existing quasi-static substrate models. As operating frequency increases beyond several tens GHz, because of magnetic coupling, quasi-static models should be replaced with a proposed non-quasi-static model. Inductance effects and electromagnetic coupling are also included to complete the discussion of signal integrity issues in substrates. Finally, this chapter provides recommendations for future research.

Appendix A

On-Chip Inductance Extraction

A.1 Introduction

Accurate integrity assessment of on-chip clock lines is difficult without any a priori knowledge about their inductance at the early stage in the design process. This section introduces an efficient approach to estimate the bounds of on-chip wire inductances. With this information, more accurate waveforms can be obtained thus greatly reducing the overall length of design cycles.

A.2 Inductance Calculation

The partial inductance (L) of an on-chip wire segment is give by [101]:

$$L = \frac{\mu_0 l}{2\pi}[\ln(\frac{2l}{w+t}) + \frac{0.2235(w+t)}{l} + \frac{1}{2}],$$

where *w*, *t*, and *l* are the width, thickness, and length of the segment, respectively. μ_o is the permeability. And, similarly, the mutual inductance (*M*) between two equal length (*l*) wires is given by:

$$M = \frac{\mu_0 l}{2\pi}[\ln(\frac{2l}{s}) + \frac{s}{l} - 1],$$

where *s* is the distance between two wires.

(a)

(b)

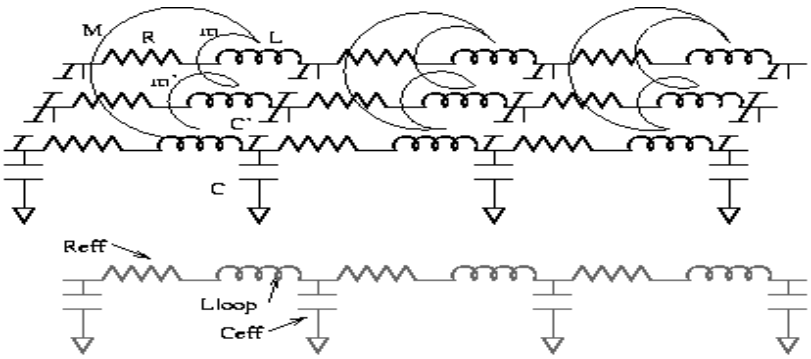


Figure A-1 (a) Distributed RLC model for wires, (b) effective loop model of (a).

Using the two equations above, the self and mutual inductances can be calculated, and be used to construct an equivalent RLC circuit model of high speed interconnects, as shown in Figure A-1(a). However, the setup is too complicated for real systems. Thus the loop inductance method should be applied, instead. In the loop inductance model, the impedance associated with the neighboring ground wires are combined into an effect value, and the equivalent circuit is further simplified from Figure A-1(a) to Figure A-1(b) without losing information on the wire interested. The loop inductance can be described as:

$$L_{loop} = L_{ss} + \sum_{K=1}^{n} 2\alpha_K M_{sK} + \sum_{\substack{I=1,\\ I\neq J}}^{n}\sum_{J=1}^{n} \alpha_I \alpha_J M_{IJ} + \sum_{K=1}^{n} \alpha_K^2 L_{KK},$$

$$\alpha_I = \frac{-Z_{gnd}}{Z_I},$$

$$Z_{gnd}^{-1} = \sum_{I=1}^{n} Z_I^{-1}.$$

where L_{ii} stands for the self partial inductance of a certain wire, M_{ij} is the mutual inductance between any two wires, and Z_I is the impedance of the return path I.

Unlike the capacitance and resistance cases, the inductance coupling is not limited to the nearest neighbor. Consequently, there should be a method to decide where the best

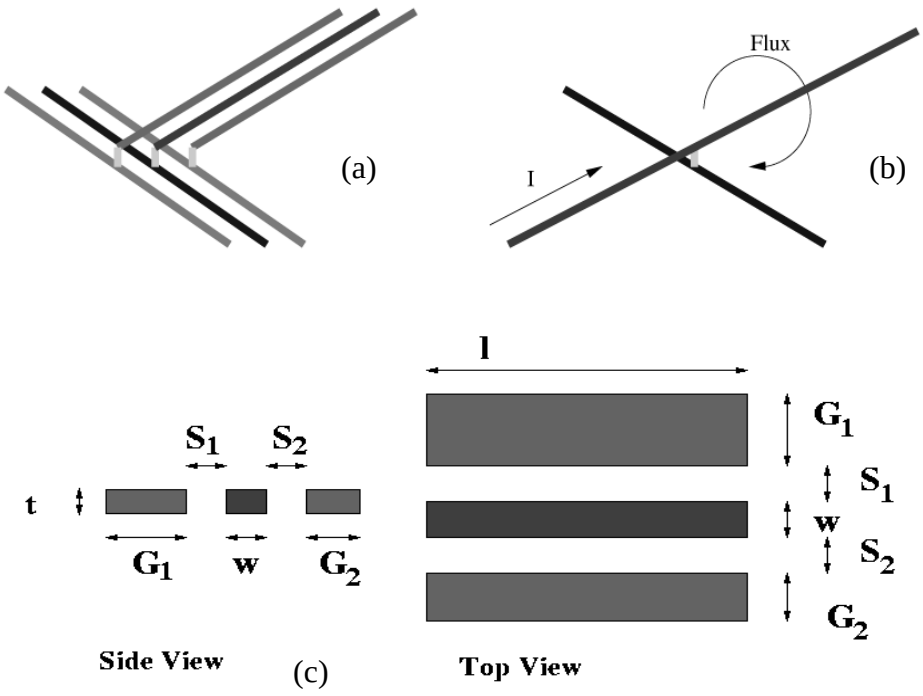


Figure A-2 (a) G-S-G configuration of high speed wires, (b) flux linkage diagram, (c) geometry information of the G-S-G configuration.

locations of the return wires are to minimize the loop inductance, or to identify the minimum available inductance on the chip.

Intuitively, it is an optimization problem:

$\min(L_{loop})$

subject to: all geometry limitations (i.e. layout rules).

In high-speed designs, three-wire configurations (ground-signal-ground, G-S-G, Figure A-2(a)) are usually seen. Therefore, it is used as an example to demonstrate how to use this concept to layout the wires to minimize the loop inductance.

Adjacent layers have small magnetic flux linkages, because of the direction of the current, Figure A-2(b). Therefore, coupling from perpendicular wires is ignored. Figure A-2(c) shows the top and side views of a G-S-G configuration. The loop inductance equation above indicates that its value is a multi-variable function, and can be expressed

as $L_{loop}(G_1, G_2, s_1, s_2)$. Since the height of wires is fixed, it is not included in the optimization process. The minimum loop inductance problem becomes:

$\min(L_{loop})$

subject to $s_1 \geq s_{\min}, s_w \geq s_{\min}, G_1 \geq w_{\min}, G_2 \geq w_{\min}$,

where s_{min} and w_{min} are the minimum spacing and metal width for a certain technology.

Using the Lagrange method [102], the Lagrangian function is:

$$\Lambda(G_1, G_2, s_1, s_2) = L_{loop} - \lambda_1(s_1 - s_{\min}) - \lambda_2(s_2 - s_{\min}) - \lambda_3(G_1 - w_{\min}) - \lambda_4(G_2 - w_{\min}).$$

Assuming the ground wires are symmetric ($s_1 = s_2, G_1 = G_2$), the function can be simplified as:

$$\Lambda(G, s) = L_{loop} - \lambda_1(s - s_{\min}) - \lambda_2(G - w_{\min}).$$

The first-order optimality conditions can be stated as:

$$\nabla\Lambda(G, s) = \begin{bmatrix} \frac{\partial}{\partial s} L_{loop} - \lambda_1 \\ \frac{\partial}{\partial G} L_{loop} - \lambda_2 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix},$$

$$\lambda_1(s - s_{\min}) = 0, \lambda_2(G - w_{\min}) = 0, \lambda_1 \geq 0, \lambda_2 \geq 0.$$

Solving the conditions above, the minimum loop inductance will occur at:

$$s = s_{\min}, G = \frac{-a - \sqrt{a^2 - 4b}}{2},$$

where $a = t + w + 2s_{\min} - \frac{2l}{0.7765}, b = t(w + 2s_{\min}) + \frac{l(w + 2s_{\min} - 3t)}{0.7765}$.

For cases where more than two return paths exist, a similar approach can be used to find the optimal solution. However, the loop inductance in those cases would always be greater than the case presented above. The reason is that the "mean" of the return paths will always greater than the s_{min}. Therefore, the lower bound of the loop inductance:

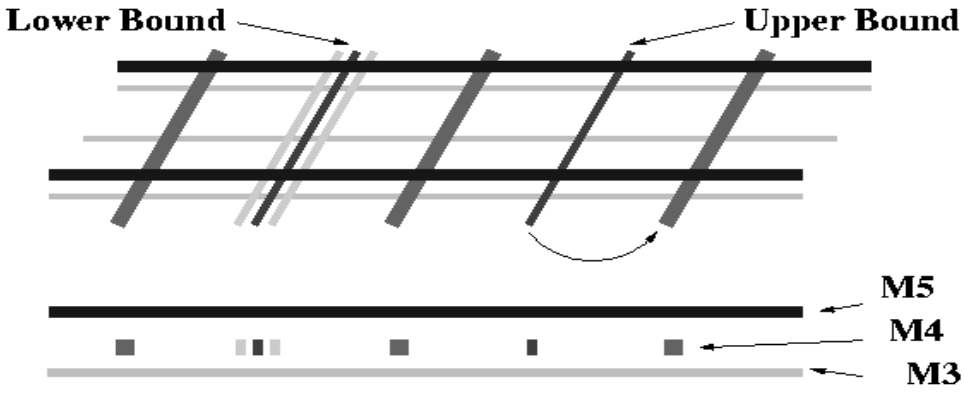


Figure A-3 Lower bound and upper bound of the loop inductances.

$$L_{loop} = \frac{\mu_0 l}{2\pi}[\ln(\frac{2l}{w+t}) + \frac{0.2235(w+t)}{l} + \frac{1}{2}] + \frac{\mu_0 l}{4\pi}[\ln(\frac{2l}{G+t}) + \frac{0.2235(G+t)}{l} + \frac{1}{2}]$$
$$- \frac{\mu_0 l}{\pi}[\ln(\frac{2l}{s}) + \frac{s}{l} - 1] + \frac{\mu_0 l}{4\pi}[\ln(\frac{2l}{2s+w}) + \frac{(2s+w)}{l} - 1].$$

For cases where there are no obvious return paths, the absolute upper bound of the loop inductance is $L_{loop} = L_{ss}$, i.e. the current returns at infinity. However, in real VLSI designs, there are always power grids distributed over the chip, which can provide current return paths. Therefore, the upper bound of the loop inductance can be found by:

$\min(-L_{loop})$

subject to $-0.5 \geq \alpha_1 \geq -1, (D-G-w)/2 > d > s_{\min}$,

where D is the distance between the power rails, G is power grid width, w is signal wire width, d is the distance between the wire and closest power grid, and α_1 is the current returning coefficient of closest power grid. The Lagrangian function can be written as:

$$\Lambda(\alpha_1, d) = -L_{loop} - \lambda_1(\alpha_1 + 1) - \lambda_2(-\alpha_1 - \frac{1}{2}) - \lambda_3(-2d + D - G - w) - \lambda_4(d - s_{\min}).$$

The first order optimal conditions should be:

$$\nabla\Lambda(G,s)=\begin{bmatrix}-\dfrac{\partial}{\partial\alpha_1}L_{loop}-\lambda_1+\lambda_2\\ -\dfrac{\partial}{\partial d}L_{loop}+2\lambda_3-\lambda_4\end{bmatrix}=\begin{bmatrix}0\\0\end{bmatrix},$$

$$\lambda_1(\alpha_1+1)=0,\lambda_2(-\alpha_1-0.5)=0,\lambda_3(-2d+D-G-w)=0,\lambda_4(d-s_{\min})=0\,,$$

$$\lambda_1\ge 0,\lambda_2\ge 0,\lambda_3\ge 0,\lambda_4\ge 0\,.$$

From above, as expected, the worst case occurs at:

$\alpha_1=-1, d=\dfrac{D-G-w}{2}$. Therefore, the upper bound of the inductance:

$$L_{loop}=\frac{\mu_0 l}{2\pi}[\ln(\frac{2l}{w+t})+\frac{0.2235(w+t)}{l}+\frac{1}{2}]+\frac{\mu_0 l}{2\pi}[\ln(\frac{2l}{G+t})+\frac{0.2235(G+t)}{l}+\frac{1}{2}]$$
$$-\frac{\mu_0 l}{\pi}[\ln(\frac{4l}{D-G-w})+\frac{D-G-w}{2l}-1].$$

The upper bound and lower bound cases are plotted in Figure A-3. The estimated range of the inductance can be used in simulators to provide more accurate information about the substrate noise in high-frequency ranges of operation.

A.3 Conclusion

A new analytical model for estimating the minimum and maximum loop inductance for on-chip RLC interconnect signal path is proposed. By avoiding the need for a field solver, this work can be used for performance estimation and design optimization during the early phase of design.

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