EXPERIMENTS AND SIMULATIONS OF GALLIUM ARSENIDE MESFET SIDEGATING EFFECTS

A DISSERTATION

SUBMITTED TO THE DEPARTMENT OF

ELECTRICAL ENGINEERING

AND THE COMMITTEE ON GRADUATE STUDIES

OF STANFORD UNIVERSITY

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

Yi Liu

December 1994

Abstract

It has been discovered long time ago that GaAs MESFET devices built on semi-insulating substrates suffer from ‘‘sidegating effects,’’ which refers to the phenomenon that the current in a MESFET decreases when a negative voltage is applied to an electrode of a neighboring device. In this work, sidegating effects are investigated by both experiments and simulations.

For experimental study of sidegating, test structures are designed and fabricated. The electrical measurements on the test structures reveal two types of sidegasting effects. One type is related to the n-i-n structure formed by the n-type region of the MESFET and the n-type sidegate. The significant reduction of the measured device current starts after the negative sidegate votlage reaches a threshold, and the substrate leakage current between the device and sidegate remains low within the voltage range of the measurement. The other type of sidegating is related to the Schottky-i-n structure formed by the gate metal overlapping on the substrate and the sidegate. In this case, the measured drain current is reduction is more severe than that related to the n-i-n structure, and the leakage current in the substrate is higher by several orders of magnitude.

Sidegating mechanisms are investigated by performing simulations using PISCES, a two-dimensional semiconductor device simulator. A trap model based on SRH theory is implemented in PISCES to take into account of deep-level traps, such as EL2, in GaAs. The simulations reveal that sidegating is a direct consequence of the expansion of the negative space-charge region in the SI substrate at the channel-substrate interface, which is caused by the trapping of electrons by the deep-level electron trap EL2.

For sidegating related to the n-i-n structure, the simulations show that a stationary high-field domain forms at the channel-substrate interface because of the negative-differential-mobility (NDM) in the velocity vs. field relation for electrons in GaAs. In the high-field domain, electron concentration increases due to the NDM, leading to enhanced electron-trapping by EL2 and expansion of the negative space-charge region. More electrons in the channel, causing the drain current of the device to decrease.

For the sidegating related to the Schottky-i-n structure, the simulations reveal that, when a negative voltage is applied to the sidegate, holes are injected into the substrate from the Schottky contact and electrons from the sidegate. This double-injection process leads to increased electron and hole concentration in the bulk of the substrate. But in the region below the channel-substrate interface, holes are depleted. This also causes enhanced electron-trapping and expansion of the negative-space charge region, leading to current reduction in the device. The double-injection, which leads to increased electron and hole concentration, also explains the high substrate leakage current obeserved in the experiments.

Acknowledgments

I would like to thank my adviser, Professor Robert W. Dutton, for his support, guidance and encouragement during this work. I would like to thank Dr. Michael D. Deal, who coordinated the GaAs project in the IC Lab at Stanford, for his guidance and encouragement. I also appreciate both Dr. Michael D. Deal and Professor C. Robert Helms for serving on my dissertation reading committee.

I would like to thank Dr. Zhiping Yu, who offered a lot of help and guidance for my research. Dr. Yu implemented the trap model in PISCES, which was very important for my simulation work.

I would like to thank Dr. Datong Chen for the disscussions that helped me understand some issues related to my work.

I would like to thank Robin King and other technicians in the IC Lab for their help on processing when I worked on the fabrication of the test structures used in the measurements.

I would like to thank my parents and grandparents for their love and support.

Finally, I want to thank my wife, Christabel, for her love, patience, understanding, sacrifices, and continuous support.

This work was supported by ARPA under Contract

Contents

List of Figures

Chapter 1

Introduction

This dissertation describes the research work on issues concerning isolation among GaAs MESFET devices: the sidegating effect and substrate leakage current. In this chapter of introduction, the properties of GaAs are first briefly reviewed. The problem of MESFET sidegating is defined and its consequence with respect to the device and circuit performances are discussed. The approach taken to study the problem in this work is then outlined, followed by a description of the organization of this dissertation.

1.1 About GaAs

When discussing the use of GaAs to build semiconductor devices, its high electron mobility has usually been mentioned as one of its advantages. At a typical doing level of $N_D = 10^{17}\,\mathrm{cm}^{-3}$, the low-field electron mobility in GaAs is $\mu_n = 4000 \sim 5000\,\mathrm{cm}^2/\mathrm{Vs}$, which is about five times higher than that in Si at compatible doping levels [1]-[4]. The drift-velocity of electrons in GaAs reaches a peak at a relatively low field around $E \approx 3.3\,\mathrm{KV/cm}$ [5]-[7]. These characteristics of the electron velocity-field relation motivated early efforts to achieve high-speed, low power devices using GaAs [8]. Some comparisons between devices built with GaAs and those with Si do demonstrated the high-speed/low-power advantage of the GaAs devices [4] [8]. But it should be realized that Si device technologies have made tremendous progress and Si devices such as bipolar and CMOS have greatly improved to meet high-speed requirements, as pointed out by Saul [9].

Another advantage of GaAs is the availability of semi-insulating substrates, with resistivity greater than $10^7\,\Omega\text{-cm}$. The semi-insulating property of GaAs substrates conveniently provides isolation among devices built close to each other. Because of the high resistivity of GaAs substrates, GaAs devices have much smaller device-to-substrate and device-to-device parasitic capacitances [2] [9], as compared to Si devices for which p-n junctions are frequently used for isolation purposes in analog circuits. And the reductions in parasitic capacitances contribute to improve speed and power-delay product of digital circuitry. The semi-insulating property has also made it possible to integrate inductors as well as capacitors, resistors and active devices on the chip, leading to the Monolithic Microwave Integrated Circuit (MMIC) [9].

The noise power generated in GaAs devices in high frequency ranges ($f > 100\text{MHz}$) is considerably lower than that in Si devices, and this makes GaAs very attractive for applications in low noise amplifiers at microwave frequencies [4] [9]. On the other hand, Flicker noise, which is proportional to *1/f*, in GaAs becomes dominant at a much higher frequency ($f \approx 100\text{MHz}$) than in Si, so GaAs is not as good for low noise amplification at low frequencies [4].

GaAs, because of its band structure, has the advantage of light emission over silicon [9], and the light-emitting diode was one of the early applications of GaAs [3]. When combined with related light-emitting materials such as AlGaAs, integration of electronic and optical functions can be achieved on the same chip [4]. Other advantages of GaAs includes better device operation at high temperatures because of wider energy band gap ($E_g = 1.424\text{eV}$ at $T = 300\text{'K}$) [9], and higher radiation hardness [4] [9].

There are certainly disadvantages associated with GaAs. Its very low hole mobility makes it impractical to build complementary devices as seen in silicon CMOS. The thermal conductivity of GaAs is only about a third of that in silicon, and low frequency noise power is high as mentioned above. Unlike silicon, GaAs does not have a stable native oxide. Moreover, a much higher density of surface energy states ($\geq 10^{12}\text{cm}^{-2}$) exists at the GaAs surface than that at the silicon surface ($\leq 10^{10}\text{cm}^{-2}$); it is also impractical to

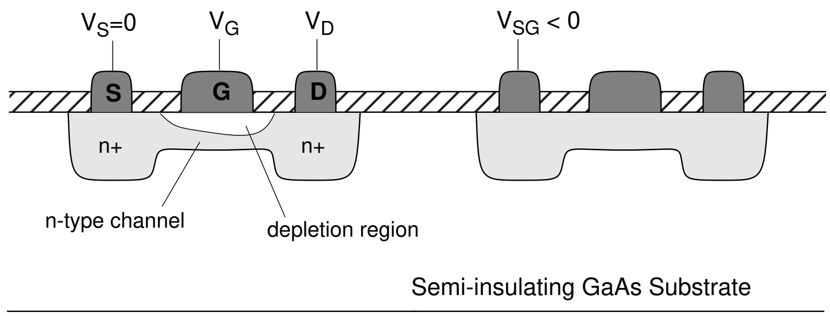


Figure 1.1 Schematic Cross sections GaAs MESFETs. The semi-insulating substrate provides isolation between devices.

produce insulated-gate field-effect transistor (IGFET) devices, such as the silicon MOSFET, with useful characteristics by depositing a dielectric films on the GaAs surface [3] [4]. A GaAs FET device employs a metal-semiconductor junction (MESFET), a p-n junction (JFET), or a hetero-junction (HFET) for its controlling gate electrode.

The GaAs MESFET has been used for microwave amplification since late 1960s, together with the Gunn and IMPATT diodes [3]. Applications of the GaAs MESFET in digital integrated circuits started around the mid 1970s, and the technology has since developed to reach LSI levels [3] and many kinds of MESFET-based circuits have been produced. The research work described in this dissertation focuses on the sidegating effect of the GaAs MESFET, which is defined in the following section.

1.2 Sidegating Effect of GaAs MESFETs

The GaAs MESFET is built by forming an n-type conductive channel, by either epitaxial or implantation methods, on semi-insulating GaAs material, as shown in Figure 1.1. A current flows between the source (S) and drain (D) in the channel when there is a potential difference ($V_{DS} = V_D - V_S$) between the two electrodes (Figure 1.1). A Schottky contact, formed on top of the channel between the source and the drain, functions as the gate (G). Because of the work function difference between the Schottky gate material and the n-type GaAs, there is a space-charge region depleted of electrons under the gate. The effective opening of the channel for current flow under the gate is less than the thickness of the n-type channel layer due to the extension of the depletion region into the channel, the width of which is controlled by the voltage bias applied to the gate (V_G). A large enough negative gate voltage will bring the channel into a “pinch-off” situation in which electrons are depleted across the whole thickness of the channel and current flow in the channel is blocked. The Schottky contact is therefore the “gating” electrode which can control the amount of current in the device and can also turn the device “on” and “off.” This function of the Schottky gate is the only desirable current modulation effect in the normal operation of the MESFET device.

There are undesirable effects on the current in the MESFET. One of these anomalies is the influence on the device current from the negative bias voltages applied to neighboring devices. Suppose two MESFET devices are built next to each other on a semi-insulating GaAs substrate, as shown in Figure 1.1. It has long been observed that the current in one of the devices is reduced when a negative voltage (V_{SG} in Figure 1.1) is applied to an ohmic type electrode of the other, and the current continues to decrease as the negative voltage increases. This kind of interaction between MESFET devices is called the ‘‘sidegating[1]’’ effect, referring to the phenomenon that the current in one device is undesirably modulated, or ‘‘gated,’’ by a ‘‘sidegate’’ — an ohmic-type electrode of the neighboring device.

Figure 1.2 is an example illustrating the sidegating effect. The normal current-voltage characteristics of a MESFET are shown in Figure 1.2(a). Each curve corresponds to a specific gate voltage value (V_G), while the sidegate voltage is zero ($V_{SG} = 0$).

1. In the literature, the term ‘‘backgating’’ has also been used for the same phenomennon. Some authors specifically used ‘‘backgating’’ to refer to the effect of an electrode fabricated on the back side of the substrate while ‘‘sidegating’’ was reserved for that of the one on the same surface of the substrate on which the device concerned was built. Since the research of this work is on the mechanisms that are fundamental to both the ‘‘sidegating’’ and ‘‘backgating’’ situations, distinguishing the two cases bears little significance. To avoid confusion, only terms such as ‘‘sidegating’’ and ‘‘sidegate’’ are used in this dissertation.

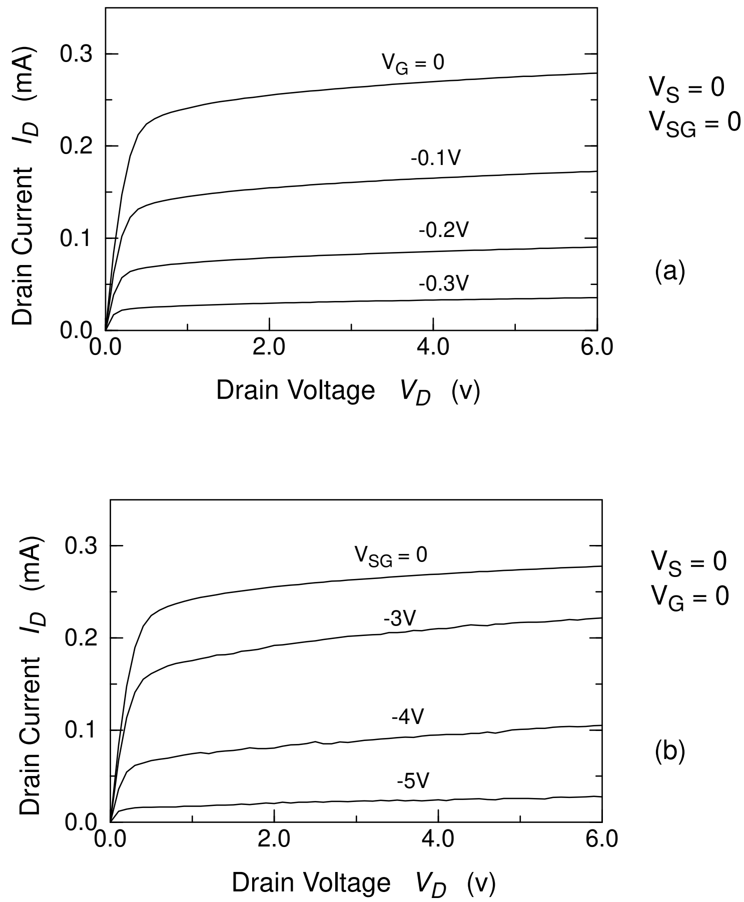


Figure 1.2 An example of sidegating effect of GaAs MESFET.

These characteristics demonstrate the modulation of the drain current by the gate (normal ‘‘gating’’). The effect of the negative sidegate voltage is shown in Figure 1.2(b). It can be seen that the drain current I_D is smaller for a greater negative sidegate voltage V_{SG}. It is evident that the current in the MESFET is ‘‘sidegated’’ by the sidegate voltage.

The sidegating effect adversely affects operations and functions of MESFET devices and circuits. In digital GaAs MESFET integrated circuits, a negative supply voltage is often used, such as in the Schottky-diode FET logic (SDFL) gate; the negative supply voltage causes the lowering of the current in the pull-up transistor [10]. The negative consequence of this effect has been demonstrated by Lee *et. al.* [11]: the gate delay of a ring oscillator formed by SDFL gates became longer for higher values of the negative supply voltage V_{SS}. The slowing down of the circuit was attributed to the reduced current driving capability of the pull-up transistor. The sidegating effect has also been found to affect the performance of MESFETs for microwave applications, as described by Itoh *et. al.* [12], who showed degradation of the s-parameters of the MESFET devices when the space-charge region at the channel-substrate interface was altered by a negative sidegate voltage.

Although sidegating phenomena have long ago been discovered and documented, sidegating has remained a not-well-understood problem. On the other hand, the issue of sidegating has become increasingly important as more and more devices are packed into circuits and placed close to each other. The sidegating problem has increasingly become a limiting factor in achieving larger scale of integration of GaAs MESFET circuits. Further advancement of GaAs IC requires better understanding of the sidegating problem so that measures can be designed to avoid, or reduce, or even eliminate this effect. This is the motivation of this research effort to study the GaAs MESFET sidegating effects.

1.3 Approach of Study

The existence of the sidegating problem indicates that the semi-insulating GaAs material is not a perfect insulator, though the convenience in isolation and the low parasitic capacitances it can offer are highly desirable for GaAs IC's. In fact the high resistivity of a GaAs substrate is achieved through the compensation of shallow impurities by deep-level centers. The MESFET devices built on the semi-insulating substrate are basically composed of n-type regions plus metal contacts of both ohmic and Schottky types. The questions concerning sidegating effects are then: (1) how a device is affected by the negative voltage applied to an electrode of a certain distance away; (2) how some properties unique to the semi-insulating material, such as the existence of large amount of deep-level centers, are related to sidegating; (3) under what conditions sidegating takes place; (4) how some properties of carrier transport in the substrate material are related to sidegating; and (5) what details of device structures also affect sidegating. The purposes of this research effort are to find a physical basis for the answers to these and related questions and to provide understanding of basic mechanisms of sidegating effects.

The investigation of the sidegating problem consists of two parts: experiments and computer simulations. The experimental part includes test structure design, device fabrication, and electrical measurements of sidegating effects. The test structures were specifically designed for studying sidegating effects, allowing the issues related to the problem to be investigated experimentally. The purposes of the electrical measurements on these test structures are to identify different types of sidegating effects, reveal the correlation of sidegating to other isolation problems such as substrate leakage current, clarify some observations that have been misinterpreted in the literature, and provide clues on possible physical mechanisms.

The other part of the work on sidegating is computer simulation using PISCES, a two-dimensional semiconductor simulator [13] [14]. Based on certain assumptions about factors that influence sidegating, the effects of electron and hole deep-level traps, the presence/absence of carrier injection electrodes, and the electron drift-velocity vs. field characteristics in GaAs are each investigated. Simulations results are compared to experimental observations. The simulations provide calculated distribution profiles of potential, field, charge, carriers, and deep-level traps occupied by electrons or holes, which reveal information on how sidegating takes place. By analyzing simulations results, knowledge can be gained on basic mechanisms of sidegating effects.

1.4 Organization of the Dissertation

Chapter 2 is a brief review of early research on the topic of sidegating published by others in the literature. Theories and models proposed by other to explain experimental observations are described and discussed. This brief review identifies the questions that have remained to be clarified and helps to define the goals of experimental work and simulations of this research effort.

Chapter 3 first provides some background information on GaAs MESFET technologies with respect to how the conductive layer for the n-type channel of a device is formed. The process procedures for fabrication of the test structures used in the electrical measurements of this work are then described. The results of basic DC characterization of fabricated devices are also described.

Chapter 4 describes the electrical measurements of sidegating and discusses the information revealed by the measurement results. The effects on sidegating of a metal contact fabricated on the undoped substrate are experimentally investigated. The correlation between sidegating and substrate leakage current are also studied by monitoring the current at the sidegate. The sidegating and leakage current characteristics are discussed to clarify how they should be interpreted. The implications of the measurement results are also discussed, based on which suggestions of possible mechanisms are made.

Chapter 5 describes the work of computer simulations of the sidegating effects based on certain assumptions, using an enhanced version of PISCES. The effects of electron and hole traps, the role of a Schottky type metal-substrate contact, and the effect of negative-differential-mobility of electrons in GaAs are all investigated. Simulation-generated distributions of electron and hole concentrations, electric field, charge, and occupancy of deep-level centers are analyzed. The conditions under which negative space-charge is created in the substrate at the channel-substrate interface of a device are discussed to provide a basis for understanding the underlying mechanisms responsible for sidegating effects. Three types of sidegating mechanisms are analyzed: (1) the trapping of electrons; (2) the double-injection and electron-trapping; and (3) the de-trapping of holes.

Chapter 6 summarizes the work on the sidegating effects and leakage current, lists the conclusions that can be drawn, points out the contributions this research effort to the understanding of the sidegating problem, and make suggestions for the work that can be done in the future.

Chapter 2

A Brief Review of Early Studies of Sidegating Effects

In this chapter, published results related to the sidegating effect and substrate leakage current are described, and theories and models proposed to explain experimental observations are discussed. This brief review identifies the questions that need to be clarified with respect to sidegating and leakage current problems. It is also helpful to define the purposes of the experimental studies and the simulations which will be described and discussed in following chapters.

2.1 Effect of Channel-Substrate Interface

In the normal operation of a GaAs MESFET, the current in the channel should only be modulated by the current-controlling electrode, the Schottky gate. The current modulation is achieved through changing the width of the space-charge region, which results from depletion of electrons, by applying a voltage bias to the Schottky gate. Another space-charge region exists at the channel-substrate interface, which results from the difference in Fermi level positions within the bandgap in the n-type channel and in the semi-insulating substrate [15] [16]. The positive charge on the channel side of the space charge region is provided by the ionized donors, and the negative charge on the substrate side results from the combined effect of shallow-level impurities and deep-level centers. It can been seen in Figure 2.1 that electrons are depleted from both the gate and the channel-substrate interface and space-charge regions are formed. For a device built by implanting dopants directly into a substrate the channel-substrate interface is not as sharply defined as that shown in Figure 2.1, in which the uniformly doped channel is terminated at a certain depth. For a device built by growing epitaxial layers on a substrate, although the interface between the channel and the substrate is well defined, localized states at the interface may lead to potential distributions, such as that of a back-to-back junction [17], that deviate from that shown in Figure 2.1. In either case the space-charge associated with the channel-to-substrate transition is always present.

It has long been recognized that some anomalies of MESFET operation are associated with the channel-substrate interface [17]-[24]. Among these undesirable effects is the sidegating effect. Many early studies of the sidegating effect of MESFETs were done on devices built by growing epitaxial layers on Cr-doped SI substrates [17] [19] [24]. Drain current reduction in the MESFETs was observed when the substrates or buffer layers were negatively biased relative to the devices [17] [19] [21] [22] [24], which was attributed to the increase of negative space-charge density on the substrate (or buffer) side at the channel-substrate (or channel-buffer) interface. By means of charge balance, the width of the space-charge region on the channel side increases correspondingly by depleting electrons, extending further into the channel, leading to a thinner conductive channel and hence a smaller channel current. In some cases the drain current reduction starts from zero or very low values of the substrate biases [21] [22]. In many early studies of the sidegating effect, no results on substrate leakage currents were reported.

Models proposed in those early studies by different groups to explain the sidegating effect have the common character that the channel-substrate (or channel-buffer) interface behaves in a way similar to that of a reverse-biased pn-junction when the substrate (or the buffer layer) is negatively biased. Some of these models also assumed that all of the applied negative voltage was dropped across the interface [19] [21] [22] [24]. The increase of the negative charge density or the expansion of the negative space-charge region on the substrate (or buffer) side was attributed to trapping of electrons or emission

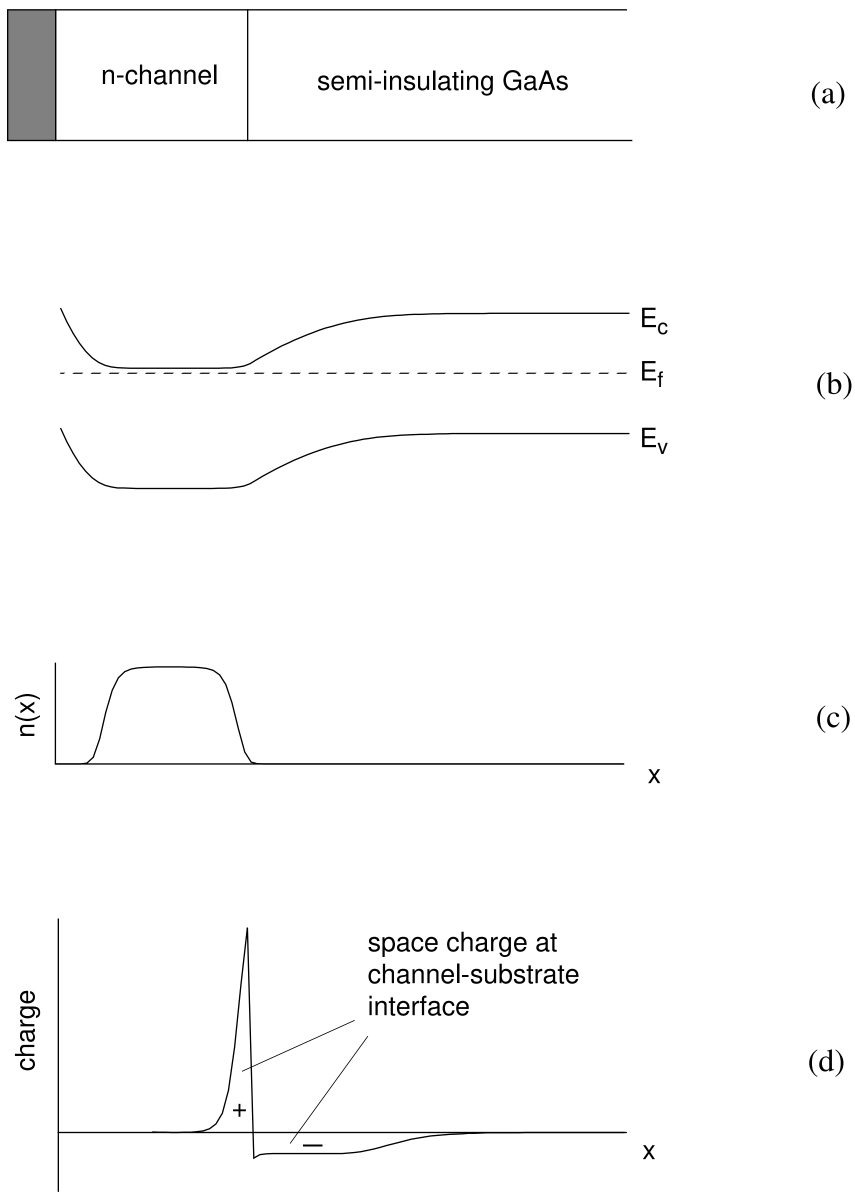


Figure 2.1 Profiles along the metal-n-channel-SI GaAs substrate cross section of a MESFET
(a) Schematic diagram of the cross section of a MESFET. (b) Band diagram in equilibrium. (c) Electron concentration. (d) Space charge at the channel-substrate interface; space charge of the Schottky barrier is not shown.

of holes form deep-level traps present in the substrate (or buffer layers) [17] [19] [21] [22] [24]. In attempts to shield the channel from the trap effect, buffer layers were added between the substrate and the n-type channels for devices built by growing epitaxial layers [17] [21] [22] [24]. The effectiveness of the buffer layers varied; in some cases the buffer reduced the substrate biasing effect, and in other cases the buffer had little effect or even aggravated the sidegating effect [17] [19] [21] [22] [24].

The models based on the reverse-biased pn-junction behavior interprets the sidegating effect in terms of space charge region expansion. Some experimental results of early studies can be qualitatively explained with these models. But little is offered by these models as to possible mechanisms through which the negative voltage applied to an electrode isolated from the device influences the channel-substrate interface space charge. These models explain neither the threshold characteristics in the sidegating effect nor the high substrate leakage current observed in some later studies.

2.2 Trap-Filling-Limit Model

There have been studies on the sidegating effect in GaAs integrated circuits that investigated not only the MESFET drain current reduction but also the substrate leakage current behavior, and some important aspects of the problem were revealed [11] [25]-[29]. High leakage currents in the substrate, at 0.1-1 μA levels, were observed for device-to-sidegate distances on the order of $20\,\mu m$ and sidegate voltages within the range of $0 \sim -10$ volts [11] [25] [29]. Another important observation is that in some cases it was at a threshold value of the sidegate voltage that the leakage current began to rise rapidly and the drain current started to decrease [11] [25]-[29].

Some correlation between the high substrate leakage current and the onset of the drain current reduction in a MESFET was suggested [25]. The similarity of the substrate leakage current behavior to that observed in bulk SI GaAs led Lee *et. al.*, to propose a model based on the electron-injection/trap-filling theory by Lampert [11] [25] [30] [31]. In this model a trap-filling voltage V_{TFL} is defined as the point where all of the deep-level states are occupied by the electrons injected into the substrate from the negatively biased sidegate. As the sidegate voltage goes beyond V_{TFL} all of the additional electrons injected contribute to the current conduction leading to the rapid rise of the substrate leakage current. Therefore the threshold voltage observed in sidegating effect experiments is considered to be the trap-filling voltage in this model which is usually referred to as trap-fill-limitrd (TFL) model. V_{TFL} depends on the empty concentration N_t and the distance L between the device and the sidegate and follows the relation $V_{TFL} \propto N_t L^2$ [31]. The TFL model explains the threshold characteristics of the drain current reduction in a MESFET as follows: at low sidegate voltages the leakage current in the substrate and through the channel-substrate is too small to maintain a substantial voltage drop across the interface [25]. When the sidegate voltage reaches and exceeds the threshold value the drain current starts to decrease because, according to the model, a much higher current flowing through the channel-substrate interface causes the voltage drop across the interface to increase [25].

But the physical basis for this interpretation offered by the TFL model is not clear. The value of threshold voltages were found to increase with the distance between the device and sidegate, but not following the relation $V_{TFL} \propto L^2$ predicted by the TFL model. The rapid rise of the leakage current around V_{TFL} calculated with the TFL model is by six or seven orders of magnitude [32] [33], but only two or three orders of magnitude of current rise at threshold voltages have been observed. The most important point is that threshold voltages predicted by the model are far greater, by one or two orders of magnitude, than those observed in experiments [34]. Outdiffusion of electron traps in region near the surface has been proposed to account for this difference [35]. But there have also been measurement results showing that, between two n-type contacts, the substrate current does not necessarily rise to high values within reasonable voltage ranges [36] [37], suggesting mechanisms other than that proposed in the TFL model.

2.3 Trap-Impact-Ionization Model

Li *et. al.* reported observations of not only the threshold characteristic but also hysteresis and S-shaped characteristics in their voltage-controlled and current-controlled measurements respectively [38] [39]. These new characteristics, which could not be explained with the TFL model, were attributed to a supposed S-type negative differential conductivity (S-NDC) behavior in SI GaAs substrates. The S-NDC behavior in semiconductors has been originally proposed to be associated with impact-ionization of donors by Schöll [40] [41]. Following Schöll's approach, Li *et. al.* proposed the trap-impact-ionization model to account for the S-NDC [38] [39] of substrate leakage currents observed in their experiments. In this model, two coupled deep-level traps are required to participate in the processes of producing the S-NDC when impact-ionization of these traps takes place. Charge neutrality in the bulk GaAs is also assumed in calculating the *I-V* characteristics.

In the impact-ionization model, the high substrate leakage current is caused by excitation of electrons from deep-level traps to the conduction band by impact ionization. It is shown that with large enough impact ionization coefficients, the SI GaAs could transfer from a high resistivity state with low electron concentration to a low resistivity state with high electron concentration, leading to a high current in the substrate and an S-type behavior in its *I-V* characteristics. The abrupt change at a threshold observed in the voltage-controlled measurements results from this transition as the applied sidegate voltage increases and passes the threshold value. To account for drain current reduction in a MESFET, it was argued that the transition to a low resistivity state lead to a potential redistribution such that most of the sidegate voltage dropped across the channel-substrate interface.

The impact-ionization-model provides an alternative explanation for the threshold characteristics. The predicted values of threshold are also more reasonable than those predicted by the TFL model. But the model lacks a physical basis for how the proposed potential redistribution occurs, which is the key point linking the current reduction in the channel to the impact-ionization of traps in the substrate. Moreover, there have been other experiments reported in the literature showing that the trap-impact-ionization, a process that may take place between two n-type contacts, does not necessarily occur within the voltage ranges for the distances between the two contacts as reported [36] [37].

2.4 “Hot Electron” Model

Markarm-Ebeid and Minondo explained the threshold characteristics observed in their experiments using a “hot electron” model [42] [43]. This model attributes the increase of negative space charge on the substrate side at the channel-substrate interface to a “hot electron effect,” which in this model refers to the enhanced transfer, under high field conditions, of electrons from the Γ conduction band minimum to the L and X satellite valleys in GaAs. This intervalley transfer of electrons results in a decrease of electron drift-velocity starting from a critical field value. According to this model, when the field in the substrate exceeds the critical value, the slower average movement of electrons in the region near the channel-substrate interface leads to an accumulation of electrons and higher occupancy of electron traps in the region. The negative space charge on the substrate side near the channel-substrate interface is therefore increased [42] [43], leading to depletion of electrons in the channel. The formation of negative space charge because of the “hot electron” mechanism is similar to that in an n^+-n^--n^+ Gunn diode.

The “hot electron” model, compared to other models describe so far, has a physical basis to explain how the space-charge at the channel-substrate interface increases and causes the sidegating effect. This model does not, however, explain the high leakage currents observed in the experiments by others [11] [25]-[29]. No report of high leakage currents was given by Markarm-Ebeid and Minondo [42] [43].

2.5 Surface Effects on Sidegating and Leakage Current

Surface effects, including those from both GaAs surface and near surface regions within the GaAs substrate, have been found to influence the sidegating effect [42] [44]. It was suspected that outdiffusion of electrons traps due to heat treatment during MESFET fabrication may leave the near-surface region slightly p-type. The p^-n-junction formed by this slight p-type near-surface region and the n-type channel could be reverse-biased by the negative sidegate voltage [43] [45] [46]. The sidegating effect was observed to be very sensitive to wet and dry chemical treatments and dielectric capping conditions of the GaAs surface, with some reducing and others aggravating it [42] [43]. These surface effects were attributed to large local field regions due to inhomogeneities at the GaAs surface; a large field region near the channel of a MESFET would cause the "hot electron" effect described above and cause or aggravate the sidegating effect. Some of the chemical treatments were believed to reduce or eliminate, and others to worsen the inhomogeneity at the surface.

Hasegawa *et. al.* observed that the threshold voltages for high substrate leakage currents were sensitive to surface treatment during process and passivation conditions [44] [47]. White-light emission was also observed to accompany the high leakage current [44]. Based on these findings, Hasegawa *et. al.* proposed that trapping of electrons by large numbers of surface states created a high field region near the anode which may trigger avalanche surface breakdown, leading to high leakage current and the threshold characteristic [44] [47]. It was suggested that high energy electrons generated by avalanche were accumulated under the channel and were in turn trapped by the deep levels centers there, thus increasing the negative space-charge on the substrate side at the channel-substrate interface.

2.6 The Effect of Metal Contact

Based on their numerical simulation results, Goto *et. al.* and Yano *et. al*. proposed that the drain current reduction and high substrate leakage current could be related to hole injection from the small portion of the gate metal of a MESFET in direct contact with the substrate [48]-[50]. Both hole and electron traps were assumed to exist in SI GaAs substrates. Because of the hole-injection, electrons will also be drawn into the substrate. High leakage currents could thus result from the increased hole and electron concentrations. The number of trapped holes and electrons on hole-traps and electron-traps, respectively, increased from the equilibrium values, yet bulk charge neutrality was still maintained. According to this model, when a sidegate voltage is applied, holes in the substrate are depleted in the region under the channel-substrate interface. Trapped holes are emitted from the traps and are also depleted, resulting in a net increase of negative space-charge in the region and causing the current in the channel to decrease.

This model introduces metal contacts into the explanation of the sidegating effect and leakage current, as compared to other models that focus on physics occurring between two n-type electrodes. Measurement results from this work [36] [37] and others [51] provided the first experimental evidence that, in qualitative agreement with the published results of simulation*s* [48]-[50]*,* the gate electrode of a MESFET plays an important role in causing high substrate leakage currents and serious sidegating effect.

2.7 Summary

The published experimental results described above concerning the GaAs MESFET sidegating effect can be grouped into three categories: (1) drain current decrease starts at zero or very low sidegate voltages and no information on leakage current is available; (2) both drain and leakage currents exhibit threshold characteristics and the leakage current reaches high levels; and (3) drain current reduction shows threshold characteristics but there is no observation of high leakage current. In the different models proposed, it is through altering the space-charge at the channel-substrate interface, one way or another, that the channel current in a MESFET is affected. To understand the sidegating effect, the physical basis for the processes in which the space-charge at the interface is disturbed from its equilibrium state still needs to be clarified. While there may be different mechanisms, it is important to understand the conditions under which each mechanism becomes the dominant one.

Chapter 3

Device Fabrication

In this chapter, different technologies developed for GaAs MESFET fabrication are first briefly described and compared mainly in terms of the methods for active layer formation, the ways to achieve isolation, and suitability for large scale integrated circuits. The process procedures used to fabricate the devices for electrical measurements in this study are described in detail. Results of basic DC characterizations of the fabricated devices are also described.

3.1 GaAs MESFET Technologies

GaAs MESFETs were first developed for applications in microwave technologies, taking advantage of the high electron mobility in GaAs. The early MESFET devices were fabricated by growing a thin epitaxial n-type layer on a semi-insulating substrate [17] [19] [22]. For the purpose of isolation, mesas of active areas of devices were formed by etching through the epitaxial layer. This mesa/epitaxial approach was also taken later to fabricate GaAs MESFETs used in digital circuits [52]. These early mesa/epitaxial MESFETs had the problem of poor device uniformity because of the thickness variations of the epitaxial layers. When an effective and reliable ion-implantation technology in GaAs was developed, the epitaxial layer was often replaced with an n-type layer formed by implanting dopants directly into the semi-insulating substrate [53]-[55]. Mesas were again used for device isolation by etching through the implanted layer. MESFETs for both microwave and digital applications were fabricated using this mesa/implantation technology [53]-[55], and better device uniformity was achieved compared to those fabricated with the mesa/epitaxial technology.

In the mesa technologies, only a single active layer is produced by either the epitaxial method or ion-implantation, and this restricts them from being used to fabricate circuits which may require multiple active layers for device optimization [8] [56]-[58]. Density of the circuits fabricated using the mesa technologies is also limited to low levels [56]. These limitations prohibit the mesa/epitaxial and mesa/implantation technologies from being employed to develop large scale integrated circuits.

An alternative to the mesa approach for device isolation is to render the epitaxial/ implanted layer semi-insulating by bombarding the material outside the active device areas using particles such as proton and oxygen or boron atoms. This technology yields planar device structures as compared to the mesa approach. But the use of a single active layer in this technology still limits the extent of its application.

A planar multiple-local-implantation technology was later developed with the potential of being use to fabricate LSI and VLSI GaAs circuits [56] [59]. In this technology, dopants are implanted into selected areas of a substrate where active devices are to be located. No mesa-etch is necessary; isolation among devices is directly provided by the un-implanted area of the semi-insulating substrate. This results in planar device structures allowing the devices to be located closer together because no space needs to be allocated for mesa side walls, which is desirable for fabrication of complex large scale integrated circuits [56] [57] [58]. The multiple-local-implantation approach allows on the same substrate active layers of different doping levels and depths. This technology was used to fabricate circuits requiring individual optimization of different devices [56] [59]. The flexibility of the multiple-localized-implantation technology makes available more options of circuit approaches that can not be realized with the single epitaxial/implanted layer technologies. Devices fabricated using the planar multiple-localized-implantation technology showed good uniformity, which is an important quality required to reach high level circuit integration [56] [59] [60]. These advantages have made the planar multiple-localized-implantation approach a desirable technology for fabricating large scale GaAs MESFET integrated circuits. Some high-speed, low-power digital GaAs integrated circuits were produced with this technology after its early development, demonstrating the promise of its extension to LSI and VLSI level [8] [56] [58] [59].

3.2 Device Fabrication Process

The devices used for electrical measurements in the experimental work of this study of the sidegating effect of ion-implanted GaAs devices were fabricated in the IC Lab at Stanford University. The fabrication processes used were also developed at the Stanford IC Lab, based on the planar multiple-localized-implantation technology described in last section. The fabrication processes are as follows:

- The substrates chosen to be used were from undoped LEC-grown GaAs material. The substrates were first cleaned in the sequence of using TCA, acetone, and isopropyl alcohol, and then were slightly etched with a solute of $NH_4OH{:}H_2O_2{:}H_2O$ (1:1:50) for 25 seconds.

- A layer of Si_3N_4 of about 800 A was deposited by plasma-enhanced chemical-vapor-deposition (PECVD) method on the front side of each wafer, which served the purposes of both surface protection and capping for thermal annealing.

- The active regions were defined through optical lithography using positive photoresist and the proper mask. The photoresist in the areas where devices were to be built were exposed to ultraviolet light on a 4:1-projection aligner (Canon FPA-141) and was then developed.

- Si^{+}_{29} ions were implanted into the GaAs substrates through the Si_3N_4 caps to achieve channel doping. The photoresist pattern defined in the previous step served as the mask to the implanted ions so that only the active regions were doped. Different doses and energy values were chosen depending on that the devices plan to be built were

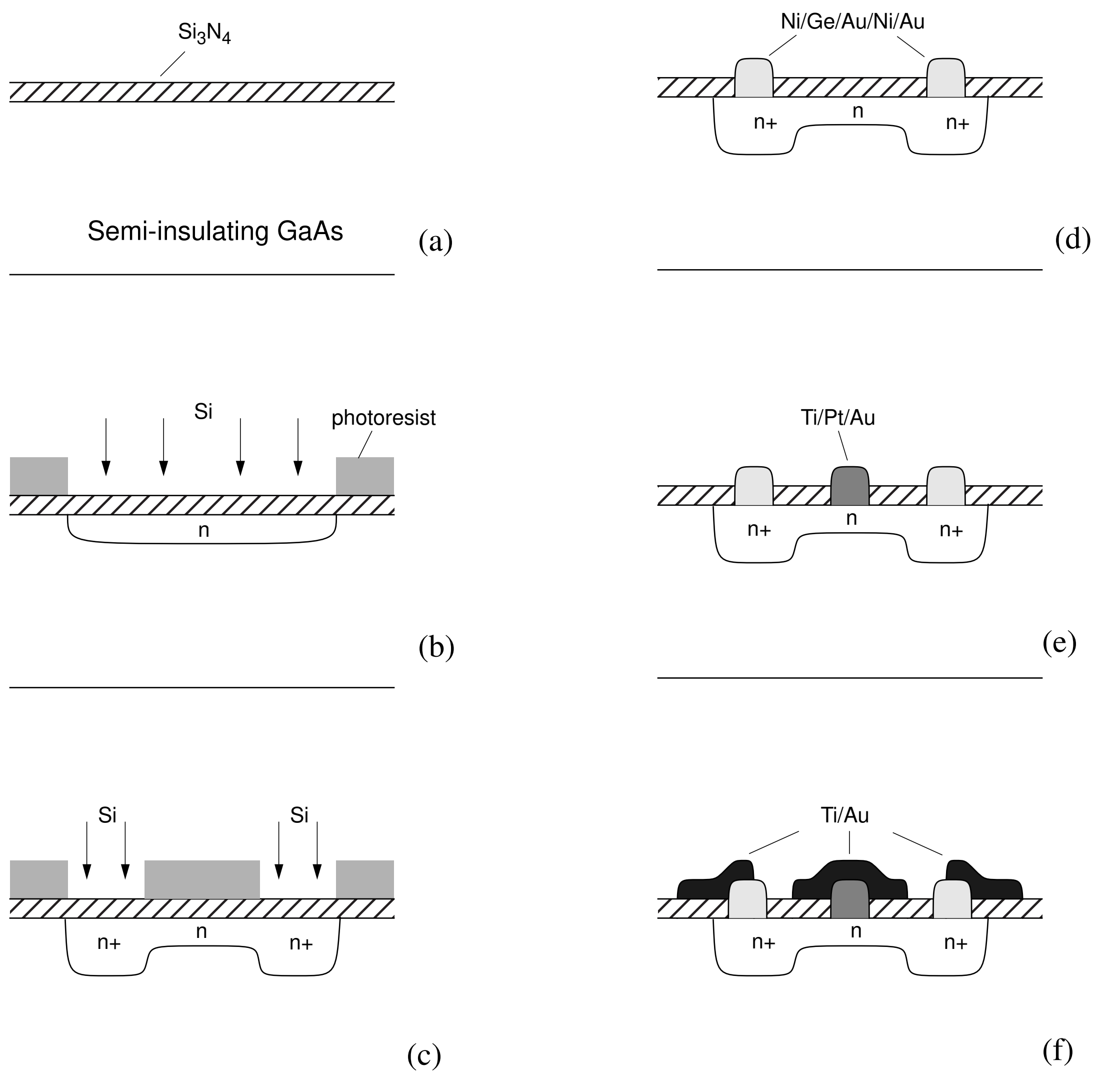


Figure 3.1 Schematic flow of MESFET process procedures.

regular FETs or FETs with buried p-type layers. The photoresist films were removed with oxygen plasma.

- After the channel implantation, another mask was used to define the source and the drain regions of a device, and sidegate regions as well. An additional dose of Si_{29}^{+} was implanted at 150 KeV.
- After all of the implantations were done, the samples were annealed in a furnace at 800 °C for 30 minutes in a forming gas ambient. The purposes of this annealing step were to repair the damage to the crystal structure by the energetic ions during implantation and to activate the implanted dopants.
- A mask was then used to define the source and drain contact openings, and the Si_3N_4 films were etched through by the method of reactive-ion-etching (RIE) with CF_4 and O_2 plasma. A layer of photoresist served as the etching mask.
- Metal layers of Ni/Ge/Au/Ni/Au (50Å/110Å/300Å/200Å/100Å) were deposited by e-beam evaporation to make contact with the source and drain regions. The samples with the metals were immersed in acetone for lift-off.
- The samples were then rapidly thermal-annealed (RTA) at 450 °C for 20 seconds to alloy the metals with GaAs to form ohmic contacts.
- A mask was used to defined the gate regions, and again the dielectric films were etched through by RIE. Metals layers of Ti/Pt/Au (700 Å/200 Å/700 Å) were deposited, and lift-off was done to form the gate patterns.
- In the last step, final metallization was done by depositing 200 Å Ti and 2500 Å Au to form the contact pads.

3.3 Basic Device Characterization

The fabricated MESFET devices are tested by measuring their current-voltage characteristics, threshold voltage, transconductance, and Schottky barrier heights.

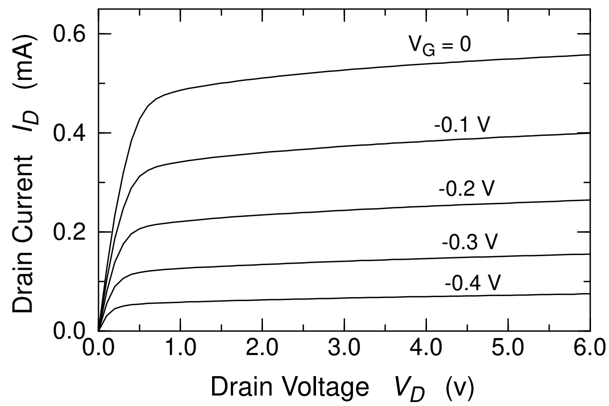


Figure 3.2 Measured MESFET current-voltage characteristics.

3.3.1 Current-Voltage Characteristics

Figure 3.2 shows the characteristics of the drain current vs. drain voltage at different gate bias voltages of a MESFET. The width of this specific device is W_G = 20 µm, and the gate length is L_G =2 µm. The spaces between the gate and source/drain are $L_{GS} = L_{GD}$ = 2 µm. The channel of this device was implanted at the energy of 135KeV with a dose of Si ions of $5 \times 10^{12} \mathrm{cm}^{-2}$.

It can been seen from Figure 3.2 that the drain voltage at which the drain current (measured at V_G = 0) starts to saturate is V_D = 0.7 V, at which I_D = 0.47 mA. For the purpose of studying sidegating effects as to be described in a later chapter, ungated devices were also fabricated. The measured current-voltage characteristics of such a device is shown in Figure 3.3. The channel doping, width, and the distance between the source and drain are all the same as those of the MEFET The only difference is that there is not a Schottky gate on top of the channel of the ungated device.

3.3.2 Threshold Voltage Measurement

For a long channel MESFET, the drain current I_D in the saturation region as a function of the gate voltage V_G can be expressed as [61]

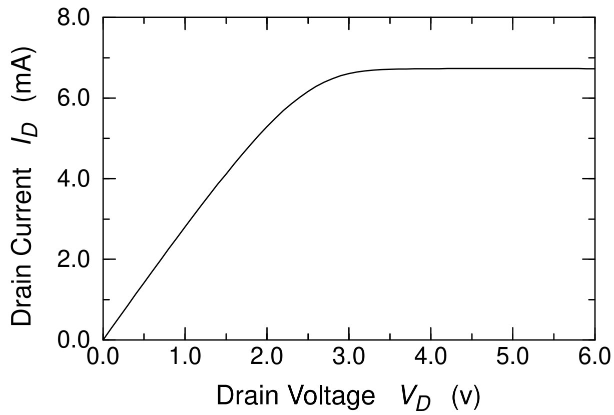


Figure 3.3 Measured current-voltage characteristics of an ungated device.

$$I_D = K(V_G - V_{th})^2 \tag{3.1}$$

where V_{th} is the threshold voltage and K a constant. For a depletion-mode MESFET, which is the type of device fabricated to be used in this study, the threshold voltage is negative ($V_{th} < 0$). The drain current vs. gate voltage measured in saturation region at the drain voltage of $V_D = 2.0$ V is shown in Figure 3.4(a).

Taking the square-root on both sides of Equation (3.1) results in $I_D^{1/2} = K^{1/2}(V_G - V_{th})$. Based on this relation, a common method to determine the threshold voltage is to make a $I_D^{1/2}$ vs. V_G plot with measured data and fit the curve with a straight line. The value of the threshold voltage is read from the intersection of the extrapolated straight line with the V_G-axis, as illustrated in Figure 3.4(b). The K value can be obtained from the slope of the fitting straight line. For the device shown in Figure 3.4, the threshold voltage measured is $V_{th} = 0.61$'V, and the K constant is $K = 1.4 \times 10^{-3}$ A/V^2 .

The I_D vs. V_G characteristics calculated from Equation (3.1) using the measured values of threshold voltage and the K factor is shown as the dashed curve in Figure 3.4(a). It can be seen that the curve fits the measured data well for $V_G < 0$, which is the range a depletion-mode MESFET usually operates. The discrepancy between the measured data and those calculated from Equation (3.1) becomes larger for higher current levels. This

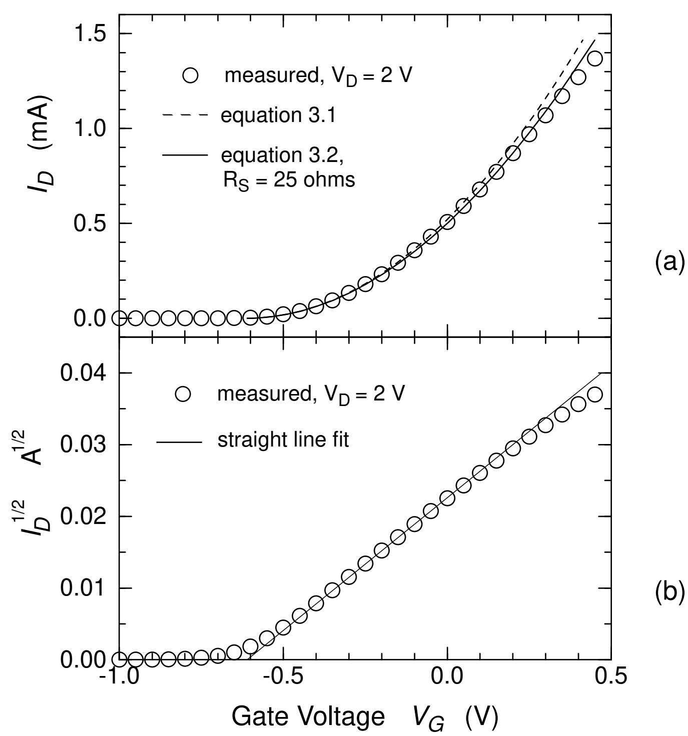


Figure 3.4 (a) I_D vs. V_D and (b) square-root of I_D vs. V_D characteristics.

can be attributed to the fact that the voltage drop across some source resistance R_S, which can be ignored at low current levels, becomes significant at higher current levels. A simple way to take the effect of this voltage drop into account is to modify Equation (3.1) as follows

$$I_D = K(V_G - I_D R_S - V_{th})^2 \tag{3.2}$$

The I_D vs. V_G characteristics calculated from Equation (3.2) using the same measured K factor and choosing $R_S = 25\Omega$, shown as the solid curve in Figure 3.4(a), makes a better fit with the measured data. It should be pointed out that Equation (3.2) is still a very crude approximation, and it is mentioned here simply to demonstrated the effect of the series resistance on device characteristics.

If the MESFET is approximated by a device with its channel uniformly doped to a depth *a,* the K factor is expressed as [61]

$$K = W_G \mu_n \varepsilon_o \varepsilon_s / 2a L_G \tag{3.3}$$

where μ_n is electron mobility in the channel, and ε_s is the dielectric constant of GaAs which takes the value of 13.1. The mobility of the electrons in the channel should be $\mu_n = 4000 \sim 5000\ \mathrm{cm^2/V\ s}$ [62]. For this range of the mobility, the channel depth calculated from Equation (3.3) is $a = 1.7 \sim 2.1\ \mu\mathrm{m}$.

The uniform channel doping level used in approximating the device can be estimated with the measured threshold voltage and Schottky barrier height and the estimated channel depth. The threshold voltage in Equation (3.1) is related to the built-in potential V_{bi} associated with the Schottky contact and the channel pinch-off voltage V_p by $V_{th} = V_{bi} - V_p$ [61]. For a uniformly doped channel, the built-in voltage and the pinch-off voltage can be calculated, respectively, as $V_{bi} = \phi_b - (kT/q)\ln(N_c/N_D)$ and $V_p = qN_D a^2 / 2\varepsilon_o \varepsilon_s$ [61]. The doping level N_D can then be estimated by the relation

$$V_{th} = \phi_b - (kT/q)\ln(N_c/N_D) - qN_D a^2 / 2\varepsilon_o \varepsilon_s \tag{3.4}$$

Based on the measurements made on Schottky diodes, the Schottky barrier value is taken to be $\phi_b = 0.73\ \mathrm{V}$. With the measured threshold voltage $V_{th} = 0.61\ \mathrm{V}$ and the estimated channel depth $a = 1.7 \sim 2.1\ \mu\mathrm{m}$, the uniform channel doping level should be $N_D = 4.2 \sim 6.8 \times 10^{16}\ \mathrm{cm^{-3}}$. This estimation of the channel doping range is consistent with the range of electron mobility $\mu_n = 4000 \sim 5000\ \mathrm{cm^2/V\ s}$ assumed at the beginning to estimate the channel depth using Equation (3.3) when checking against the published mobility values at different doping levels [62].

3.3.3 Transconductance Measurement

The transconductance g_m of a MESFET is defined as

$$g_m = \Delta I_D / \Delta V_G \tag{3.5}$$

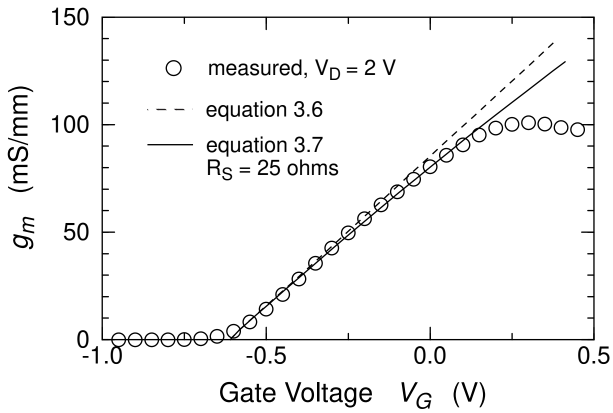


Figure 3.5 Transconductance g_m vs. gate voltage V_G.

Figure 3.5 shows the transconductance at different gate voltages measured at $V_D = 2.0$ V, with the gate voltage step of $\Delta V_G = 0.05$ V. The transconductance at zero gate voltage ($V_G = 0$), which is often one of the parameters used to characterize a MESFET, is $g_m = 80$ mS/mm.

Directly differentiating I_D expressed in Equation (3.1) with respect to the gate voltage V_G gives the intrinsic transconductance

$$g_{m0} = dI_D/dV_G = 2K(V_G - V_{th}) \tag{3.6}$$

The transconductance calculated from Equation (3.6) using the measured K factor and threshold voltage V_{th} is shown as the dashed curve in Figure 3.5. It can be seen that the curve fits the measured transconductance data well for gate voltages closer to the threshold voltage, but as the gate voltage approaches $V_G = 0$ and the drain current is relatively high, the transconductance is overestimated by Equation (3.6). The overestimation is partially because Equation (3.6) neglects the voltage drop across the source resistance and assumes the gate voltage V_G, which is referenced to the source contact, is the applied gate-to-channel voltage. In fact, because of the voltage drop across the source series resistance R_S, the potential of the channel under the gate is raised by the amount of $I_D R_S$, and the effective applied gate-to-channel voltage V_{G0} then should be $V_{G0} = V_G - I_D R_S$. The effect of the source resistance can be seen by deriving the transconductance using Equation (3.2) through the differentiation $g_m = (dI_D/dV_{G0})(dV_{G0}/dV_G)$, which results in

$$g_m \;=\; g_{m0}/(1 + g_{m0}R_S) \tag{3.7}$$

where in this case $g_{m0} = dI_D/dV_{G0}$. The existence of the source series resistance lowers the effective transconductance. The transconductance calculated with a resistance $R_S = 25\Omega$ being taken into account is shown as the solid curve in Figure 3.5 and fits the measured data well from $V_G = V_{th}$ to $V_G = 0$, which is the range a depletion mode MESFET usually operates.

3.3.4 Schottky Barrier Height Measurements

The barrier heights of the Schottky contacts were measured using Schottky diodes. A typical diode used in the work consists of a Schottky contact on n^{-}-doping and an n^{+} ohmic contact, with two contacts placed side by side. The dimension of the Schottky contact is $100\mu'\mathrm{m} \times 100\mu'\mathrm{m}$, and the ohmic contact is of the same size.

The method used to measure the Schottky barrier heights is based on the thermionic-emission model, according to which the ideal forward-bias current-voltage characteristics of a Schottky diode is expressed as [61] [63]

$$J \;=\; A^{*}T^{2}\exp(-q\phi_b/kT)\;\left[\;\exp(qV/kT) - 1\;\right] \tag{3.8}$$

where ϕ_b is the Schottky barrier height and V is the bias voltage. The effective Richardson constant A^{*} is defined as $A^{*} = 4\pi m_e qk^2/h^3 = 120 m_e/m$ A cm^{-2}'K^{-2} , where m_e is the electron effective mass and m the electron mass in vacuum. But practical current-voltage characteristics deviate from the ideal because of the bias voltage-dependence of the barrier height due to the barrier lowering effects such as image force and the existence of an interfacial layer [63]. Equation (3.8) for the ideal case is then modified, and an expression taking into account the barrier lowering effects is [63]

$$J = J_0 \exp(qV/nkT)\,[\,1 - \exp(-qV/kT)\,] \tag{3.9}$$

$$J_0 = A^* T^2 \exp[-q(\phi_{b0} - \Delta\phi_{b0})/kT\,] \tag{3.10}$$

where n is the ideality factor and $(\phi_{b0} - \Delta\phi_{b0})$ is the zero-bias barrier height including barrier lowering.

Dividing both sides of Equation (3.9) with $[\,1 - \exp(-qV/kT)\,]$, substituting J_0 (Equation (3.10)), and then taking the logarithm on both sides yields the expression [63]

$$\ln\left[\frac{J}{1 - \exp(-qV/kT)}\right] = \frac{qV}{nkT} + \frac{-q(\phi_{b0} - \Delta\phi_{b0})}{kT} + \ln(A^* T^2) \tag{3.11}$$

which gives a linear relation of $\ln\{J/[\,1 - \exp(-qV/kT)\,]\}$ vs. V. The barrier height $(\phi_{b0} - \Delta\phi_{b0})$ was then determined by measuring the current I of a Schottky diode as a function of the applied bias voltage, plotting $\ln\{I/[\,1 - \exp(-qV/kT)\,]A\}$ vs. V, and fitting the plotted data with a straight line. The value of the straight line at $V = 0$ gives the barrier height $(\phi_{b0} - \Delta\phi_{b0})$, and the slope of the line gives the ideality factor n.

Measured values of barrier heights from the diodes tested are in the range $(\phi_{b0} - \Delta\phi_{b0}) = 0.72 \sim 0.75$ eV and those of the ideality factors in the range $n = 1.1 \sim 1.2$. These values of barrier heights are smaller than the value of 0.83 eV measured by Waldrop on Schottky contacts formed by Ti on heat-cleaned GaAs (100) surfaces [64]. The measured ideality factor values are also a little larger than the diodes that could be considered close to ideal. The non-idealities shown in the measured $(\phi_{b0} - \Delta\phi_{b0})$ and n could be attributed partially to the existence of the relatively thick interfacial layers resulting from the imperfect surface conditions when the metal layers were deposited to form the Schottky contacts [63].

3.4 Summary

Ion-implanted GaAs MESFETs and ungated devices were fabricated using the processing procedures developed in the IC lab at the Stanford University, and the devices were tested by making DC electrical measurements. Measured device parameters such as threshold voltage, transconductance, and Schottky barrier height were in reasonable ranges, showing the fabrication of the devices were successful.

The ion-implanted channel of a MESFET is approximated with a uniform doping profile. The doping level, electron mobility, and channel depth are estimated using the measured parameters and data published in literature [61] [62]. Some of these parameters, both measured and estimated, will be used in simulations described in a later chapter.

It should be pointed out here that efforts were made during device fabrication to built reasonably well behaved devices, and the results of the DC measurements showed this goal was achieved. But it is not the purpose of this work to try to produce high-performance devices. The devices fabricated were to be used in the experimental studies of isolation problems such as the sidegating effect and the substrate leakage current between devices, which will described in the next chapter.

Chapter 4

Experimental Results

This chapter discusses experimental work on the sidegating effects. Results from the electrical measurements are presented. The measurements include the leakage currents in semi-insulating (SI) GaAs substrates between electrodes of different types, the drain current reduction of a MESFET under the influence of the negative voltage applied to a sidegate electrode, and the effect of metal contacts placed directly on the undoped SI substrates. The results are discussed to clarify how they should be interpreted and to suggest what are the possible mechanisms for the observed characteristics.

4.1 MESFET Sidegating: Preliminary Results

In this section, experimental results of MESFET sidegating effect and substrate leakage current are presented. The purpose of the measurements is to study the basic characteristics of the drain current degradation in a MESFET and the leakage current in the substrate, and to identify the problems that need to be further clarified experimentally. By comparing the measurement results of this work to those reported in the literature, the role of the gate electrode of the MESFET is also investigated.

4.1.1 Test Structures

The MESFETs used in this experiment were fabricated on undoped LEC GaAs substrates using the selective ion implantation method, following the basic process procedures described in Chapter 2. Si_3N_4 films of 900 Å thick were used for capping and surface protection. SiO_2 films were deposited after annealing for the purpose of dielectric-assisted

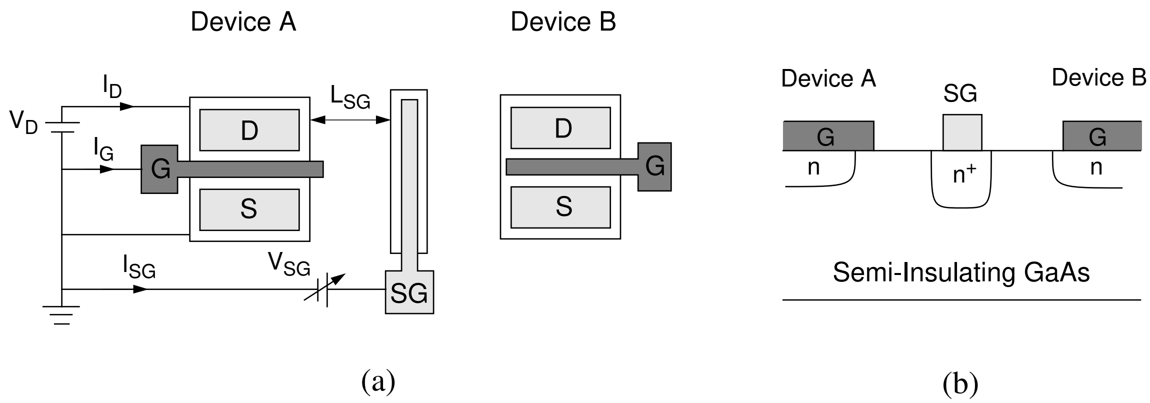


Figure 4.1 The test structure used for MESFET sidegating effect measurements. (a) Schematic top view of the test structure and the configuration for the measurements. (b) Cross section of the test structure.

lift-off. The gate metals used were Ti/Pt/Au, and metals used for ohmic contacts were Au/Ge/Ni/Au. The contacts pads were on top of the dielectric films.

The test structure used in the experiment includes two MESFETs, Device A and Device B, with each of the two positioned on opposite sides of a sidegate (see Figure 4.1). The sidegate is an n-type electrode, which simulates the contact electrode of a neighboring device in real GaAs ICs. The gate length of each device is 5 µm, and the width 270 µm. The distance L_{SG} from the sidegate to one device is the same as to the other.

The two MESFETs were fabricated in such a way that the tip of the gate metal of Device A is beyond the doped region boundary, touching the undoped SI substrate, while the end of the gate of Device B is within the doped region boundary (see Figure 4.1). A normal device requires the structure like that of Device A so that coverage of the whole width of the device is ensured. The lack of full control of the whole width of the conduction channel by the gate of Device B is evident in that, as shown in Figure 4.2, its drain current measured with its gate bias well below (more negative than) its threshold voltage is orders of magnitude higher than that of Device A.

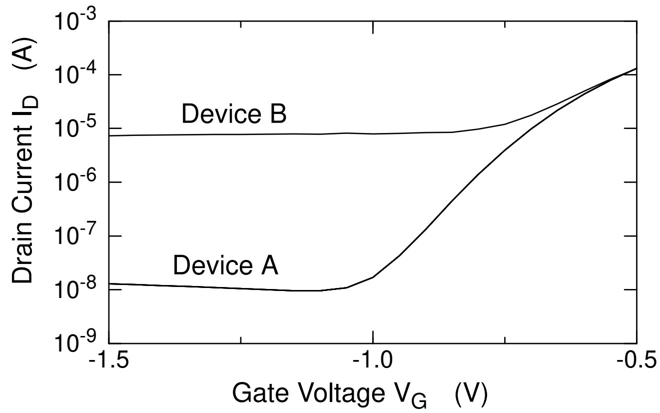


Figure 4.2 Subthreshold currents of Device A and Device B in Figure 4.1

4.1.2 Measurement Results

A. Sidegating effect and leakage current measurements

The behavior of the drain current of both Devices A and B and the leakage current in the substrate under the influence of a negative sidegate voltage are investigated. With the gate and source contacts at the ground potential and the drain biased at a constant voltage of V_{DS} = 2.0 V, a variable negative voltage V_{SG} is applied to the sidegate (Figure 4.1(a)). The substrate is kept floating in this and all the measurements described below in this section; no bias is applied to the backside of the substrate. The drain current of the MESFET I_D, and the sidegate current I_{SG}–which is the leakage current through the SI GaAs substrate between the sidegate and the MESFET–are simultaneously recorded as functions of the sidegate voltage, as was done in many experiments of early studies on the sidegating effect [11] [25] [26] [28] [29]. But the current through the gate electrode of the MESFET I_G, which has been ignored before, is also measured [36].

The measured drain and sidegate currents, for L_{SG} = 35 µm, are shown in Figure 4.3. Showing threshold characteristics, the drain current I_D of Device A, decreases rapidly for sidegate voltages beyond a certain threshold value (Figure 4.3(a)) and, at the same threshold of the sidegate voltage, the sidegate current I_{SG} begins rising rapidly towards high

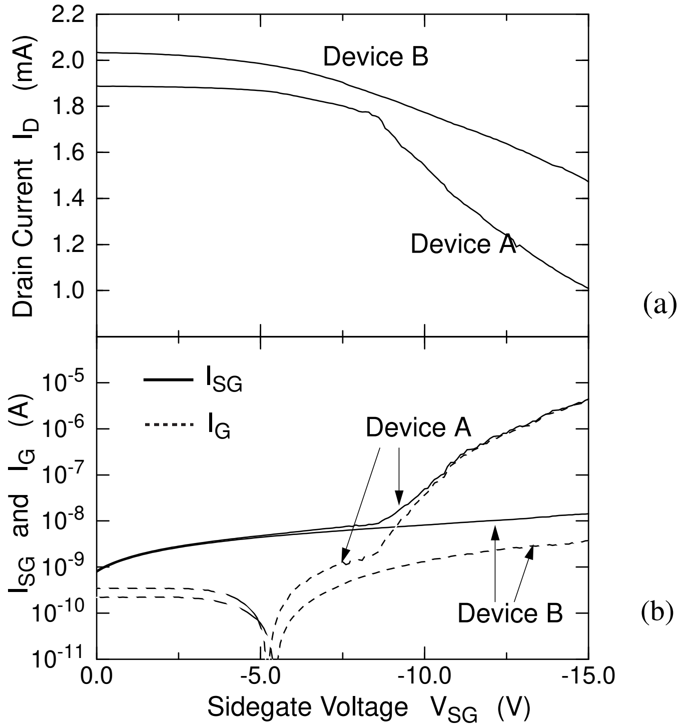


Figure 4.3 Measured Sidegating and Leakage Characteristics of Devices A and B. (a) Drain currents as functions of the sidegate voltage. (b) Sidegate currents and gate currents as functions of sidegate voltage.

levels (Figure 4.3(b)). For sidegate voltages below the threshold value, the rate of the drain current decrease is considerably lower and the sidegate current is small. In contrast, no threshold characteristics as pronounced as those of Device A are observed with Device B. The drain current I_D of Device B is seen to decrease with the negative sidegate voltage, but the overall reduction is considerably smaller than that of Device A (Figure 4.3(a)). The transition from the lower rates of the drain decrease to higher rates is very gradual over a voltage range of several volts.The measured I_{SG} is low and shows no rapid rise within the voltage range of the measurements (see Figure 4.3(b)).

For the measured gate currents, an important observation is that I_G of Device A quickly approaches and merges with I_{SG} as the sidegate voltage reaches and goes beyond the threshold value, as seen in Figure 4.3(b). Again in contrast, the gate current of

Device B remains low and does not show any dramatic increase.

B. Leakage current between the drain and the sidegate

This measurement investigates the behavior of the leakage current between the drain contact of a MESFET and the sidegate. The gate and source contacts of the MESFET are not used (i.e. V_S and V_G are floating). With the drain grounded, the substrate current, designated as I_{D-SG} in this case, is measured as a function of the negative voltage V_{SG} applied to the sidegate.

The measured I_{D-SG} between the sidegate and the drain contact of each of Devices A and B varies slowly with the applied sidegate voltage and remains at low levels for the entire voltage range of the measurement, as shown in Figure 4.4. No rapid rise to high levels starting at the threshold sidegate voltage, as observed with I_{SG} in the sidegating effect measurement, is seen the I-V characteristic of $I_{D\text{-}SG}$.

C. Leakage current between the gate and the sidegate

To further verify from which electrode of the MESFET the high leakage current comes from, the behavior of the current between the gate of a MESFET and sidegate, designated as I_{G-SG}, is investigated. With the drain and source contacts of a MESFET left floating but the gate grounded, the current I_{G-SG} is measured as a function of the negative voltage V_{SG} applied to the sidegate.

The I_{G-SG} between the gate terminal of Device A and the sidegate rises rapidly with a threshold sidegate voltage, as seen in Figure 4.4, and the characteristics are very similar to those observed with the I_{SG} and I_G in the sidegating effect measurements (see Figure 4.3(b)). The measured I_{G-SG} of Device A is about two orders of magnitude higher than I_{D-SG} of the same device at high voltages. I_{G-SG} of Device B, in contrast, remains low for the entire voltage range of the measurement.

4.1.3 Discussion

A. Correlation between the drain current reduction and the leakage current

The threshold characteristics in both the drain and leakage currents of Device A and the

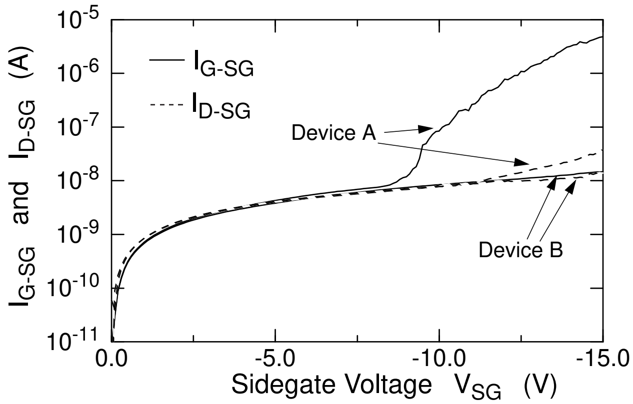


Figure 4.4 Substrate currents between the device contacts and the sidegate gate. $I_{G\text{-}SG}$ is the current between the gate of a device and the sidegate, and $I_{D\text{-}SG}$ is the current between the drain and the sidegate.

absence of the similar characteristics in those of Device B (Figure 4.3) demonstrate that there is a correlation between the behavior of the substrate leakage current and that of the drain current. This is in agreement with the observations by others [11] [25] [26]. However, these results do not provide sufficient evidence that the reduction of the drain current is a consequence of the high leakage current. The leakage current between Device B and the sidegate is low while the drain current is still observed to decrease with the sidegate voltage, though with different characteristics from, and with considerably less amount than, that for Device A. What can be suggested based on these measurement results is that different physical processes may be responsible for the different characteristics of the drain and leakage currents observed with Devices A and B. To understand the correlation between the leakage current and the drain current reduction, however, it is important to first identify the source of the high leakage current between Device A and the sidegate.

B. The role of the gate of a MESFET

Trap-fill-limited process (TFL) [11] [25] [26], trap-impact-ionization [38] [39], and surface breakdown [44] [47], have been proposed to explain high leakage currents, and these processes have been supposed to take place between two n-type electrodes, with one being the MESFET and the other the sidegate. But the low levels, or even the absence, of any rapid rise in the current between the drain contact of a device (either Device A or B) and the sidegate (see Figure 4.4), give no evidence of the occurrence of these processes. Some mechanisms, other than those mentioned above, must be responsible for the observed high substrate current.

Comparing the current I_G through the gate of Device A and the sidegate current I_{SG} (Figure 4.3(b)) observed in the sidegating effect measurement, it is clear that when the leakage current between the device and the sidegate enters the region of rapid increase, it is the gate terminal that contributes the dominant part of the total current. This is verified by the measurement of the current I_{G-SG} between the sidegate and the gate of Device A (see Figure 4.4). Considering the differences between these currents measured with Device A and those measured with Device B, it is natural to suggest that it is the small portion of the gate metal directly in contact with the substrate (see Figure 4.1 (b)) that causes the high leakage currents between Device A and the sidegate. It is also natural to propose that the threshold characteristics and the enhanced drain current reduction of Device A, compared to that of Device B, are because of some physical processes related to the gate metal contact on the substrate. The measurement results described above provided one of the first experimental verifications [36] for the importance of the gate electrode of a MESFET in relation to the sidegating effect and the substrate leakage current, and are consistent with the published simulation results on MESFET sidegating that included the effect of the gate electrode [48]-[50].

4.1.4 Summary

Comparisons of measurement results from the two devices, Device A and Device B, show that the gate terminal of a MESFET plays an important role in isolation problems of GaAs MESFETs. These experimental results show that it is not sufficient to consider the structure formed by a MESFET and a sidegate only as an n-i-n structure, as in most of the early studies of MESFET isolation problems; the m-i-n structure, formed by the gate metal, more specifically the portion of it in contact with the substrate and the sidegate, should also be taken into account in interpreting experimental results. Trap-fill-limited and trap-impact-ionization processes may not be in reality the primary mechanisms responsible for the high leakage currents and drain current reduction.

Based on the measurement results described above, the following issues need to be clarified by further experiments: (1) substrate leakage current characteristics in m-i-n and n-i-n structures; (2) sidegating characteristics in the presence of a metal contact on the substrate; and (3) sidegating characteristics when there is no metal contact effect.

4.2 Currents in m-i-n and n-i-n Structures

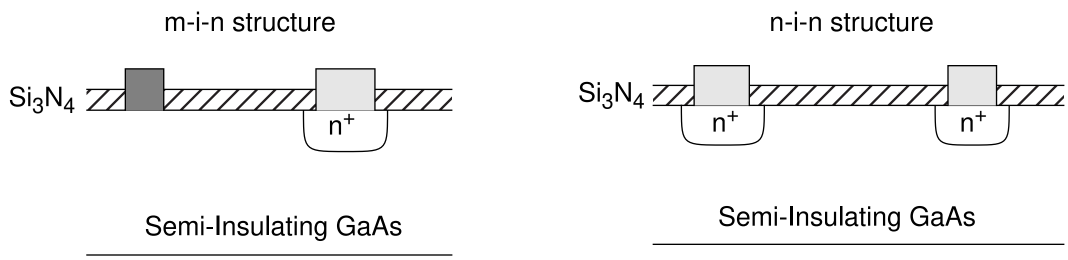
In this section, the leakage current characteristics in m-i-n and n-i-n structures are investigated and compared.

4.2.1 Test Structures

Figure 4.5 shows the cross-sections of the m-i-n (Figure 4.5(a)) and n-i-n (Figure 4.5(b)) structures used for measuring leakage currents in substrates. The m-i-n test structure consists of two contacts in parallel: one is a metal contact made directly on the undoped SI substrate and the other is an n-type ohmic contact. The metals used for the metal contact are Ti/Pt/Au, which are the same as used for the gate of a MESFET. The length of the metal contact is 2 µm. The n-i-n structure consists of two n-type electrodes. The ohmic metals are Au/Ge/Ni/Au. The length of the n-type region for the ohmic contact is 35 µm. Both the m-i-n and n-i-n structures are 80 µm wide. The surface of the substrate was capped with a layer of 900 Å thick Si_3N_4.

4.2.2 Measurement Results

To measure the current in an m-i-n structure, the metal contact is grounded and a variable negative voltage is applied to the n-type electrode. In an n-i-n structure, one of the n-type electrode is grounded. In Figure 4.6 the measured currents in m-i-n structures with



(a) (b)

Figure 4.5 Test structures used for measuring substrate leakage currents.

different distances ($L = 2 \sim 50$ µm) between the contacts are compared with the current measured in an n-i-n structure with a distance of $L = 4$ µm between the two n-type contacts. While the current in the n-i-n structure remains very low, not exceeding 1 nA within the entire voltage range of the measurement, the currents in the m-i-n structures, even those with much larger spacings between the contacts ($L = 30$ µm and 50 µm), all reach levels of several orders of magnitude higher when the n-type electrode is negatively biased relative to the metal contact (Figure 4.6). The rise of the currents in the m-i-n structures is continuous over the entire voltage range, showing no abrupt changes or hysteresis. No S-shaped characteristics are observed for current-controlled measurements either. When the applied voltage is positive relative to that of the metal contact, the measured current (not shown) is even lower than that in the n-i-n structure.

On the other hand, in the n-i-n structures in which the spacings between the two n-type contacts are relatively large ($L \geq 4$ µm), the measured currents remain low over the entire voltage range of the measurements, as seen in Figure 4.7(a) in which the currents are plotted in linear scales. The currents are seen to increase first linearly at low voltages and then at lower and lower rates as the voltage becomes higher. The currents can be considered as eventually entering a region of saturation as the voltage increases further.

High substrate leakage currents in n-i-n structures are only observed for very small distances ($L < 4$ µm) between the two n-type electrodes, as shown in Figure 4.7(b). For

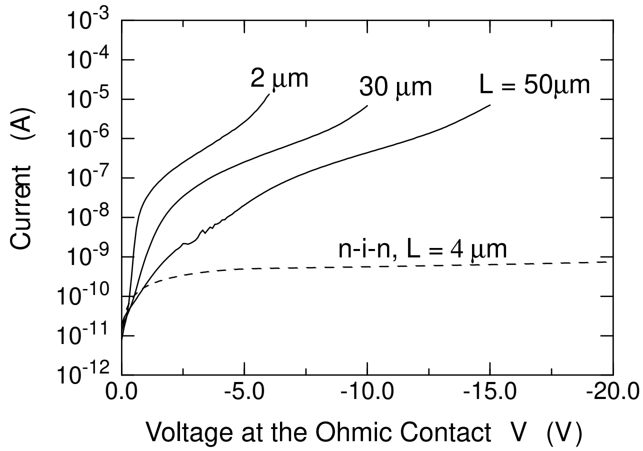


Figure 4.6 Measured currents in m-i-n structures with different electrode spacings. The current in an n-i-n structure is also shown for comparison.

$L = 2$ µm and 3 µm, the currents rise rapidly by about five or six orders of magnitude over small voltage ranges when the voltage is sufficiently high.

4.2.3 Discussion

A. Currents in m-i-n Structures

The high substrate leakage currents in the m-i-n structures cannot be explained with the models such as the trap-fill-limited process [11] [25] [26], the trap-impact-ionization [38] [39], or surface breakdown [44] [47], all originally proposed to take place in n-i-n structures. First, the fact that only low currents are observed in the n-i-n structures for $L \geq 4$µ'm (see Figure 4.7(a)) rules out the occurrence of these processes in the structure, and there is no physical basis to support that these processes should take place in the m-i-n structures. Secondly, the current characteristics in the m-i-n structures do not resemble those that would result from either trap-fill-limited process or trap-impact-ionization.

The high current in an m-i-n structure then must be related to the metal contact on the undoped substrate. The metal contact in an m-i-n structure can inject holes into the substrate under proper bias conditions. The hole-injecting mechanisms include thermionic emission, thermionic-field emission, and field emission [63]. When the n-type ohmic

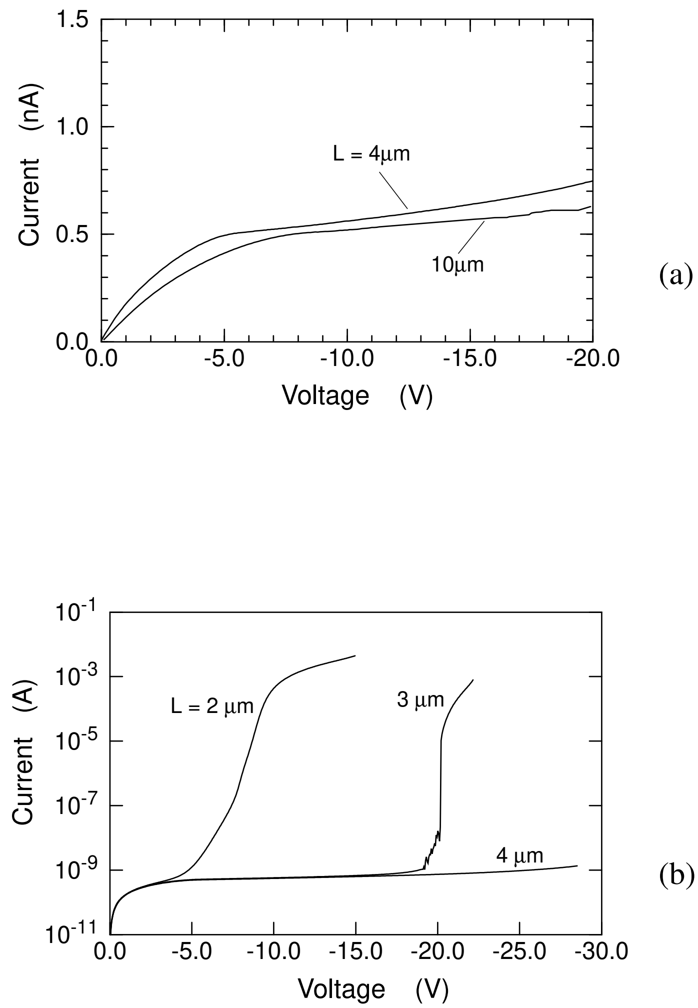


Figure 4.7 Current characteristics in n-i-n structures

contact in an m-i-n structure is negatively biased, the transport of holes at the metal-GaAs interface is such that there is a net flow of holes into the substrate. The holes injected into the substrate move towards the n-type contact by drift and diffusion. Electrons are drawn into the substrate because of this hole-injection and are attracted to and collected by the metal contact. This double-injection results in higher concentrations of both electrons and holes and therefore lead to high currents in the substrate. Electrons are injected into the substrate when the n-type electrode is positively biased relative to the metal contact, but the electron current at the metal contact resulting from the electron-injection is considerably smaller than the hole-current when the n-type electrode is negatively biased. Besides, the n-type electrode can supply few holes to support an effective double-injection that would lead to a high substrate current.

B. Currents in n-i-n Structures

The rise of the currents to high levels (see Figure 4.7(a)) in the n-i-n structures with two closely placed n-type ohmic contacts ($L < 4$ µm) can be explained with the theory based on the electron-injection/trap-fill-limited (TFL) process [63]. According to this theory, at low voltages most of the electrons injected into the substrate from the cathode are captured and trapped by deep-level electron-traps. Thus there is little increase of electron concentration in the conduction band that contributes to the current conduction, and the current in the substrate is low. When the voltage reaches sufficiently high values, nearly all of the previously empty electron traps become occupied, and all of the additional electrons injected into the substrate contribute to increase the electron concentration, resulting in high current in the substrate. A trap-fill-limit voltage V_{TFL} is defined as the voltage at which all of the electrons-traps are filled and the current starts to rise. V_{TFL} is estimated using $V_{TFL} \approx qN_tL^2/2\varepsilon_o\varepsilon_s$ [63], where q is the electron charge, N_t the concentration of empty traps, L the distance between two electrodes, ε_o the permittivity constant, and ε_s is the dielectric constant of the material. In an undoped LEC GaAs substrate, the concentration of the empty electron traps should be equal to the concentration of residual shallow-acceptors. Taking $N_t = 5.0\times10^{15}\,\mathrm{cm}^{-3}$, which is typical for an undoped LEC GaAs substrate, the V_{TFL} estimated is 8.3 V and 18.6 V for $L = 2$ µm and 3 µm respectively. These are reasonable values compared to the measured current characteristics (see Figure 4.7(b)).

The trap-fill-limited voltage V_{TFL} estimated for the n-i-n structures with large spacings ($L \geq 4$ µm) between the two n-type contacts are well beyond the voltage ranges of the measurements. Therefore only low currents in these structures are observed. The currents saturate because, at high fields, the drift velocity of electrons in GaAs does not increase with the increasing field values at it does at low fields. The current saturation behavior will be addressed when discussing the sidegating effect related to n-i-n structures.

4.2.4 Summary

The experiment results described have shown that, within reasonable voltage ranges, high substrate leakage currents are more likely to occur in an m-i-n structure than in an n-i-n structure. These results confirm that the high leakage currents observed between a sidegate and a MESFET in sidegating effect measurements are in fact between the sidegate and the unavoidable gate metal contact on the substrate. The gate metal on the substrate and the sidegate form an m-i-n structure, and the negative voltage applied to the sidegate creates the bias condition that leads to the high substrate leakage current. The experimental results described above are consistent, in terms of high leakage current, with the results of the simulations by Goto *et. al.* [48], [49], who included metal contacts as the hole-injection sources in their simulations.

However, the measured m-i-n currents do not shown any threshold characteristics. This suggests that the threshold characteristics observed in the drain and substrate currents in the MESFET sidegating effect experiments are not necessarily caused by the current conduction in an m-i-n structure.

The low currents in the n-i-n structures (see Figure 4.7(a)) indicate that good isolation between n-type regions can be achieved as far as leakage current is concerned. High

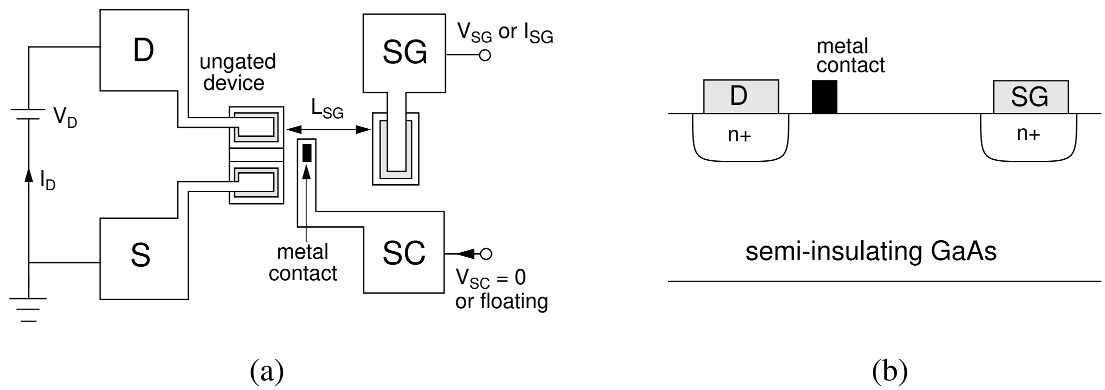


Figure 4.8 Test structure including an ungated device and a metal contact on substrate. (a) Top view of the test structure. (b) Cross section of the test structure showing the drain contact of the device, the metal contact, and the sidegate.

leakage current between n-type electrodes becomes a problem only when they are positioned very close to each other.

4.3 Metal Contact and Sidegating Effect

In this section, the sidegating characteristics in the presence of a metal contact on the substrate are studied through electrical measurements. The origins of the hysteresis and the S-shaped characteristics are also investigated. Possible mechanisms responsible for the observed phenomena are proposed.

4.3.1 Test Structure

The test structure used in this experiment consists of an ungated device, a metal contact on the substrate, and a sidegate which is an n-type electrode (see Figure 4.8). Both the ungated device and the sidegate are ion-implanted n-type regions on an undoped LEC semi-insulating GaAs substrate. The ungated device is like a MESFET with its gate removed. The width of the ungated device is 20 µm, and the length of the channel between the heavily doped source and drain regions is 6 µm. The sidegate is 35 µm long and 25 µm wide, located a distance L_{SG} from the ungated device (see Figure 4.8 (a)). The metal contact on the substrate is 4 μm long and 2 μm wide, place 2 μm from the ungated device. It simulates the small portion of the gate of a MESFET that is in contact with the undoped substrate. The metals used for the metal contact are Ti/Pt/Au, which are same as used for the gate of a MESFET. The substrate is capped with a layer of 900 Å thick Si_3N_4, and all of the contact pads are on the Si_3N_4 film. The use of the ungated device and the separate metal contact excludes any effect of the gate on the channel of the device and isolates the effect of the metal contact.

4.3.2 Sidegating Effect and Leakage Current

A. Measurement Results

The basic sidegating characteristics are measured with the source of the ungated device grounded ($V_S = 0$) and the drain biased at a constant voltage V_D. A variable negative voltage V_{SG} is applied to the sidegate. The substrate is kept floating; no bias is applied to the back side of the substrate. The metal contact is also grounded ($V_{SC} = 0$) to investigate its effect. The drain current I_D of the ungated device, the sidegate current I_{SG}, and current at the metal contact I_{SC} are all measured as functions of the negative voltage V_{SG} applied to the sidegate.

Figure 4.9 shows the current characteristics measured at $V_{DS} = 0.1$ V using a test structure with $L_{SG} = 20$ μm. The drain current first decreases slowly at low sidegate voltages and then decreases at higher rates with the increasing V_{SG} (see Figure 4.9(a)). The transition from the low-rate decrease to the high-rate decrease is gradual and smooth; no pronounced threshold characteristics are observed. The sidegate current I_{SG} rises rapidly with V_{SG} to high levels, as shown in Figure 4.9(b). The current in the substrate is dominated by the current between the metal contact and the sidegate, as is evident in the behavior of the metal contact current I_{SC} which approaches and merges with I_{SG} at low sidegate voltages (see Figure 4.9(b)).

To underscore the effect of the metal contact, the drain current I_D and the sidegate current I_{SG} are also measured with the metal contact left floating. The measurement results

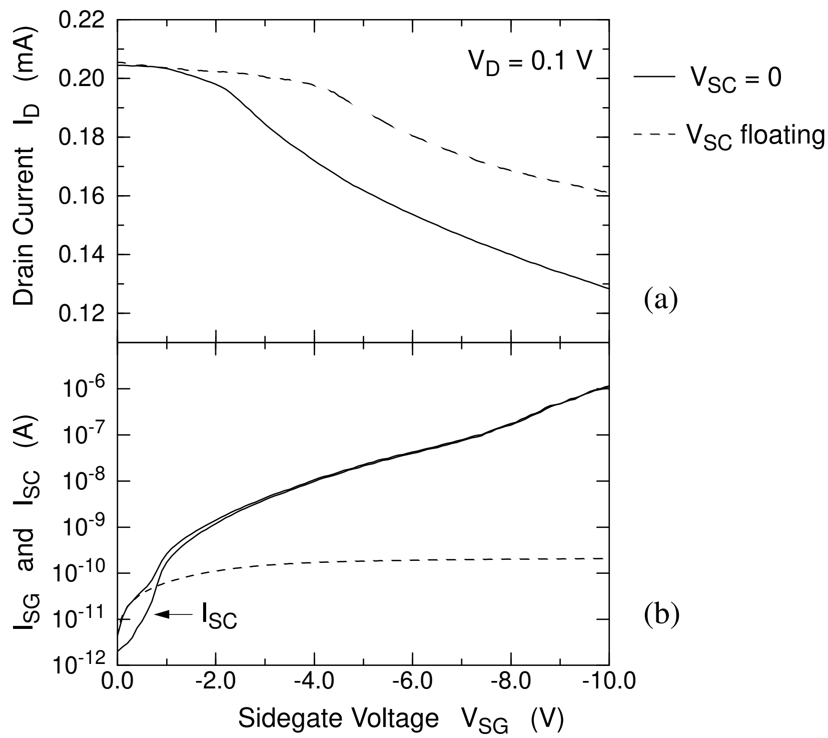


Figure 4.9 Basic sidegating characteristics in the presence of a metal contact. Measurement results for $V_{SC} = 0$ (solid curves) and those for V_{SC} floating (dashed curves) are shown together for comparison. (a) Drain current of the ungated device. (b) Sidegate and metal contact currents.

show that the drain and sidegate currents have very different characteristics from those measured with the metal contact grounded, shown as seen in Figure 4.9. The characteristics measured with V_{SC} floating are to be discussed in detail later in this chapter. But it is clear that in the presence of the metal contact, not only is the substrate leakage current much higher, but the sidegating problem also becomes more serious.

B. Discussion

As discussed in section 4.1.3 of this chapter, the high leakage current in the substrate can be explained with the process of double-injection — hole-injection from the metal contact and electron-injection from the n-type sidegate. The occurrence of the double-injection is further investigated by taking advantage of the fact that the metal contact is separated

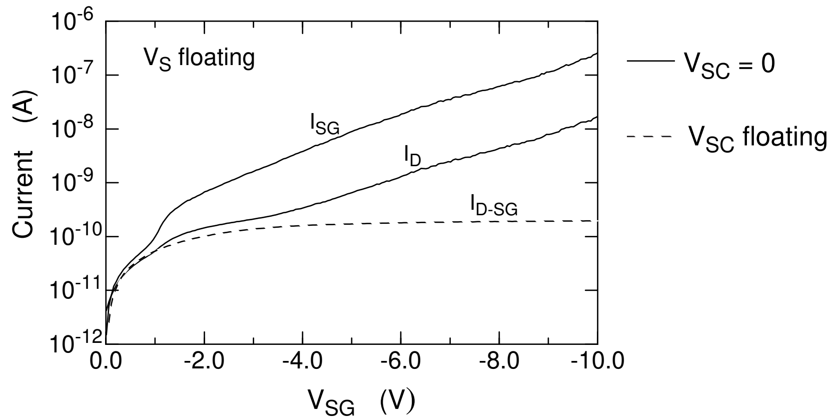


Figure 4.10 Leakage currents between the sidegate and the ungated device. The source of the ungated device is floating. The current I_D measured at the drain with the metal contact grounded ($V_{SC} = 0$) is much greater than the current $I_{D\text{--}SG}$ at the drain measured with the metal unconnected (V_{SC} floating).

from, yet placed very close to, the ungated device. With the drain of the ungated device grounded, the current $I_{D\text{-}SG}$ measured between the drain and the sidegate with both the source and the metal contact floating is low as expected, as shown by the dashed curve in Figure 4.10. However, with the metal contact also grounded in the measurement, while the current I_{SG} measured at the sidegate is seen to rise rapidly as expected for the current in an m-i-n structure, the current I_D measured at the drain is two orders of magnitude higher than $I_{D\text{-}SG}$. The higher current indicates the higher electron concentration in the substrate, which can be attributed to the double-injection process.

Drain current degradation can also be related to the double-injection process. When a negative sidegate voltage is applied, while hole concentration in the bulk of the substrate is also increased due to hole-injection from the metal contact, holes are depleted in the region below the channel-substrate interface. On the other hand, electron concentration in the same region is higher than its equilibrium value. The combined effect of hole-depletion and higher electron concentration leads to a higher steady-state electron occupancy of some deep-level traps in the region. As a result, this may disturb charge-neutrality and create a net negative space-charge in the region below the channel-substrate interface, leading to depletion of electrons in the channel of the ungated device and causing current of the device to decrease.

4.3.3 Threshold, Hysteresis, and S-shaped Characteristics

A. Threshold and Hysteresis Characteristics

The basic sidegating and leakage current characteristics measured at $V_D = 0.1$ V (see Figure 4.9) show no threshold behavior. But threshold characteristics are observed in the measurements at higher drain bias voltages. Figure 4.11 shows the drain current I_D, sidegate current I_{SG}, and metal contact I_{SC} measured when drain is biased at $V_D = 3.0$ V, 4.0 V and 5.0 V. As the sidegate voltage increases from zero, the drain current (Figure 4.11(a)) starts to decrease and the sidegate current (Figure 4.11(b)) begins to rise toward high levels only when V_{SG} reaches a threshold. Both I_D and I_{SG} make abrupt changes at the threshold voltage. These characteristics are similar to some of the published results of experimental studies on MESFET sidegating effect [11] [25] [26] [28] [29]. However, it is important to note that the measured characteristics in Figure 4.11 show the threshold voltage to be larger for a higher drain bias voltage.

The current through the metal contact I_{SC} is low for sidegate voltages smaller than the threshold, as seen in Figure 4.11(c). The metal contact starts to conduct high current only after the sidegate voltage V_{SG} reaches and goes beyond the sidegating threshold voltage, at which I_{SC} jumps to a high level and dominates the total substrate current.

Hysteresis behavior is observed in both I_D and I_{SG} when the sidegating voltage is first increased from zero to a value beyond the threshold and then decreased towards zero, as demonstrated by the drain and sidegate currents measured at $V_D = 6.0$ V shown in Figure 4.12. The hysteresis characteristics are not observed for low drain bias voltages such as $V_D = 0.1$ V.

B. S-shaped Characteristics

If a negative current (flowing out of the electrode), instead of a voltage, is applied to the sidegate, S-shaped characteristics are observed in both the drain and sidegate currents

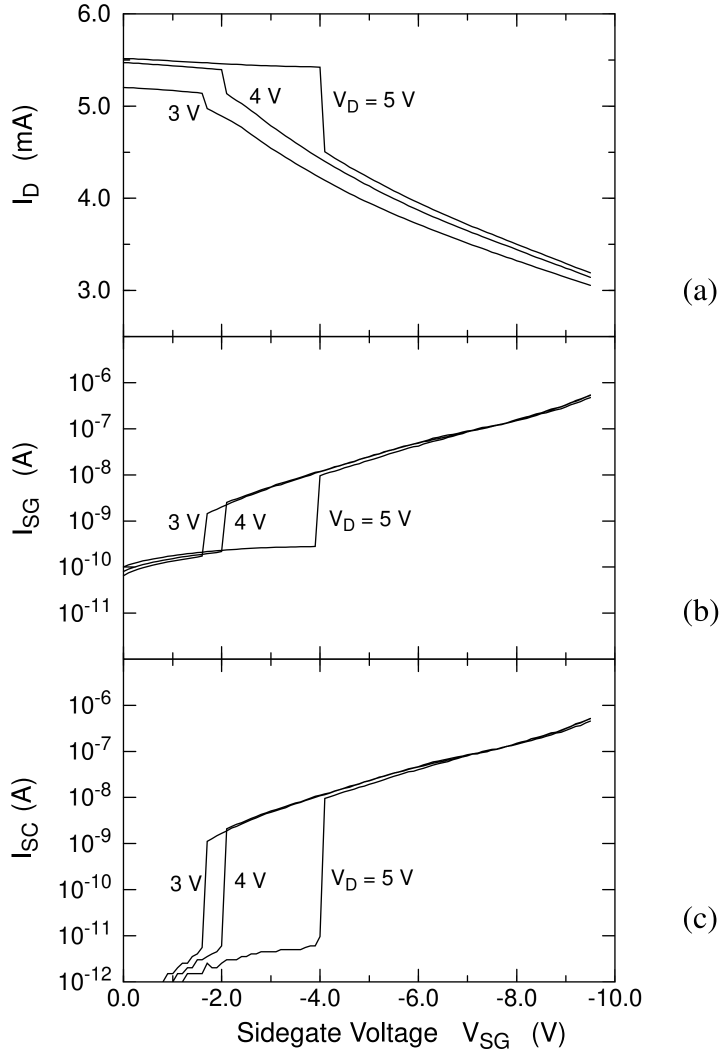


Figure 4.11 Threshold characteristics measured at higher drain bias voltages.

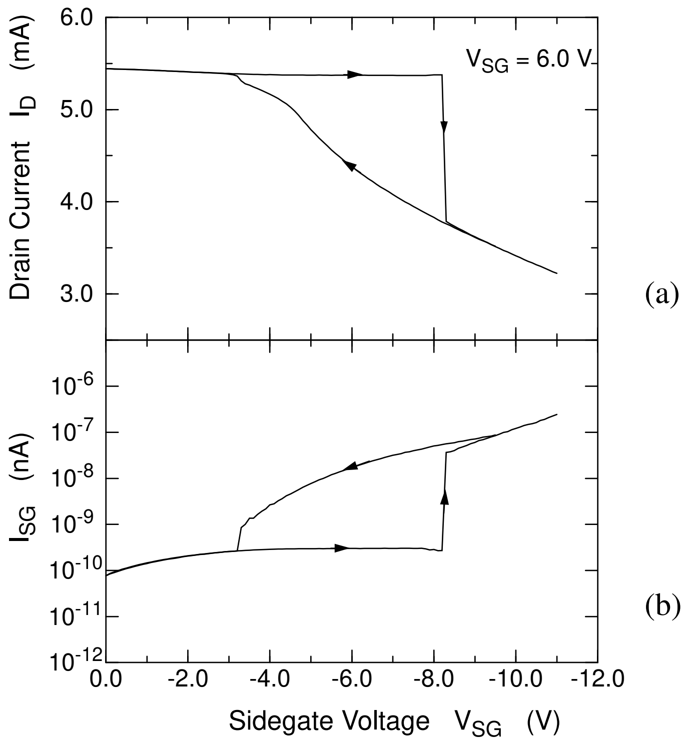


Figure 4.12 Hysteresis characteristics of measured drain and sidegate currents.

when the drain is biased at a relatively high voltage. Figure 4.13 shows the results of such current-controlled measurements at $V_D = 3.0$ V and 5.0 V. Again, the S-shaped behavior is found to disappear at low drain voltages such as $V_D = 0.1$ V.

C. Discussion

The threshold behavior in the drain current and sidegate current characteristics (see Figure 4.11) cannot be explained with trap-fill-limited [25] and trap-impact-ionization processes [38] [39]; the fact that the threshold voltage is larger for a higher drain bias voltage (see Figure 4.11) contradicts what the models based on these two processes would predict. Examining the behavior of measured current at the metal contact for sidegate voltages before and after reaching the threshold, the threshold of sidegate voltage can be considered as the onset point of the double-injection process.

The value of the threshold at which the double-injection is "turned on" is affected by

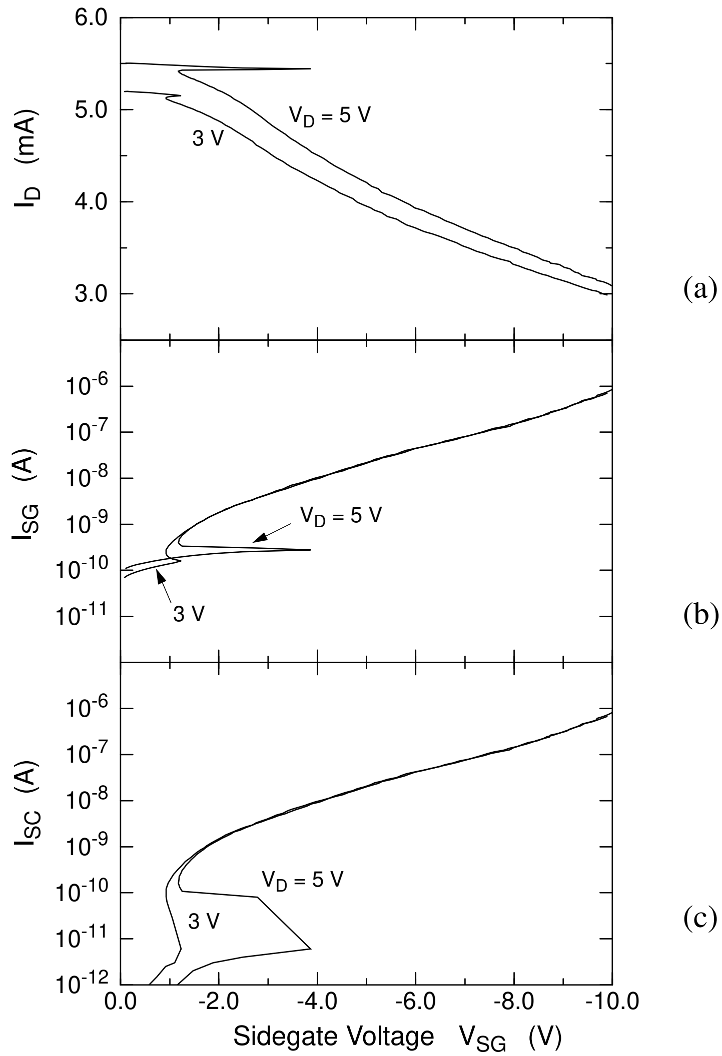


Figure 4.13 S-shaped characteristics in the current-controlled measurements. (a) Drain currents of the ungated device. (b) Sidegate currents. (c) Metal contact currents.

the drain bias voltage (see Figure 4.11). While the negative voltage V_{SG} applied to the sidegate induces hole-injection from the metal contact, the effect of the positive voltage V_D at the drain of the ungated device is the opposite -- it impedes the hole-injection process. Due to the hampering effect of a relatively large drain bias voltage, there are not enough holes being injected into the substrate from the metal contact to trigger the double-injection for low sidegate voltages. The current conduction in the substrate is dominated by the low current in the n-i-n structure formed by the ungated device and the sidegate. Only when the negative sidegate voltage reaches a sufficiently high value at which the effect of the drain voltage is overcome, are holes injected into the substrate to initiate the double-injection process. The current conduction in the substrate is then dominated by the high current in the m-i-n structure formed by the metal contact and the sidegate, and the measured sidegate current jumps to a much higher level. The abrupt change of the sidegate current I_{SG} (see Figure 4.11(b)) at a threshold of the sidegate voltage is a manifestation of the transition from the n-i-n conduction to the m-i-n conduction in the substrate. This transition occurs at a larger threshold voltage for a higher drain bias because a larger sidegate voltage is required to overcome the stronger effect hampering the hole-injection. As the transition takes place, the potential, field, and charge distributions in the substrate change correspondingly; net negative charge is created below the channel-substrate interface, causing electron depletion and therefore current reduction in the channel.

In a current-controlled measurement, when the negative current applied at the sidegate is sufficiently large, the effect of the drain bias voltage is overcome and the double-injection process is started. Once the current conduction in the substrate is switched from the n-i-n current to the m-i-n current, a lower sidegate voltage is needed to sustain the same current level. Therefore there is a backlash of V_{SG} and the resulted I_{SG}-V_{SG} relation shows the S-shaped characteristics (see Figure 4.13). The hysteresis characteristics observed in the voltage-controlled measurements (see Figure 4.12) can be understood based on the same reasoning.

The threshold, hysteresis, and S-type characteristics are also observed with

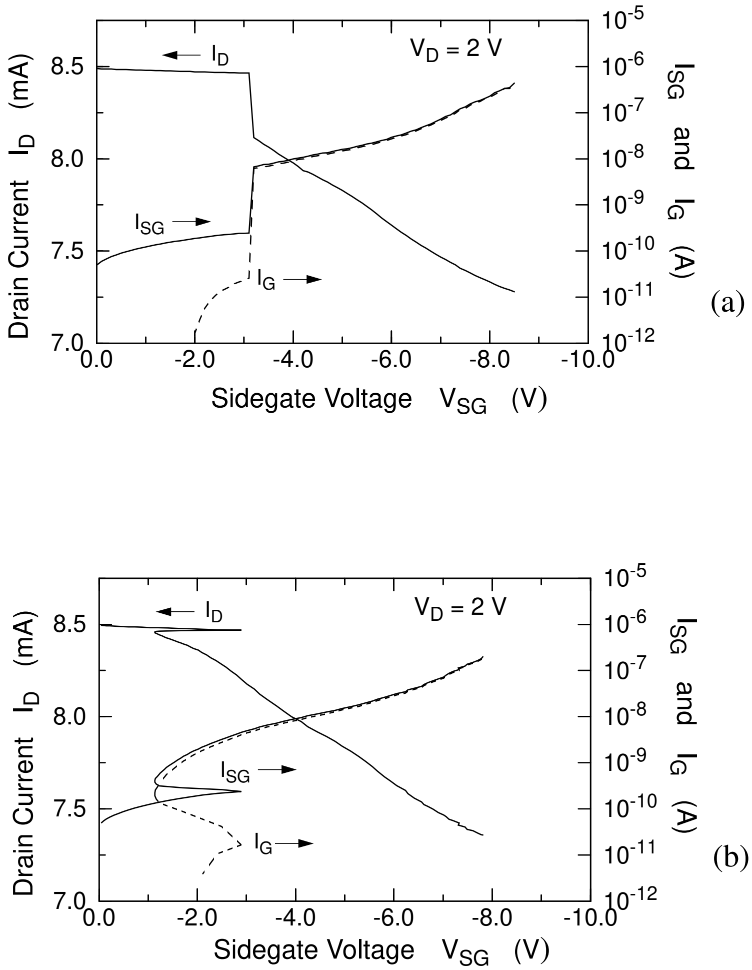


Figure 4.14 Sidegating effect of MESFET device and leakage current characteristics. The measurements were made on a test structure of the distance between the MESFET and the sidegate L_{SG} = 15 μm. Results of the voltage-controlled measurement showing abrupt changes at a threshold sidegating voltage. (b) Results of the current-controlled measurements showing S-shaped characteristics.

MESFET devices, as shown in Figure 4.14.

4.3.4 Summary

The measured basic sidegating characteristics (see Figure 4.9) have shown that the metal contact on the substrate not only causes the high substrate leakage current but also aggravates drain current reduction when the negative sidegate voltage is applied. This provides the direct experimental evidence that the small portion of the gate metal of a MESFET plays an import role in causing serious problems of sidegating and leakage current. The aggravated drain current reduction is attributed to that, while both electron and hole concentrations are increased in the bulk of the substrate due to the double-injection, hole-depletion in the region below the channel-substrate interface disturb the charge-neutrality, leading to the creation of net negative space-charge.

The threshold, hysteresis, and S-shaped characteristics are found to be related to the positive bias voltage at drain of the ungated device. The effect of the positive drain voltage is to impede the hole-injection from the metal contact. The onset of the double-injection process is then postponed to the point that the effect of the drain bias is overcome when the voltage or current at the sidegate is sufficiently large. The threshold, hysteresis and S-shaped characteristics result from the "on" and "off" of the double-injection process.

It should be pointed out that the threshold characteristics can be influenced by factors such as substrate quality, device geometry, and test structure configurations. There may be sources other than the positive drain bias that hamper the hole-injection, such as poor conditions of the metal-substrate interface of the metal contact, from which the threshold characteristics may also result.

4.4 Sidegating Effects Related to n-i-n Structures

In this section, the sidegating characteristics measured in the absence of a hole-injecting source such as a metal contact are discussed. The purpose is to investigate the sidegating mechanisms related to n-i-n structures.

4.4.1 Test Structure and Measurements

The test structure used for this experiment is the same as that shown in Figure 4.8. But to investigate the sidegating effect related to only the n-i-n structure formed by the device and the sidegate, the metal contact is not used (i.e. V_{SC} floating). With the source of the device grounded ($V_S = 0$) and the drain biased at a contact voltage V_D, the drain current I_D and the sidegate current I_{SC} are measured as functions of the variable negative voltage V_{SG} applied to the sidegate.

4.4.2 Sidegating Effect and n-i-n Current

Figure 4.15 shows the drain current and sidegate current characteristics measured from a test structure with the distance $L_{SG} = 20$ µm between the ungated device and the sidegate at the drain bias voltage of $V_D = 0.1$ V. The sidegate current I_{SG}, which is the substrate leakage current between the ungated device and the sidegate, first increases linearly as the sidegate voltage rises from zero and then increases at lower rates as the voltage becomes higher (see Figure 4.15(b)). The sidegate current saturates at sufficiently high sidegate voltages, only increasing very slowly as the voltage continues to rise. The sidegate current remains below 0.3 nA within the entire voltage range of the measurement. The low substrate leakage current is expected; as has been experimentally investigated (see Section 4.2), the current in an n-i-n structure remains low except for very small distances between the contacts.

A threshold behavior is observed in the measured drain current characteristics as shown in Figure 4.15(a). The drain current is found to decrease at much higher rates after the increasing sidegate voltage passes a distinguishable threshold value; the amount of drain current reduction for voltages smaller than the threshold is small in comparison. The important observation to make here is that the threshold sidegate voltage is also approximately the point at which the sidegate current can be considered saturated.

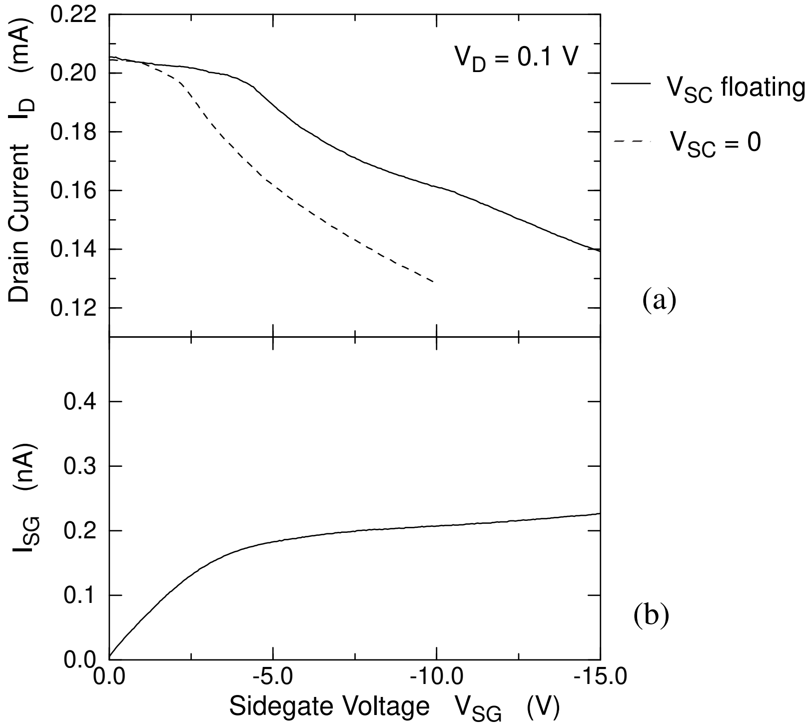


Figure 4.15 Sidegating and leakage characteristics without the metal contact effect. (a) Drain currents of the ungated device. The current measured with the $V_{SC} = 0$ is also shown (dashed curve) for comparison. (b) Sidegate current.

4.4.3 Discussion

For low sidegate voltages, electron concentration in the substrate is essentially not significantly changed, while holes are depleted. For a substrate made from undoped LEC GaAs material, the major deep-level center for compensation is an electron-trap. The charge-neutrality in equilibrium in the substrate is then easily disturbed by changes in electron concentration, but variations in hole concentration have little effect. Therefore, no significant amount of negative space-charge is created in the substrate, and the reduction of the drain current is small.

The decrease of the drain current for sidegate voltages greater than the threshold (see Figure 4.15(a)) indicates the creation of significant amounts of negative space-charge in the region below the channel-substrate interface. This can be explained by adopting the theory used to explain the steady state currents in Gunn diodes [65], which also requires taking into consideration of the negative-differential-mobility in the velocity-field relation of electrons in GaAs. Following the analysis of this theory, the fields in the substrate reach the critical value at the which the electron velocity peaks when the sidegate voltage becomes sufficiently high. Further increase of the sidegate voltage leads to the formation of a stationary high-field domain in the region right below the channel-substrate interface. In this high-field domain, electron concentration is increased to compensate the lower electron velocity in order to maintain current continuity. The higher electron concentration leads to more electrons being captured by and trapped on the deep-level electron-traps. The charge-neutrality is then disturbed and net negative-space charge is created in the high-field domain which is located below the channel-substrate interface, leading to electron-depletion in the channel of the device and causing the channel current to decrease.

As the sidegate voltage increases further, the domain of high-field and negative space-charge expands, while the fields in the bulk of the substrate outside of the domain changes very little. Therefore the current in the substrate saturates. The mechanisms related to the negative-differential-mobility will analyzed in greater detail using computer simulations in Chapter 4.

4.5 Summary and Conclusions

Experiments described in this chapter clarify several issues concerning substrate leakage currents and sidegating effects for devices built on undoped LEC GaAs substrates. First, the experimental results reveal two types of sidegating effects. One type is that, in the presence of a metal contact on the substrate, the degradation of the drain current of a device is accompanied by a high substrate leakage current. The other type is that, when the effect of a hole-injecting source is absent, the reduction of the drain current shows threshold characteristics while the substrate leakage current saturates and remains at low levels.

Experiments have shown that high leakage currents are more likely to occur between a metal contact on the substrate and an n-type electrode biased at lower potentials, than between two n-type contacts. The semi-insulating substrate provides good isolation among n-type regions as far as substrate leakage currents are concerned. Serious leaking between two n-type contacts take place only when the contacts are positioned very close to each other ($L \leq 3\mu\text{'m}$). However, the semi-insulating substrate does not necessarily prevent devices from interacting with each other; serious drain current reduction still occurs when the substrate leakage current is low. Low leakage does not mean absence of sidegating effects.

The presence of the metal has two effects: (a) it causes high substrate leakage currents; and (b) it aggravates the degrading effect of the negative sidegate voltage on the drain current. These two effects are obviously correlated. The dramatic differences in the sidegating and leakage current characteristics observed in the presence and absence of the effects of the metal contact strongly suggest different underlying physical mechanisms in the two cases.

The experimental results cannot be explained consistently by either the trap-fill-limited process or trap-impact-ionization. In the case in which the effects of the metal contact are present, the double-injection (i.e. hole-injection from the metal contact and electron-injection from the sidegate) and the related changes in carrier concentrations and charge distributions are proposed to explain the high leakage currents and the aggravated sidegating effects. In the case that no hole-injecting sources such as a metal contact are present, the sidegating effect is attributed to changes of charge distributions due the negative-differential-mobility of electrons in GaAs. These mechanisms are analyzed with the aid of computer simulations in Chapter 5.

Chapter 5

Simulations and Analyses

In this chapter the characteristics of the sidegating effects observed in the experiments described in Chapter 4 are simulated using an enhanced version of PISCES, a two-dimensional device simulator [13] [14]. Simulation-generated distributions of electron and hole concentrations, electric field, charge, and occupancy of deep-level centers are analyzed. The conditions under which negative space-charge is created in the substrate at the channel-substrate interface of a device are investigated to provide a basis for understanding the underlying mechanisms responsible for the sidegating effect. Three types of sidegating mechanisms are analyzed: (1) the trapping of electrons; (2) the double-injection and electron-trapping; and (3) the de-trapping of holes.

5.1 Electron-Trapping and the Sidegating Effects

The sidegating characteristics measured in the absence of a hole-injecting source for example a metal contact, are such that the drain current of a device shows threshold behavior and the substrate leakage current saturates and remains at low levels, as described in Chapter 3. In this section, the conditions for the occurrence of such characteristics are investigated with the aid of simulations. The role of an electron-trap is also analyzed.

5.1.1 Simulations Using a Vertical Structure

Figure 5.1 shows two structures to be used in simulations. Simulations are first performed using the vertical structure shown in Figure 5.1(a). The vertical structure does not reflect

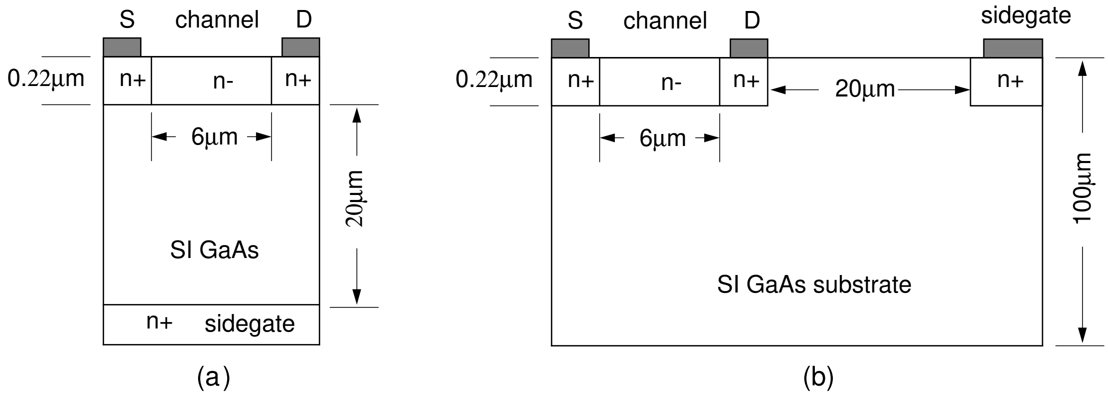


Figure 5.1 Vertical (a) and lateral (b) structures used for simulations.

the real test structure used in measurements as well as the lateral structure in Figure 5.1(b). However, because of the symmetry of the vertical structure, analyses of the simulation results at low drain bias voltages become relatively straight forward. The important parameters and models used in the simulations and the simulation results are described as follows.

A. Vertical Structure: Device and Sidegate

An ungated device and an n-type sidegate are separated from each other by a semi-insulating GaAs substrate of a thickness of L_{SG} = 20 μm, with the device at the top and the sidegate electrode at the bottom (Figure 5.1(a)). The channel-depth of the ungated device is 0.22 μm, and the channel doping is set at $4.0\times10^{16}\text{cm}^{-3}$. The values for the channel-depth and channel doping are chosen based on approximating the channel of the real device with a uniform doping profile, as described in Chapter 3. These values are also adjusted to achieve a good agreement between measured results and those simulated using the lateral structure in Figure 5.1(b) as described later. The sidegate and the source and drain contact regions of the device are all doped to $1.0\times10^{17}\text{cm}^{-3}$.

B. Semi-insulating Substrate

Undoped LEC GaAs substrates are used to built the devices used in the electrical measurements described in Chapter 3. For undoped LEC GaAs, acceptor-type shallow-level impurities such as carbon are unintentionally incorporated into the material during crystal growth [62]. The semi-insulating property of such substrates is achieved through the compensation of the shallow-acceptors by a native defect, EL2, which is also a deep-level donor [66]-[72]. For simulations the substrate is specified to have a shallow-acceptor with a concentration of $N_A = 5.0\times10^{15}\text{cm}^{-3}$ and the deep-donor EL2 concentration is chosen to be $N_t = 5.0\times10^{16}\text{cm}^{-3}$.

There have been a number of published studies on EL2 about its origin [73]-[81], energy level, electron and hole capture cross-sections, and concentrations [82]-[87]. According to Martin *et. al.* [69] the EL2 energy level at different temperatures can be calculated using

$$E_c - E_t(\text{EL2}) = 0.759 - 2.37\times10^{-4}T \quad \text{eV} \tag{5.1}$$

The electron and hole capture cross-sections as measured by Mitonneau *et. al.* [83] are:

$$\sigma_n(\text{EL2}) = 6\times10^{-15}e^{-0.066\text{eV}/kT}\text{cm}^2 \tag{5.2}$$

$$\sigma_p(\text{EL2}) = 2\times10^{-18}\text{cm}^2 \tag{5.3}$$

Although the σ_n and σ_p listed in (5.2) and (5.3) were measured for different temperature ranges, their applicability can be extrapolated to room temperature as suggested by Blakemore [87]. The values of these parameters at $T = 300$ K used in the simulations are $\sigma_n = 4.7\times10^{-16}\text{cm}^2$ and $\sigma_p = 2\times10^{-18}\text{cm}^2$. The energy level at $T = 300\text{ K}$ is $E_c - E_t = 0.688$ eV.

The fact that the electron capture cross-section is much greater than the hole capture cross-section ($\sigma_n \gg \sigma_p$) makes EL2 an electron-trap. The implication concerning sidegating effects will be discussed when simulation results are analyzed.

C. Electron Drift-Velocity vs. Electric-Field

The electron drift-velocity vs. electric-field relations in GaAs has been observed to have a

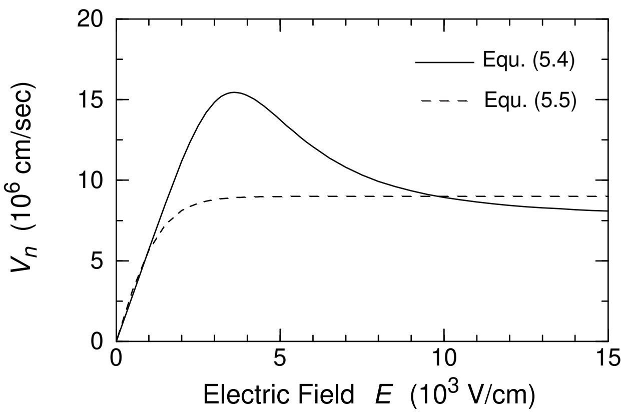


Figure 5.2 Electron velocity-field relations used for simulations.

negative-differential-mobility characteristic; the electron velocity decreases with increasing field when the field is greater than a critical value [6]. This characteristic results from the so-called transferred-electron effect which refers to the fact that some electrons in the high-mobility valley are transferred to the low-mobility satellite valleys under the influence of sufficiently high electric fields [61] [88]. For simulations the velocity-field relation with the negative-differential-mobility characteristic is modeled with the expression [89]

$$v_n = \frac{\mu_o E + v_{sat}(E/E_o)^4}{1 + (E/E_o)^4} \tag{5.4}$$

where E is electric field, μ_o the low-field mobility, v_{sat} the saturation velocity at high fields, and E_o is a constant. The saturation velocity is temperature dependent; at $T = 300$ K $v_{sat} = 7.7 \times 10^6$ cm/sec [90]. Choosing $\mu_o = 5700\ \text{cm}^2/\text{Vs}$ and $E_o = 4000$ V/cm, the velocity-field characteristic calculated using (5.4) is shown in Figure 5.2 as the solid curve.

An expression for a velocity-field relation not yielding the negative-differential-mobility characteristics is also used in the simulations for the purpose of comparison:

$$v_n = v_{sat} \,\text{than}(\mu_o E / v_{sat}) \tag{5.5}$$

With $\mu_o = 5700\text{cm}^2/\text{Vsec}$ and $v_{sat} = 9.0\times10^6\text{cm/sec}$ the velocity-field characteristic resulting from this expression is also shown in Figure 5.2 (the dashed curve).

D. Simulation Results

In a simulation, the source of the ungated device is at the ground potential ($V_S = 0$), and the drain is biased at $V_{DS} = 0.1$ V. A variable negative voltage V_{SG} is applied to the sidegate, and the drain current I_D of the ungated device and the current at the sidegate I_{SG} are calculated as functions of V_{SG}. The sidegate current is in fact the leakage current in the semi-insulating substrate.

The results of the simulations are shown in Figure 5.3. Completely different results are produced by the simulations using the two different electron velocity-field relations. The I_D-V_{SG} characteristic (dashed curve in Figure 5.3(a)) given by the simulation using the velocity-field relation without the negative-differential-mobility (Equation (5.5)) shows little reduction of the drain current over the entire range of the sidegate voltage.

In contrast, the simulation using the velocity-field relation with the negative-differential-mobility (Equation (5.4)) produces the I_D-V_{SG} characteristic (solid curve in Figure 5.3(a)) that shows significant drain current reduction with a threshold behavior. The threshold value is $V_{SG,th} = -6.8$'V in this case. As shown in Figure 5.3(a), for the sidegate voltages smaller than the threshold ($|V_{SG}| < |V_{SG,th}|$) there is little decrease of the drain current. The drain current I_D starts to be modulated by the sidegate voltage only when V_{SG} reaches the threshold and then decreases with V_{SG} as it goes beyond the threshold ($|V_{SG}| \geq |V_{SG,th}|$). The sidegate current I_{SG} (solid curve in Figure 5.3(b)) first increases with the sidegate voltage before the threshold value is reached ($|V_{SG}| < |V_{SG,th}|$), and then it saturates at the threshold and remains constant at the saturation level as the sidegate voltage in creases further ($|V_{SG}| > |V_{SG,th}|$). Both the threshold and saturation behaviors in the simulation-generated I_D-V_{SG} and I_{SG} -V_{SG} characteristics (solid curves in Figure 5.3) have the features that are qualitatively similar to those observed in the experiments

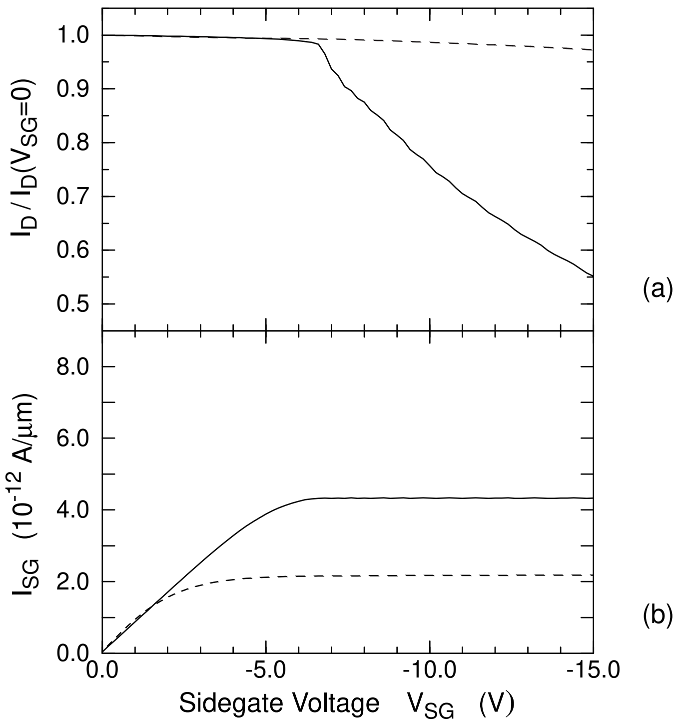


Figure 5.3 Results of simulations using the structure in Figure 5.1(a). The the solid curves (——) are simulated with the negative-differential-mobility model of Equation (5.4), and the dashed curves (- - -) with the mobility model of Equation (5.5).

described in Chapter 4 (see Figure 4.15)

5.1.2 Analysis of Simulation Results

The decrease of the drain current of a device indicates the creation of a negative space-charge in the region of the semi-insulating substrate very close to or right below the channel-substrate interface, which depletes electrons in the channel near the interface. Comparison of the results given by the simulations using the two different electron velocity-field relations demonstrates the importance of the negative-differential-mobility. To understand the underlying mechanisms responsible for the particular sidegating characteristics, it is necessary to analyze the effect of the electron negative-differential-mobility and how negative space-charge is created in the type of substrate used.

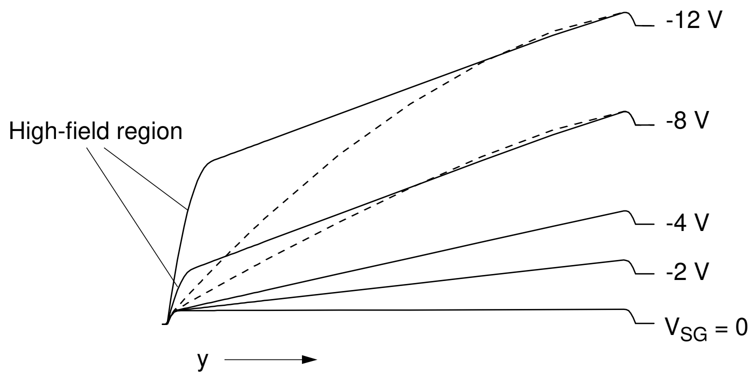


Figure 5.4 Band edge profiles from simulation using the structure in Figure 5.1(a) in vertical (y) dimension. The solid curves (——) are simulated with the negative-differential-mobility model of Equation (5.4), and the dashed curves (- - -) with the mobility model of Equation (5.5).

A. Negative-Differential-Mobility and Stationary High-Field Domain

In their analyses of Gunn diodes, Böer and Döhler showed theoretically that a stationary high-field domain of negative space-charge may form at the anode of a diode in steady state under the influence of high fields because of the negative-differential-mobility of electrons [65]. The condition for this to occur requires that the cathode should be an injecting contact, i.e. the conductivity of the cathode is greater than that of the bulk [65]. The same theory can be applied to the n-i-n structure composed of the ungated device, the semi-insulating substrate, and the n-type sidegate which is an electron-injecting electrode when negatively biased. When the sidegate voltage is high enough, a high-field region of negative space-charge is then expected to be created right below the channel-substrate interface, as proved to be the case by the profiles generated by the simulations.

Figure 5.4 shows the conduction-band edge profiles in the vertical dimension from the top surface of the channel to the bottom of the sidegate along the symmetry line of the structure in Figure 5.1(a). The linearly graded band edges for sidegate voltages smaller than the threshold indicate that the applied voltage drops uniformly across the whole length of the substrate and the slope of the band edge becomes steeper as the voltage increases, as seen for V_{SG} = -2.0 V and -4.0 V in Figure 5.4. As the sidegate voltage goes beyond the threshold, on the other hand, the slope of the band edge in the bulk of the substrate does not become steeper, as seen when comparing the profiles for $V_{SG} = -8.0$ V and -12.0 V in Figure 5.4. However, in the narrow region below the channel-substrate interface the slope of the band edge becomes steeper as the sidegate voltage increases, indicating the formation of the high-field domain. The high-field domain also expands with the increasing sidegate voltage while the slope of band edge outside of the domain remains unchanged. In contrast, no such distinguishable high-field domain is displayed by the band edge profiles (dashed curves in Figure 5.4) given by the simulation without the negative-differential-mobility.

Figure 5.5(a) shows the distribution of the vertical component of the electric field along the vertical dimension for a length of up to 3 μm from the top surface of the channel. For a sidegate voltages smaller than the threshold the field in the bulk of the substrate is increased to a value approximately of $E_y = |V_{SG}|/L_{SG}$; for example at V_{SG} = -4.0 V the field in the substrate given by the simulation is $E_y = 2000$ V/cm. However, the field in the region right below the channel-substrate interface is not sufficiently increased from that for zero sidegate voltage, as seen also for V_{SG} = -4.0 V in Figure 5.5(a). For sidegate voltages greater than the threshold, field values are significantly increased in the high-field domain located right below the channel-substrate interface, as demonstrated by the field distributions for $V_{SG} = -8.0$ V and $V_{SG} = -12.0$ V in Figure 5.5(a). On the other hand, the field outside the domain in the bulk of the substrate remains fixed at the value of $E_y = |V_{SG,\,th}|/L_{SG} = 3400$ V/cm. It should be noted that this is also the critical value of field at which the electron drift-velocity reaches its peak (solid curve in Figure 5.2). From this observation it should be clear that the high-field domain starts to be formed as the field in the substrate reaches this critical value when the sidegate voltage is increased to the threshold. As the sidegate voltage goes beyond the threshold the field in the bulk of the substrate remains at $E_y = |V_{SG,\,th}|/L_{SG}$ while the field increases further in the high-field domain, which also expands with the increasing sidegate voltage.

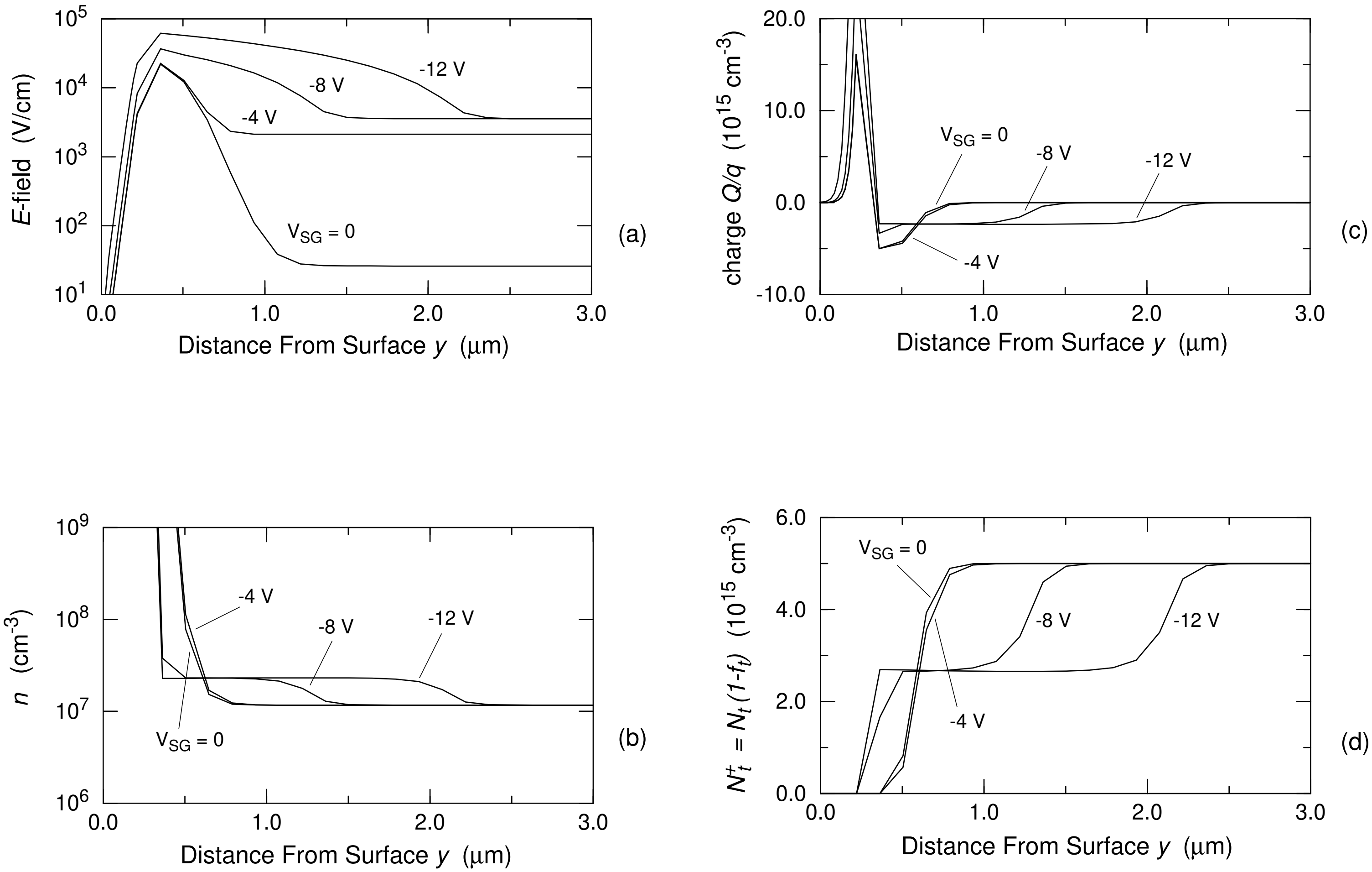


Figure 5.5 Profiles along the vertical dimension given by simulations.

Since the field in the high-field domain is higher the critical value, the electron velocity in the domain is lower than that outside the domain. To maintain the continuity of the electron current in steady state electron concentration in the high-field domain then must be higher to compensate the slower average movement of electrons. As shown in Figure 5.5(b), electrons concentrations for $V_{SG} = -8.0$'V and $V_{SG} = -12.0$'V are indeed higher than that in the bulk of the substrate, where electron concentration is the same as that for zero sidegate voltage. Since the field outside the domain is still at $E_y = |V_{SG,th}|/L_{SG}$ for $|V_{SG}| \geq |V_{SG,th}|$, the current in the substrate therefore saturates as the sidegate bias goes beyond the threshold, as seen in Figure 5.3(b).

B. Negative Space-Charge and Electron-Trapping

Accompanying the formation of the high-field domain is the creation of negative space-charge as seen for $V_{SG} = -8.0$'V and $V_{SG} = -12.0$'V in Figure 5.5(c), while charge-neutrality is maintained outside the domain. In response to the creation of the negative space-charge, electrons in the channel of device are depleted from the region near the channel-substrate interface, leading to the decrease of channel current. But for a sidegate voltage smaller than the threshold, for example $V_{SG} = -4.0$'V in Figure 5.5(c), the charge distribution is not significantly altered from that for $V_{SG} = 0$. Therefore the sidegate voltage starts to modulate the current in the channel only after the high-field domain is formed and negative-space charge is created when the sidegate voltage reaches the threshold value.

The density of the negative space-charge in the high-field domain cannot be accounted for with the amount of increase of electron concentration. Hole-depletion can not create that amount of negative charge either because the hole concentration in equilibrium itself is much lower than that of the shallow-acceptors. The creation of the negative space-charge then must be originated from changes of the concentration of ionized deep-level center $N_t^+ = N_t\,(1 - f_t)$. Following the analysis by Shockley and Read, the electron-occupation function f_t in steady state takes the form which results from the balance between the net capture rates of electrons and holes [91]:

$$f_t = 1/[1 + (c_n n_t + c_p p)/(c_n n + c_p p_t)] \tag{5.6}$$

where n_t and p_t are defined as $n_t = N_c e^{(E_t - E_c)/kT}$ and $p_t = N_v e^{(E_v - E_t)/kT}$. The electron and hole capture coefficients are defined as $c_n = \sigma_n \bar{v}_n$ and $c_p = \sigma_p \bar{v}_p$, where $\bar{v}_n$ and $\bar{v}_p$ are electron and hole thermal velocities respectively.

Since EL2 is an electron-trap ($\sigma_n \gg \sigma_p$), the conditions $c_n n_t \gg c_p p$ and $c_n n \gg c_p p_t$ hold for electron and hole concentrations in the ranges of interest. The electron-occupation function can be approximated as $f_t \approx 1/(1 + n_t/n)$ and the concentration of ionized EL2 as $N_t^+ \approx N_t/(1 + n/n_t)$. Charge-neutrality in the substrate requires:

$$p + N_t^+ = n + N_A \tag{5.7}$$

which can be approximated as $N_t^+ = N_A$ since the values of n and p are insignificant compared to N_A. However, even though not making n itself large enough to be counted as a significant contribution, the increase of electron concentration in the high-field domain (Figure 5.5(b)) leads to a decrease of N_t^+ because of its dependence on n. The balance between N_t^+ and N_A is then disturbed and a net negative space-charge is created, as shown in Figure 5.5(c).

From a physical point of view, the fact that electron capture cross-section of the electron-trap is much greater ($\sigma_n \gg \sigma_p$) means that it has a more active interaction with electrons than with holes — it captures and emits electrons more actively. As long as hole concentration is not high ($p \ll c_n n_t/c_p$), the probability of the electron-trap captures and traps electrons depends only on electron concentration while hole concentration has little influence. Therefore, depletion of holes in the substrate upon the application of a sidegate voltage does not change N_t^+. On the other hand, the increase of electron concentration in the high-field domain lead to more electrons being captured. The number of electrons occupying the electron-trap increases until the balance between the electron capture and emission is re-established. As a result, more electrons are trapped and N_t^+ is decreased, creating net negative space-charge.

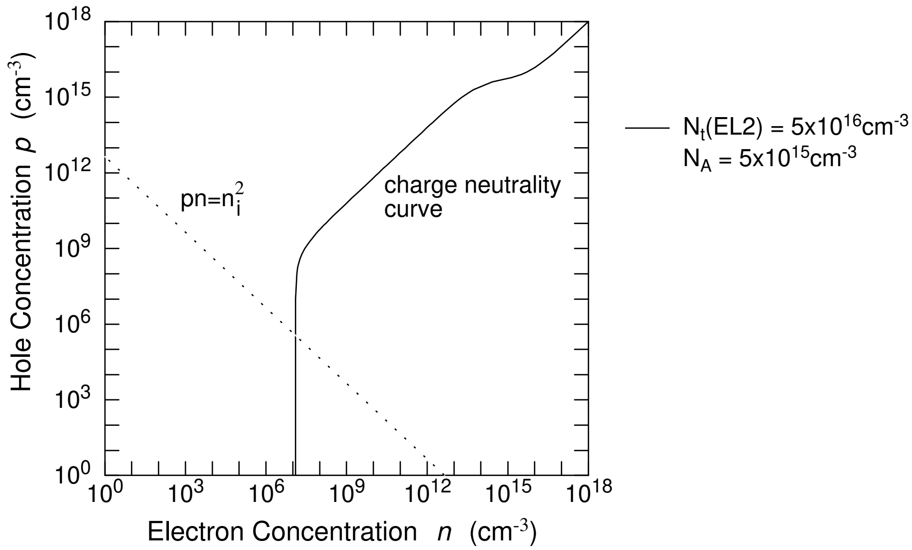


Figure 5.6 Charge-neutrality curve.

The distribution of N_t^+ (Figure 5.5(d)) calculated using (5.6) with simulation-generated electron and hole concentrations show that N_t^+ is indeed decreased in the high-field domain by amounts that agree with the negative-space charge (Figure 5.5(c)).

The above analysis relating electron-trapping to the creation of negative space-charge can be visualized using the charge-neutrality curve shown in Figure 5.6, which is obtained by solving n and p from Equations (5.7) and (5.6). Below and to the right of the charge-neutrality curve is a region where the n and p values that result in net negative charge; above and to the left of the curve the n and p values lead to a net positive charge. The point of intersection of the charge-neutrality curve with the dotted line for n and p values that satisfy $pn = n_i^2$ represents the equilibrium state, which is on the vertical section of the charge-neutrality curve (i.e. the section parallel with the p-axis). When a negative sidegate voltage smaller than the threshold is applied, holes are depleted in the substrate but electron concentration essentially remains unchanged, as seen for $V_{SG} = -4.0$'V in Figure 5.5(b). The values of n and p are still on the vertical section of the charge-neutrality curve; charge-neutrality in the substrate is not disturbed and no new negative space-charge is created. Once the high-field domain is formed when the sidegate voltage exceeds the threshold, the increased electron concentration in the domain pulls n and p away from the charge-neutrality curve, resulting in a net negative space-charge. The vertical section of the charge-neutrality curve reflects the sensitivity of charge to the electron concentration when the major deep-level center for compensation in the substrate is an electron-trap.

5.1.3 Simulation Using a Lateral Structure

The lateral structure of Figure 5.1(b) is a better reflection of the configuration used in the test structures for the experiments (see Chapter 3) in the sense that both the device and the sidegate are on the same surface of the substrate. The doping conditions and the geometry of both the device and the sidegate of this lateral structure are the same as those of the vertical structure. The distance between the device and the sidegate is again $L_{SG} = 20$ µm. The 100µm-thick semi-insulating substrate contains shallow-acceptor of concentration $N_A = 5.0\times10^{15}\mathrm{cm}^{-3}$ and deep-donor/electron-trap EL2 of concentration $N_t = 5.0\times10^{15}\mathrm{cm}^{-3}$, which are also the same as those in the vertical structure. Simulations are performed with the electron velocity-field relation with the negative-differential-mobility characteristic of Equation (5.2).

The simulated drain current I_D and sidegate current I_{SG} as functions of the sidegate voltage V_{SG} are shown (solid curves) in Figure 5.7. The threshold behavior and current saturation are seen in the I_D -V_{SG} and I_{SG} -V_{SG} characteristics given by the simulation. The experimentally measured drain and sidegate currents are also shown (dashed curves) in Figure 5.7 for comparison. The simulated and measured results are in excellent agreement. The simulated sidegate current still increases, but at a much lower rate, after the sidegate voltage reaches the threshold, unlike the current simulated with the vertical structure that reaches complete saturation (Figure 5.3(b)). The increase of the sidegate current after the threshold is also observed in the measured current. This is due to the fact that

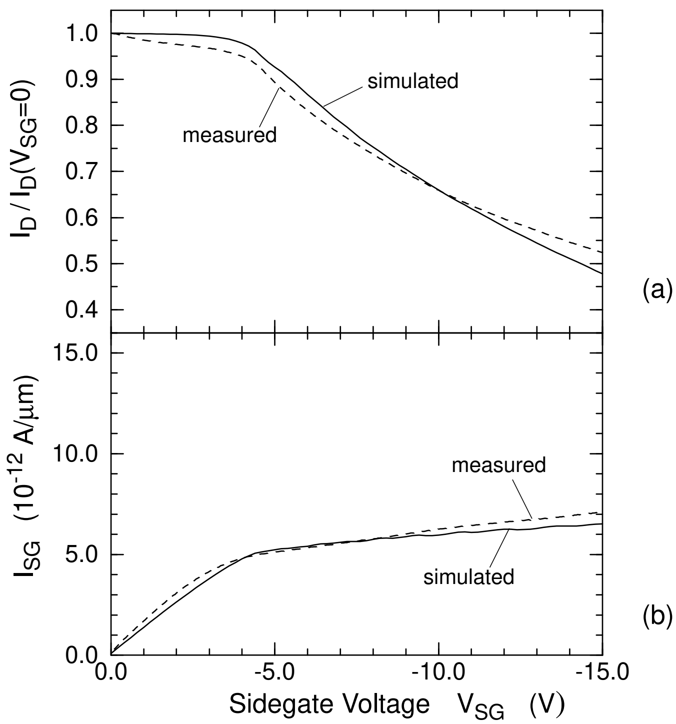


Figure 5.7 Simulated and measured I_D-V_{SG} and I_{SG}-V_{SG} characteristics. The simulations are done using the structure in Figure (5.1)(b), and the measurements are made on a structure like the one in Figure 4.8.

after the sidegate voltage reaches the threshold there is still an additional voltage drop across the bulk of the substrate in the lateral structure.

Due to two-dimensional effects, the value of the threshold sidegate voltage measured in experiments and obtained from the simulations of the lateral structure are different from those obtained from the simulations of the vertical structure, especially for large distances between the device and the sidegate. Values of threshold voltages measured and obtained from simulations at different distances L_{SG} are shown in Figure 5.8. It can be seen that the simulations using the lateral structure makes much better predictions than with the vertical structure.

5.1.4 Summary

Sidegating and leakage current characteristics of devices built on an undoped LEC

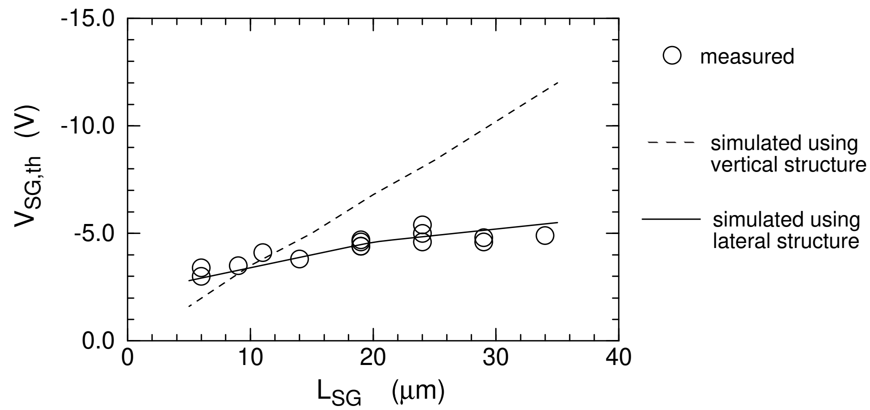


Figure 5.8 Sidegating threshold voltages given by simulations and measurements.

substrate are simulated and analyzed. The substrate is modeled with a shallow-acceptor and the deep-donor/electron-trap EL2. The degradation of the drain current of a device is a direct consequence of the existence of negative space-charge below the channel-substrate interface which depletes electrons in the channel. The creation of negative space-charge results from more electrons being captured and trapped by the electron-trap owing to the increased electron concentration in the high-field domain and the strong dependence on the electron concentration of the steady state electron-occupancy function of the electron-trap. The formation of the high-field domain is due to the negative-differential-mobility characteristics in the velocity-field relation of electrons in GaAs, and electron concentration in the domain has to rise to compensate for the slower average movement of electrons so current continuity is maintained. The trapping of electrons reduces the density of the positively-charged deep-donor/electron-trap EL2, leading to the creation of net negative space-charge in the region below the channel-substrate interface. The electrons needed for the increased electron concentration and electron-trapping are supplied by the n-type side-gate which injects electrons into the substrate.

The threshold behavior in the sidegating characteristics result from the fact that the domain of high-field and negative space-charge is formed only when the field in the substrate is sufficiently high. The substrate leakage current saturates and remains at low levels because, once the high-field domain is formed, in the bulk of the substrate (i.e. outside the domain) the field increases very little with the increasing sidegate voltage and the electron concentration remains unchanged.

5.2 Double-Injection and Sidegating Effect

In the measurements of the sidegating effects involving a metal contact, aggravated degradation of the drain current of a device and the high leakage current in the substrate were observed, as described Chapter 4. In this section, the sidegating and substrate leakage current characteristics in the presence of a metal contact are simulated. The underlying mechanisms are investigated by analyzing simulation results.

5.2.1 Simulation of Sidegating and Leakage Current

A. Vertical Structure Used for Simulation

Figure 5.9(a) shows the vertical structure used for simulations. The channel-depth of the ungated device is 0.22 µm and the channel doping is set at $4.0\times10^{16}\mathrm{cm}^{-3}$. The sidegate and the source and drain contact regions of the device are all doped to $1.0\times10^{17}\mathrm{cm}^{-3}$. The distance from the device to the sidegate is L_{SG} = 20 µm.

The semi-insulating GaAs in the structure is assumed to be an undoped LEC substrate, which is the type of substrate on which the devices used for electrical measurements (see Chapter 4) have been built. For simulations the substrate is specified to have a shallow-acceptor of concentration $N_A = 5.0\times10^{15}\mathrm{cm}^{-3}$ and the deep-donor/electron-trap EL2 of concentration $N_t = 5.0\times10^{16}\mathrm{cm}^{-3}$. The energy level and electron and hole capture cross-sections of EL2 are given by Equations (5.1)-(5.3).

The structures in Figure 5.9(a) are basically the same as those in Figure 5.1(a) except the existence of the metal contacts located 3 µm away from the drain electrodes of the ungated device. The metal contact simulates the effect of the small portion of the gate metal of a MESFET that touches the substrate.

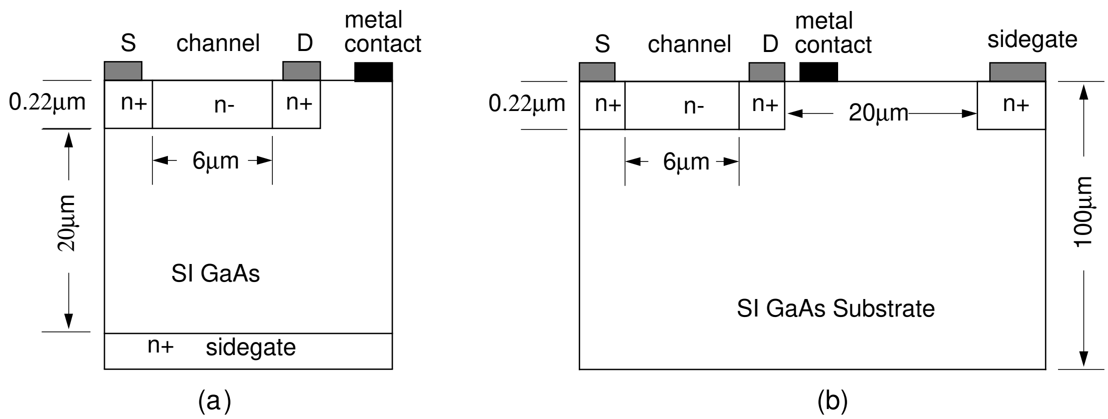


Figure 5.9 Structures including metal contacts used for simulations

In simulations the metal contact is treated as a Schottky type contact. The Fermi level at the metal-GaAs interface is taken to be pinned at a position 0.83 eV below the conduction band edge in the energy gap. In PISCES, a Schottky contact is modeled based on the thermionic-emission theory [13] [61] [92]. The effective Richardson constant for holes is $A^{*}=120(m_l + m_h)/m_o$ 'Acm^{-2}'K^{-2}, where m_o is the electron mass in vacuum, and m_l and m_h are the effective mass for light and heavy holes respectively. Similarly for electrons $A^{*}= 120\,m_e/m_o$ 'Acm^{-2}'K^{-2}. Because of optical-scattering and quantum-mechanical reflection, the effective Richard constant is expected to deviate from the values given by the expression above and also be field-dependent [93]-[96]. However, in PISCES A^{*} is treated as a constant to simplify simulations.

When a negative voltage is applied to the sidegate, the bias condition of the m-i-n structure formed by the metal contact and the sidegate is such that holes are injected into the semi-insulating substrate through the thermionic-emission process [61] [92]. Although tunneling mechanisms such as field emission and thermionic-field emission also participate in the hole-injection process under high fields [63], [97], only thermionic-emission is included in the simulations to be described below, which is sufficient to offer a good understanding of the mechanisms of the hole-injection related sidegating effect.

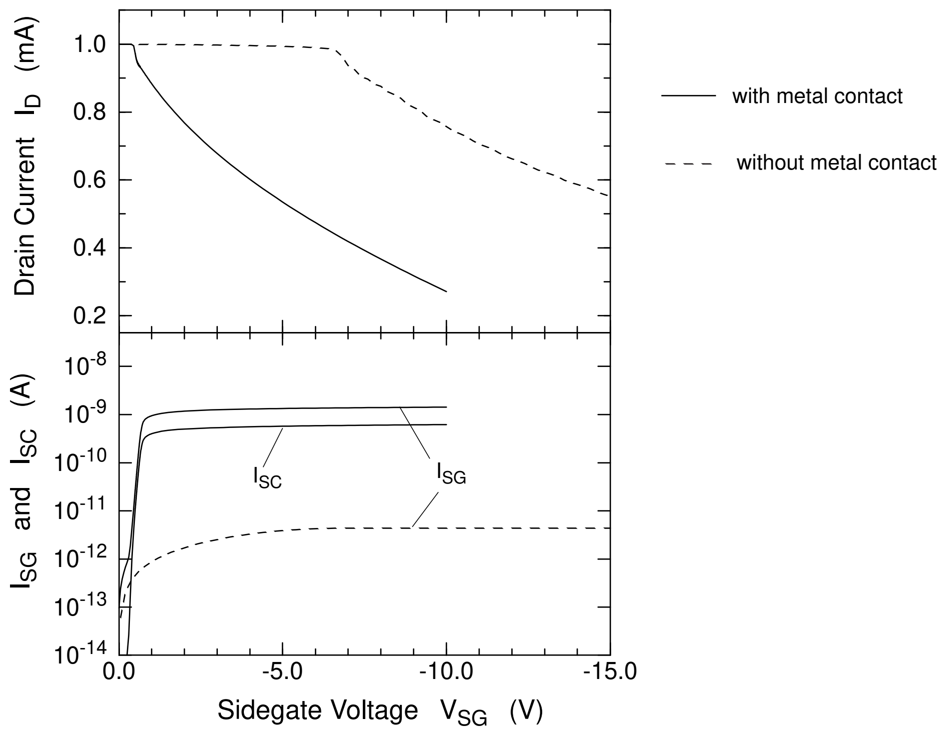


Figure 5.10 Results of simulation using the vertical structure in Figure 5.9(a).

B. Results of Simulation Using the Vertical Structure

To simulate the basic sidegating the leakage current characteristics in the presence of a metal contact, the source of the ungated device in the vertical structure (Figure 5.9(a)) is grounded ($V_S = 0$), and drain is biased at a constant voltage $V_D = 0.1$ V. The metal contact is also at ground potential ($V_{SC} = 0$). The drain current I_D of the ungated device, the side-gate I_{SG} which is in fact the substrate leakage current, and current at the metal contact I_{SC} are all calculated as functions of the negative voltage V_{SG} applied to the sidegate.

The simulation results are shown as the solid curves in Figure 5.10, in which drain and sidegate currents simulated when there is no metal contact are also shown for comparison. The results shown in Figure 5.10 reveal three important features of the effect of including the metal contact in the simulation. One feature is the aggravated sidegating effect, as seen in Figure 5.10(a). The simulated drain current I_D (the solid curve) decreases rapidly with the sidegate voltage V_{SG}, and the reduction of the drain current starts at a value of the sidegate voltage much smaller than the sidegating threshold seen in the drain current (the dashed curve) simulated when the metal contact is absent.

The other important feature, as seen in Figure 5.10(b), is the high sidegate current. The simulated sidegate current I_{SG} (one of the solid curves) is, compared to that from the simulation that does not include the metal contact (the dashed curve), at least two orders of magnitude higher. It can also be seen in Figure 5.10(b) that the current though the metal contact I_{SC} is very high, too. It is then natural to relate the high substrate leakage current to the current conduction between the sidegate and the metal contact.

The third feature is that the value of the sidegate voltage at which the drain current starts to decrease is also the point around which the level of the metal contact current I_{SC} becomes comparable to that of the sidegate current I_{SG}. This suggests the correlation between the drain current reduction and the high current in the m-i-n structure formed by the metal contact and the sidegate.

The simulation results described above are qualitatively consistent with the experimental results in that they directly link the aggravated sidegating effect and the high substrate leakage current to the existence of the metal contact.

5.2.2 Analyses of Simulation Results

To understand the drain current degradation and high leakage current shown in Figure 5.10, the underlying mechanisms are analyzed in terms of how the existence of the metal contact affects the carrier concentration in the substrate and the creation of negative space-charge under the channel-substrate interface.

A. Double-Injection and Increased Electron and Hole Concentrations

The metal contact and the sidegate form an m-i-n structure. When a negative voltage is applied to the sidegate, there is a net flow of holes into the substrate from the metal contact due to some hole-injection process such as thermionic-emission and tunneling. The injected holes move towards the sidegate under the influence of the negative sidegate

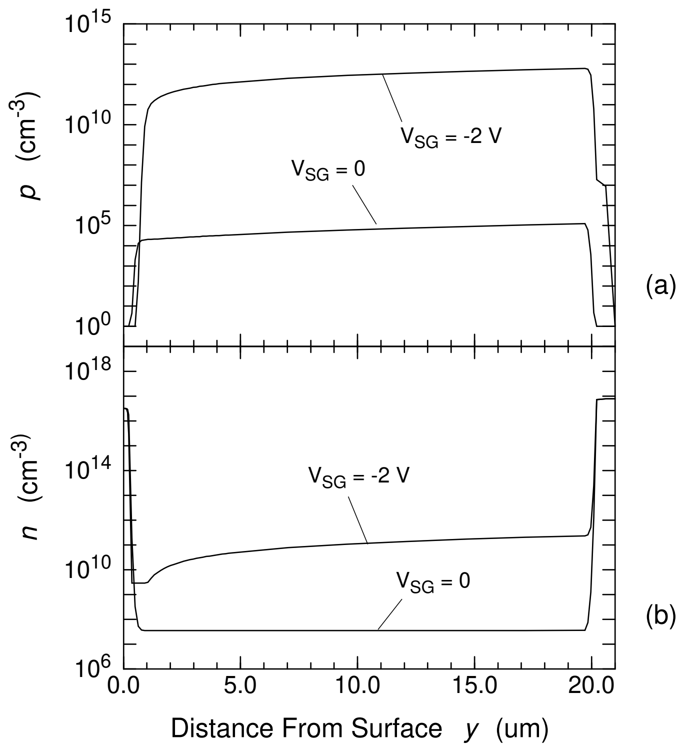


Figure 5.11 Electron and hole concentrations given by simulations.

voltage and to other regions of the substrate by diffusion, and they also recombine with electrons in the substrate and in the heavily doped n-type sidegate region. The n-type sidegate electrode, on the other hand, can supply electrons to be injected into the substrate. Thus, a double-injection process could be triggered as a negative voltage is applied to the sidegate.

Because of the hole-injection from the metal contact, the hole concentration in the substrate is increased. Figure 5.11(a) shows the hole concentration profiles in the vertical dimension from the top surface of the channel to the bottom of the sidegate along the symmetry line of the ungated device, for sidegate voltages of $V_{SG} = 0$ and $V_{SG} = -2.0$ V. The concentration of the holes in the bulk of the substrate is around $10^{12}\mathrm{cm}^{-3}$ at $V_{SG} = -2.0$ V, which is seven orders of magnitude higher than that at $V_{SG} = 0$.

The increased concentration of holes at $V_{SG} = -2.0$ V is not negligible when considering the electron occupancy of the deep-level electron-trap EL2, which is calculated using Equation (5.6). For low hole-concentration conditions ($p < 10^9 \mathrm{cm}^{-3}$ for EL2), for example at $V_{SG} = 0$, holes can be ignored in Equation (5.6) because $p \ll c_n n_t / c_p$. But with the hole concentration increased to the level of $10^{12} \mathrm{cm}^{-3}$ at $V_{SG} = -2.0$ V, due to hole-injection, the condition is reversed and there is now $p \gg c_n n_t / c_p$. The hole concentrations in this range would increase the number of positively charged deep-level EL2 centers and disturb charge balance if the electron concentration was still kept at its equilibrium level. To maintain charge neutrality more electrons are drawn into the substrate from the n-type sidegate, and a double-injection process is thus started. The electron concentration in the bulk of the substrate is increased because of the electron-injection from the sidegate. As shown in Figure 5.11(b), the electron concentration in the bulk is around $10^{11} \mathrm{cm}^{-3}$ at $V_{SG} = -2.0$ V, which is four orders of magnitude higher than that at $V_{SG} = 0$. Thus, both hole and electron concentrations become higher because of the double-injection process.

The charge neutrality in steady state is still maintained in the bulk of the substrate even with the much higher carrier concentrations at $V_{SG} = 2.0$ V. As long as the carrier concentrations are much lower than that of the shallow acceptors in the substrate ($n, p \ll N_A$), the charge neutrality condition can still be written as $N_A \approx N_t (1 - f_t)$. The electron occupation function f_t for the deep-donor/electron-trap is now strongly dependent on both n and p and can be approximated as $f_t \approx 1 / (1 + c_p p / c_n n)$. The n and p values that satisfy the charge neutrality condition fall on the sloped section of the charge neutrality curve in Figure 5.6.

From a physical point of view, the rate at which the deep-level center EL2 captures holes is significantly increased due to the increased hole concentration, owing to the hole-injection from the metal contact, even the hole capture cross-section of EL2 is much smaller than its electron capture cross-section. On the other hand, when the hole concentration is high enough to influence the number of the positively charged deep-level EL2 centers, thus affecting the charge neutrality condition, large number of electrons are injected into the bulk of the substrate. This electron-injection increases the electron concentration in the substrate and in turn increases the rate of electrons being captured by the deep-level. The result is that both hole and electron concentrations are increased, a new balance is established between the rates electrons and holes being captured by the deep-level centers, and charge neutrality in the bulk of the substrate is maintained. The increased electron and hole concentrations lead to a leakage current in the substrate which is orders of magnitude higher than that when there is no double-injection.

B. Creation of Negative Space-charge

Figure 5.12 shows the profiles generated by simulations along the symmetry line of the ungated device for the distance of up to 2.5 μm from the top surface of the channel. It can be seen in Figure 5.12(a) that while charge neutrality is maintained in the bulk of the substrate, net negative space-charge is created in the region below the channel-substrate interface after the double-injection process is started, as shown by the charge distribution for sidegate voltages V_{SG} = -2.0 V and -4.0 V. At the higher sidegate voltage V_{SG} = -4.0 V the region of negative space-charge is wider than that at the lower value of V_{SG} = -2.0 V; deep in the negative space-charge region the charge density normalized to the electron charge is $5\times10^{15}\mathrm{cm}^{-3}$ and equal to the concentration of shallow-acceptors in the substrate.

As has been pointed out before, when a negative sidegate voltage is applied, the bias condition of the n-i-n structure formed by the ungated device and the sidegate is such that holes in the substrate are depleted from the channel-substrate interface. It can be seen in Figure 5.12(b) that even though the hole concentration in the bulk of the substrate is greatly increased at V_{SG} = -2.0 V and -4.0 V, holes are almost completely depleted in the region right below the channel-substrate interface. On the other hand, the electron concentrations in the same region at these two sidegate voltage values are still several orders of magnitude higher than that at $V_{SG} = 0$, as seen in Figure 5.12(c). The increased electron concentration means there are more electrons available to be captured and trapped by the deep-level center EL2, while there are too few holes available in the hole-depleted region to balance this effect. Therefore, most of the deep-level centers in the region become neutral, charge neutrality is disturbed, and a negative space-charge is created. Figure 5.12(d)

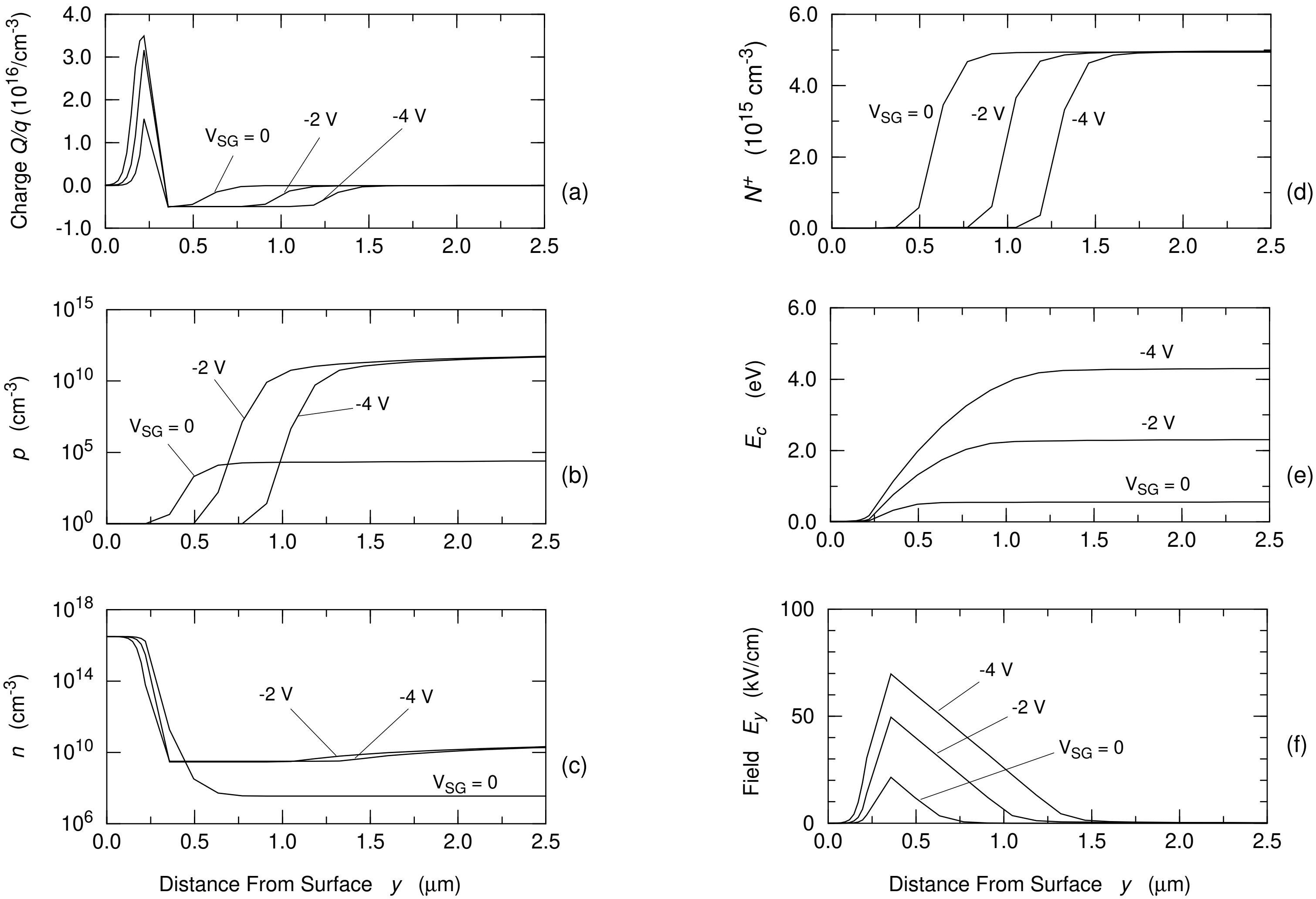


Figure 5.12 Profiles given by the simulation using the vertical structure of Figure 5.9(a).

shows the distribution of the positively charged deep-level centers calculated using simulation-generated electron and hole concentrations. Comparing these to the charge distributions shown in Figure 5.12(a), it is clear that the region in which $N_t\,(1-f_t) \ll N_A$ is the region where there are net negative space-charges. Referring to the charge neutrality curve in Figure 5.6, it can be seen that with the electron concentration above its equilibrium level, the charge neutrality condition also becomes sensitive to the hole concentration; a decrease in hole concentration pulls the n and p values to the region representing net negative space-charge.

Because the bulk of the substrate is charge-neutral, the applied sidegate voltage is only dropped across the negative space-charge region below the channel-substrate interface, as seen in Figure 5.12(e). The profile of the conduction band edges are flat in the bulk region of the substrate, which would have slopes of approximately V_{SG}/L_{SG} if the metal contact was not present. Correspondingly, the distributions of electric field in Figure 5.12(f) show that non-zero field-strength values are only confined to the region of negative space-charge; the field in the bulk of the substrate is zero.

The creation of negative space-charge in the substrate in the region below the channel-substrate interface causes electrons in the channel to be depleted from the interface, leading to the reduction of drain current in the ungated device. From the analysis above, it can be seen that the sidegating effect is closely related to the process of hole-injection from the metal contact and electron-injection from the n-type sidegate. The decreasing of the drain current begins when the double-injection process starts to significantly affect the carrier concentrations in the substrate. When there is a metal contact present, the drain current starts to decrease at a much lower sidegate voltage than that when the metal contact is absent, since the double-injection process is usually initiated before the field in the substrate reaches the critical value at which electron drift velocity begins to decrease. This correlation between sidegating and double-injection also explains why drain current reduction is always observed to be accompanied by high substrate leakage current in the presence of a metal contact.

5.2.3 Threshold, Hysteresis, and S-Shaped Characteristics

Threshold characteristics have been observed in the sidegating effect of GaAs devices, as described in Chapter 3 and in many published experimental studies on the subject. In some cases abrupt changes at a threshold value of the sidegate voltage were seen in both the drain current of a device and sidegate current. Hysteresis and S-shaped characteristics have also been observed. These phenomena will be simulated using the lateral structure in Figure 5.9(b), and the underlying mechanisms will be discussed based on the double-injection process in the presence of a metal contact.

A. Results of Simulation Using the Lateral Structure

The lateral structure in Figure 5.9(b) is more realistic in that both the ungated device and the sidegate are on the top surface of a semi-insulating substrate which is assumed to be 100 μm thick. The dimensions and doping levels of the ungated device are the same as those of the vertical structure in Figure 5.9(a). The width of the metal contact is 4 μm and placed 3 μm from the edge of the drain of the ungated device. The distance from the ungated device to the sidegate is L_{SG} = 20 μm. The substrate is, as in the vertical structure, assumed to be LEC type of substrate, containing shallow-acceptors of concentration $N_A = 5.0\times10^{15}\,\text{cm}^{-3}$ and the deep-donor/electron-trap EL2 of concentration $N_t = 5.0\times10^{16}\,\text{cm}^{-3}$.

In real GaAs substrates, there exist deep-level centers other than EL2, such as HL2 and HL3 which are hole-traps, as published experimental results have shown. Recombinations of electrons and holes through recombination centers in substrates also take place in reality. These factors theoretically can be included in simulations. For simulations using the lateral structure to be discussed below, only one deep-level center in addition to EL2 is assumed in the substrate. This additional deep-level center is assumed to be a deep-donor and hole-trap ($\sigma_p \gg \sigma_n$). Also included in the simulations is the process of recombination of electrons and holes through a neutral recombination level located at the intrinsic Fermi level E_i,. However, due to the lack or incompleteness of experimentally verified data, parameter values such as the energy level and capture cross-sections of the additional deep-donor/hole-trap and carrier lifetimes associated with the neutral recombination level are arbitrarily chosen. As long as the energy level of this additional deep-level is below that of EL2 and its concentration much lower, most of these deep-donor/hole-trap centers are occupied in equilibrium and the compensation of shallow acceptors by EL2 is not compromised. The introduction of the additional deep-donor/hole-trap level and the recombination through a neutral level does have an effect on the magnitude of the substrate leakage current. The energy level of the deep-donor/hole-trap and the lifetimes of the recombination process are adjusted to achieve appropriate current levels. However, the basic mechanisms responsible for the high substrate leakage current and the drain current reduction are still the same as those discussed in explaining the results of the simulation using the vertical structure. For the results from the simulations using the lateral structure to be described below, the energy level of the additional deep-donor/hole-trap is set at $E_c - E_t = 0.774\,\mathrm{eV}$ which is below that of EL2, and its concentration is $5.0\times10^{15}\mathrm{cm}^{-3}$. The electron and hole lifetimes associated with the recombination through the neutral level are chosen to be $\tau_n = \tau_p = 10^{-8}$'s.

The drain current I_D, sidegate current I_{SG}, and the current through the metal contact $I_{SC,}$ are all simulated as functions of the negative voltage V_{SG} at the sidegate with the drain biased at $V_D = 0.1$ V (see Figure 5.13). The simulated drain current (Figure 5.13(a)) first decreases slowly as the sidegate voltage increases from zero and then decreases at higher rates as the sidegate voltage becomes higher. The drain current experimentally measured from a test structure is also shown in Figure 5.13(a) for comparison. The drain current reduction characteristics given by the simulation are in excellent agreement with the measurement results.

The simulated sidegate current I_{SG} shown in Figure 5.13(b) is seen to rise rapidly with the increasing sidegate voltage and reaches high levels. The simulated current through the metal contact I_{SC}, also shown in Figure 5.13(b), is also seen to increase rapidly and merges with the simulated sidegate current, demonstrating that the high leakage in the

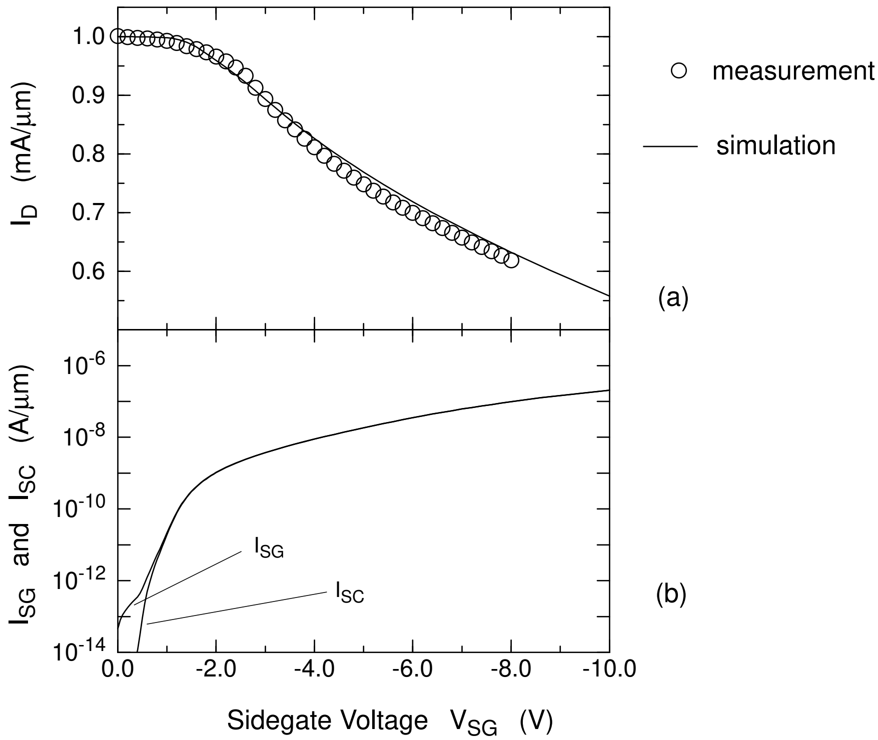


Figure 5.13 Results of simulation using the lateral structure in Figure 5.9(b)

substrate in fact comes from the metal contact. And this is qualitatively the phenomenon observed in experiments.

No experimentally measured sidegate current is shown in Figure 5.13(b). Due to the asymmetry in sizes between the metal contact (2μ'm × 4μ'm) and sidegate electrode (20μ'm × 35μ'm) in the test structures used in experiments, it is unrealistic to convert the measured sidegate current to the unit of A/μm and make a quantitative comparison to the simulated $I_{SG.}$ What is important here is that the simulation demonstrates the basic trend of the substrate leakage current that has been observed in experiment. The sidegating and leakage current mechanisms can be understood in terms of the double-injection process and the creation of negative space-charge due to the electron-trapping effect by EL2, as discussed in the explanation of the results of the simulation using the vertical structure.

B. Threshold Characteristics

As described in Chapter 3, abrupt changes in drain current and sidegate currents at a threshold value of sidegate voltage are observed in experiments only when the drain bias voltage is relatively high; no such threshold characteristics are seen at low drain bias voltages. Though not seen in the drain and sidegate currents simulated at $V_D = 0.1$V, the threshold behavior can be reproduced by simulations at higher drain voltages, which will be described and analyzed below.

Figure 5.14 shows the characteristics of the drain and sidegate currents as functions of the sidegate voltage simulated at three different drain bias voltages: $V_D = 0.1$V, 2.0V, and 5.0V. Threshold characteristics are seen in both the drain and sidegate currents for each of the two higher drain bias voltages. And the threshold voltage is 2.0V for $V_D = 2.0$V and 3.0V for $V_D = 5.0$V. For sidegate voltages smaller than the threshold values, there is no significant reduction in the drain currents (Figure 5.14(a)) and the sidegate currents are low (Figure 5.14(b)) at either one of these two higher drain voltages. Only when the sidegate voltage reaches the threshold value at which the drain current abruptly drops to a lower value and the sidegate current jumps to a much higher level, does the drain current start to decrease with the increasing sidegate voltage and the sidegate current begins to increase rapidly. The simulated metal contact current (Figure 5.14(c)) also shows that only when the sidegate voltage reaches and goes beyond the threshold value does high current flows through the metal contact. It is also important to note that the sidegate threshold is greater for the higher drain bias voltage. All these are qualitatively the same characteristics of the drain and sidegate currents observed in experiments (see Figure 4.11).

Since the occurrence of the high leakage current has been attributed to the double-injection, the low sidegate current indicates the double-injection process is not initiated for low sidegate voltages smaller than the sidegate threshold. And since the value of the sidegate threshold is greater for a higher drain bias voltage, it is natural to link the positive drain bias to some effect that hampers the initiation of the double-injection process.

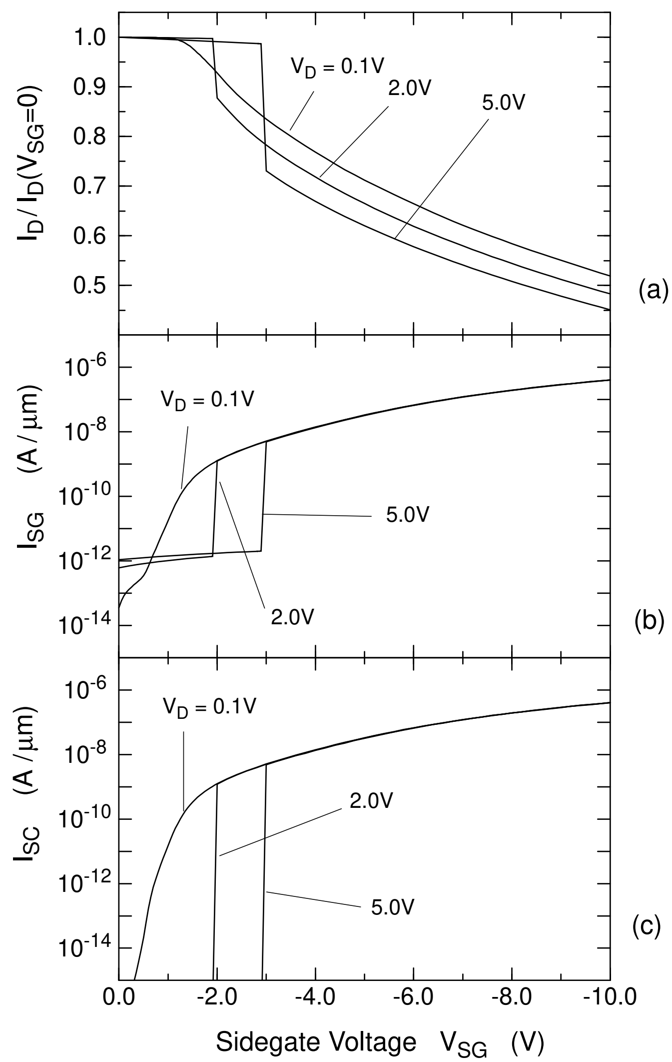


Figure 5.14 Simulated threshold characteristics.

While the negative voltage at the sidegate induces double-injection, the effect of the drain bias is the opposite; the positive voltage at the drain pulls up the potential in the region under and near the metal contact, making it more difficult for holes to be injected from the metal contact and be transported into the substrate.

Figure 5.15(a) shows the valence band edge profiles at zero sidegate voltage ($V_{SG} = 0$) in the vertical direction right under the metal contact (up to 2.0 μm from the top surface) for three the drain bias voltages. For the two higher drain voltages $V_D = 2.0$V and 5.0V, the band edges bend more upward in the region right below the metal contact compared to that for $V_D = 0.1$ V, creating much stronger retarding fields to the hole-injection from the metal contact. The more severe upward bending of the band edges is directly caused by the positive voltages at the drain of the ungated device. At $V_{SG} = 1.0$V, the band edge profiles for $V_D = 2.0$V and 5.0V still exhibit the shapes that impede hole-injection, shown in Figure 5.15(b). The relatively high drain voltages of $V_D = 2.0$V and 5.0V are still effective in blocking the hole-injection from the metal contact and therefore the double-injection process cannot be initiated.

Only when the negative sidegate voltage is large enough to overcome the hampering effect of the positive drain bias can holes be injected and transported into the substrate to trigger the double-injection. Once the double-injection process is started, negative space-charge is created under the channel-substrate interface and the metal contact due to hole-depletion and increase of electron concentration. This leads to a large proportion of the applied sidegate voltage being dropped across the region of negative space-charge including the region under the metal-substrate interface. This change in potential distribution in the substrate enhances the hole-injection from the metal contact and therefore drive the double-injection to a higher level. The process is self-sustaining and goes on until a steady state is reached in which most of the applied sidegate voltage is across the region of negative space-charge under the channel-substrate and metal-substrate interfaces and the potential over the rest of the substrate is relatively flat. The redistribution of potential in the substrate at the on-set of the double-injection process accounts for the abrupt changes at a sidegate threshold in both the drain and sidegate currents.

Figure 5.15(c) shows the band edge profiles under the metal contact at V_{SG} = 2.0V, at which the effect of the drain voltage of V_D = 2.0V is overcome, but that of V_D = 5.0V is still not. The band edge for V_D = 2.0V now bends downward the metal-substrate interface, indicating the field in the region is in the direction that aids transporting injected holes into the substrate. Under these conditions, the double-injection process is on for the case of V_D = 2.0V, and the drain current is reduced and the substrate leakage current is high, as can be seen in Figure 5.14. At V_{SG} = 3.0V, the band edge for V_{SG} = 5.0V now bends downward as shown in Figure 5.15(d), indicating the sidegate voltage is high enough that the effect of the drain voltage of V_{SG} = 5.0V is also overcome. By examining the band edge profiles in Figure 5.15 and the drain and substrate current characteristics in Figure 5.14, it is clear that the threshold behavior results from the combined effects of drain bias voltage and sidegate voltage.

C. Hysteresis and S-shaped Characteristics

At relatively high drain bias voltages, hysteresis and S-shaped characteristics have also been experimentally observed in both the drain and sidegate currents. The hysteresis is observed when the sidegate voltage was first increased from zero beyond the threshold and then was decreased towards zero. The S-shaped feature was observed when a current source was applied to the sidegate.

The hysteresis characteristics can be reproduced qualitatively by simulations. Figure 5.16 shows the drain and sidegate currents simulated with both the increasing and decreasing sidegate voltages, with the drain biased at V_D = 5.0 V. It can be seen that for sidegate voltage values smaller than the sidegate threshold, the drain and sidegate currents simulated with the decreasing sidegate voltage do not follow the same paths as those simulated with the increasing voltage. This hysteresis behavior can be understood by examining the potential distribution in the substrate. For the sidegate voltage decreasing from a value greater than the threshold, the substrate starts with the potential distribution that most of the applied sidegate voltage is dropped over the region near the channel-substrate

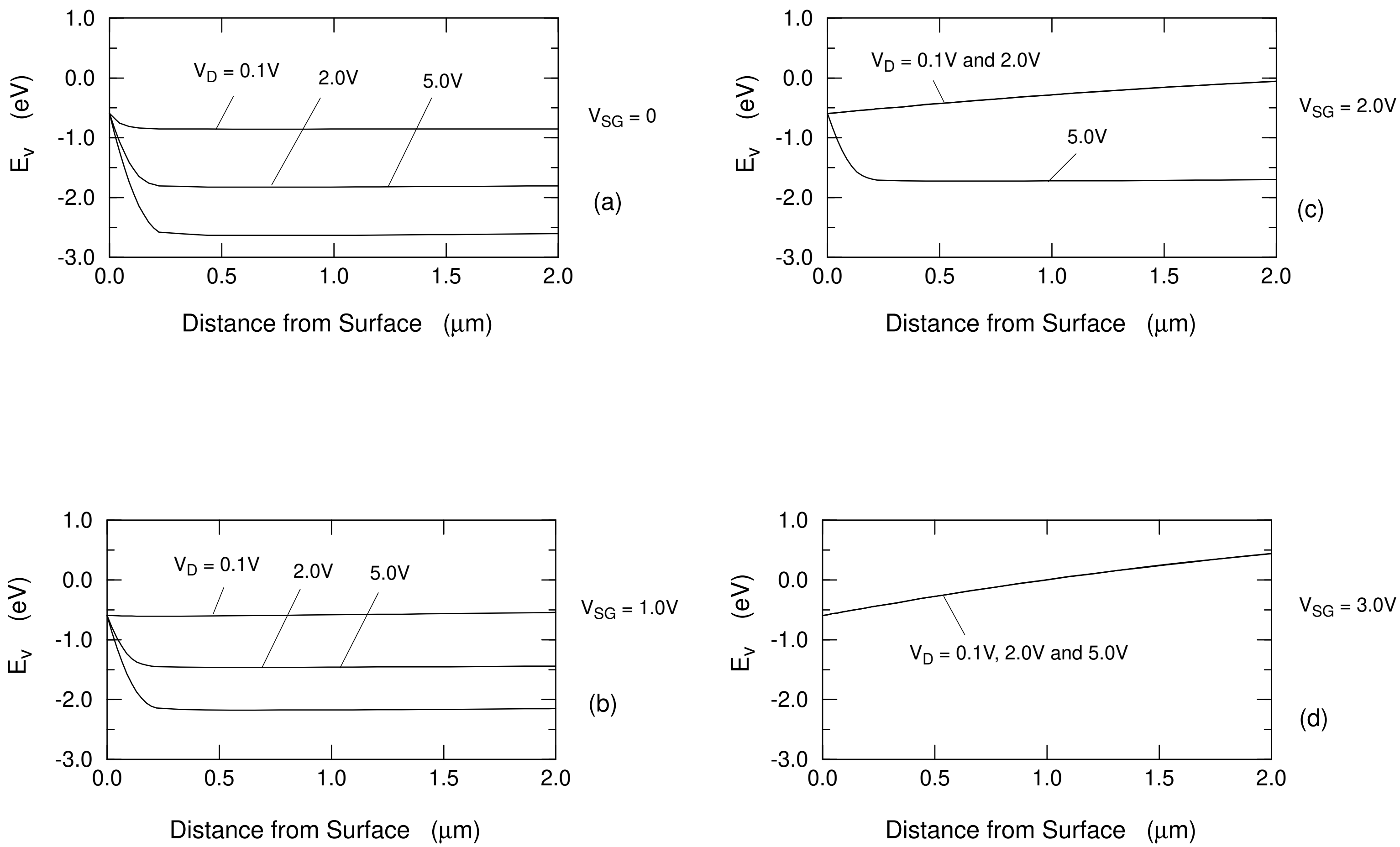


Figure 5.15 Valence band edge profiles under the metal contact.

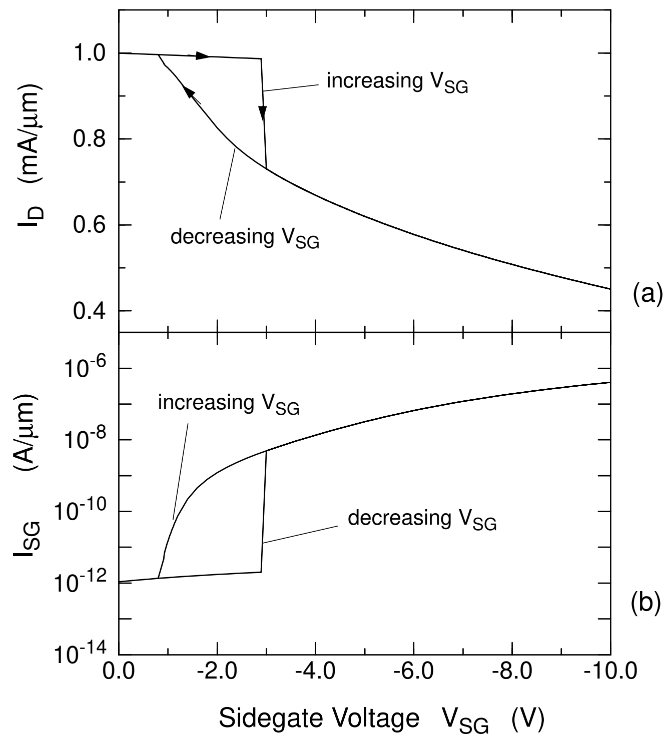


Figure 5.16 Hysteresis characteristics from simulation

and metal-substrate interfaces. This basic feature of potential distribution in the substrate is maintained as the sidegate voltage is lowered to some values smaller than the threshold. This can be seen in Figure 5.17 which compares two profiles of the valence band edge in vertical dimension under the metal contact at $V_{SG} = 2.0$ V. The band edge for the increasing sidegate voltage bends upward, and therefore few holes can be injected into the substrate to start the double-injection process. But at the same V_{SG}, the band edge for the decreasing sidegate voltage bends downward, indicating that the double-injection process is still on, even though the sidegate voltage is at a value smaller than the threshold. The hysteresis behavior results from the fact that once the potential distribution is formed in the substrate that most of the potential variation is confined to the region near the channel-substrate and metal-substrate interfaces, it is not easily altered by the positive drain voltage until the negative sidegate voltage is decreased to a value much lower than

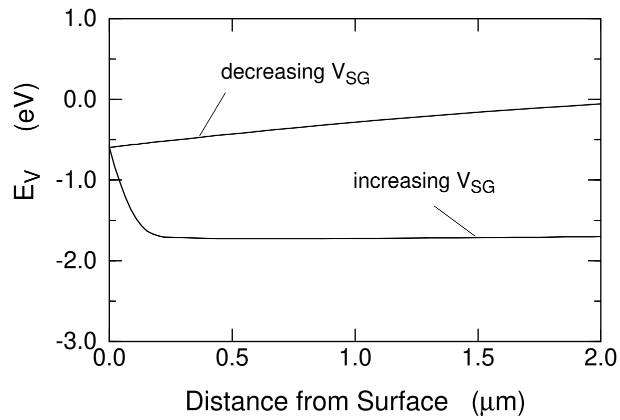


Figure 5.17 Valence band edge profiles for increasing and decreasing sidegate volt-

the threshold.

The S-shaped characteristics observed in current-controlled measurements at relatively high drain voltages have the same origin as the hysteresis behavior. As the negative current (flowing out the electrode) applied at the sidegate voltage rises from zero, the potential at the sidegate increases to accommodate the increasing current. At low current levels the potential in the substrate is distributed over the whole region between the device and the sidegate because the positive drain bias prevents the double-injection from taking place. When the applied current and the corresponding sidegate voltage at the sidegate are strong enough that the effect of the drain bias is overcome, the double-injection process is started and potential distribution in the substrate is changed to that most of the potential variation is confined to the region near the channel-substrate and metal-substrate interfaces. Under these conditions, the voltage at the sidegate needed to maintain the same current level and the double-injection process is lowered and a voltage backlash results.

5.2.4 Summary

The simulations have shown that in the presence of the hole-injecting effect of a metal contact, the sidegating effect is aggravated and leakage current in the substrate is orders of magnitude higher, as compared to the case where there is no metal contact (see section 5.1). The degradation of the drain current of a device is again caused by the creation of negative space-charge under the channel-substrate interface. The creation of net negative space-charge again is a direct consequence of more electrons being captured and trapped by the electron-trap, which is caused by the double-injection process induced by hole-injection at the metal contact under the influence of the negative sidegate voltage. Because of the double-injection, both electron and hole concentrations in the substrate are increased, and electron occupancy of the deep-donor/electron-trap EL2 is essentially not changed and charge-neutrality is maintained in the bulk. However, in the region below the channel-substrate interface, holes are depleted while the electron concentration in the same region is increased due to the double-injection. This causes more electrons being captured and trapped due to the strong dependence on electron concentration of the steady state electron-occupancy function of the electron-trap. The trapping of electrons lowers the density of positively charged deep-donor/electron-trap centers, resulting in a net negative space-charge below the channel-substrate interface. The increased electron and hole concentrations in the substrate, caused by the double-injection process, also result in high substrate leakage current.

The drain current degradation of a device and the high substrate leakage current depend on the occurrence of the double-injection in this case. Therefore the threshold behavior in the sidegating and leakage current characteristics are explained in terms of the double-injection being “turned on” at a threshold sidegate voltage at which the effects that hamper the hole-injection at the metal contact, such as the positive bias voltage at the drain, are overcome. The threshold and S-shaped characteristics are also explained as resulting from the transition of the current conduction in the substrate from the single-carrier electron transport process in the n-i-n structure formed by the device and sidegate to the double-injection process in the m-i-n structure formed by the metal contact and the sidegate, or vice versa.

5.3 De-Trapping of Holes and Sidegating Effects

In many early studies of the sidegating effects, the decrease of device drain currents was found to start at zero or very low sidegate voltages, while no high substrate leakage current was reported [21] [22]. Sidegating characteristics of this type were usually observed when there were large number of hole-traps around the channel-substrate of the interface [21] [22]. Also many of the devices used in early studies of the sidegating effects were built on substrates doped with Cr, which is a deep-level hole-trap in GaAs [17] [19] [21] [22] [24]. The purpose of doping substrates with Cr, which is also a deep-acceptor in GaAs, is to compensate shallow-donors unintentionally incorporated into GaAs material during crystal growth [62]. Substrates from this kind of GaAs material are referred to as Cr-doped. In this section, the sidegating effect of devices built on substrates of Cr-doped type is first simulated and then analyzed in terms of trapping, or more accurately de-trapping, of holes.

5.3.1 Simulation Using a Vertical Structure

A. The Structure and Conditions for Simulations

The vertical structure used is basically the same as that shown in Figure 5.1(a), which has been used for simulating the electron-trap related sidegating effect. The distance from the channel-substrate interface to the sidegate is $L_{SG} = 20\ \mu\text{m}$. For the simulations to be discussed in this section, the channel-depth of the ungated device is 0.3 μm. The channel doping is set at $5.0\times10^{16}\text{cm}^{-3}$. The source and drain contact regions of the device and the sidegate are all doped to $1.0\times10^{17}\text{cm}^{-3}$.

The substrate is assumed to contain shallow-donors of concentration $N_A = 5.0\times10^{15}\text{cm}^{-3}$. The semi-insulating property of the substrate is achieved by compensation of the shallow-donors by deep-level acceptors of concentration $2.0\times10^{16}\text{cm}^{-3}$. The energy level and carrier capture cross-sections of Cr are used as the parameters of the deep-level acceptor for simulations.

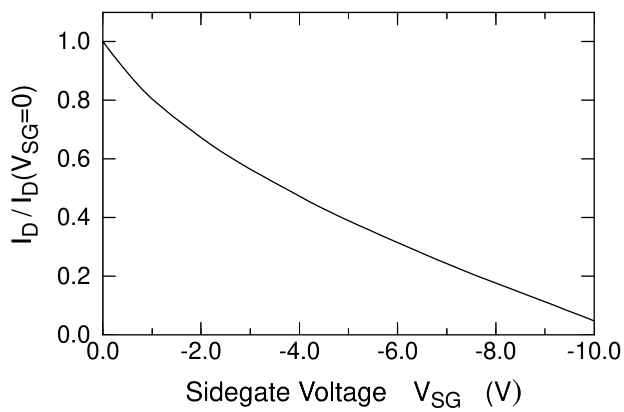


Figure 5.18 Results of simulation using the vertical structure.

There are multiple levels associated with Cr in GaAs [24]. The energy level of interest is associated with the Cr^{2+}, which acts as an acceptor and is responsible for compensation. According to G. M. Martin *et. al.*, the energy level can be expressed as [69]

$$E_t(\mathrm{Cr}) - E_v = 0.81 - 3.0\times10^{-4}\,T^2/(T+204)\ \ \mathrm{eV} \tag{5.8}$$

and the electron and hole capture cross-sections are [98]

$$\sigma_n(\mathrm{Cr}) = 1.3\times10^{-17}e^{-0.117\mathrm{eV}/kT}\ \mathrm{cm}^2 \tag{5.9}$$

$$\sigma_p(\mathrm{Cr}) = 1.0\times10^{-16}e^{-0.020\,\mathrm{eV}/kT}\,\mathrm{cm}^2 \tag{5.10}$$

At $T = 300$ K, the energy level is $E_t - E_v = 0.76$ eV. The electron and hole capture cross-sections are $\sigma_n = 1.4\times10^{-19}\mathrm{cm}^2$ and $\sigma_p = 4.6\times10^{-17}\mathrm{cm}^2$, respectively.

The fact that the hole capture cross-section is much greater than the electron capture cross-section ($\sigma_p \gg \sigma_n$) makes Cr a hole-trap. Its implication concerning sidegating effect will be discussed when simulation results are analyzed.

B. Simulation Results

To simulate the sidegating effects, the source of the ungated device is at the ground potential ($V_S = 0$), and the drain is biased at $V_D = 0.1$ V. A variable negative voltage V_{SG} is applied to the sidegate. The drain current I_D of the ungated device calculated as a function of V_{SG} is shown in Figure 5.18.

The drain current I_D is seen to be modulated by the negative sidegate bias starting at the zero sidegate voltage. The drain current decreases rapidly with the increasing sidegating voltage over the whole voltage range of the simulation. The simulated current does not show any threshold characteristics, and this is in contrast to the drain current characteristics simulated for a device on an undoped LEC type substrate in which the major deep-level center for compensation is an electron-trap (see Figure 5.3(a)).

The simulated sidegate current I_{SG} (not shown), which is in fact the leakage current in the substrate, is very low; the current is three orders of magnitude lower compared to the simulated leakage current in a undoped LEC substrate (see Figure 5.3(b)).

5.3.2 Analysis of Simulation Results

A. Distributions of Potential, Field, Charge, and Electron Concentration

Figure 5.19 shows the various simulation-generated profiles in the vertical dimension along the symmetry line of the ungated device for a length of up to 2 μm from the top surface of the channel. It can be seen from distributions of the conduction band edge at different sidegate voltages (see Figure 5.19(a)) that all of the voltage applied at the sidegate drops across a region around the n-i junction at the channel-substrate interface. In the bulk of the substrate the band edge maintains a zero or near-zero gradient as the sidegate voltage increases, in contrast to the case of an undoped LEC substrate in which the major deep-level center is an electron-trap (see Figure 5.4). This means that non-zero electric fields are only confined within the region under the channel-substrate interface across which the applied voltage is dropped, as seen in Figure 5.19(b). Correspondingly, there is a space-charge in the non-zero-field region, as shown in Figure 5.19(c). The negative space-charge on the substrate side of the channel-substrate interface is balanced by the positive charge on the channel side which results from depletion of electrons. As the

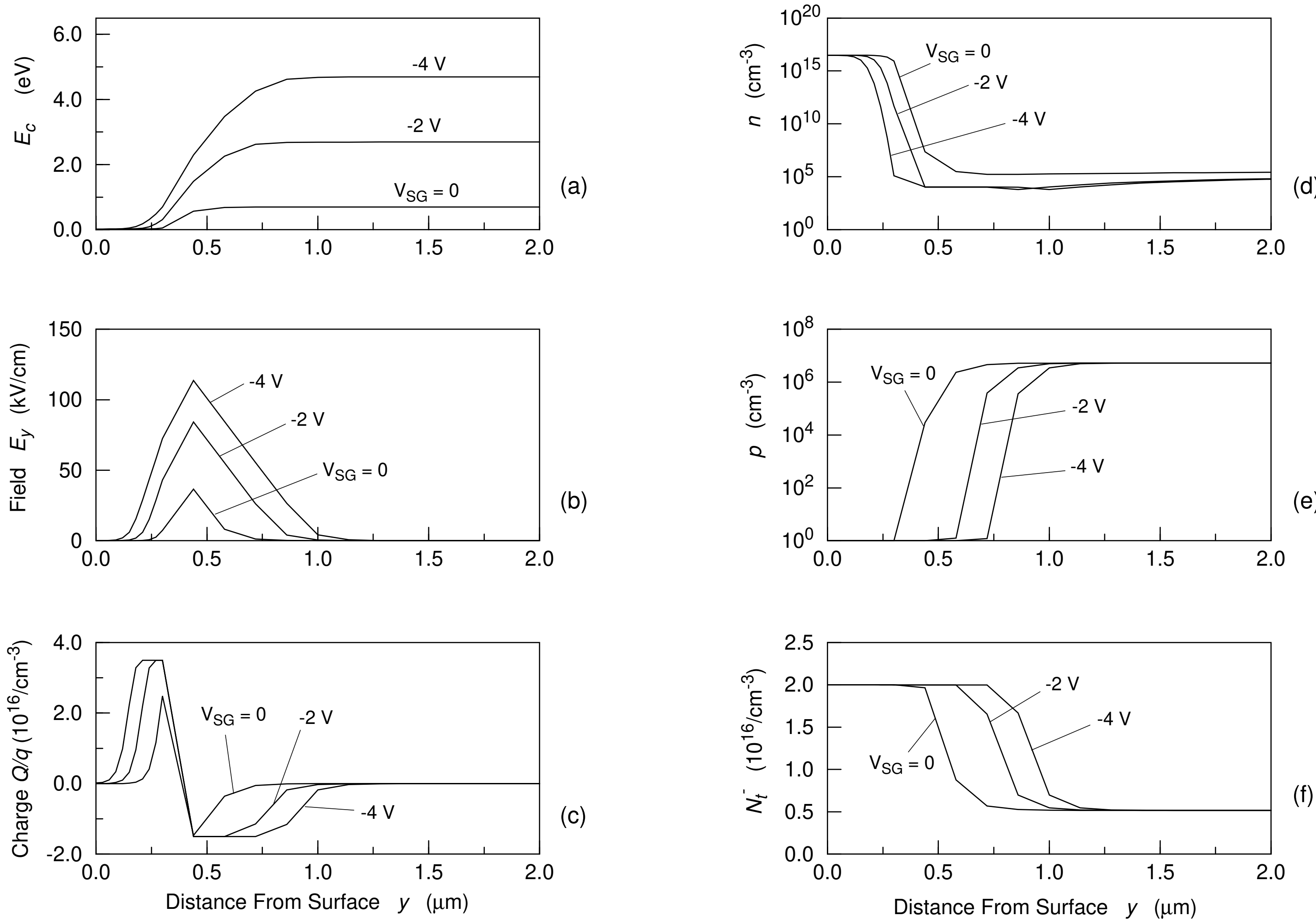


Figure 5.19 Profiles given by the simulation using the veritcal structure.

sidegate voltage increases the negative space-charge region in the substrate expands, causing the region electron-depletion to extend further into the channel and resulting in shallower electron concentration profiles, as illustrated in Figure 5.19(d). Since the expansion of the negative space-charge region starts as the sidegate voltage increases from zero, the drain current reduction begins at $V_{SG} = 0$; no threshold characteristics are displayed. This is in contrast to the behavior of the simulated drain current of the device on a substrate in which the major deep-level center is an electron-trap, as in an undoped LEC type substrate. The important question need to be answered is how the negative space-charge is created.

B. Hole-Emission and Negative Space-charge

As seen the in Figure 5.19(c), charge neutrality is maintained in the bulk of the substrate, which requires

$$p + N_D = n + N_t^- \tag{5.11}$$

where N_t^- is the concentration of the deep-level/hole-trap center in GaAs that are occupied by electrons (or empty of holes). The existence of the negative space-charge in the region below the channel-substrate interface means that the charge-neutrality expressed by Equation (5.11) is disturbed because of the applied sidegate voltage.

Upon applying the negative voltage to the sidegate holes in the substrate are depleted away from the channel-substrate interface (see Figure 5.19(e)). The region where holes are depleted is also the region where negative space-charge is created. However, because of the low equilibrium hole concentration in the substrate ($p < 10^7 \mathrm{cm}^{-3}$), the hole-depletion by itself cannot account for the creation of the amount of negative space-charge which is on the order of $10^{16} \mathrm{cm}^{-3}$ after being normalized to the electron charge q. In fact, since both electron and hole concentrations in the substrate are very low compared to that of the shallow-donor (i.e. $n, p \ll N_D$), n and p can be ignored and the charge-neutrality condition of Equation (5.11) can be approximated as $N_D = N_t^-$.

The concentration of the negatively charged deep-acceptor can be expressed as $N_t^- = N_t f_t$, where f_t is the electron-occupation function of the deep-level center defined by Equation (5.6) as $f_t = 1/[1 + (c_n n_t + c_p p) / (c_n n + c_p p_t)]$. Since the deep-acceptor is also a hole-trap ($\sigma_p \gg \sigma_n$), the electron-occupation function can be approximated by $f_t \approx 1/(1 + p/p_t)$ as long as $n \ll c_p p_t / c_n \approx 10^9 \mathrm{cm}^{-3}$, and the concentration of the negatively charged deep-acceptors as $N_t^- \approx N_t / (1 + p/p_t)$. Since the concentration of the negatively charged deep-acceptors N_t^- in steady state mainly depends on the hole concentration, the charge neutrality condition in the substrate can be easily disturbed when the hole concentration changes, while changes in the electron concentration have little effect. Depletion of holes in the region below the channel-substrate interface increases the concentration of the negatively charged deep-acceptor to $N_t^- \approx N_t$, because the lowered hole concentration leads to $f_t \approx 1$. The charge-neutrality condition in the region is disturbed because there is now $N_t^- > N_A$, and negative space-charge is created. The distributions of N_t^- calculated using the simulation-generated electron and hole concentrations show that N_t^- is indeed increased in the region below the channel-substrate interface by amounts that can account for the negative-space charge in the region, as seen in Figure 5.19(f).

From a physical point of view, the fact that the hole capture cross-section of the deep-acceptor/hole-trap is much greater ($\sigma_p \gg \sigma_n$) means that it has a more active interaction with holes than with electrons. As long as the electron concentration is not high ($n \ll c_p p_t / c_n \approx 10^9 \mathrm{cm}^{-3}$), the probability of a deep-acceptor/hole-trap center being occupied by an electron or by a hole is much more strongly influenced by the hole concentration than by the electron concentration. The depletion of holes in the substrate with the application of a sidegate voltage disturbs the previously established balance between the capture and emission of holes by the deep-acceptor/hole-trap centers. Holes previously trapped are emitted from the deep-level centers to the valence band and are also depleted. This process of de-trapping of holes continues until a new balance between the capture and emission of holes is established in steady state. The result is the increase of the con-

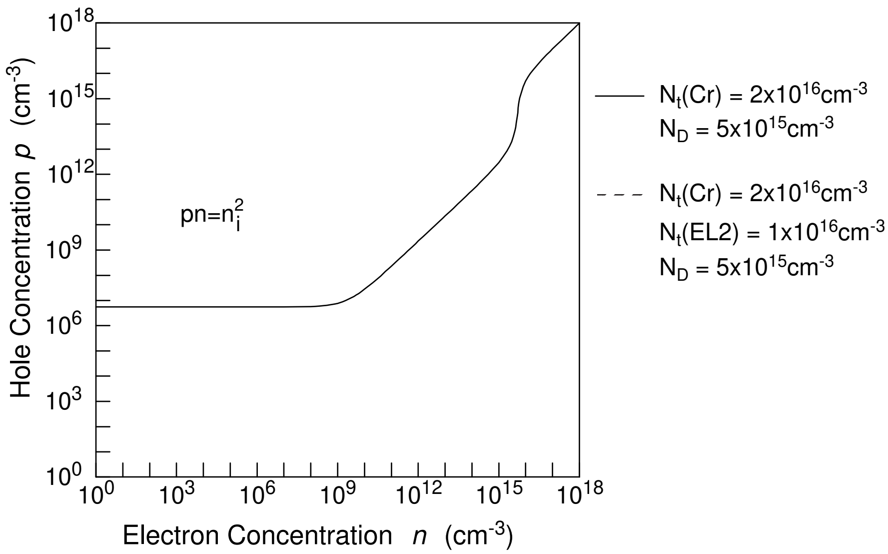


Figure 5.20 Charge-neutrality curve.

centration N_t^- of the negatively charged deep-acceptor/hole-trap centers empty of holes (or occupied by electrons), leading to the creation of negative space-charge.

The above analysis relating the de-trapping of holes to the creation of negative space-charge can be visualized using the charge-neutrality curve (the solid curve) shown in Figure 5.6, which is obtained by plotting n and p values that satisfies Equation (5.11). Below and to the right of the charge-neutrality curve is the region of the n and p values that result in net negative charge; above and to the left of the curve are the n and p values that lead to net positive charge. The point of intersection of the charge-neutrality curve with the dotted line for n and p values that satisfy $pn=n_i^2$ represents the equilibrium state, which is on the horizontal section of the charge-neutrality curve (i.e. the section in parallel with the n-axis). When a negative sidegate voltage is applied, the depletion of holes in the substrate pulls the n and p values away from the charge-neutrality curve and into the ranges that result in net negative space-charge. The horizontal section of the charge-neutrality curve reflects the sensitivity of charge to changes in the hole concentration when the major deep-level center for compensation in the substrate is a hole-trap.

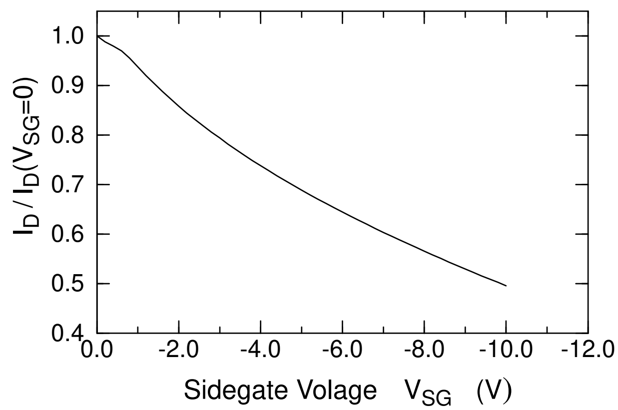


Figure 5.21 Results of simulation using the lateral structure.

5.3.3 Simulation Using the Lateral Structure

A lateral structure similar to that in Figure 5.1(b), in which both the ungated device and the sidegate are on the top surface of the substrate, is also used for simulations. The dimensions and doping levels of the ungated device in this lateral structure are all the same as those in the vertical structure. The substrate, chosen to be 100 μm thick, contains a shallow-donor of concentration $5.0\times10^{16}\text{cm}^{-3}$ and the deep-acceptor/hole-trap of concentration $2.0\times10^{16}\text{cm}^{-3}$, which are also the same as those in the vertical structure. Since EL2 always exists in bulk grown GaAs as a native defect, the substrate in this case is also assumed to have deep-donor/electron-trap centers of concentration $1.0\times10^{16}\text{cm}^{-3}$ in it. The carrier capture cross-sections of EL2 are assigned to the deep-donor/electron-trap. And the energy level of this deep-donor/electron-trap is also assumed to be at that of EL2's (Equations (5.1)), which at $T = 300$ K is slightly below that of Cr's (Equation (5.8)) in the GaAs energy bandgap.

With the source of the ungated device grounded ($V_S = 0$) and the drain biased at $V_D = 0.1$ V, the drain current I_D is calculated as a function of the negative voltage V_{SG} applied to the sidegate. The simulation results are shown in the Figure 5.21. The drain current is again seen to decrease rapidly with the increasing sidegate voltage. The degradation

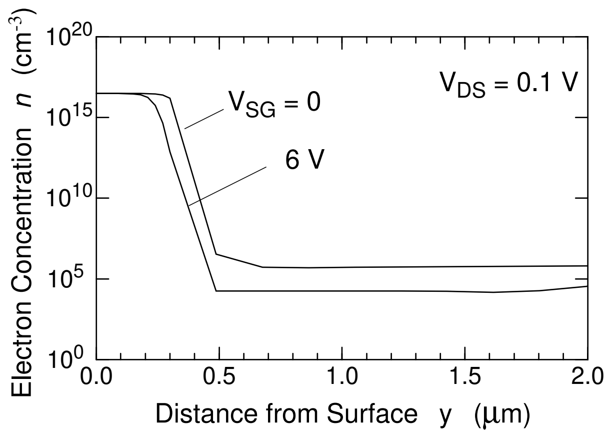


Figure 5.22 Electron concentration from the simulation of the lateral structure.

of the drain current is a direct consequence of creation of negative space-charge under the channel-substrate interface, which causes electrons in channel near the interface to be depleted. The depletion of electrons in the channel is shown in Figure 5.22.

Because the substrate contains deep-donors in addition to deep-acceptors, the decrease of the simulated drain current in the lateral structure is not as fast as that in the vertical structure in which no deep-donor is assumed to exist in the substrate. The charge-neutrality curve calculated where the shallow-donor ($5.0\times10^{15}\text{cm}^{-3}$), deep-acceptor ($2.0\times10^{16}\text{cm}^{-3}$), and deep-donor ($1.0\times10^{16}\text{cm}^{-3}$) are all included is shown in Figure 5.6 as the dashed curve. The charge-neutrality curve in this case deviates from that when the deep-donor is not taking into account (the solid curve) for electron concentrations $n \le 10^{7}\text{cm}^{-3}$. However, the shape of the charge neutrality curve still reveals that hole-depletion upon applying a negative voltage to the sidegate lead to the conditions that negative space-charge is created in the region below the channel-substrate interface.

5.3.4 Summary

Sidegating characteristics are simulated and analyzed for devices built on substrates in which the major deep-level center for compensation is a hole-trap. The simulation results agree qualitatively with the published experimental results of some early studies on MESFET sidegating effect in that the reduction of the drain current starts at zero sidegate voltage and the drain current decreases rapidly [21], [22]. The degradation of the drain current is again attributed to the creation of negative space-charge below the channel-substrate interface. In this case, negative space-charge is created because of the de-trapping of holes from the deep-acceptor/hole-trap centers in the substrate. The de-trapping (emission from the hole-trap) of holes is caused by depletion of holes when the negative sidegate voltage is applied, because the number of holes being trapped by the hole-trap in steady state strongly depends on the hole concentration. The density of negatively charged deep-acceptor/hole-trap centers is increased because of the de-trapping of holes, and therefore net negative space-charge is created. Based on the simulations and analyses in this section, it can be concluded that devices built on substrates with large amount of the hole-traps are more susceptible to the sidegating effect, even though the substrate leakage current is very small; the leakage current is essentially the junction leakage of the n-i junction at the channel-substrate interface when impact ionization and tunneling are not significant.

5.4 Summary of Analyses and Simulations

Simulations and analyses in this chapter have given three types sidegating mechanisms: (1) negative-differential-mobility coupled with injection and trapping of electrons; (2) double-injection and electron-trapping; and (3) depletion and de-trapping of holes. The first two types of sidegating effects occur in the type of GaAs material in which the major deep-level center form compensation is an electron-trap, such as undoped LEC GaAs substrates. The third type is the dominant mechanism in the substrate in which the major deep-level center is a hole-trap.

The simulations have shown that the degradation of the drain current of a device under the influence of a negative sidegate voltage is a direct consequence of the creation of negative space-charge in the region under the channel-substrate interface. Understanding the mechanisms that negative space-charge is created is the key to understanding the resulted sidegating and leakage current characteristics. Negative space-charge results from the changes of the densities of charged deep-level traps due to the trapping of electrons or de-trapping of holes, which in turn are caused by the changes in the respective carrier concentrations. Sidegating characteristics are influenced by the carrier transport properties such as negative-differential mobility of electrons, hole depletion, and double-injection which are important factors affecting how negative space-charge is created.

Simulations have also shown that a high leakage current is much more likely to occur due to the double-injection process when a source of hole-injection such as a metal contact on the substrate is present. This is in agreement with the experimental results described in Chapter 4 and some published results of simulations by others [48]-[50]. However, the high leakage current itself is not the cause of the aggravated drain current degradation as suggested by early studies on MESFET sidegating effect [25] [39]; it is only a manifestation of the double-injection process. As the simulations for the cases without the metal contact have shown, the mechanisms that are responsible for serious drain current degradation do not always also result in high substrate leakage current. Sidegating effect and substrate leakage are two aspects of the problem concerning isolation among devices built on semi-insulating substrates. A semi-insulating substrate may provide good isolation between two n-type devices as far as the leakage current between them is concerned, it does not necessarily prevent them from interacting with each other. Double-injection processes may be induced under certain bias conditions because of the existence of a hole-injecting source such as a metal contact, which not only aggravates interaction among devices, but also causes high leakage current in the substrate. These issues must be taken into account in designing GaAs integrated circuits

Bibliography

[1] J. P. Klein, ‘‘Chapter 1, History and Perspectives,’’ in *Applications of GaAs MESFETs*, Eds. R. Soares, J. Graffeuil, and J. Obrégon, Artech House Inc., 1983 (TCH.12).

[2] O. Wing, *Gallium Arsenide Digital Circuits,* Kluwer Academic Publishers, 1990. (TCH.13)

[3] S. I. Long and S. E. Butner, *Gallium Arsenide Digital Integrated Circuit Design*, McGraw-Hill, 1990. (TCH.14)

[4] S. J. Harrold, *An Introduction to GaAs IC Design,* Prentice Hall International, 1993. (TCH.15)

[5] P. N. Butcher and W. Fawcett, ‘‘Calculation of the Velocity-Field Characteristic for Gallium Arsenide,’’ *Phys. Lett.,* vol. 21, no. 5, 15 June, 1966.

[6] J. G. Ruch and G. S. Kino, ‘‘Measurement of the Velocity-Field Characteristics of Gallium Arsenide,’’ *Appl. Phys. Lett,* vol. 10, no. 2, pp 40-42, 15 January, 1967.

[7] J. G. Ruch and G. S. Kino, ‘‘Transport Properties of GaAs,’’ *Phys. Rev.,* vol. 174, no. 3, pp. 921-931, 15 October, 1968.

[8] R. C. Eden, B. M. Welch, R. Zucca, and S. I. Long, ‘‘The Prospects for Ultra-high-Speed VLSI GaAs Digital Logic,’’ *IEEE Trans. Electron Devices,* vol. ED-26, no. 4, pp. 299-317, April 1979. (TCH.5)

[9] P. H. Saul, ‘‘Chapter 5, Technology comparison: Galolium Arsenide vs. Silicon,’’

in *GaAs Technology and Its Impaect On Cirduits and Systems,* Eds. D. Haigh and J. Everard, Peter Peregrinus Ltd., (TCH.16)

[10] S. J. Lee, C. P. Lee, E. Shen, and G. R. Kaelin, ''Modeling of Backgating Effects on GaAs Digital Integrated Circuits,'' *IEEE J. Solid-State Circuits,* vlol. SC-19, no. 2, pp. 245-249, April 1984. (SG.e5)

[11] C. P. Lee, R. Vahrenkamp, S. J. Lee, Y. D. Shen, and B. M. Welch, "Effect of Substrate Conduction and Backgating On the Performance of GaAs Integrated Circuits," In *GaAs IC Syposium*, pp. 169-172, 1982. (SG.e2)

[12] T. T. Itoh and H. Yanai, "Stability of Performance and Interfacial Problems in GaAs MESFET's," *IEEE Trans. Electron Devices,* vol. ED-27, no. 6, pp. 1037-1045, June 1980. (SG.e7)

[13] M. R. Pinto, C. S. Rafferty, and R. W. Dutton, ''PISCES II: Poisson and Continuity Equation Solver,'' Stanford Eelctronics Laboratories, Department of Electrical Engineering, Stanford University, September 1984.

[14] M. R. Pinto, C. S. Rafferty, H. R. Yeager, and R. W. Dutton, ''PISCES-IIB, Supplementary Report,'' Stanford Electronics Laboratories, Department of Electrical Engineering, Stanford University.

[15] G. W. Taylor, H. M. Darley, R. C. Frye, and P. K. Chatterjee, "A Device Model for an Ion-Implanted MESFET," *IEEE Trans. Electron Devices,* vol. ED-26, no. 3, pp. 172-182, March 1979. (FET.m1)

[16] C. H. Chen, M. Shur, and A. Peczalski, "Trapping-Enhanced Temperature Variation of the Threshold Voltage of GaAs MESFET's," *IEEE Trans. Electron Devices,* vol. ED-33, no. 6, pp. 792-798, June 1986. (FET.m2)

[17] N. Yokoyama, A. Shibatomi, S. Ohkawa, M. Fukuta and H. Ishikawa, "Electrical

Properties of the Interface Between An n-GaAs Epitaxial Layer and A Cr-doped Substrate," in *Gallium Arsenide and Related Compounds 1976,* Inst. Phys. Conf. Ser. No. 33b, pp. 201-209. (SG.e12)

[18] Y. M. Young and G. L. Pearson, "Deep Trapping Effects at the GaAs-GaAs:Cr Interface in GaAs FET Structures," *J. Appl. Phys.*, 49(6), pp. 3348-3352, June, 1978. (SG.e10)

[19] H. Tranduc, P. Rossel, J. Graffeuil, C. Azizi, G. Nuzillat and G. Bert, "Substrate and Interface Effects in GaAs FET's," *Rev. Phys. Appl.,* vol. 13, pp. 655-659, December 1978. (SG.e9)

[20] A. Zylbersztejn, G. Bert and G. Nuzillat, "Hole Traps and Their Effects in GaAa MESFETS," in *Gallium Arsenide and Related Compounds 1979*, Inst. Phy. Conf. Ser. No. 45, pp. 315-325. (SG.e13)

[21] T. Itoh and H. Yanai, "Long-term Drift of GaAs MESFET Characteristics and Its Dependence on Substrate With Buffer Layer," in *Gallium Arsenide and Related Compounds 1979*, Inst. Phy. Conf. Ser. No. 45, pp. 326-334. (SG.e11)

[22] T. Itoh and H. Yanai, "Stability of Performance and Interfacial Problems in GaAs MESFET's," *IEEE Trans. Electron Devices,* vol. ED-27, no. 6, pp. 1037-1045, June 1980. (SG.e7)

[23] S. J. Lee and C. P. Lee, "Temperature Effect On Low Threshold Voltage Ion-implanted GaAs MESFETS," *Elec. Lett,* vol. 17, no. 20, 1st October 1981. (SG.e16)

[24] C. Kocot and C. A. Stolte, " Backgating in GaAs MESFET's," *IEEE Trans Electron Devices,* vol. ED-29, no. 7, July 1982. (SG.e17)

[25] C. P. Lee, S. J. Lee, and B. M. Welch, "Carrier Injection and Backgating Effct in

GaAs MESFET's," *IEEE Electron Device Lett.*, vol. EDL-3, no. 4, pp. 97-98, April 1982. (SG.e1)

[26] C. P. Lee, "Influence of Substrates On the Electrical Properties of GaAs FET Devices and Integrated Circuits," in *Semi-Insulating III-V Materials,* pp. 324-335, 1982. (SG.e18)

[27] M. Ogawa and T. Kamiya, "Correlation Between the Backgating Effect of a GaAs MESFET and the Compensation Mechanism of a Semi-Insulating Substrate," *IEEE Trans. Electron Devices,* vol. ED-32, no. 3, pp. 571-576, March 1985. (SG.e19)

[28] C. P. Lee and M. F. Chang, "Shielding of Backgating Effects in GaAs Integrated Circuirts," *IEEE Electron Device Lett.,* vol. EDL-6, no. 4, pp. 169-171, April 1985. (SG.e6)

[29] C. P. Lee and M. F. Chang, "Temperature Dependence of Backgating Effect in GaAs Integrated Circuits," *IEEE Electron Device Lett.*, vol. EDL-6, no. 8, August 1985. (SG.e3)

[30] R. W. Haisty and P. L. Hoyt, "Investigation of Voltage Breakdown in Semi-insulating GaAs," *Solid-State Electronics,* vol. 10, pp. 795-800, 1967. (SG.e28)

[31] M. A. Lampert and P. Mark, *Current Injections in Solids,* New York: Academic Press, 1970

[32] K. Horio, T. Ikoma, and H. Yanai, "Computer-Aided Analysis of GaAs n-i-n Structures with a Heavily Compensated i-Layer," *IEEE Trans. Electron Devices,* vol. ED-33, no. 9, pp. 1242-1250, September 1986. (SG.m4)

[33] J.-C Lee, A. J. Strojwas, T. E. Schlesinger, and A. G. Milnes, "Electrical Isolation Rule for GaAs Integrated Circuits Fabricated on Semi-Insulating Substrates,"

IEEE Trans. Electron Devices, vol. 38, no. 3, pp. 447-454, March 1991. (SG.m5)

[34] Y. Liu, R. W. Dutton, and M. D. Deal, “Schottky Contact Effects in the Sidegating Effect of GaAs Devices,” *IEEE Electron Device Lett.,* vol. 13, no. 3, pp. 149-151, March, 1992. (SG.e24)

[35] M. F. Chang, C. P. Lee, L. D. Hou, R. P. Vahrenkamp, and C. G. Kirkpatrick, “Mechanism of Surface Conduction In Semi-insulating GaAs,” *Appl. Phys. Lett.,* 44 (9), pp. 869-871, 1 May 1984. (SG.e4)

[36] Y. Liu, R. W. Dutton, and M. D. Deal, “Reply to Comments on ‘Schottky Contact Effects in the Sidegating Effect of GaAs Devices,’” *IEEE Electron Device Lett.,* vol. 13, vol. 10, pp. 547-548, October 1992. (SG.e26)

[37] Y. Liu, R. W. Dutton, and M. D. Deal, “Sidegating Effect of GaAs MESFET’s and Leakage Current in a Semi-Insulating GaAs Substrate,” *IEEE Electron Device Lett.,* vol. 11, no. 11, pp. 505-507, November,1990. (SG.e23)

[38] Z. -M. Li, S. P. McAlister, W. G. McMullan, C. M. Hurd, and D. J. Day, “Impact Ionization of Deep Traps in Semi-insulating GaAs Substrates,” *J. Appl. Phys.,* 67 (12), pp. 7368-7372, 15 June 1990. (SG.e21)

[39] Z. -M. Li, D. J. Day, S. P. MaAlister, and C. M. Hurd, “Inclusion of Impact Ionization in the Backgating of GaAs FET’s,” *IEEE Electron Device Lett.,* vol. 11, no. 8, pp. 342-345, August 1990. (SG.e20)

[40] E. Schöll, “Bistability and Nonequilibrium Phase Transitions in a Semiconductor Recombination Model with Impact Ionization of Donors,” *Z. Phys. B,* vol. 46, pp. 23, 1982.

[41] E. Schöll, *Nonequilibrium Phase Transitions in Semiconductors,* Berlin: Springer-Verlag, 1987.

[42] S. Makram-Ebeid and P. Minondo, “Side-gating in GaAs Integrated Circuits: Surface and Bulk Related Phenomena,” in *GaAs IC Symposium,* pp. 142-144, 1983. (SG.e15)

[43] S. Markram-Ebeid and P. Minondo, “The Roles of the Surface and Bulk of the Semi-Insulating Substrate in Low-Frequency Anomalies of GaAs Integrated Circuits,” *IEEE Trans. Electron Devices,* vol. ED-32, no. 3, pp. 632-642, March 1985. (SG.e22)

[44] H. Hasegawa, T. Kitagawa, T. Sawada, and H. Ohno, “A New Side-gating Model for GaAs MESFETs Based on Surface Avalanche Breakdown,” in *Gallium Arsenide and Related Compounds 1984,* Inst. Phys. Ser. Conf. No. 74, pp. 521-526. (SG.e27)

[45] A. Mircea, A. Mitonneau, L. Hollan, and A. Briere, “Outdiffusion of Deep Electron Traps in Epitaxial GaAs,” *Appl. Phys.,* vol. 11, pp. 153-158, 1976.

[46] S. Makram-Ebeid, D. Gautard, P. Devillard, and G. M. Martin, “Outdiffusion of the Main Electron Trap in Bulk GaAs,” *Appl. Phys. Lett.*, vol. 40, pp. 161-163, 1982.

[47] H. Hasegawa, T. Kitagawa, and H. Ohno, “Surface Electrical Breakdown with White-light Emission on Semi-insulating GaAs Substrates,” *Elect. Lett.,* vol. 20, no. 13, pp. 561-562, 21st June 1984. (SG.e14)

[48] N. Goto and Y. Ohno, “Two Dimensional Simulation of GaAs MESFET Side-gating Effect,” in *Semi-insulating III-V Materials 1988,* pp. 253-257. (SG.m1)

[49] N. Goto, Y. Ohno, and H. Yano, “Threshold Voltgae Model for Side-gating Effect in GaAs MESFETs Based on Hole Injection and Recombination,” in *Gallium Arsenide and Related Compounds 1989,* Inst. Phys. Conf. Ser. No. 106, pp. 671-676. (SG.m2)

[50] H. Yano, S. Kumashiro, N. Goto, and Y. Ohno, "Two Demensional Transient Device Simulator with Deep Trap Model for Compound Semiconductor Devices," in *IEDM Tech. Dig. 1989,* pp. 151-154. (SG.m3)

[51] K. Inokuchi, Y. S. Itoh, and Y. Sano, "Influence of Metal Structure on Sidegating Properties in GaAs LSIs," *J. Electrochem. Soc.,* vol. 137, no. 9, p. 464C, Sept. 1990. (SG.e25)

[52] R. L. Van Tuyl and C. A. Liechti, "High-Speed Integrated Logic with GaAs MESFET's," *IEEE J. Solid-State Circuits,* October 1974. (TCH.8)

[53] B. M. Welch, F. H. Eisen, and J. A. Higgins, "Gallium Arsenide Field-Effect Transistors by Ion Implantion," *J. Appl. Phys.,* vol. 45, no. 8, pp. 3685-3687, August 1974. (TCH.9)

[54] P. T. Ho, A. Rosen, and J. Klatskin, "Performance of Sulphur-ion-Implanted GaAs F.E.T.s," *Elec. Lett.,* vol. 12, no. 1, pp. 17, 8th January 1976. (TCH.10)

[55] R. C. Eden and B. M. Welch, "Low Power Depletion Mode Ion-Implanted GaAs FET Integrated Circuits," *IEEE Trans. Electron Devices,* vol. ED-24, no. 9, pp. 1209-1210, September 1977. (TCH.11)

[56] R. C. Eden, B. M. Welch, and R. Zucca, "Planar GaAs IC Technology: Applications for Digital LSI," *IEEE J. Solid-State Circuits,* vol. SC-13, no. 4, pp. 419-426, August 1978. (TCH.7)

[57] F. H. Eisen, "Materials and Processes for GaAs Integrated Circuits," in *Gallium Arsenide and Related Compounds 1981,* nst. Phy. Conf. Ser. no. 63, pp. 515-520. (TCH.4)

[58] S. I. Long, B. M. Welch, R. Zucca, P. M. Asebeck, C-P Lee, C. G. Kirkpatrick, F. S. Lee, G. R. Kaelin, and R. C. Eden, "High Speed GaAs Integrated Circuits,"

Proc. IEEE, vol. 70, no. 1, pp. 35-45, January 1982. (TCH.6)

[59] B. M. Welch, Y-D Shen, R. Zucca, R. C. Eden, and S. I. Long, “LSI Processing Technology for Planar GaAs Integrated Circuits,” *IEEE Trans. Electron Devices,* vol. ED-27, no. 6, pp. 1116-1124, June 1980. (TCH.1)

[60] R. Zucca, B. W. Welch, R. C. Eden, and S. I. Long, “GaAs Digital IC Technology/ Statistical Analysis of Device Performance,” *IEEE Trans. Electron Devices,* vol. ED-27, no. 6, pp. 1109-1115, June 1980. (TCH.3)

[61] S. M. Sze, *Physics of Semiconductor Devices,* John Wiley & Sons, 1981. (DEV.2)

[62] R. W. Williams, *Gallium Arsenide Processing Techniques,* Dedham, MA: Artech House, 1984. (TCH.2)

[63] E. H. Rhoderick and R. H. Williams, *Metal-Semiconductor Contacts,* Lodon: Clarendon Press, 1988. (DEV.1)

[64] J. R. Waldrop, *J. Vac. Sci. Technol.,* B2, 445, 1984

[65] K. W. Böer and G. Döhler, “Influence of Boundary Conditions on High-Field Domains in Gunn Diodes,” *Phy. Rev.,* vol. 186, no. 3, pp. 793-800, 15 October 1969

[66] D. E. Holmes, R. T. Chen, K. R. Elliott, and C. G. Kirkpatrick, ‘’Stoichiometry-controlled Compensation in Liquid Encapsulated Czochralski GaAs,” *Appl. Phys. Lett.,* vol. 40, no. 1, pp. 46-48, 1 January 1982. (DP.e13)

[67] P. F. Lindquist, “A Model Relating electrical Properties and Impurity Concentrations in Semi-insulating GaAs,” *J. Appl. Phys.,* vol. 48, no. 3, pp. 1262-1267, March 197”7. (DP.m2)

[68] R. Zucca, “Electical Compensation in Semi-insulating GaAs,” *J. Appl. Phys.,*

vol. 48, no. 5, pp. 1987-1994, May 1977. (DP.e4)

[69] G. M. Martin, J. P. Farges, G. Jacob, and J. P. Hallais, "Compensation Mechanisms in GaAs," *J. Appl. Phys.,* vol. 51, no. 5, pp. 2840-2852, May 1980. (DP.e3)

[70] D. E. Holmes, R. T. Chen, K. R. Elliott, and C. G. Kirkpatrick, ''Compensation Mechanism in Liquid Encapsulated Czochralski GaAs: Importance of Melt Stoichiometry," *IEEE Trans. Mirowave Theory and Techniques,* vol. MTT-30, no. 7, pp. 949-954, July 1982. (DP.e5)

[71] D. E. Holmes, K. R. Elliott, R. T. Chen, and C. G. Kirkpatrick, "Stoichiometry-Related Centers in LEC GaAs," in *Semi-Insulating III-V Material,* pp. 19-27, 1982. (?)

[72] E. J. Johnson, J. A. Kafalas, and R. W. Davies, "The Role of Deep-level Centers and Compensation in Producing Semi-insulating GaAs," *J. Appl. Phys.* vol. 54, no. 1, pp. 204-207, January 1983. (DP.m1)

[73] A. G. Milnes, *Deep Impurities in Semiconductors,* Wiley, New York, 1973.

[74] A. M. Valladon, J. L. Debrun, G. M. Martin, A. Mitonnearu, and A. Mircea, "Direct Evidence for the Nonassignment to Oxygen of the Main Electron Trap in GaAs," *J. Appl. Phys.,* vol. 50, no. 6, pp. 4022-4025, June 1979. (?)

[75] R. J. Wagner, J. J. Krebs, G. H. Stauss, and A. M. White, "Submillimeter EPR Evidence for the As Antisite Defect in GaAs," *Solid-State Comm.,* vol. 36, pp. 15-17, 1980. (?)

[76] J. Lagowski, H. C. Gatos, J. M. Parsey, K. Wada, M. Kaminska, and W. Walukiewicz, "Origin of the 0.82-eV Electron Trap in GaAs and Its annihilation by Shallow donors," *Appl. Phys. Lett.,* vol. 40, no. 4, pp. 342-344, 15 Feruary 1982. (DP.e7)

[77] J. Lagowski, J. M. Parsey, M. Kaminska, K. Wada, and H. C. Gatos, "On the Behavior Deep Level (EL2) in GaAs," in *Semi-Insulating III-V Materials,* pp. 154-159, 1982. (?)

[78] D. E. Holmes, R. T. Chen, and J. Yang, "EL2 Distributions in Doped and Undoped Liquid Encapsulated Czochralski GaAs," *Appl. Phys. Lett.,* vol. 42, no. 5, pp. 419-421, 1 March 1983. (DP.e14)

[79] H. J. von Bardeleben, D. Stievenard, D. Deresmes, A. Huber, and J. C. Bourgoin, "Indentification of Defect in a Semiconductor: EL2 in GaAs," *Phys. Rev. B,* vol. 34, no. 10, pp. 7192-7202, 15 November 1986. (?)

[80] J. F. Wager and J. A. Van Vechten, "Atomic Model for the EL2 Defect in GaAs," *Phys. Rev. B,* vol. 35, no. 5, pp. 2330-2339, 15 February 1987-I. (?)

[81] G. A. Baraff and M. Schluter, "Electronic Structure and Binding Energy of the As_{Ga}-As_i Pair in GaAs: El2 and the Mobility of Interstitial Arsenic," *Phys. Rev. B,* vol. 35, no. 12, pp. 6145-6164, 15 April 1987-II. (?)

[82] G. M. Martin, A. Mitonneau, and A. Mircea, "Electron Traps in Bulk and Epitaxial GaAs Crystals," *Elec. Lett.,* vol. 13, no. 7, pp. 191-193, 31st March 1977. (DP.e8)

[83] A. Mitonneau, A. Mircea, G. M. Martin, and D.Pons, "Electron and Hole Capture Cross-sections at Deep Centers in Gallium Arsenide," *Rev. Phys. Appl.,* vol. 14, pp. 853-861, October 1979. (DP.e10)

[84] M. Taniguchi and T. Ikoma, "Variation of the Midgap Electron Traps (EL2) in Liquid Encapsulated Czochralski GaAs," *J. Appl. Phys.,* vol. 54, no. 11, pp.6448-6451, November 1983. (DP.e9)

[85] J. Lagowski, D. G. Lin, T. Aoyama, and H. d. Gatos, "Identification of Oxygen-

related Midgap Level in GaAs," *Appl. Phys. Lett.,* vol. 44, no. 3, pp. 336-338, 1 February 1984. (DP.e6)

[86] M. Henini, B. Tuck, and C. J. Paull, "Deep States in GaAs LEC Crystals," *Solid-State Electronics,* vol. 29, no. 5, pp. 483-488, 1986. (DP.e1)

[87] J. S. Blakemore, "Electron Capture and Emission for Midgap Centers," *J. Phys. Chem. Solids,* vol. 49, no. 6, pp. 627-631, 1988. (DP.e2)

[88] . E. Aspnes, "GaAs Lower Conduction Band Minimum: Ordering and Properties," *Phys. Rev.*, vol. 14, pp. 5331, 1976.

[89] S. Selberherr, "Process and Device Modeling VLSI," *Microelectron. Reliab.,* vol 24, no. 2, pp. 225-257, 1984.

[90] M. A. Littlejohn, J. R. Hauser, T. H. Glisson, "Velocity-field Characteristics GaAs with Γ_6^c-L_6^c-X_6^c conduction band ordering," *J. Appl. Phys.,* vol. 48, no. 11, pp. 4587-4590, Nov. 1977.

[91] W. Shockley and W. T. Read, Jr., "Statistics of the Recombinations of Holes and Electrons," *Phys. Rev.,* vol. 87, no. 5, pp. 835-842, September 1, 1952.

[92] H. A. Bethe, "Theory of the Boundary layer of Crystal Rectifiers," *MIT Radiat. Lab. Rep.,* 43-12, 1942.

[93] C. R. Crowell, "The Richardson Constant for Thermionic Emission in Schottky Barrier Diodes," *Solid State Electron.,* vol 8, pp. 395, 1985.

[94] C. R. Crowell and S. M. Sze, "Electron-Optical-Phonon Scattering in the Emitter and Collector Barriers of Semiconductor-Metal-Semiconductor Structures," *Solid State Electron.,* vol. 8, pp. 979, 1965.

[95] C. W. Kao, L. Anderson, and C. R. Crowell, "Photoelectron Injection at

Metal-Semiconductor Interface,'' *Surface Sci.,* vol. 95, pp. 321, 1980.

[96] C. R. Crowell and S. M. Sze, ''Quantum-Mechanical Reflectrion of Electrons at Metal-Semiconductor Barriers: Electron Transport in Semiconductor-Metal-Semiconductor Structures,'' *J. Appl. Phys.,* vol 37, pp. 2685, 1966.

[97] F. A. Padovani and R. Stratton, ''Field and Thermionic-Field Emission in Scholttky Barriers,'' *Solid State Electron.,* vol. 9, pp. 695, 1966.

[98] G. M. Martin, A. Mitonneau, D Pons, A. Mircea, and D. W. Woodard, ''Detailed Electrical Characterisation of the Deep Cr Acceptor in GaAs,'' *J. Phys. C: Solid State Phys.,* vol 13, pp. 3855-3882, 1980. (DP.e11)