HIGH FREQUENCY CHARACTERIZATION AND MODELING OF ON-CHIP INTERCONNECTS AND RF IC WIRE BONDS

A DISSERTATION

SUBMITTED TO THE DEPARTMENT OF ELECTRICAL ENGINEERING

AND THE COMMITTEE ON GRADUATE STUDIES

OF STANFORD UNIVERSITY

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

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June, 2001

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Abstract

Continuous scaling of transistors combined with increased chip area results in the ratio of global wire delay to gate delay increasing at a super-linear rate. For sub-0.25 μm technology and multi-gigahertz clock frequencies, on-chip interconnects may exhibit transmission line behavior. Simple RC models have become inadequate for simulation of modern VLSI circuits; parasitic inductance of the wires can no longer be ignored. In addition, parasitic inductance and capacitance of IC packages impose limits on the performance of circuits at high frequencies.

In this work, 3-D geometry-based physical extraction is exploited in the modeling of on-chip and off-chip inductance and capacitance. Modeling of on-chip inductance is presented for chips with power/ground wires and grids that emulate those used in practical circuits. The models capture 3-D geometry and process technology effects. Analytical formulae suitable for circuit design as well as for screening of inductance effects in CAD tools are developed to estimate the on-chip wire inductance. S-parameter characterization of fabricated chips up to 10 GHz shows good agreement with simulation and analytical calculations. Consideration of substrate effects may result in reduction of wire inductance when

the spacing between the signal and ground wires becomes large. Eddy currents in ground planes or dense grids in a chip can also significantly reduce wire inductance. Design insight and suitable guidelines for minimizing interconnect inductance are demonstrated. On-chip capacitance modeling capabilities including 3-D rendering of solid objects, surface meshing, electrical parameter extraction for arbitrarily shaped objects are presented, which provide a direct link between design parameters and electrical performance.

Bonding wires are extensively used in IC packaging and circuit design in RF applications. An approach to fast 3-D modeling of the geometry for bonding wires in RF circuits and packages is demonstrated. The geometry can readily be used to extract electrical parameters such as inductance and capacitance. An equivalent circuit is presented to model the frequency response of bonding wires. To verify simulation accuracy, test structures have been constructed and measured. Excellent agreement between modeled results and measured data is achieved for frequencies up to 10 GHz.

Acknowledgments

I am grateful to many people who made this work possible and helped me before and during my Ph.D. studies at Stanford. First of all, I would like to thank my advisor Prof. Robert W. Dutton for giving me such a wonderful opportunity to study and work in his great group at Stanford. He encouraged me to define research topics by myself, and gave me research freedom and guidance. His extraordinary engineering vision and insight have lead me to many successful investigations. He never gave me pressure in research, but instead, much motivation and inspiration. I am very grateful for his many thorough paper reviews and talk rehearsals. Studying in his group has been one of the most productive and enjoyable times in my life. Time will pass by, but my gratitude will never fade.

I would like to thank my associate advisor Prof. Simon S. Wong. I benefited a lot from the interesting discussions in his group meetings. His advice was extremely valuable to my research on VLSI interconnects. Collaborations with his group members were very pleasant and fruitful. I would like to thank Senior Research Scientist Dr. Zhiping Yu at Dutton's group. Dr. Yu's advice and help span my entire research activities – from device physics to LaTex questions. Detailed technical discussions with him are always helpful. I also thank

both of them for reading my thesis. I am also indebted to Prof. R. Fabian Pease for his chairing my Ph.D. oral examination committee.

Stanford is such an exciting place to learn. It brings together the most outstanding students around the world. Working with them really enriched my learning and life experience. I am thankful to many group-mates at Dutton's group for their helpful discussions. I am indebted to Ken Wang who was the first student talking to me about Ph.D. research, Edward K. Chan and Gaofeng Wang for their helpful discussions on electromagnetics. I especially thank Kinyip Sit for his helping me adjust to the new environment in my first year at Stanford. I am also thankful to Francis Rotella, Tao Chen, Xin-Yi Zhang, Jae-June Jang, Jung-Suk Goo, Changhoon Choi, Michael Kwong, Choshu Ito, Atsushi Kawamoto, Kwang-Hoon Oh, Yi-Chang Lu, Nathan Wilson and visiting scholars Hiroyuki Sakai (Matushita) and Olof Tornblad (Ericsson). Research associates at Dutton's group deserve special recognition. I would like to thank Edward Kan (now faculty of Cornell University) for helping me start my research in the first year at Stanford, Daniel Yergeau for his always complete answers to my many computer questions. I also thank Ze-Kai Hsiau and Sherry Y. Shen for the research collaborations.

I am grateful to many students in other groups for the productive collaboration and enjoyable friendship. I thank C. Patrick Yue for his co-authoring my first IEDM paper, and Bendik Kleveland for our successful trips to IEDM'99 and ISSCC'00 as well as his sense of humor. I also thank Richard T. Chang, Niranjan Talwalkar, Chet Soorapanth, SoYoung Kim, Takeshi Furusawa (Hitachi), Min Xu, S. Mohan, Mar Hershenson and Eui-Young Chung. I especially thank my officemate Hamid Rategh and Joel L. Dawson for their

encouragement and friendship which provided me such a friendly working space. I also would like to thank Paul Jerabek of the Center for Integrated Systems (CIS) at Stanford for the training in the CIS Labs.

I would like to thank the administrators in Dutton's group as well as in CIS. I am indebted to Fely Barrera, Maria Paz F. Perea and Miho Nishi for their excellent help and support. I also would like to thank Dr. Richard Dasher, Carmen Miraflor, Maureen Rochford, Joanna Evans of CIS for their help and the successful SPIE trip to IBM.

The Ph.D. students at Stanford especially benefit from the dynamic relationships with industry mentors. I am grateful to Tak Young of Monterey Designs for talking to me about research in the first month of my joining Stanford and for his offering me summer internship at Synopsys. I thank Norman Chang of HP Labs for helping me define the on-chip interconnect project. I also thank Mohiuddin Mazumder of Intel and Alina Deutsch of IBM T. J. Watson Research Center for helpful discussions. I would like to specially thank Torkel Arnborg of Ericsson for his help and advice on the RF device and package modeling.

I also would like to thank my undergraduate and Master Degree advisor, Prof. Xiaolang Yan, for presenting me the great opportunities of integrated circuit researches in my early years of college studies.

Finally, I would like to thank my parents for their constant support and caring, especially in my difficult times. I would like to thank my wife, Han, for her love, support and patience.

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Chapter 1

Introduction

As semiconductor technology continues to scale, wires, not devices, gradually dominate the delay, power and area of microprocessors and ASIC designs. The constant increasing clock frequency combined with increased chip area results in the ratio of global wire delay to gate delay increasing at a super-linear rate. For sub-0.25 μm technology at gigahertz-scale clock frequencies, interconnects exhibit transmission line behavior. This has spawned the need to accurately model the parasitics – resistance, inductance and capacitance – for on-chip wires. In addition, parasitics of IC packages, such as bonding wires, imposes a limit on the performance of circuits at radio frequencies (RF). In this chapter, the evolution of integrated circuit (IC) technology is reviewed in Section 1.1. RF integrated circuit packaging technology is briefly reviewed in Section 1.2. IC simulations are discussed in Section 1.3 and organization of the thesis is previewed in Section 1.4.

Figure 1.1: From Bell Telephone Laboratories: the first transistor.

1.1 VLSI Digital Systems

Modern microelectronics started with the invention of the first transistor. On 23 December 1947, John Bardeen and Walter Brattain demonstrated their invention of a solid-state amplifier at Bell Telephone Laboratories. It was the point-contact transistor, whose active part was the interface between metal leads and a germanium semiconducting crystal, as shown in Fig. 1.1. On September 12, 1958, the integrated circuit was developed by Jack Kilby of Texas Instruments. He had conceived of creating components in silicon by diffusing it with impurities to make p-n junctions. He built a complete oscillator on a chip. The interconnects of these devices were made manually in a way similar to the bonding wires [34] [35]. Almost at the same time, Robert Noyce and Jean Hoerni at Fairchild Semiconductor developed the planar process that lead to the commercialized IC process. The planar process enabled electrical conducting material, such as aluminum, to be laid down directly on the insulating materials, forming metal layers to make the necessary electrical interconnections [52] [35]. Forty-two years later, in 2000, Jack Kibly won the Nobel Prize for inventing the IC that made microelectronics possible and changed the world altogether with its attendant

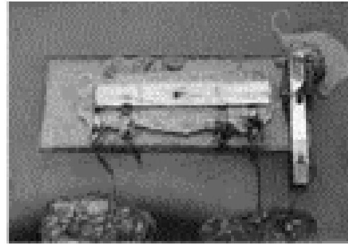


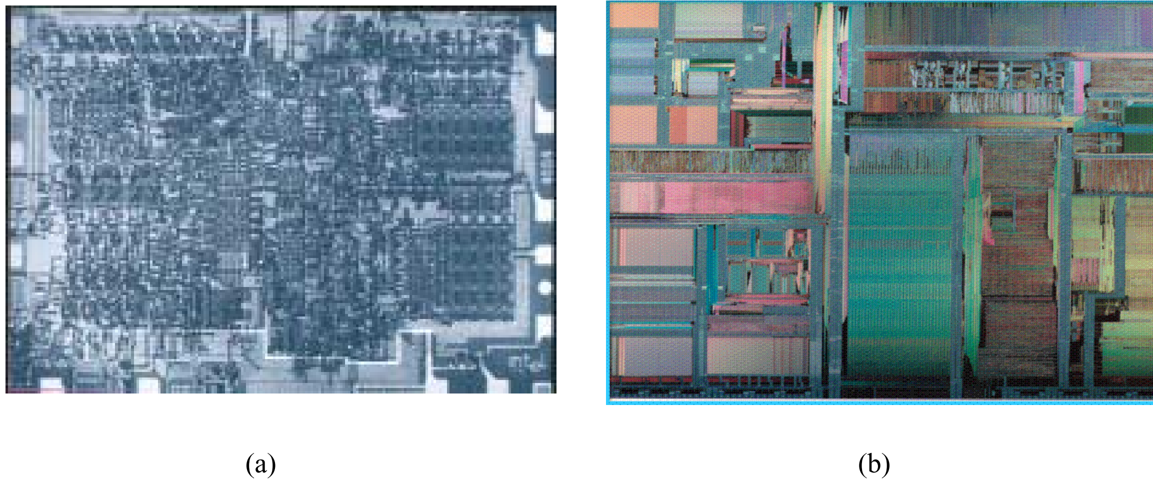
Figure 1.2: From Texas Instrument: the first integrated circuit.

technology. A piece of semiconductor containing active (transistors) and passive (resistors and capacitors) components, together with their interconnections are shown in Fig. 1.2. The dimensions of the devices and interconnections are comparable as shown on the photo. Since then, IC technologies have been advanced from simple circuits to complex microsystems. In 1971, Marcian E. Hoff of Intel developed the first microprocessor. It was a 4-bit processor and a single IC that performed all the elementary functions of a computer, see Fig. 1.3(a). As shown in the die photo, the chip consists of much smaller transistors[1], and in addition, lots of interconnects. Fig. 1.3(b) shows the first Pentium Processor[2] which is the representative of modern IC technology. It consists of millions of transistors which are aggressively scaled down while on-chip interconnects have increased significantly in terms of both quantity and length.[3] Interconnects have become the bottle neck for both chip performance and area. Consider a fixed-length interconnect (say 1 mm long), the ratio of its delay to the gate delay increases 2× per technology generation [26]. Interconnect scaling becomes the dominant factor for high performance VLSI. Interconnect delays, crosstalk, power and area pose many challenges for IC designers [7][14]. Computer-Aided Design (CAD) tools

[1]The minimum feature size of IC chips at the early 60's was about 40 μm while the one at the early 70's was around 10 μm. Generally, the feature size reduces 0.7 × per every three years (Moore's Law) [54].

[2]The processor, manufactured in 0.8 μm BiCMOS process, runs at 66 MHz clock frequency.

[3]Virtually transistors can not be seen from the photo while all one can see is *wires* everywhere.



(a) (b)

Figure 1.3: (a) The first microprocessor: the Intel 4004. (b) The first Intel Pentium processor.

must now deal with wires as the dominant facing future designs.

1.2 IC Packaging

On-chip interconnects ultimately are connected to the board level via IC packaging. Wire bonds are extensively used in IC packaging and especially for circuit design in RF applications. The recent boom in wireless communications has strengthened the demand for design of integrated circuits for cellphones, base stations and a growing number of wireless applications. Fig. 1.4 shows a packaged RF power transistor (BJT) used in wireless communications. It is not uncommon that the number of wire bonds reaches hundreds. Among these wires, some are used for packaging purposes, and others function as part of the matching network in RF circuit. At wireless communication frequencies (up to 2.5 GHz or even higher), impedance matching networks (normally matched to 50 Ω) are required between the circuit blocks in RF systems to ensure maximum power transfer [40]. Wire bonds are

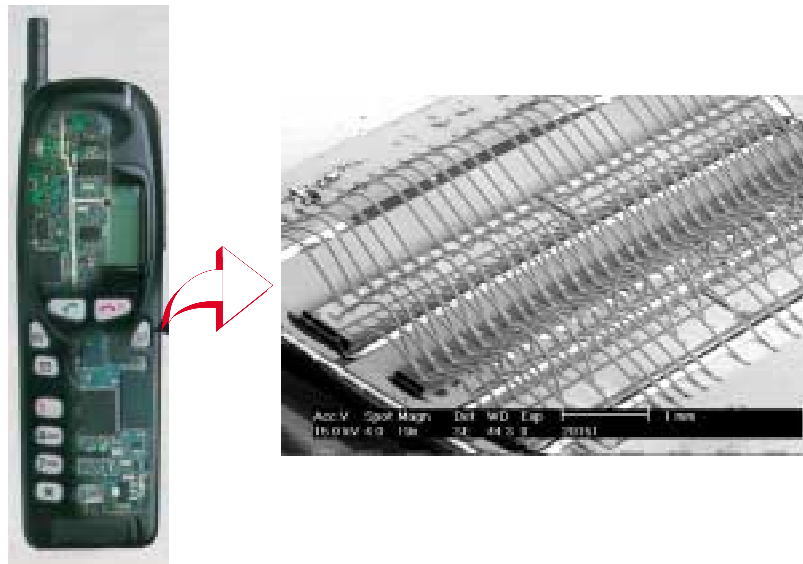


Figure 1.4: Wire bonds in the RF power transistors (BJT): Ericsson 20151.

also used in matching networks in MMIC (Monolithic Microwave IC) and HIC (Hybrid IC using ceramics) implementations. For high speed VLSI circuits, libraries of package models are also needed to achieve accurate system level simulations. Modeling bonding wires is a key issue in establishing such libraries.

1.3 Computer-Aided Design and Simulation

Computer-aided design plays a key and indispensable role in IC technology development and circuit design. Due to the ever-increasing complexity of microsystems, CAD and technology CAD (TCAD) tools provide insight that augments measurement techniques [20]. These tools after calibration to a relatively small number of experiments, exhibit very impressive predictive power, which can save time and cost in the IC manufacturing process. Fig. 1.5 shows the different levels of CAD and simulation - from technology simulation to

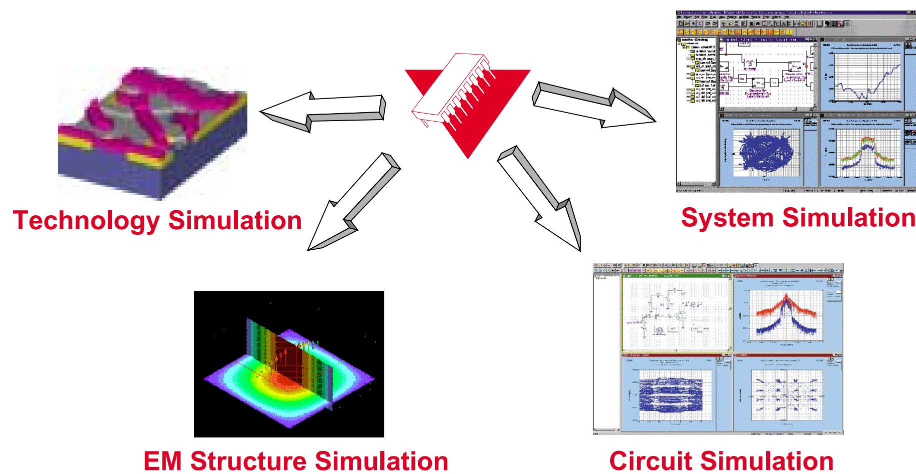


Figure 1.5: Simulations from technology to systems.

the system level. Technology simulation mainly addresses the physics and processing side of IC technology development. Electrical properties of devices are captured in electromagnetic structure simulation, which can be used in higher level simulations. Circuit and system level simulations use information from the two lower level simulations, and are able to demonstrate performance characteristics at the higher levels. This thesis work mainly focuses on simulation at the two lower levels in the hierarchy.

1.4 Organization of the Thesis

This research focuses on the 3-D geometry modeling, electrical parameter extraction and analysis of on-chip interconnects and off-chip packaging interconnects. Modeling and simulation results are verified with measurement data from test chips. In Chapter 2, problem descriptions of the present efforts are outlined, followed by the review of previous work in

the field. Chapter 3 discusses electromagnetic theory with emphasis on inductance calculation since knowledge of field is a key foundation to solving complicated on-chip interconnect problems. Modeling of inductance for real chips with power/ground wires and grids is then presented in Chapter 4. The 3-D geometry tools and analytical formulae are also presented; these equations provide quick inductance estimation for CAD tools and can help to establish design guidelines. Chapter 5 moves to the package level, considering wire bonds modeling for RF ICs. A novel 3-D geometry modeling tool, test chip fabrication and a simple equivalent circuit are presented. Modeling of the ground plane effects for both on-chip interconnects and wire bonds are discussed in Chapter 6. The conclusions are summarized in Chapter 7.

Chapter 2

Previous Work

In this chapter the problem descriptions for modeling of VLSI on-chip interconnects and RF IC wire bonds are outlined. Then the previous work in both fields are reviewed.

2.1 Problem Description

2.1.1 VLSI On-Chip Interconnects

Modern IC technologies enable VLSI interconnects to be routed on many different metal layers. In current technology, designs can exploit up to six layers. Fig. 2.1 illustrates six layers of interconnect with their respective widths and heights. The lower metal layers, namely metal one and metal two layers, are used to route local interconnects which normally are short and narrow. The intermediate layers, layers three and four, are allocated for relatively longer interconnects or buses. The top metal layers, metal layer five and six, are generally used for global clock nets and power and ground grids/nets. This is because the

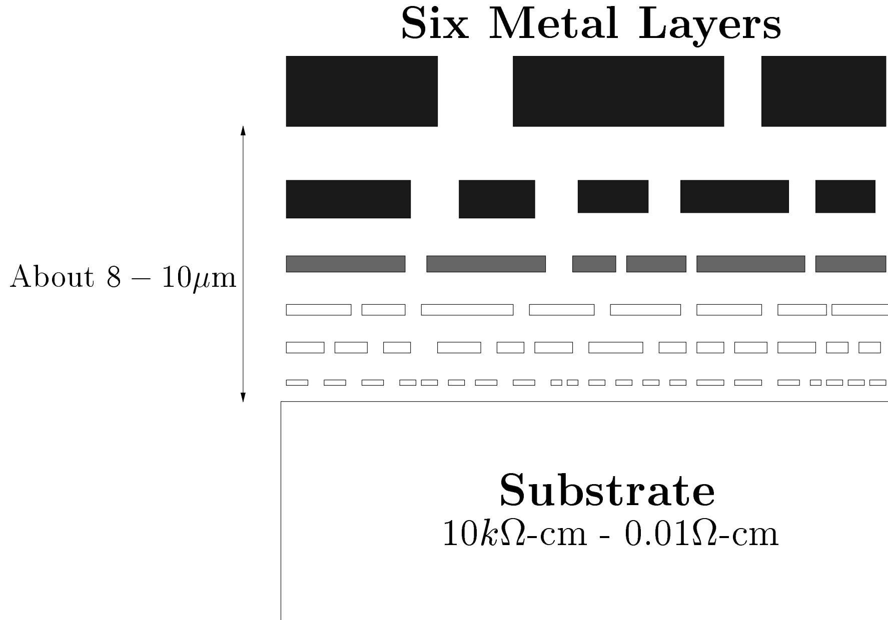


Figure 2.1: Approximation of six metal layers: widths and heights.

upper layers are much thicker and wider with coarser design rules, therefore, less resistive. In addition, they are farther away from the substrate and therefore have less coupling and loss at high frequencies. There are also small resistivity variations for different metal layers due to the process. If copper technology is used, the reported measured *average* Cu resistivity is $\rho \simeq 1.97\mu\Omega$-cm for M6 layer, and 2.03-2.17 $\mu\Omega$-cm for layers M3, M4, and M5 [16]. Interconnects are generally passive in nature. That is, they can only dissipate or store energy. Except for very regular arrays (such as memories), on-chip functional units tend to be wire-limited [13] [14].

RLC Transmission Line

In the analysis phase of design, lower metal layer's short on-chip wires can be modeled as lumped capacitive loads and longer wires can be modeled as lossy *RC* transmission lines.

Any wire whose resistance is small compared with the impedance of the circuit driving it can be considered short. Typically, wires under 1 mm are short, but resistance must be considered for all longer wires. Because of their relatively high resistivity, short length, and tight pitch, lower metal layers on-chip wires almost have inductance values that are sufficiently low to be safely ignored.

In modern IC technology with clock frequencies reaching the multi-gigahertz regime, long global interconnects on upper metal layers exhibit RLC transmission line effects. By using wider wires on upper metal layers for critical signal nets, such as clocks, and using copper interconnects, the wire resistance is reduced. As a result, the inductive impedance part, ωL, becomes comparable to the wire resistance, R. For these interconnects, inductance can no longer be ignored and needs to be carefully modeled.

As a rule of thumb, interconnects should be modeled as transmission lines if the signal rise time, t_r, is comparable to (or smaller than) the one-way signal propagation time delay through the signal path, t_d. Namely, if $t_r/t_d < 2.5$, lumped analysis is not appropriate and transmission lines model or distributed model should be used [28].

Partial differential equation formulations can be used to model transmission lines.[1] Consider voltage, V, to be a function of position, x, and time, t; equations can be derived to describe V from examination of Fig. 2.2. If I is the current through the series elements, the following equations describe the relationship of I and V:

$$\frac{\partial V}{\partial x} = RI + L\frac{\partial I}{\partial t} \tag{2.1}$$

[1] It can also be derived from electromagnetic waves theory instead of circuit theory [28].

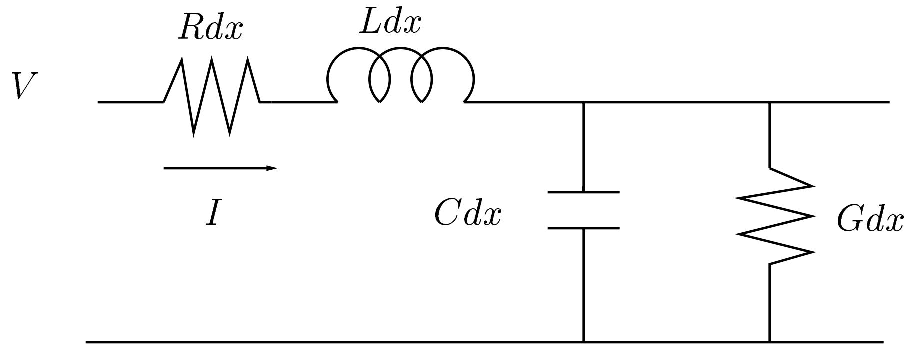


Figure 2.2: Infinitesimal model of a transmission line.

$$\frac{\partial I}{\partial x} = GV + C\frac{\partial V}{\partial t} \tag{2.2}$$

Differentiating the first equation with respect to x and substituting the second equation into the results gives

$$\frac{\partial^2 V}{\partial x^2} = RGV + (RC + LG)\frac{\partial V}{\partial t} + LC\frac{\partial^2 V}{\partial t^2} \tag{2.3}$$

If we ignore conductance of the dielectric material and set $G = 0$,

$$\frac{\partial^2 V}{\partial x^2} = RC\frac{\partial V}{\partial t} + LC\frac{\partial^2 V}{\partial t^2} \tag{2.4}$$

If wire inductance is small and can be neglected, Equation (2.4) becomes the diffusion equation,

$$\frac{\partial^2 V}{\partial x^2} = RC\frac{\partial V}{\partial t} \tag{2.5}$$

and signals *diffuse* as they move along the wire with pulse edges becoming dispersed with distance. Fig. 2.3 shows a 10 mm RC line and the waveform of its driving signal with 200

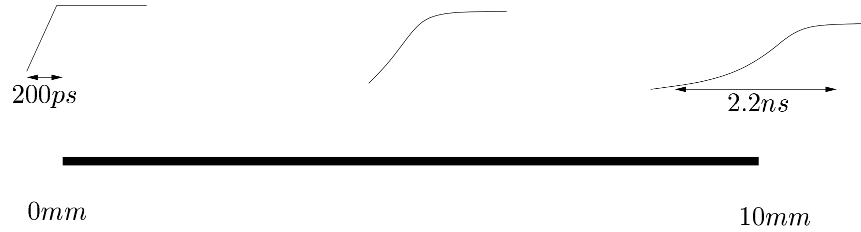


Figure 2.3: Response of a lossy RC line.

ps rise time at the left end of the wire as well as the waveform that appears 10 mm location to the right. Because of the diffusive nature of the RC line, the signal rise time has been increased to 2.2 ns at the 10 mm point.

Solving Equation (2.5) results in the familiar $\tau = RC$ delay constant[2]. Because both the resistance and capacitance increase with the length of the wire, the delay of a signal on an RC wire is increased quadratically with wire length.

If, instead, wire resistance is small and can be neglected, Equation (2.4) becomes a wave equation that governs the propagation of signals on LC wires.

$$\frac{\partial^2 V}{\partial x^2} = LC\frac{\partial^2 V}{\partial t^2} \tag{2.6}$$

Solving Equation (2.6) gives the signal propagation velocity, v, as

$$v = \frac{1}{\sqrt{LC}}$$

The signal is a waveform that propagates down the wire with velocity, v, without distortion

[2]Fig. 2.3 illustrates a typical 0.6 μm square wire with $R = 0.12\Omega/\mu m$, $C = 0.16fF/\mu m$. It has time constant of $RC = 1.9 \times 10^{-17} s/\mu m^2$. A 10 mm such wire has an approximate delay of 1.9 ns. As a rule of thumb, the delay, t_l, of a wire with length of l, is given by $t_l = 0.4l^2RC$. The rise time, t_{rl}, of a step response of a RC wire of length l is $t_{rl} = l^2RC$ [14].

of its waveform. Both forward and reverse traveling waves satisfy Equation (2.6). Because velocity is inversely proportional to the square-root of both the inductance and capacitance per wire length, the delay of a signal on a LC wire is directly proportional to length, namely, $l\sqrt{LC}$ where l is the length of the wire. This delay is also known as *Time of Flight*.

RLC Extraction

To extract resistance, R, for on-chip interconnects, skin effects and proximity effects should be considered [72]. These effects are frequency dependent, and will increase wire resistance at high frequencies. To model interconnect capacitance, both capacitance to the ground/substrate as well as capacitance to the neighboring wires need to be taken into account. Based on the definition of inductance, identification of current loops is necessary to calculate inductance. Because of multiple current return paths for on-chip interconnects, calculating wire inductance is more difficult than calculating capacitance. In extraction, multiple wires around the current-carrying wire need to be included for any possible current return paths. The substrate may also offer return paths for signals, therefore, needs to be included in the simulation. Skin effects and proximity effects also affect current return paths and decrease wire inductance at high frequencies. The frequency dependence of inductance is important especially when there is a ground plane, substrate, or other conductive grids nearby the interconnects.

Inductance and capacitance are characteristics of geometry configurations of the conductors. Accurate 3-D geometry is crucial for inductance and capacitance extraction; this point will be discussed further in Chapter 3 and Chapter 4.

2.1.2 RF IC Wire Bonds

Wire bonds are the most common technique for electrically attaching chips to packages. Wire bonds are formed by compression welding one end of a thin ($\sim$ 1 mil diameter) gold wire to a bond pad (typically 100μm on each side) on the chip and the other end to a pad on the package. Wire bonds are relatively inexpensive and geometrically compliant, allowing materials of unequal thermal expansion (i.e., chip and package to be bridged). They have significant self-inductance ($\sim$ 1nH/mm) and mutual inductance (up to $\sim$ 50% of mutual inductance depending on the separation of the wires); hence only one or two rows of pads around the periphery of the chip are typically used. Wire bonds are also used as circuit elements in matching networks or to realize high Q inductors for RF ICs. The length of a bonding wire and its shape (curvature) determine the inductance value. Bonding machines are used to bond these wires. While the shape can be repeatably controlled, the curvature of the wires is difficult to predict.

RLC Extraction

If the conducting interconnect leads are fabricated in pairs or at uniform height over a return plane, the lead is best modeled as a transmission line. With proper control of wire length, its shape and spacing, the impedance of the bonding wire can be matched to other transmission media (usually a 50 Ω stripguide on a PC board). If the spacing to a return is large and irregular or the structure consists of many parallel wires (up to several hundred) as in most RF IC power devices, the wire is modeled as a lumped inductor using the partial inductance concept [65]. Depending on how the chip is bonded and packaged, it is not

unusual for the conductor from the chip pad to the PC board to have as much as 10 nH of self-inductance and 5 nH of mutual inductance to adjacent conductors [14]. At higher frequencies (above 6 GHz), bonding wire capacitance can no longer be ignored and needs to be modeled as well [58].

As for the case of on-chip interconnect modeling, access to accurate 3-D geometry information is desirable for inductance and capacitance extraction for bonding wires.

2.2 Previous Work

2.2.1 Inductance Modeling for On-Chip Interconnects

On-chip inductance modeling for VLSI interconnects has not been important until last decade as die size has increased and chip clock frequencies reached the gigahertz range. Although there has been some inductance modeling work for board level designs, it can not be directly adopted for on-chip interconnects because of the more complicated wiring environment and different geometries that occur with on-chip interconnects.[3]

The earliest work in calculating inductances can be traced back to Maxwell and Neumann in late 1800's. By assuming that current returns from infinitely far away, Neumann derived the mutual and self-inductance formulae for cylindrical wires [64]. Maxwell showed how to calculate mutual and self-inductance in several important cases by means of what he called the *geometrical mean distance* (GMD) – either of one conductor from another or

[3]For example, it is usually cheap for board level design to have ground plane everywhere to reduce the inductance, and the distance from wire to ground plane is much greater than the wire thickness so that some approximate inductance formulae can be derived.

of a conductor from itself [64].[4] Most of this early work was summarized by E. B. Rosa and F. W. Grover in their books [64][24].

The most important milestone of on-chip inductance calculation came with the work of A. E. Ruehli in 1970's. Since it is very difficult to find the return paths for on-chip interconnects due to their complexity, Ruehli extended Neumann's early work and proposed *Partial Inductance* or *Partial Element Equivalent Circuit* (PEEC) concepts [65] [66]. He extended "current returns from infinity" to any two wires with arbitrary relative positions (not just two parallel wires). Conductor loops are divided into segments for which partial inductance are calculated. The partial inductances are then appropriately added to yield the desired loop inductance. Ruehli's work laid the foundation for many inductance extraction tools. Greenhouse used the PEEC method and circuit theory to derive inductance equations that include negative mutual inductance for on-chip spiral inductors [23]. Weeks studied the modeling of frequency dependent skin effects for inductance and resistance, and compared the results with measured data [79].

In the early 1990's, Kamon and White used the partial inductance concepts and developed a program, FASTHENRY, to automate the inductance calculations [33]. In this program, discretized magnetoquasistatic equations are reformulated using a circuit analysis technique known as mesh analysis. Generalized Minimal residual (GMRES) and multipole accelerated algorithms are used. The computational complexity and memory requirements grow linearly with the number of volume-elements required to discretize the conductors.

[4] Maxwell's powerful *geometrical mean distance*, *arithmetical mean distance* (AMD) and *arithmetic mean square distance* (AMSD) concepts make it possible to calculate many important on-chip inductances including the spiral inductor in RF circuits [46].

However, with complex on-chip geometries and increasing numbers of discretized elements, important in modeling skin and proximity effects, the time to extract wire inductance grows rapidly. Technology Modeling Associates, Inc. (TMA)[5], developed a similar tool, Raphael, for inductance extraction. Beattie also worked on efficient partial inductance extraction method by introducing "equipotential shells" [4] [5].[6]

It was not unitl the mid-1990's that identification and modeling of on-chip transmission line effects have been reported by IBM researchers [16]-[19] [62]. These papers, for the first time, pointed out the transmission line and inductive effects for on-chip interconnects using test chips and time domain analysis. Waveforms from a set of test chips show the importance of transmission line effects and crosstalk for both in-plane and vertical coupling. In [17], Deutsch, based on transmission line theory, proposed conditional expressions to determine when transmission line and inductance effects are important for accurate delay and crosstalk prediction for on-chip interconnects. Design guidelines and technology changes were proposed to achieve minimum delay and address crosstalk issues for local and global wirings. Kleveland used the frequency domain method to demonstrate the inductance effects at the sub-0.25 μm IC technology [36]. In recent years, major industry microprocessor designs, such as Intel's Itanium[7] and Compaq's Alpha chips, were reported to have to model the on-chip inductance [67] [80] [48] – both used co-planar waveguide structures, or ground plane for critical clock and signal wires to reduce inductance effects at the cost of

[5]TMA was merged with Avant! Corp. in 1997.

[6]By introducing the ellipsoidal shells to model the equipotential surfaces for filament currents, the positive definiteness of the resulting sparse inductance matrix is preserved for this and all other potential- shell models when the compensating currents are placed on equipotential surfaces of the original current distribution.

[7]The first IA-64 microprocessor.

chip area.

Extraction methods based on applying a field solver to generate look-up tables and equivalent circuits for high frequencies have been reported [25] [37] [38]. At HP Labs, He and Chang [25] show that without loss of accuracy, the extraction problem of n traces can be reduced to a number of one-trace and two-trace sub-problems. The one-trace and two-trace sub-problems then can be solved via a table-based approach. In addition, a quick inductance screening process and rules to identify those inductive interconnects and victim wires were established by Shen [41]. Clock-tree RLC extraction based on the generated look-up table are proposed by Chang [10] also at HP Labs. In 1999, Restle [63] presented IBM's full-wave extraction and simulation methods at DAC. Effects such as overshoot, reflections, frequency dependent effective resistance and inductance were illustrated using the full-wave simulation tool. Simple examples of design techniques to avoid, mitigate, and even take advantage of on-chip inductance effects were described. Another practical approach for extracting approximate inductances of on-chip interconnects was reported by Shepard [69], which models signal and power/ground wires independently and localizes inductive coupling by assuming currents only return via nearby power and ground wires. The commercial version of the program was reported at IC-CAD 2000 [68].

With extracted inductances, signal integrity and delay optimization can be studied. At IEDM'00, Huang[27] and Cao [8] reported RLC signal integrity analysis and analytical models of noise and delay for high speed on-chip global interconnects. Reference [27] indicates that the impact of inductive coupling on delay and noise is comparable to capacitive effects in high-speed buses; shielding strategies were also proposed. Because of the complexity, the

analytical method mainly focus on the two wires case [8]. Ismail [29]-[30] studied analytical propagation delay formulae including inductance; a repeater insertion technique was also proposed. Based on modeling results, some simple layout design rules have been proposed. Massoud [43] used interdigitated ground lines to minimizing self-inductance while Sinha [70] used multi-layered meshes for on-chip power supplies.

2.2.2 Modeling for RF IC Bonding Wire

Because of their relatively long length (compared to device dimensions) and owing to high RF frequencies (several gigahertz) routinely used for communication circuits, bonding wire inductance modeling captured RF designer's attention many years earlier than VLSI on-chip interconnects. Although, measured S-parameters of packaged devices at certain bias are usually provided by the manufacturers, they are typically good for small signal analysis only. These models provide little information for large signal analysis – for example, gain, power efficiency, and distortion (or linearity) analysis. A compact model for packaged devices, including bonding wires, is desirable for circuit simulation. March used simple equations to characterize bonding wires [42]. The formulae are mainly based on the early inductance calculation work as described in the last section [64][24]. Only wire lengths were used in inductance calculation. Shape (curvature) of the wires was not considered.

In order to model package parasitics, simulation of the intrinsic device is compared to the measured S-parameters of a packaged device [31]. This modeling approach relies on the accuracy of the intrinsic device model and requires measurement for individual devices. Accurately de-embedding of the device characteristics is difficult in most circumstances.

For complex 3-D geometries, a new physical method is needed to link geometry extraction and the modeling process. A method based on bonding wire geometries has been previously reported by Mouthaan in [49]. However, it involves manual measurement of the wire length; the shape of the wires has not been sufficiently considered. Analytical calculations for straight wires is used to estimate the inductance. Since manual measurement is error prone and 3-D geometry information is not completely captured, accuracy of this approach is limited. Patterson [53] used analytical formulae to calculate the bonding wire's self- and mutual inductance. But these equations were derived only for one specific geometry, shape or curvature of the wires – the methodology is not suited to generalized bonding wire configurations. For general 3-D geometries, automation in both generation and extraction would be preferred for modeling applications. Work in package modeling for RF circuit based on 3-D geometry information has been reported, primarily using a proprietary tool [32]. This thesis work on bonding wires focused on automated, fast and accurate general 3-D geometry generation. Wire shapes are correctly captured.

For microwave circuits, bonding wires used to interconnect microwave components and packages cannot be ignored in circuit analysis. Lee studied the bonding wire modeling for microwave and millimeter-wave integrated circuits including radiation effect (up to 100 GHz) [39].

Chapter 3

Electromagnetic Formulation

In this chapter, Maxwell's equations and boundary conditions important for analysis of interconnects are reviewed. Methods of calculating inductance and capacitance are summarized; one example is given for inductance calculation. Fundamentally important electromagnetic field concepts related to inductance and capacitance are studied.

3.1 Maxwell's Equations

All classical electromagnetic phenomena are governed by a compact and elegant set of fundamental rules known as *Maxwell's equations* [11][28]. Maxwell's equation are based on three experimentally established facts, namely Coulomb's law, Ampère's law (or the Biot-Savart law), Faraday's law, and the principle of conservation of electric charge. The physical meaning of the equations is better perceived in the context of their integral forms, which are listed below. The physical quantities that appear are the electric field $\bar{\mathcal{E}}$, the

magnetic flux density $\bar{\mathcal{B}}$, the electric flux density $\bar{\mathcal{D}}$, the magnetic field intensity $\bar{\mathcal{H}}$, electric current density $\bar{\mathcal{J}}$, and electric charge density $\tilde{\rho}$.

1. Faraday's law is based on the experimental fact that time-varying magnetic flux induces an electromotive force:

$$\oint_C \bar{\mathcal{E}} \cdot d\mathbf{l} = -\int_{S_C} \frac{\partial \bar{\mathcal{B}}}{\partial t} \cdot d\mathbf{s} \tag{3.1}$$

   where the contour C encloses the surface S_C and the sense of the line integration over the contour C (i.e., the direction of $d\mathbf{l}$) must be consistent with the direction of the surface vector $d\mathbf{s}$ in accordance with the so-called right-hand rule.

2. Maxwell's second equation actually is Gauss's law which is a mathematical expression of Coulomb's law. Coulomb's law states the experimental fact that electric charges attract or repel one another with a force inversely proportional to the square of the distance between them.

$$\oint_{S_V} \bar{\mathcal{D}} \cdot d\mathbf{s} = \int_V \tilde{\rho} dv \tag{3.2}$$

   where the surface S_V encloses the volume V.

3. The third equation is a generalization of Ampère's law which states that the line integral of the magnetic field over any closed contour must equal the *total* current[1]

[1] The total current, $\bar{\mathcal{J}}_{total} = \bar{\mathcal{J}} + \frac{\partial \bar{\mathcal{D}}}{\partial t}$. The first term on the right hand side is the sum of the conduction current and the source current while the second term represents the displacement current.

enclosed by that contour:

$$\oint_C \bar{\mathcal{H}} \cdot d\mathbf{l} = \int_{S_C} \bar{\mathcal{J}} \cdot d\mathbf{s} + \int_{S_C} \frac{\partial \bar{\mathcal{D}}}{\partial t} \cdot d\mathbf{s} \tag{3.3}$$

This equation expresses the fact that time-varying electric fields produce magnetic fields. The first term on the right-hand side is the conduction-current whereas the second term is known as the displacement-current term. This equation is very important in understanding inductance related issues.

4. The last equation is based on the fact that there are no magnetic charges, hence magnetic field lines always close on themselves.

$$\oint_{S_V} \bar{\mathcal{B}} \cdot d\mathbf{s} = 0 \tag{3.4}$$

This equation is not completely independent for it can be derived from the Biot-Savart law [28].

The two constitutive relations $\bar{\mathcal{D}} = \epsilon\bar{\mathcal{E}}$ and $\bar{\mathcal{B}} = \mu\bar{\mathcal{H}}$ relate the $\bar{\mathcal{E}}$ and $\bar{\mathcal{B}}$ to medium-independent quantities, $\bar{\mathcal{D}}$ and $\bar{\mathcal{H}}$.[2] The current density $\bar{\mathcal{J}}$ is given by $\bar{\mathcal{J}} = \bar{\mathcal{J}}_{source} + \bar{\mathcal{J}}_c$ where $\bar{\mathcal{J}}_{source}$ represents the source currents from which magnetic fields originate, and $\bar{\mathcal{J}}_c = \sigma\bar{\mathcal{E}}$ is the conduction current, which flows in a conducting media ($\sigma \neq 0$) whenever there is an electric field present.

[2]See Sections 4.10 and 6.8 in [28] for the detailed discussion of electromagnetic fields in material media.

Maxwell equations can also be represented in the differential form which is shown below for the case of time-harmonic (sinusoidal steady-state) conditions:

$$\nabla \times \mathbf{E} = -j\omega \mathbf{B} \tag{3.5}$$

$$\nabla \cdot \mathbf{D} = \rho \tag{3.6}$$

$$\nabla \times \mathbf{H} = \mathbf{J} + j\omega \mathbf{D} \tag{3.7}$$

$$\nabla \cdot \mathbf{B} = 0 \tag{3.8}$$

The $\mathbf{E}$, $\mathbf{D}$, $\mathbf{H}$, $\mathbf{B}$, ρ are complex phasors that do not vary with time.

3.2 Boundary Conditions

Electromagnetic boundary conditions can be derived based on Maxwell equations. The following boundary conditions are vital in understanding and solving capacitance and inductance problems.

1. $\bar{\mathcal{E}}_{1t} = \bar{\mathcal{E}}_{2t}$, where $\bar{\mathcal{E}}_{1t}$ and $\bar{\mathcal{E}}_{2t}$ are the tangential components of the electric field $\bar{\mathcal{E}}$ at two adjoining surfaces.

2. $\bar{\mathcal{H}}_{1t} = \bar{\mathcal{H}}_{2t}$, where $\bar{\mathcal{H}}_{1t}$ and $\bar{\mathcal{H}}_{2t}$ are the tangential components of the magnetic field $\bar{\mathcal{H}}$. However, if surface currents ($\bar{\mathcal{J}}_s$) exist, such as at the surface of a perfect conductor (i.e., $\sigma = \infty$): $\hat{\mathbf{n}} \times \bar{\mathcal{H}}_1 = \bar{\mathcal{J}}_s$ The field inside the perfect conductor is zero.

3. $\bar{\mathcal{D}}_{1n} - \bar{\mathcal{D}}_{2n} = \tilde{\rho}_s$, where $\bar{\mathcal{D}}_{1n}$ and $\bar{\mathcal{D}}_{2n}$ are the normal components of electric flux density

$\bar{\mathcal{D}}$ across the interface. $\tilde{\rho}_s$ is the surface charge that exists on the interface.

4. $\bar{\mathcal{B}}_{1n} = \bar{\mathcal{B}}_{2n}$, where $\bar{\mathcal{B}}_{1n}$ and $\bar{\mathcal{B}}_{2n}$ are the normal components of magnetic field $\bar{\mathcal{B}}$ across the two regions.

The direction of the normal vector across the boundary is defined by the unit vector $\hat{\mathbf{n}}$ which is perpendicular to the interface and directed outward from medium 2.

3.3 Inductance Calculation

3.3.1 Inductance Definition

Inductance is a single measure of the distribution of the magnetic field near and inside a current-carrying conductor. It is a property of the physical layout of the conductor, and is a measure of the ability of that conductor to *link magnetic flux*, or store magnetic energy.

Consider two neighboring closed loops C_1 and C_2 as shown in Fig. 3.1. If a current I_1 flows around the closed loop C_1, a magnetic field $\mathbf{B}_1$ is produced, and some of this magnetic field links with C_2. This magnetic flux, produced by the current I_1 flowing around C_1, is linked by the area S_2 enclosed by C_2 and can be designated as

$$\Psi_{12} = \int_{S_2} \mathbf{B}_1 \cdot d\mathbf{s}_2$$

If C_1 and C_2 consist of single turn respectively, the mutual inductance M_{12} is defined as [28]

$$M_{12} = \frac{\Psi_{12}}{I_1}$$

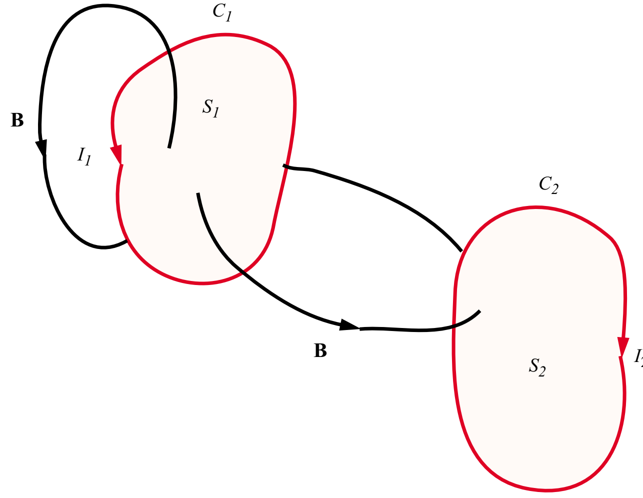


Figure 3.1: Magnetically coupled two circuit loops.

The magnetic flux produced by I_1 links the area S_1. So the *self-inductance* is defined as

$$L_{11} = \frac{\Psi_{11}}{I_1}$$

where $\Psi_{11} = \int_{S_1} \mathbf{B}_1 \cdot d\mathbf{s}_1$. The *Neumann formula* [28] shows that

$$M_{12} = \frac{\mu_0 N_1 N_2}{4\pi} \oint_{C_1} \oint_{C_2} \frac{d\mathbf{l}_1 \cdot d\mathbf{l}_2}{R} \tag{3.9}$$

which indicates that $M_{12} = M_{21}$ since the dot product is commutative and the order in performing the line integrals can be interchanged. N_1 and N_2 are the number of turns in the loops C_1 and C_2, respectively.

The self-inductance of a loop or circuit depends on the geometrical shape and the physical arrangement of the conductors that constitute the loop or circuit, as well as the permeability of the medium. For a linear medium, self-inductance does not depend on the current

in the loop or circuit. As a matter of fact, it exits regardless of whether the loop or circuit is open or closed, or whether it is near another loop or circuit. The *Neumann formula* for mutual inductance underscores the fact that the mutual inductance is only a function of the geometrical arrangement of the conductors and the medium [11].

3.3.2 Methods of Inductance Calculation

Although the inductances and mutual inductances of circuit elements, which are not associated with magnetic materials, are independent of the value of the current and dependent only on the geometry of the system[3], it is only for the simplest cases that these values can be calculated exactly. There are essentially four methods to calculate inductances.

1. The most direct method for calculating inductances is based on the definition of inductance and flux linkages. By the Biot-Savart law, the magnetic field dB, due to a differential current dI, at any point P of the field can be calculated.[4] Taking the integral of the entire current loop, the total B field at point P can be obtained. Take another integral over the surface enclosed by the current loop to calculate the magnetic flux, which is further divided by the current to finally get the inductance for the current loop. The magnetic flux that links a contour C may also be expressed

[3] Inductance frequency dependence will be discussed in Section 3.3.4

[4] The Biot-Savart law states: the $\mathbf{B}$ field vector at any point P identified by the position vector $\mathbf{r}$, due to a differential current element $Id\mathbf{l}'$ located at position $\mathbf{r}'$, is

$$d\mathbf{B_P} = \frac{\mu_0 I d\mathbf{l}' \times \hat{\mathbf{R}}}{4\pi R^2}$$

where $\hat{\mathbf{R}}$ is the unit vector pointing from the location of the current element to the field point P, and $R = | \mathbf{r} - \mathbf{r}' |$ is the distance between them. See [28].

in terms of the vector potential $\mathbf{A}$, where $\mathbf{B} = \nabla \times \mathbf{A}$ and

$$\Psi = \int_S \mathbf{B} \cdot d\mathbf{s} = \int_S \nabla \times \mathbf{A} \cdot d\mathbf{s} = \oint_c \mathbf{A} \cdot d\mathbf{l}$$

The last integral sometimes is more convenient to evaluate than $\int_s \mathbf{B} \cdot d\mathbf{s}$.[5]

2. Energy-based inductance calculation is another way to calculate the inductance of a circuit. The total energy W_m stored in a given steady-current configuration can be found by integrating $\mathbf{B}$ over the entire volume V that surrounds it:

$$W_m = \frac{1}{2} \int_V \frac{B^2}{\mu_0} dv$$

The inductance can be determined as the following:

$$L = \frac{2W_m}{I^2} \tag{3.10}$$

3. The Neumann formula Equation (3.9) is the most general expression for finding the mutual inductance but not as simple as that resulting from the use of the Biot-Savart law. For most cases it is not possible to perform the integrations. However, in such cases it is possible to obtain a numerical value or approximation by series expansions for specified cases.

4. Using some basic but fundamentally important inductance formulae is the fourth

[5]The last integral transform is based on Stokes's theorem.

method to calculate inductance. Based on these formulae and basic circuit theory (Kirchhoff's current and voltage laws), formulae for new circuit structures can be obtained. Taking the integral of a formula for a basic structure can also lead to a new inductance formula. For example, a formula for the mutual inductance of cylindrical current sheets may be derived by the integration of the formula for the mutual inductance of coaxial circles, along the cylindrical length. However, it is necessary to select a suitable formula in which the terms involve the variable of integration (e.g. a length) [24].

3.3.3 Partial Inductance Calculation

As is stated in the inductance definition, a current loop needs to be found in order to calculate inductance. However, in practice this may be difficult for IC chips where current loops are not easily identified. The so-called partial inductance concept [65] assumes that the return current for a filament is at infinity as shown in Fig. 3.2(a). Suppose one wishes to calculate the mutual inductance of the straight filaments AB and CD, for which the radii are much smaller than the length of the filaments. By constructing planes TT' and LL' which pass the ends of filament CD and are perpendicular to AB, the mutual inductance, due to current in filament AB, will be found by integrating $\mathbf{B}$ between these planes from CD out to infinity. The partial self-inductance can also be obtained.

Fig. 3.2(b) illustrates a calculation example where AB and CD are in parallel with the same length. In order to calculate the mutual inductance between AB and CD, the

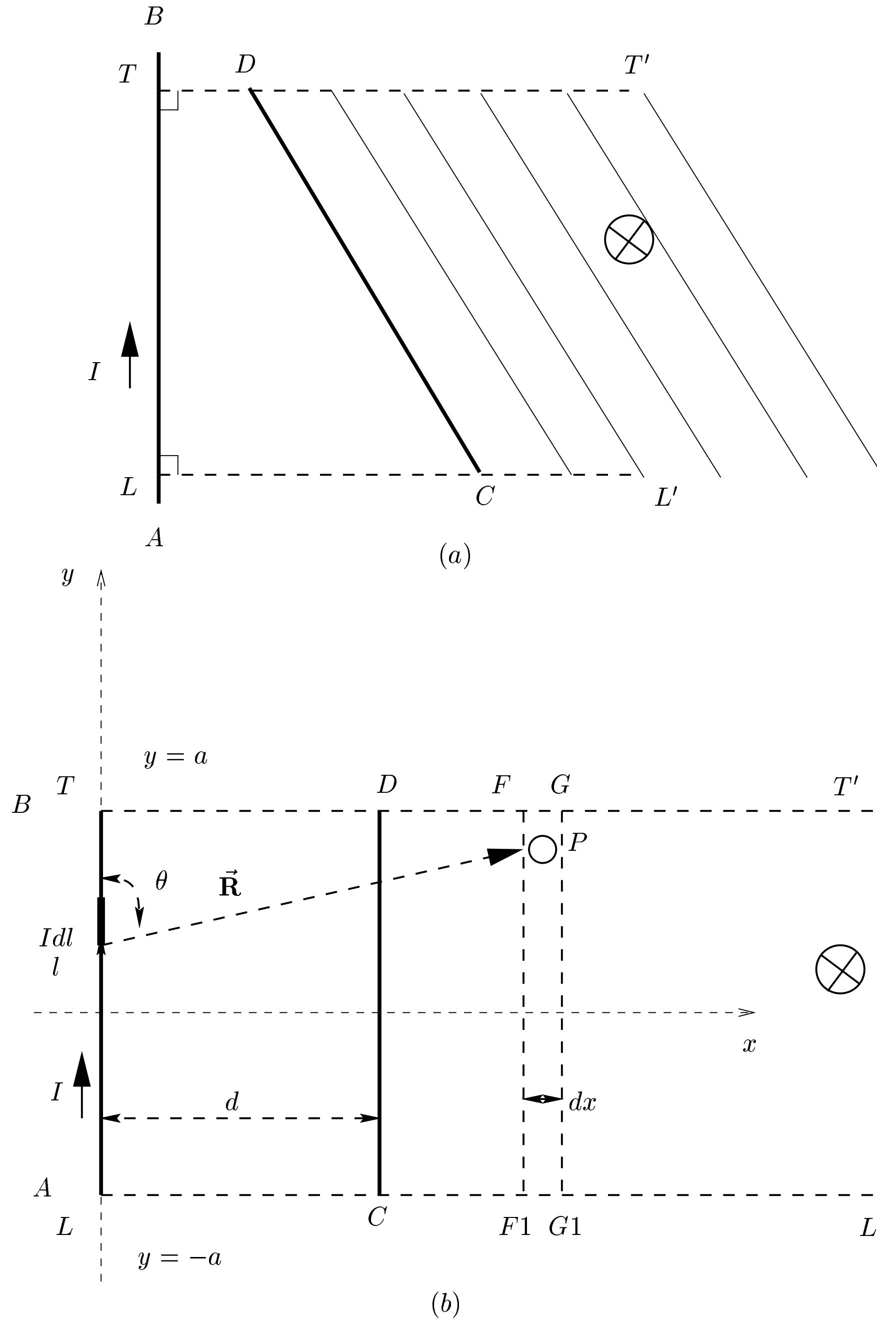


Figure 3.2: (a) The partial inductance concept. (b) Calculating of the mutual inductance of two parallel filaments with the same length assuming the return path is in the infinity.

Biot-Savart law can be used. Therefore, one has

$$d\mathbf{B_p} = \frac{\mu_0 I d\mathbf{l} \times \hat{\mathbf{R}}}{4\pi R^2} = \hat{\phi}\frac{\mu_0 I dl \sin\theta}{4\pi R^2}$$

First, choose the coordinates as shown in the figure so that the integral path l is from $y = -a$, to $y = a$ (the length of the filament is $2a$). Then

$$B_p(x,y) = \frac{\mu_0 I x}{4\pi}\int_{l=-a}^{a} \frac{dl}{[(y-a)^2 + x^2]^{3/2}} = \frac{\mu_0 I}{4\pi x}\left[\frac{y+a}{\sqrt{x^2 + (y+a)^2}} - \frac{y-a}{\sqrt{x^2 + (y-a)^2}}\right]$$

Next, take the integration along the Y axis,

$$\Psi_y = \int_{y=-a}^{a} B_p dy = \frac{\mu_0 I}{4\pi x}\left[-2\sqrt{x^2} + 2\sqrt{4a^2 + x^2}\right]$$

Then, take the integration along the X axis to get the mutual flux of AB on CD,

$$\Psi = \int_{x=d}^{\infty} \Psi_y dx = \frac{\mu_0 I}{4\pi} \times 2\left[\sqrt{4a^2 + x^2} - 2a \cdot \operatorname{atanh}\left(\frac{2a}{\sqrt{4a^2 + x^2}}\right) - x\right]_{x=d}^{\infty}$$

Finally, use $\operatorname{atanh}(z) = \frac{1}{2}\ln(\frac{1+z}{1-z})$, $|z| < 1$, and also let $l = 2a$ as the length of the filament, which results in the following expression:

$$M = \frac{\Psi}{I} = \frac{\mu_0}{4\pi} \times 2l\left[\ln\left(\frac{l}{d} + \sqrt{1 + \frac{l^2}{d^2}}\right) - \sqrt{1 + \frac{d^2}{l^2}} + \frac{d}{l}\right] \tag{3.11}$$

This method can be extended to calculate the self-inductance of a wire. If the integration of the **B** field is taken in the space between the TT' and LL' from the edge of the filament

AB to infinity, the external flux of the filament can be calculated, which corresponds to the external self-inductance. The result is the same as the mutual inductance case with r, the radius of the cross section of filament AB, in place of d in Equation (3.11). In addition, the magnetic flux inside of the cross section of a filament links the current of the filament, which corresponds to the internal inductance and must also be added to calculate the complete self-inductance of a filament. The internal inductance of a round wire[6] can be found in any electromagnetics textbook, which is of the form $\frac{\mu_0 l}{8\pi}$ [11]. The self-inductance of a filament with cross section radius of r is the sum of internal and external inductances:

$$L = \frac{\mu_0}{2\pi} \times l \left[\ln \left(\frac{l}{r} + \sqrt{1 + \frac{l^2}{r^2}} \right) - \sqrt{1 + \frac{r^2}{l^2}} + \frac{r}{l} + \frac{1}{4} \right] \tag{3.12}$$

Usually, internal inductance is quite small compared with external inductance. At high frequencies, currents tend to flow on the surface of conductors due to skin effects, internal inductance decreases. In the extreme case, internal inductance becomes zero at infinite frequencies.

3.3.4 Inductance Frequency Dependency

Frequency dependence of inductance results from the eddy currents in conductors, which are induced by the time-varying magnetic fields and governed by Faraday's law (Equation (3.1)). This varying magnetic field generates eddy currents inside of a conductor or other conductors nearby the current loop. The induced eddy currents flow in a direction that produces

[6]Uniform current distribution in the inner conductor of a wire is assumed. This assumption does not hold for high-frequency ac currents.

an opposing magnetic flux, which reduces the effective magnetic flux and therefore the inductance.

Skin and proximity effects result from eddy currents. In a conductor that is good but not perfect, an increasing magnetic field will penetrate the material to some extent. It will induce voltage, and current will flow; the current will automatically distribute itself in such a way as to weaken the magnetic field and prevent the field from penetrating further into the conductor. If this magnetic field is generated by the conductor itself, then the phenomena is called *"skin effect"*. If this magnetic field is generated by an adjacent time-varying current-carrying conductor, the phenomena is called *"proximity effect"* - regardless of whether the first conductor carries current or not [71]-[73]. Skin effects reduce wire inductance because of the reduction of the internal inductance of a conductor at high frequencies; proximity effects reduce wire inductance because currents in different conductors re-distribute themselves to form a smaller current loop at high frequencies[7] [72]. More generally, the skin-effect and proximity-effect eddy currents superimpose to form the total eddy current distribution [73].

If two conductors, parallel and close together, are carrying current in opposite directions, the current tends to concentrate at the nearer surfaces to minimize the current loop and resulting inductance [72]. In the case of a ground plane, the return current of a signal wire on the ground plane concentrates just beneath the signal wire at high frequencies to minimize the inductance loop due to eddy currents while at low frequencies, the current spreads out to minimize the resistance of the return paths on the ground plane as shown in Fig. 3.3.

[7] Fig. 3.3 can serve as a simple example.

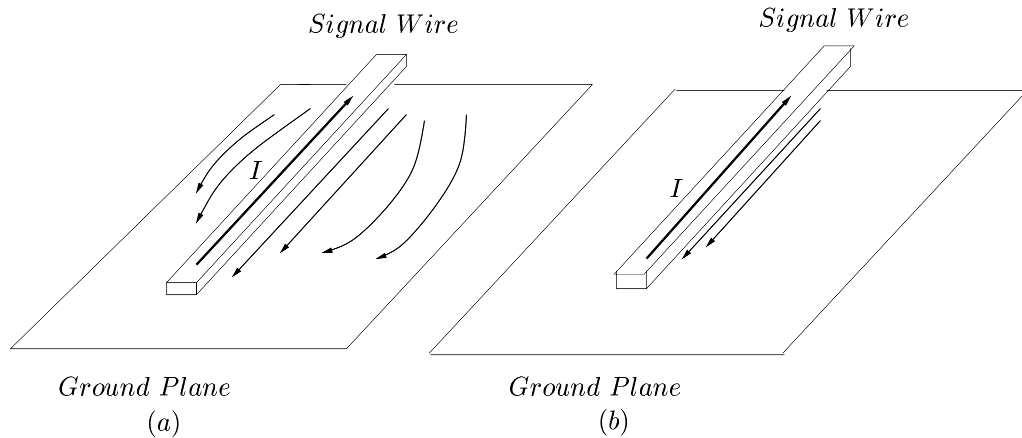


Figure 3.3: Ground plane return current (a) at low frequencies, and (b) at high frequencies.

Both skin and proximity effects increase resistance at high frequencies. Finally, it is worthwhile to point out that capacitance does not contribute to reducing inductance at high frequencies, but instead it reduces the composite impedance of equivalent circuits.

3.4 Capacitance Calculation

Capacitance is a measure of the ability of a conductor configuration to hold charge per unit applied voltage, or store electrical energy. Consider a two conductor system, where capacitance is defined as

$$C \equiv \frac{Q}{\Phi_{12}} = \frac{\oint_S \mathbf{D} \cdot d\mathbf{s}}{-\int_L \mathbf{E} \cdot d\mathbf{l}}$$

and Φ_{12} represents the voltage difference between the two conductors, S is any surface enclosing the positively charged conductor and L is any path going from the negative to the positive conductor. The capacitance is a physical property of the two-conductor system. It depends on the geometry of the conductors and on the permittivity of the medium between

them.

Capacitance of two conductors can be calculated by either (1) assuming charges $+Q$ and $-Q$ on conductors, and determining Φ_{12} in terms of Q, or (2) assuming a Φ_{12} and determining Q in terms of Φ_{12}. In the first method, Gauss's law is used to calculate $\mathbf{E}$ from Q,[8] and by performing integration along any path between the two conductors, Φ_{12} can be calculated. In the second method, Poisson's equation or Laplace's equation may be used to calculate spatial potential Φ. Applying the boundary conditions, $\mathbf{E}$ and Q can be obtained [28] [11]. To numerically solve 3-D capacitance problems, finite difference [83], finite element [75], boundary element or multipole-accelerated boundary element methods [51][50] are widely used. To achieve quick estimations, analytical formulae are also used in design and analysis [3].

In the regime below the tens of gigahertz range or at higher frequencies, capacitance has little frequency dependency because of the charge equilibrium, dictated by the *relaxation time*, which occurs on order of 10^{-18} to 10^{-19} seconds for most metallic conductors [28].

[8]The surface charge density, $\rho_s = \epsilon\mathbf{E}$.

Chapter 4

VLSI On-Chip Interconnects

In this chapter, modeling of VLSI on-chip interconnects is presented. The importance of on-chip inductance extraction is introduced first. Then modeling of on-chip inductance using field solvers as well as analytical formulae is presented. As an important methodology in this thesis, the modeling results are compared with test chip measurement results. In the last part of this chapter, capacitance modeling for on-chip interconnects and other IC structures is also studied.

4.1 Introduction

At gigahertz frequencies, long interconnect wires exhibit transmission line behavior because of the fast rise/fall times of signals. With the application of wider wires, inductive impedance at high frequencies ($j\omega L$) becomes comparable to the resistive component (R) of the major signal wires and power/ground nets. For copper technology, this phenomenon

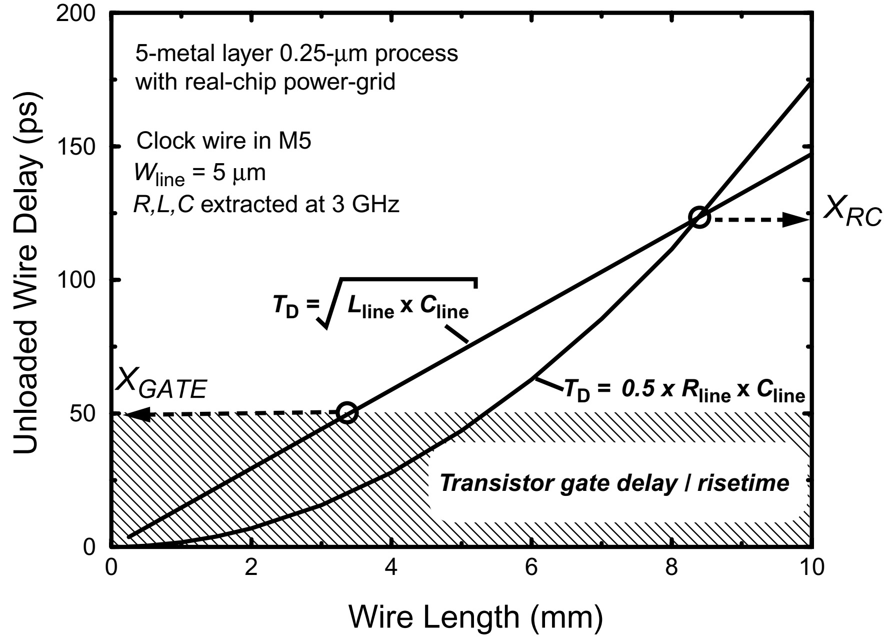


Figure 4.1: Wire delay for RC and LC delay models. X_{GATE} is the delay of a transistor gate. X_{RC} is the delay where RC delay and LC delay meets.

becomes even more prominent. The parasitic inductance can cause additional signal delays, over-shoot waveforms, and increased ground bounce problems. Also, inductive crosstalk can no longer be ignored. For high speed microprocessors and ASICs, clock trees and power/ground grids need to be designed carefully to avoid large clock skew, signal inductive coupling and ground bounce [60, 61, 67]. Inductive effects have been demonstrated in 4 mm long wires in a 0.25 μm process [36]. The extracted RC and $\sqrt{LC}$ delays of a typical clock wire from this test chip are shown in Fig. 4.1 [55]. While the $\sqrt{LC}$ delay is a linear function of wire length, the RC delay increases with the square of the wire length. As a result, the inductive effects become more prominent for wires with intermediate lengths (e.g. 3 to 8 mm for signal frequency around 3 GHz as shown in Fig. 4.1). Similar results are demonstrated when the driver and load of the wires are included [18]. The inductive

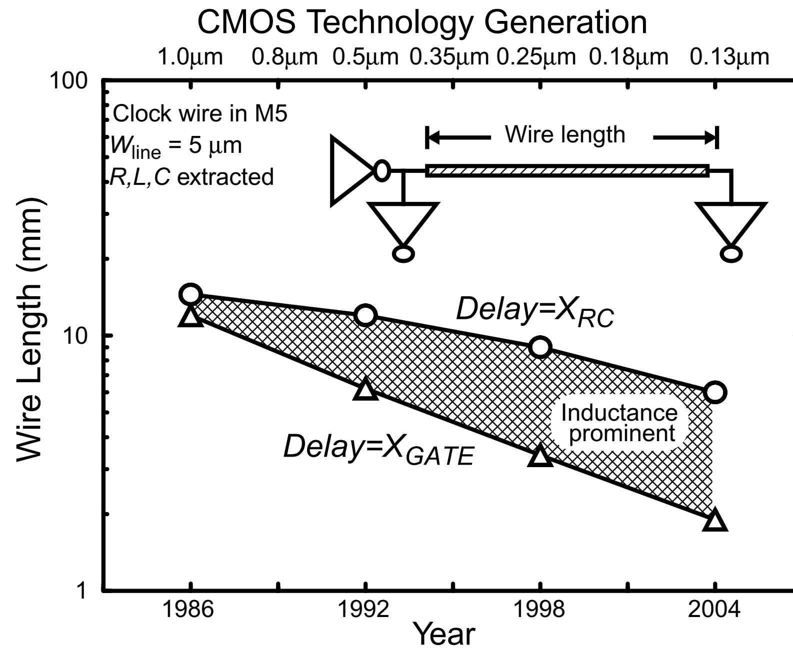


Figure 4.2: Inductive effects vs. technology scaling. As technology advances, the wire length range where inductance is important becomes larger.

effects for the buses with intermediate length as well as local clocks must be considered. As technology is scaled, the gate delay will continue to be reduced while the signal delay of short, low-resistive clock wires remains constant. The inductive effects will therefore affect progressively shorter wires as illustrated in Fig. 4.2 [55]. Fig. 4.3 shows the simulated crosstalk due to inductance effects. Larger coupling and ringing are observed when inductive coupling is included in the simulation.

Currently, the inductive effects are only considered for a few global clock wires and major signal buses. This is insufficient for future designs because of higher clock frequencies and faster signal rise/fall times. Although 3-D electromagnetic full wave field solvers are available, they do not have the capacity to manage the complexity of today's integrated circuits and are too computationally expensive. To model the inductive effects of

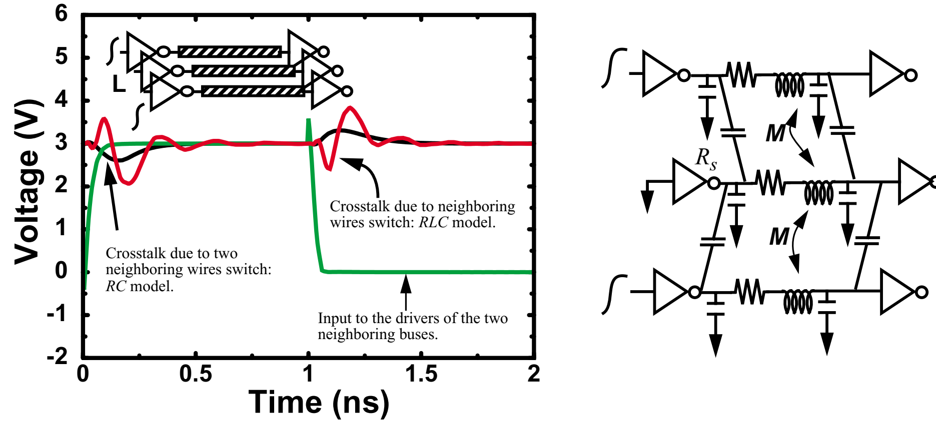


Figure 4.3: Inductance effects on crosstalk. The middle bus remains high (its driver keeps low) while the two neighboring buses switch at the same time from high to low and low to high. Crosstalk is seen at the end of the middle bus. Buses are 9.6 μm wide with spacing 1.6 μm on metal layer four.

intermediate-length buses as well as local clocks, a fast automated inductance extraction and verification tool is needed. In this chapter, an efficient 3-D modeling method is presented which captures 3-D geometry effects directly from the layout design and process technology information. Electromagnetic field solvers are used to extract inductance based on the 3-D geometric modeling and to provide the "golden standard" results for calibration. Analytical formulae are derived to estimate inductance in order to establish guidelines for circuit design. Test chips [36] have been used to characterize the high frequency behavior of on-chip interconnect structures. Simulation and analytical formula results are then compared with these measured data. In Section 4.2, geometry generation for inductance extraction using field solvers is introduced. Derivation of analytical formulae for inductance calculations is presented in Section 4.3. In Section 4.4, experimental data of two test chips and modeling results based on analytical formulae and field solvers are compared. Detailed analysis of these data is presented. Conclusions for inductance modeling are summarized

in Section 4.5. Capacitance modeling is finally presented in Section 4.6.

4.2 Layout-Based 3-D Geometry Modeling and Inductance Extraction Using Field Solvers

As is seen in electromagnetic theory, a wire inductance is determined by the wire geometry and its surrounding wire configuration. Accurate and automatic 3-D geometry modeling is essential for chip level inductance modeling with field solvers. The inductance values extracted from the field solvers can then be used as a "golden standard" for comparison with simplified analytical inductance estimations. Layout-based 3-D geometry extraction combines 2-D information from the layout design (e.g. using the GDS II format) with the layer thicknesses and other material parameters coming from the actual fabrication process. In addition to the geometry information which is needed for capacitance extraction, inductance extraction often requires the user to choose the net for extraction and identify the ports. Electromagnetic simulators such as FASTHENRY [33] can then be used to extract the inductance for each 3-D structure.

4.2.1 Geometry Modeling Based on Arcadia Database

The 3-D geometry modeling tool has been developed based on layout design and process information stored in the data base of Arcadia - a Synopsys extraction tool. Layout design and process technology files are used to generate Arcadia data base which essentially represents the layout with trapezoids. Fig. 4.4 shows the program flow chart. The user first

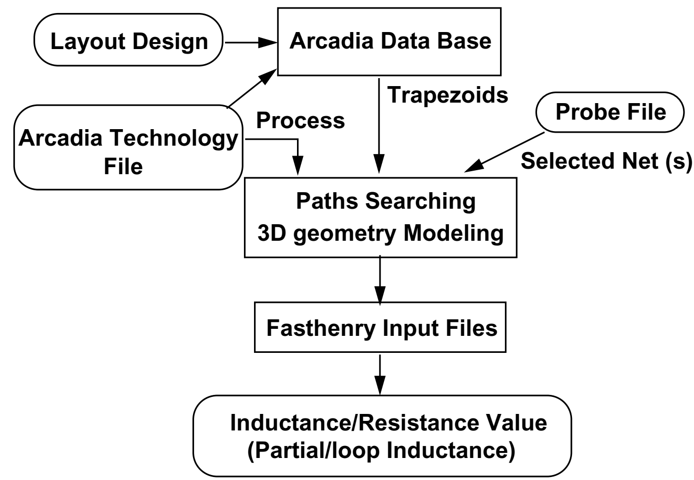


Figure 4.4: Program flow chart

chooses the net for inductance extraction and identifies the ports. Combined with process technology information, such as layer thickness and layer separation from the substrate, 3-D geometries of these nets which are suitable for inductance field solver, e.g., FASTHENRY, are constructed from the Arcadia data base.

Path Searching in 3-D Geometry Modeling

Geometry data consists of numerous trapezoids for each selected net. Electrical connection information, i.e., vias/contacts and equipotential edges, is also stored in the data base. Automatic path searching is required to construct 3-D geometries of the selected nets since each net usually includes many branches. The data structure is designed to facilitate the searching process which is a depth-first search [57].

Fig. 4.5 shows the search process used to find a net which has segment 1 and segment 10 as its ports. The algorithm identifies the trapezoids where the ports are located. Then it starts with segment 1, and does a depth-first search and constructs a tree as shown in

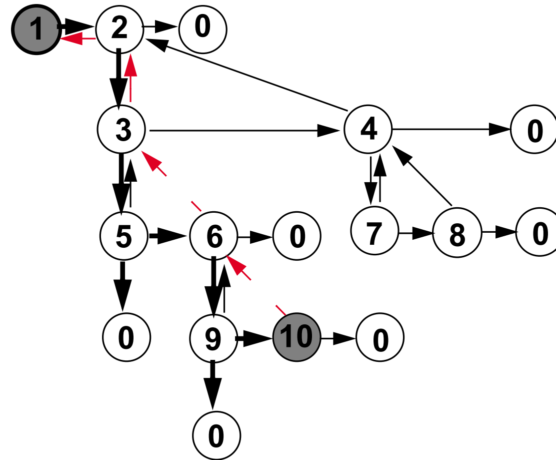


Figure 4.5: Path searching in 3-D geometry modeling.

Fig. 4.5 (thicker arrows). If the segment is the destination port of the net, the program stops; otherwise, it continues searching on another branch. This process continues until the second port is found. To build the entire path, the algorithm traces back (dashed arrows) to complete the path construction. Multi-nets/ports can be processed together in order to find the mutual inductance of different nets.

Examples of generated 3-D geometries

The program generates input files for field solvers such as FASTHENRY for inductance extraction. Because of proximity effects at high frequencies, a window enclosing the extracted nets can be defined which is bounded by nearest power/ground wires. Current return paths of the nets are assumed to be through these power/ground wires. Therefore, loop inductance as well as partial inductance can be extracted. Fig. 4.6 shows extracted 3-D geometry from a commercial chip which includes two signal wires and nearby ground wires. A wire of length of about 2.82 mm and width of 1.2 μm in this commercial chip has partial inductance

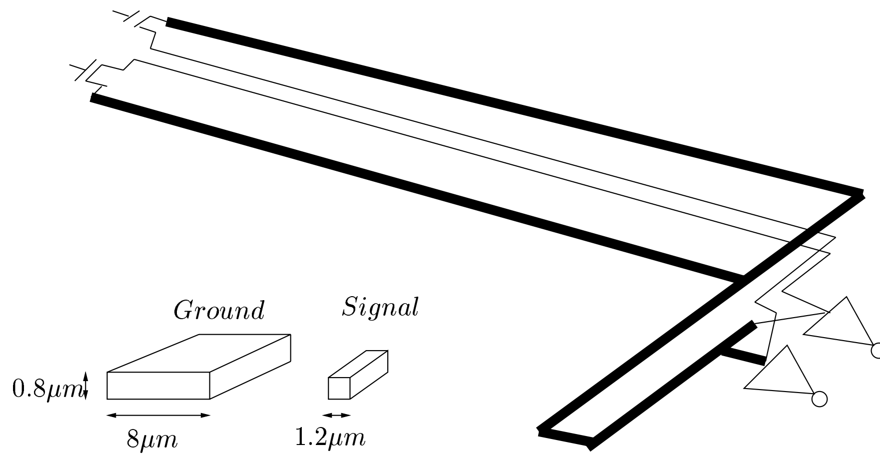


Figure 4.6: 3-D geometry of two loops extracted from a commercial chip.

4.67 nH and loop inductance 5.7 nH (with nearby ground wire width of 8 μm). The mutual (loop) inductance with one of its neighboring loop is 2.26 nH. Fig. 4.7 shows an example of the test chip layout and the extracted 3-D geometry where ground grids and signal wires are modeled. This 3-D geometry is ready for electromagnetic simulation tools [55].

4.3 Analytical Formulae for Inductance Estimation

Although accurate inductance estimation based on field solver results is desirable, it is time consuming and memory intensive. It is therefore not practical to extract the inductance for a whole chip with this method. Instead, analytical formulae are very desirable to provide design guidelines, as well as for screening and identifying nets with significant inductance for chip design and analysis. In this section, based on electromagnetic field theory, analytical formulae for self- and mutual inductance of wires and some typical interconnect structures including the coplanar waveguide are derived. These formulae, presented in Sections 4.3.1

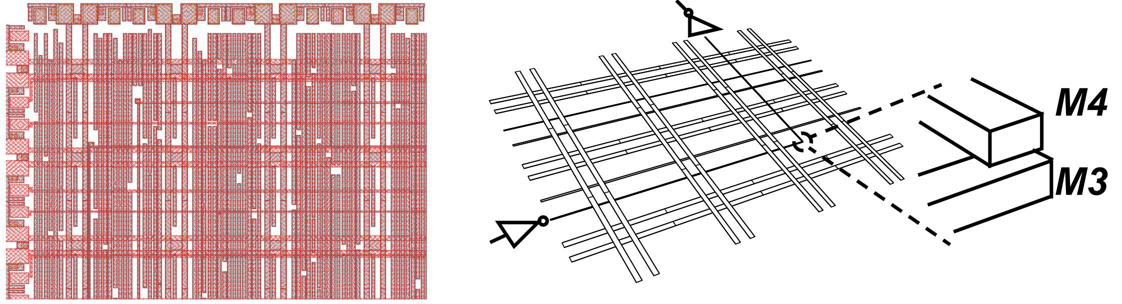


Figure 4.7: Extracted 3-D geometry with signal and power/ground wires from a test chip. A corner of metal 4 and metal 3 are magnified to demonstrate the 3-D effect. Driver and receiver are added for illustration.

and 4.3.2 are based on the assumption that the return path of each wire is at an infinite distance (from the wire) as it is stated in PEEC method [65]; while the formulae for the coplanar waveguide in Section 4.3.5 consider a loop inductance in which current returns from the two adjacent ground wires.

4.3.1 Analytical Formulae for Self- and Mutual Inductance

Self-inductance of a wire with a rectangular cross section can be derived using electromagnetic field theory and the geometry mean distance approximation (G.M.D.)[64].

$$L_{self} = \frac{\mu_0 l}{2\pi}[\ln(\frac{2l}{w+t}) + \frac{1}{2} + 0.2235\frac{w+t}{l}] \tag{4.1}$$

Equation (4.1) is for the self-inductance when $l \gg (w+t)$ (e.g. l is $10\times$ larger) where l is the length of the wire, and parameters w and t are the width and height of the rectangular

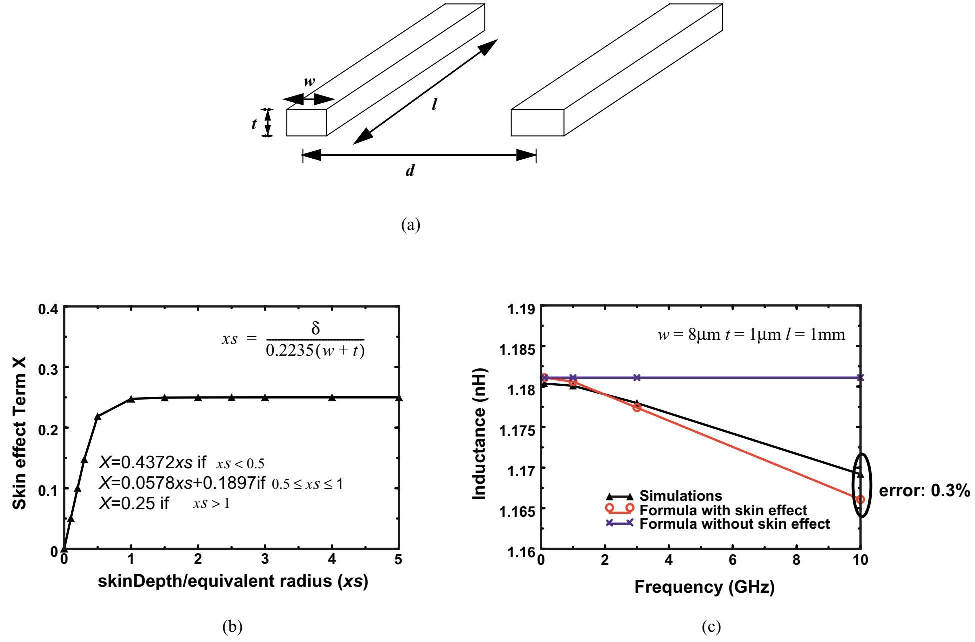


Figure 4.8: (a) Parameters in inductance formulae. (b) Fitted skin effect term, X. δ is the skin depth. (c) Comparison from the revised formula with the skin effect term.

cross section, respectively. Mutual inductance between two parallel wires with equal length can be obtained from Equation (3.11) by assuming $l/d \gg 1$,

$$M = \frac{\mu_0 l}{2\pi}[\ln(\frac{2l}{d}) - 1 + \frac{d}{l}] \tag{4.2}$$

where d is the center-to-center distance, l the length, and $l \gg d$ (e.g. l is $5 \sim 10\times$ larger than d) as shown in Fig. 4.8(a). The self-inductance is a nonlinear function of l, which means that it is not directly scalable with respect to length. In fact, it is superlinear when $l > (w + t)$.

To consider the skin effect, a frequency dependent term is added, as shown in Equation (4.3), which can be represented by a Bessel function [64] and is curve-fitted as shown

in Fig. 4.8(b) where $\delta = \frac{1}{\sqrt{\pi\sigma f\mu}}$ is the skin depth of the material at a particular parameter set where f is frequency, σ is the conductivity and μ is the permeability of the metal layer. X is a fitted parameter, and μ_r is the relative permeability of the conductor. All other parameters are the same as in Equation (4.1).

$$L_{self} = \frac{\mu_0 l}{2\pi}[\ln(\frac{2l}{w+t}) + \frac{1}{2} + 0.2235\frac{w+t}{l} - \mu_r(0.25 - X)] \tag{4.3}$$

Fig. 4.8(c) plots the comparison between simulations and values computed using the formulae, both with and without including skin effect. Equation (4.3) accurately captures the skin effect, though the frequency dependency is not large. The error falls within 1% for widths between 1 μm to 50 μm.

4.3.2 Mutual Inductance of Two Parallel Wires with Unequal Length

To calculate wire inductance in a complex wiring environment or where self-inductance consists of several cascaded segments in sequence, the mutual inductance formulae of two parallel wires with unequal lengths need to be derived. There are six different basic positions of two parallel wires which result in different mutual inductance formulae. Fig. 4.9 illustrates these different cases; parameters l, m, p, q and s represent the wire lengths as well as wire overlap lengths. Parameter d is the center-to-center separation between two wires.

If the dimension of the wire length is much smaller than the wavelength of the signal for the frequencies of interest, magnetic induction at every point of the electromagnetic field is in phase with the current. This condition can be satisfied for wires on current integrated

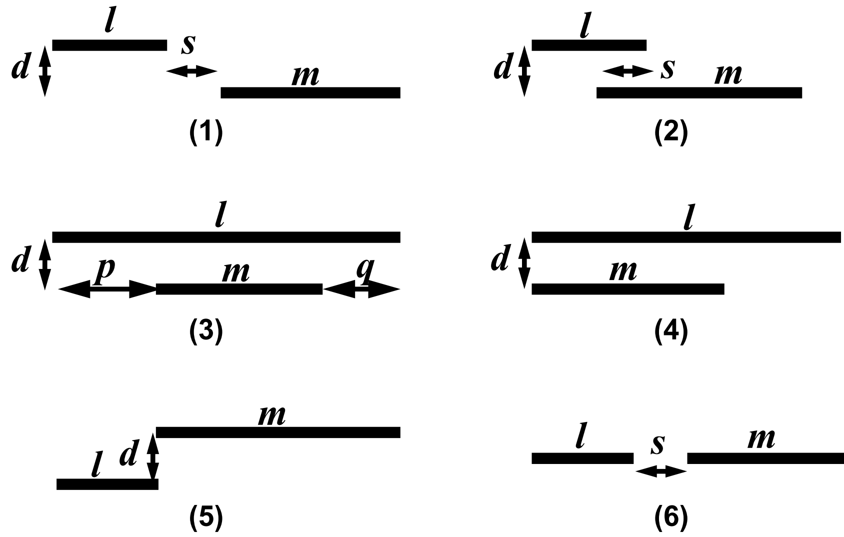


Figure 4.9: Six relative positions for mutual inductance. Wires in each case can be on the same layer or on different layers.

circuits at gigahertz frequencies (1 GHz in SiO_2 yields a wavelength of 15 cm which is much larger than the typical chip dimensions.) The induced electromotive forces are in phase at all points. The magnetic flux linked with an interconnect may be considered as the summation of the fluxes, in phase under quasi-stationary conditions, contributed by the separate elements of the inducing circuit. As a result, the mutual inductance of a wire with the inducing wires is the algebraic sum of all mutual inductances of the separate elements of the inducing wires. For example, the mutual inductance of the two wires in Case 4 can be calculated as,

$$M = \frac{1}{2}[(M_l + M_m) - M_{l-m}] \tag{4.4}$$

where M_l represents the mutual inductance of the two parallel wires with equal length of l and separation of d. The other mutual terms can be determined in an analogous manner. Mutual inductance approximations are summarized in Table 4.1. Six formulae can further

be derived as shown in Table 4.2[1] where l, m, d, p, q are as indicated in Fig. 4.9. Wires for which the lengths are greater than the wavelength can be partitioned into several segments so that mutual inductance can be calculated.

Table 4.1: Mutual Inductance Approximation

Case 1:	$M = \frac{1}{2}[(M_{l+m+\delta} + M_\delta) - (M_{l+\delta} + M_{m+\delta})]$, $s \neq 0$
Case 2:	$M = \frac{1}{2}[(M_{l+m-\delta} + M_\delta) - (M_{l-\delta} + M_{m-\delta})]$, $l \neq s$, $m \neq s$, $d \neq 0$
Case 3:	$M = \frac{1}{2}[(M_{m+p} + M_{m+q}) - (M_p + M_q)]$, $d \neq 0$, $p \neq 0$, $q \neq 0$
Case 4:	$M = \frac{1}{2}[(M_l + M_m) - (M_{l-m})]$, $l \neq m$, $d \neq 0$
Case 5:	$M = \frac{1}{2}[M_{l+m} - (M_l + M_m)]$

Table 4.2: Mutual Inductance Formulae

Case 1, 6:	$M = \frac{\mu_0}{4\pi}[(l+s)\ln(\frac{l+m+s}{l+s}) + m\ln(\frac{l+m+s}{m+s}) + s\ln(\frac{s}{m+s})]$, $s \neq 0$
Case 2:	$M = \frac{\mu_0}{4\pi}[(l-s)\ln(\frac{l+m-s}{l-s}) + m\ln(\frac{l+m-s}{m-s}) + s\ln(\frac{4s(m-s)}{d^2}) - 2s]$, $l \neq s$, $m \neq s$, $d \neq 0$
Case 3:	$M = \frac{\mu_0}{4\pi}[m\ln(\frac{4(m+p)(m+q)}{d^2}) + p\ln(\frac{m+p}{p}) + q\ln(\frac{m+q}{q}) - 2m]$, $d \neq 0$, $p \neq 0$, $q \neq 0$
Case 4:	$M = \frac{\mu_0}{4\pi}[l\ln(\frac{l}{l-m}) + m\ln(\frac{4m(l-m)}{d^2}) - 2m + d]$, $l \neq m$, $d \neq 0$
Case 5:	$M = \frac{\mu_0}{4\pi}[l\ln(\frac{l+m}{l}) + m\ln(\frac{l+m}{m}) - d]$

Fig. 4.10 shows the comparison of the model, for Case 4, with the field solver simulations. The formula gives an accurate estimation for reasonable separation distances. When the distance becomes comparable to the wire length, the formulae underestimate the mutual inductances. For on-chip interconnects, wires are usually thin and long compared to their separation in the simulation window. Therefore, it does not result in appreciable errors.

[1] The formula for case 6 was given by [64].

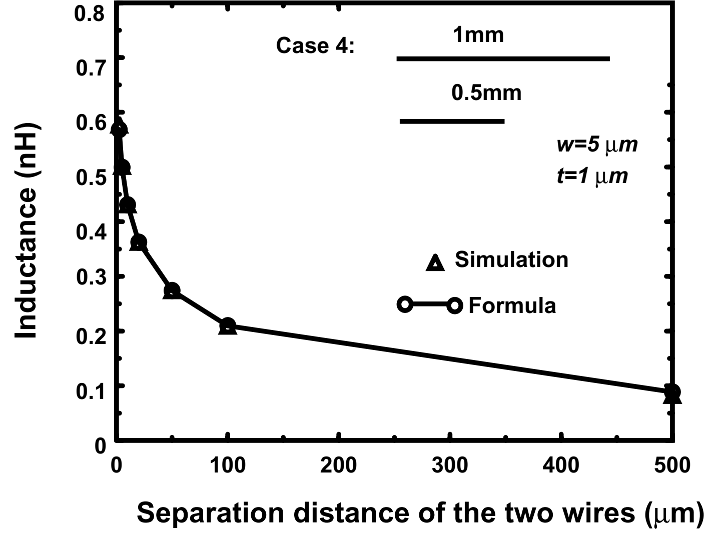


Figure 4.10: Formula and simulation comparison for mutual inductance of Case 4.

Case 1 and Case 6 share the same formula and their mutual inductances usually are negligible because the magnetic flux linking one to the other is very small. For Case 5, if $d = 0$, it represents the situation in which two wires touch each other.

4.3.3 Calculation of Self-Inductance of an Entire Wire

If a wire consists of several segments, the self-inductance of the entire wire does not equal the sum of the self-inductances of its segments; the existence of mutual inductance among segments of the wires must be considered. The self-inductances of all segments as well as mutual inductance between these segments are required to compute the entire wire inductance. It can be shown, using circuit theory, that the inductance of an entire wire constructed by several cascaded segments is as follows:

$$L_{self} = \sum_{i=1}^{N} l_i + \sum_{i=1}^{N} \sum_{j=i+1, j \leq N}^{N} 2k_{ij} M_{ij} \tag{4.5}$$

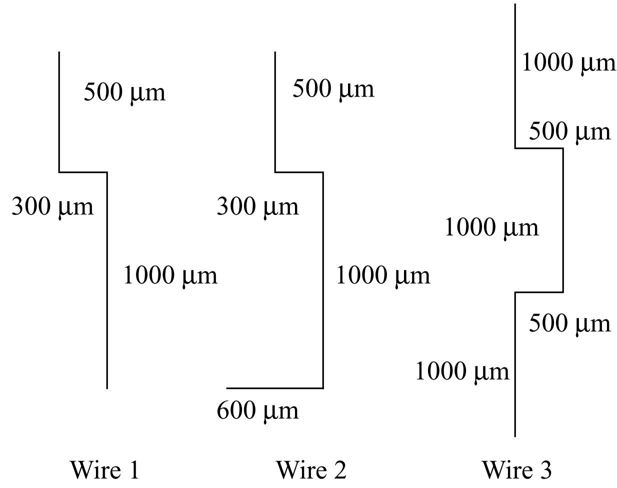


Figure 4.11: Three typical wire structures.

where N is the number of segments. l_i is the self-inductance of segment i. The parameter M_{ij} is the mutual inductance between segments i and j. Term $k_{ij} = 0$ when segment i and j are orthogonal; $k_{ij} = 1$ when i and j have same current direction; $k_{ij} = -1$ when i and j have opposite current directions. Table 4.3 shows that the results of inductance calculations using these formulae are very close to the field solver simulation results for three typical wire structures which are shown in Fig. 4.11.

Table 4.3: Simulation and calculation of self-inductance at 3 GHz

	Wire1: 3 segments and total length of 1.8 mm	Wire1: 4 segments and total length of 2.1 mm	Wire1: 5 segments and total length of 4 mm
Simulation	2.27	2.93	5.35
Formulae	2.26	2.86	5.17
Error	0.4%	2.3%	3.4%

4.3.4 Application of Inductance Calculation for Circuit Simulation

For on-chip long thin wires, self-inductance of a wire is solely determined by wire geometry, and mutual inductance of two wires is solely determined by geometries of the two wires and their spacing.[2] Therefore, the formulae developed above can be used to calculate self-/mutual inductance for RLC interconnect modeling and circuit simulations to investigate inductive effects as well as power/ground noise. Self-inductance of global wires, power wires and ground wires and mutual inductance between these wires can be calculated using the derived formulae. Capacitance and resistance can also be quickly calculated using the lookup table or field solvers. Fig. 4.12 shows one global wire (4 mm long and 5 μm wide) and two nearest power/ground wires (10 μm wide) within a selected window.[3] Fig. 4.13 shows the simulation of the signal at the output of the receiver for a global wire. The overshoots are clearly observed with inductance effects included. These inductive effects may increase signal skews and accidently turn on/off transistors causing false logic states to occur. Fig. 4.14 shows the power noise and ground bounce when power/ground inductive effects are included in circuit simulation. Corrective measures must be taken to avoid possible circuit failure, such as moving global wire closer to ground/power wires and using C4 bumps for power/ground wires[4].

[2] In a more complicated wiring environment – for example densely populated grids or ground plane – one needs to consider the environment which will be discussed in the later section.

[3] The case was proposed by HP Labs.

[4] C4 is a packaging technique developed by IBM. An area array of solder balls are used to attach a chip to a package. A chip's aluminum bond pads are processed with additional metal layers to allow adhesion of solder balls to pads. Solder balls have the advantages of very low inductance and the ability to form contacts with pads located over the entire area of the chip, not just the periphery - especially good for power distribution.

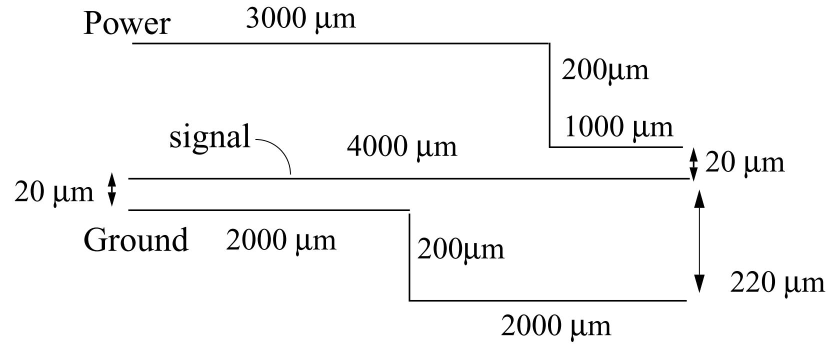


Figure 4.12: One global wire and two power/ground wires.

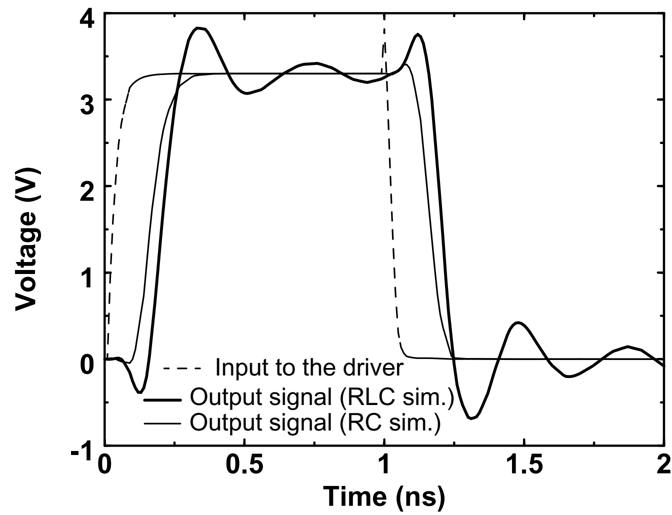


Figure 4.13: Signal wave forms at the output of the receiver: ringing effects with *RLC* simulation.

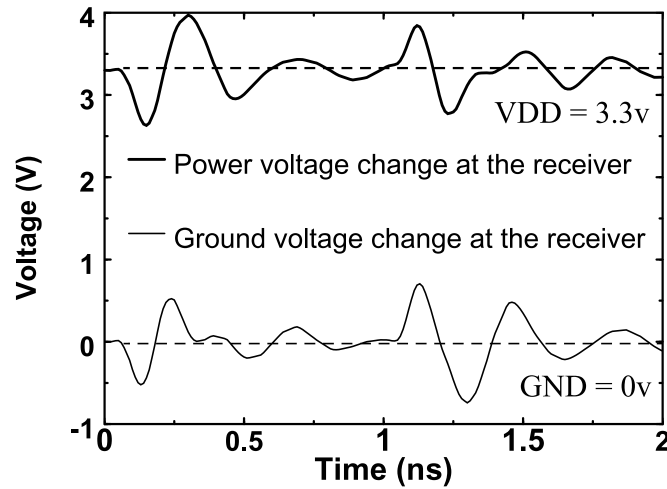


Figure 4.14: Power and ground noise observed with *RLC* simulation.

4.3.5 Analytical Formulae for Coplanar Waveguide Structure

For on-chip interconnects, one can always find the nearest ground or power wires for each signal wire because of ground/power grids which provide most of current returns. The coplanar waveguide structure is a very good approximation to most of these cases. Also the coplanar waveguide structure is frequently used as a shielding technique for critical clock and signal wires. Hence, it is necessary to study the inductance effects of coplanar waveguide structures to have a better understanding of on-chip inductance issues. In a coplanar waveguide, the signal wire is sandwiched between two ground wires (or more generally power/ground wires, since power wires are also ac ground to the signal wire) on the same layer. The electromagnetic fields are confined between the signal and ground wires. Current flows through the signal wire and returns from the two ground wires, see Fig. 4.15. In the real ground grids, two ends of the ground wires at the far end are electrically connected via a grid wire, while two ends of the ground wires at the near end are also electrically

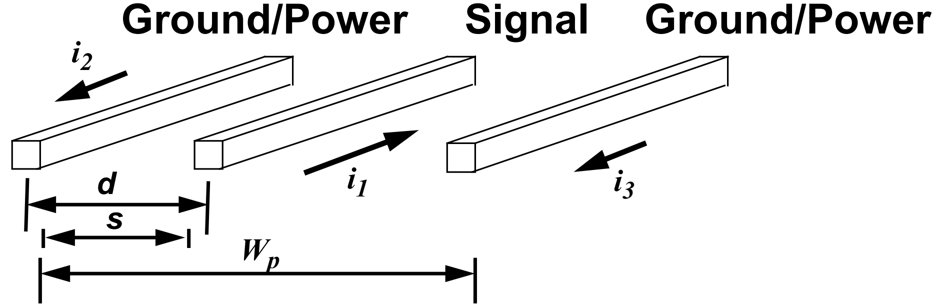


Figure 4.15: Coplanar waveguide structure: d is the center-to-center separation distance of the signal wire and the nearer ground/power wire. W_p is the ground/power wire pitch. S is the edge-to-edge spacing between the signal wire and the nearer ground/power wire. Wire connections of the two ground wires at far-end and near-end are not shown for clarity.

connected.[5] The structure is considered as a transmission line whose inductance per length can be calculated. Analytical formulation is desirable in order to have quick inductance estimation and to establish design insights and guidelines. To derive the analytical formula for the inductance of this structure, partial inductance for each wire is calculated, and combined with circuit theories, the loop inductance of the coplanar waveguide per unit length (Units: H/m) at high frequencies has been derived to be[6]:

$$\hat{L}_{coplanar} = \frac{\mu_0}{2\pi}[\ln(\frac{\pi d}{w_{sig}+t}) + \frac{1}{2}\ln(\frac{\pi d}{w_{gnd}+t}) + \frac{1}{2}\ln(1-\frac{1}{\alpha}) + \frac{1}{2}\frac{\ln\frac{\pi w_p}{(\alpha-1)(w_{gnd}+t)}}{\ln\frac{\pi w_p}{w_{gnd}+t}}\ln(\alpha-1)] \tag{4.6}$$

Where w_{sig} and w_{gnd} are the widths of the signal and ground wires, respectively, parameter w_p is ground wire pitch, and d is the center-to-center distance of the signal wire to the nearest ground wire (see Fig. 4.15). Parameter α is the ratio of ground wire pitch, w_p, to d, and $\alpha \geq 2$. As long as the width of the signal wire is smaller than that of the ground wire,

[5]For clarity, the connections are not shown in Fig. 4.15, however, the structure is completely shown in Appendix A.

[6]The frequency is high enough that internal inductance can be ignored. The complete derivation is given in Appendix A.

the ground wire width can be approximated by the signal wire width at high frequencies owing to proximity effects. If $2 \leq \alpha < 4$, the formula can be approximated by $\alpha = 2$ (the coplanar waveguide structure becomes symmetric); If $4 \leq \alpha \leq 100$, the last two terms in the Equation (4.6) can be approximated based on reasonable ground pitchs and ground wire widths. The skin effect can also be included. Considering the rectangular cross-section typical for VLSI interconnects, the following simplified formulae can be used:

when $2 \leq \alpha < 4$

$$\hat{L}_{coplanar} = 0.3 \ln(\frac{w+s}{w+t}\pi) - 0.1 \ln 2 + 0.1I \qquad (4.7)$$

when $4 \leq \alpha \leq 100$

$$\hat{L}_{coplanar} = 0.3 \ln(\frac{w+s}{w+t}\pi) + 0.1 + 0.1I \qquad (4.8)$$

The units for $\hat{L}_{coplanar}$ are nH/mm. Parameter s is the edge-to-edge spacing between the signal wire and the nearest ground wire, w is the width of signal wire and t is the thickness of the metal layer. Parameter I is the frequency dependent internal inductance given by $I = 0.75 \tanh(\frac{2\delta\pi}{w+t})$, with $\delta = \frac{1}{\sqrt{\pi\sigma f\mu}}$, the skin depth of the material. (A term of $10^{-7}I$ can also be added to Equation (4.6) to model the skin effect.) Equation (4.8) is good for a reasonable ground pitch (e.g., 250 μm) and wire width (e.g., 1 to 80 μm) while Equation (4.6) applies to all cases.

4.4 Experiment and Simulation

4.4.1 Simulation for Multi-Conductor Systems

It is well-known that capacitance is a quantitative measure of the ability of a conductor configuration to hold charge per unit applied voltage, or store electrical energy, and is a property of the physical arrangement of the conductors. Inductance is a measure of the ability of a conductor configuration to link magnetic flux, or store magnetic energy and is another property of the *physical layout* of the conductors [28]. To calculate inductance in a multi-conductor system, knowledge of the *physical* configuration of all conductors in the system is necessary. The frequency dependency of inductance comes from eddy currents which are induced by time varying magnetic fields and governed by *the law* of induction – Faraday's Law. Eddy currents manifest themselves as skin effects and proximity effects. In the case of skin effects, the eddy currents (or redistribution of time varying current) flowing through the cross section of a certain conductor is due to its own field, causing the current to flow near the surface of the conductor. By contrast, proximity effects take place when a conductor is subjected to a time-varying field due to the neighboring conductors [73].

Because of complex multi-conductor configurations, long interconnects and fast signal rise and fall times, distributed circuit models consisting of R, L, C are required to predict signal delay or crosstalk. The R, L, C for each small segment can be obtained by partitioning the conductors into smaller segments, dimensions of which are much smaller than the wavelength of the significant frequency of the signals (e.g. 250 μm in current technology) [41].

To calculate inductance for metallic conductors, the source and conducting currents are needed as shown in Ampère's law while the displacement current inside metallic conductors can be safely ignored. The displacement current in a metallic conductor plays a limited role in calculating inductance. It is shown that $| J_c |_{max} / | J_d |_{max} \simeq 10^{17}/f$, where J_c and J_d are the conducting and displacement current densities, respectively, and f is the frequency [28]. The displacement current within a metallic conductor is completely negligible compared to the conduction current at frequencies below the optical range up to $\sim 10^{15}$ Hz.

In the next two sections, the wire inductance is defined as the loop inductance of a signal wire including its ground returns, such as coplanar waveguide ground wires and ground grids or plane. The inductance is calculated as per unit length as defined in any transmission lines.

4.4.2 Modeling for Coplanar Conventional Test Structure

Wire Inductance

A test structure, named as the coplanar conventional test structures, consist of coplanar waveguide structures on upper metal layers and some vertical wires on a lower metal layer. The coplanar waveguide structure is on the fifth metal layer which is about 5 μm above the substrate.[7] Two-port S-parameters were measured using an HP 8510 Network Analyzer and Cascade Microtech coplanar ground-signal-ground probes. Measurement results and FASTHENRY simulations for the coplanar conventional test structure are compared in Fig. 4.16 and Fig. 4.17.

[7] For details of the test chip technology, see [36].

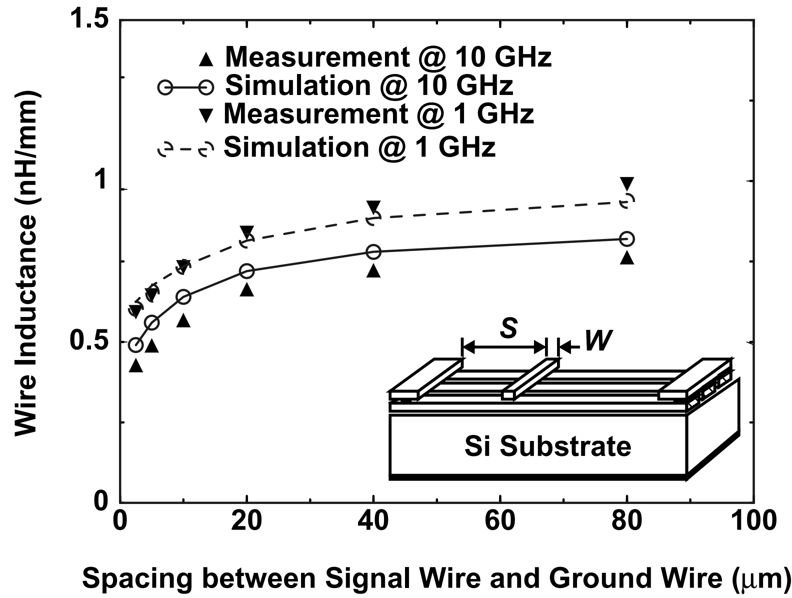


Figure 4.16: Measurement and simulation comparison: inductance vs. wire spacing. The signal wire width is 6 μm. The ground wire width is 16 μm.

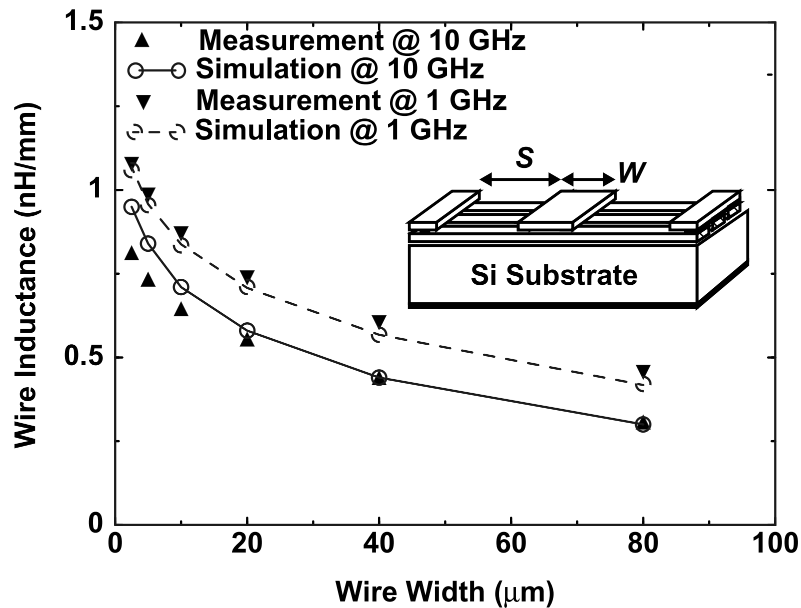


Figure 4.17: Measurement and simulation comparison: inductance vs. wire width. The spacing to ground wire is $(60 - w/2)\mu$m. w is the signal wire width.

The two figures show that inductance increases monotonically with the *spacing* between the wire and the nearest ground wire of the coplanar structure. The pitch of the ground wires, w_p in Fig. 4.15 is fixed in the test structure. Most current returns through the nearest ground wire for small spacings. For large spacings, return current is distributed between the two ground wires, which increases the current return loop and hence inductance. The inductance increase is slower when spacing becomes large and reaches its maximum when the signal wire has equal distance to the two ground wires. Wire inductance decreases monotonically with wire width since wider trace results in smaller loop with associated reduction in magnetic flux. At higher frequencies, inductance becomes smaller because of the skin effect and the proximity effect. When frequencies increase from 1 GHz to 10 GHz, measured inductance is consistently smaller compared to simulated results, which indicates that smaller return paths exist for these test chips. The inductance is decreased due to the proximity effects between the wires as well as between the wire and the substrate at high frequencies, which is more evident from the measurements. Fig. 4.18 compares the inductance results from the analytical formulae and simulations, and demonstrates the accuracy of Equations (4.6)-(4.8) for the coplanar waveguide structure.

Substrate Effects on Wire Inductance

The substrate is usually grounded, and the electromagnetic field of the signal wires can be coupled into the substrate at high frequencies. Electric fields couple to the substrate, generating conducting currents and displacement currents that flow both laterally and vertically. Time-varying magnetic fields couple to the substrate, generating eddy currents that

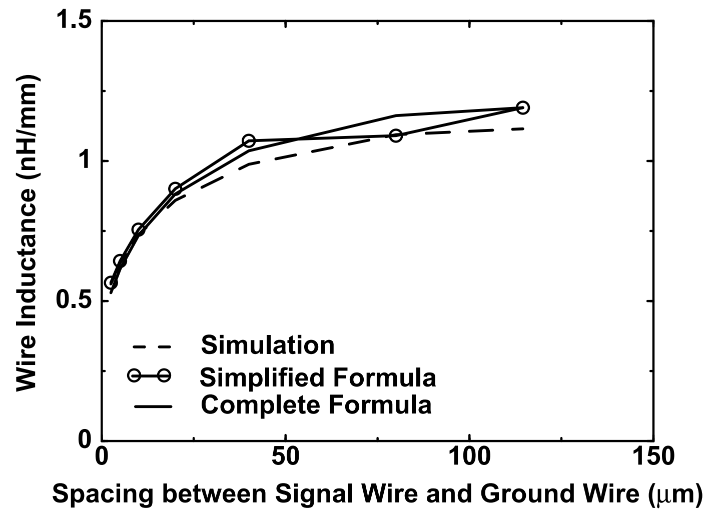


Figure 4.18: Formulae and simulation comparison for co-planar structure. The signal wire width is 6 μm. Frequency is 3.1 GHz.

flow parallel to the device above the substrate as shown in Fig. 4.19. As a result, the substrate can offer a portion of the return paths for current. With the eddy currents, the substrate can reduce wire inductance, especially for a highly conductive substrate. This phenomenon is evident for the wires without intermediate metal layers between the wires and the substrate. In this case, there is no shielding effects of the electromagnetic field of the wires, which might, otherwise, prevent the electromagnetic waves from penetrating into the substrate. It is more evident for the heterogeneous integrated IC microsystems where an additional substrate may exist above the upper metal layers.[8]

The substrate effects of reducing wire inductance at high frequencies are mainly due to the time-variant eddy current effects. To derive the exact formula for the substrate eddy current effects is difficult, however, approximations can be made to have rough inductance estimation for some structures like the coplanar waveguide. To model the substrate effect, it

[8]Inductance of short local wires on lower metal layers is not a concern for VLSI circuits, and can be safely ignored.

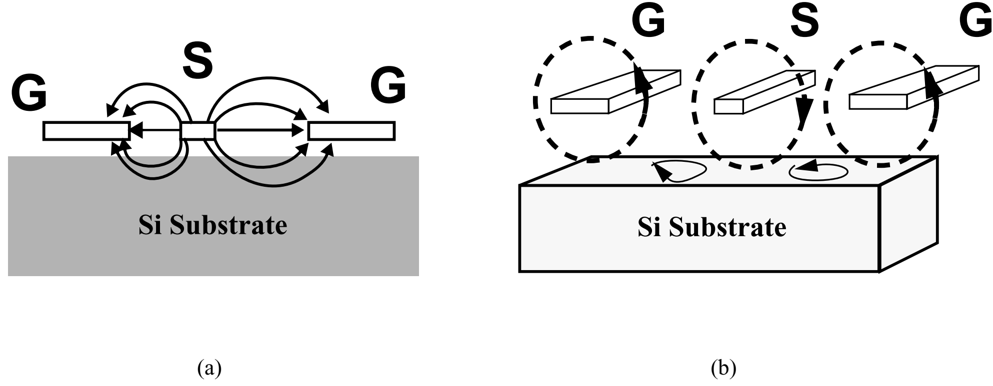


Figure 4.19: (a) Electric field couples to the substrate. (b) Magnetic field couples to the substrate shown by dashed lines. Eddy currents are also shown within the substrate.

can be treated as a return path beneath the signal wire according to proximity effects at high frequencies. Since the ground wires are connected to the substrate with ohmic substrate taps along the whole length of each wire, the substrate currents beneath each ground wire are very small compared to the currents in the ground wires themselves, and thus can be ignored. Displacement current within substrate is also ignored. The substrate skin depth is used to calculate the effective distance between signal and ground wires. Similar procedures as the derivation of Equation (4.6) can be used. The revised formula, including substrate effects, has the form (unit H/m):

$$\hat{L}_{total} = \hat{L}_{coplanar} - k\frac{\mu_0}{2\pi}\left(\ln\sqrt{(\left(\frac{s+\frac{w_{gnd}+w}{2}}{h+\frac{1}{2\sqrt{\pi f\sigma\mu_0}}}\right)^2+1}+A\right) \tag{4.9}$$

where $A = \frac{1}{2}ln\left(\frac{\pi(s+\frac{w_{gnd}+w}{2})}{2(w_{gnd}+t)}\right)$. The $\hat{L}_{coplanar}$ is the inductance without substrate effects, h is the distance of metal layer (center) from the substrate, w_{gnd} is the width of the ground wires, σ is the conductivity of the substrate, f is the signal frequency, s, w and t are the

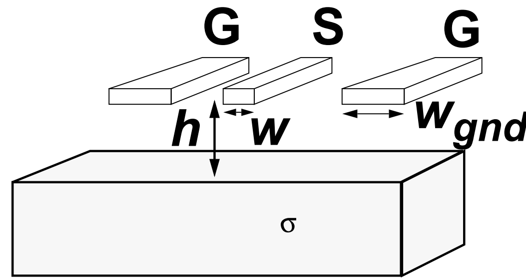


Figure 4.20: Coplanar structure and the substrate. The substrate taps are not shown in the figure.

same as that in Equations (4.7) and (4.8), and k is the percentage of current returned via the substrate, see Fig. 4.20. The parameter k is approximated by the dc current distribution under the coplanar structure, which is around 38% in this study. When the spacing between signal wire and ground wire is larger than 20 μm, with a ground wire pitch of 251 μm, analytical calculations without the substrate correction become inaccurate as seen in Fig. 4.21. More current tends to return via the substrate (i.e. the proximity effect) which forms a smaller current loop, resulting in a reduction of wire inductance. With spacings larger than 40 μm, there is more than 18% reduction of wire inductance. This effect becomes more prominent for less resistive substrates.

Important design insights can be obtained from these analytical formulae. The spacing between the signal wire and the nearest ground wire is a critical factor that determines the loop inductance. Moreover, internal inductance is small compared to external inductance. Three critical factors that determine substrate effects are: the spacing between signal wire and the nearest ground wire; the distance between signal wire and substrate and the substrate conductivity.

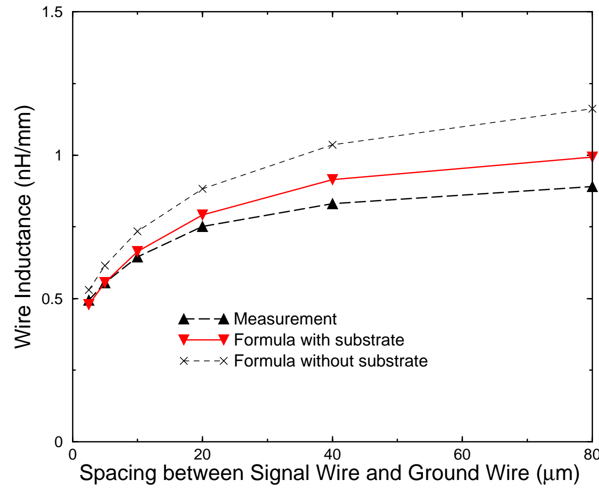


Figure 4.21: Wire inductance with substrate effects. The substrate resistivity, ρ_{sub}, is 0.015 Ω-cm.

4.4.3 Modeling for Test Structures with Power/Ground Grids and Floating or Grounded Grids

Power/Ground Grids

For VLSI digital chips, power and ground are usually distributed through grid structures in order to minimize IR drops as well as to reduce ground bounce. Fig. 4.22 shows a typical power and ground grid structure. The two-layer power/ground grids and their contacts are shown. C4 bumps can be used to directly connect the contacts to the off-chip power/ground pads in order to minimize power/ground wire inductance. Test chips with representative power and ground grids [36] have been used to study effects of these various parameters on inductance. Due to proximity effects, the nearest power and ground wires provide the return paths for most of the signal current through coupling. Since grid perpendicular to the signal wires do not contribute to the signal wire inductance (their mutual inductance is zero),

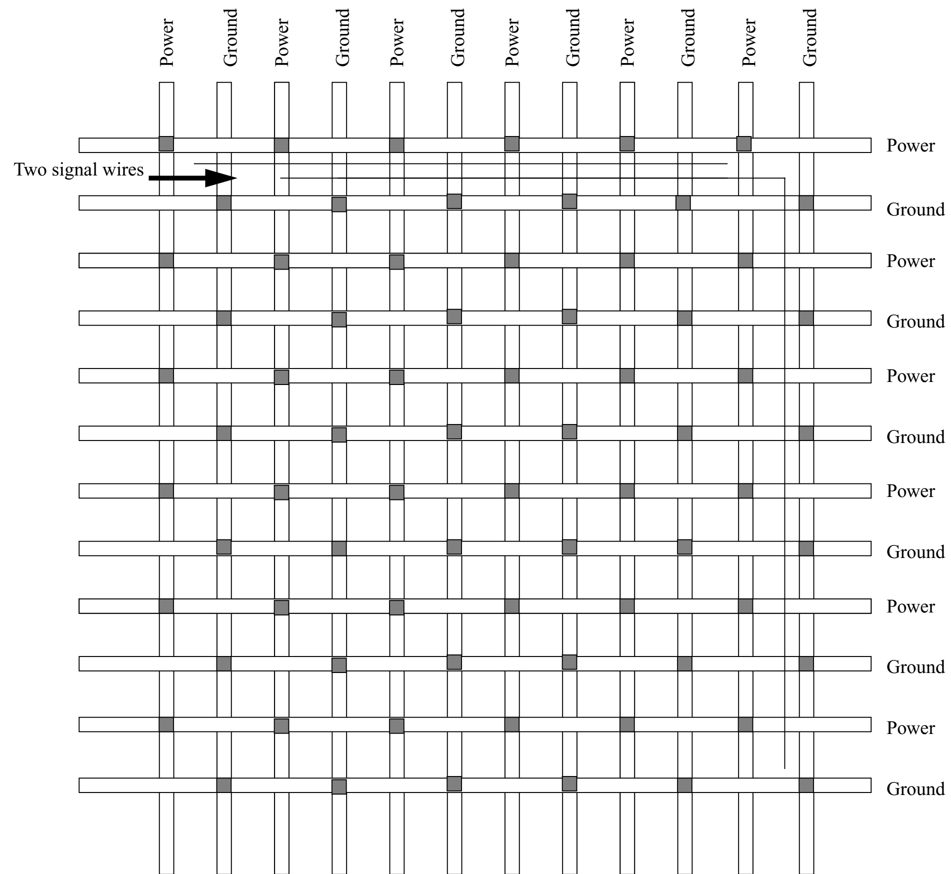


Figure 4.22: Power and ground grids are usually laid down on the top two metal layers to reduce wire resistance. Contacts are shown to connect the power or ground on the two layers. Two signal wires are also shown.

only grid parallel to the signal wires are needed to calculate the signal wire inductance. Simulations and measurements show that, with the substrate excluded, multiple parallel (with signal wires) ground wires in ground grids reduce signal wire inductance because of the multiple parallel current return paths. However, if the substrate is included, the nearest ground wires and substrate dictate the current return paths. In this case, multiple parallel ground wires in the grid cannot effectively reduce signal wire inductance. To accurately calculate a signal wire inductance, nearby signal wires can be included in the simulation. Nearby wires terminated by large impedance values to the ac ground can be approximated as floating wires. They do not affect the signal wire inductance if these wires have widths smaller than 20 μm so that their eddy currents are small enough to be ignored; nearby wires terminated to the ac ground can be treated as ground wires. All the nearby wire effects on inductance can be incorporated into one signal wire inductance which can be used in circuit simulation for delay analysis. However, for crosstalk analysis in circuit simulation, partial inductance and partial mutual inductance of signal wires as well as nearby wires are needed.

The Nature of Eddy Currents

Following Faraday's law of induction, if a **B** field in a conductor is time varying, an electric field intensity **E** is produced,

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} \tag{4.10}$$

The **E** can also be given in terms of magnetic vector **A** by

$$\mathbf{E} = -\frac{\partial \mathbf{A}}{\partial t} \tag{4.11}$$

Current will flow due to this electric field in the conductor according to Ohm's law,

$$\mathbf{E} = \frac{1}{\sigma}\mathbf{J} \tag{4.12}$$

where σ is the conductivity of the conductor and **J** the current density. Using Equation (4.12), Equations (4.10), (4.11) can be rewritten to be

$$\nabla \times \mathbf{J} = -\sigma \frac{\partial \mathbf{B}}{\partial t} \tag{4.13}$$

$$\mathbf{J} = -\sigma \frac{\partial \mathbf{A}}{\partial t} \tag{4.14}$$

Since these currents, namely the *eddy currents*, flow in a conductor of uniform permeability μ, such as a metal ground plane, they will produce a magnetic field to oppose the original magnetic field. According to the Ampère's law, the **B** field in the conductor then satisfies the following equation,[9]

$$\nabla \times \mathbf{B} = \mu \mathbf{J} \tag{4.15}$$

[9] The displacement current is again neglected here. For frequencies with wavelength larger than the dimensions of the devices this assumption introduces an absolutely negligible error [73].

By using the fact $\nabla \cdot \mathbf{J} = 0$, $\nabla \cdot \mathbf{B} = 0$, $\nabla \cdot \mathbf{A} = 0$, and $\nabla \times \nabla \times \mathbf{A} = -\nabla^2 \mathbf{A}$, the Equations (4.13)-(4.15) lead to,

$$\mu\sigma \frac{\partial \mathbf{J}}{\partial t} = \nabla^2 \mathbf{J} \tag{4.16}$$

$$\mu\sigma \frac{\partial \mathbf{A}}{\partial t} = \nabla^2 \mathbf{A} \tag{4.17}$$

$$\mu\sigma \frac{\partial \mathbf{B}}{\partial t} = \nabla^2 \mathbf{B} \tag{4.18}$$

The solution of these three equations give the eddy current density distribution in an extended conductor by properly applying boundary conditions. However, it is generally not always possible to find solutions analytically for three-dimensional configurations. Numerical methods are usually used to solve these equations. Eddy current densities are higher at the edges of the conductor body where they are developed and the skin effect is formed. For a plane boundary, eddy currents circulate parallel to the plane regardless of the form of the excitation. Analysis shows that the magnetic field and thus inductance of one conducting loop is dramatically affected by eddy currents distributed within a nearby conducting ground plane [73].

Eddy Current Effects on Wire Inductance

In the digital chip environment, if there are dense grids or ground planes on a given metal layer, they can generate eddy currents due to the existing time-varying magnetic field. A ground plane can shield electromagnetic fields and also offer current return paths for the signal current. In these cases, the signal wire inductance can be reduced significantly due

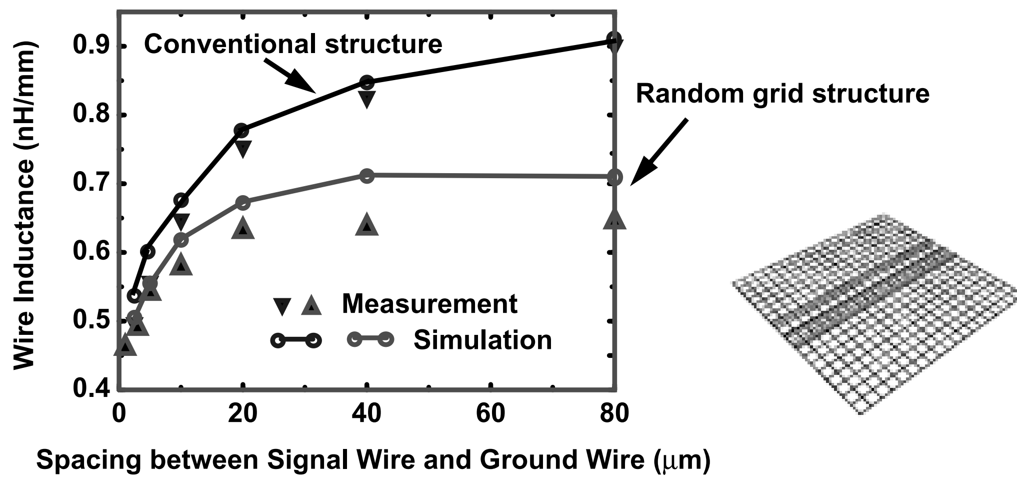


Figure 4.23: Measurement and simulation: wire inductance at 3 GHz is reduced with floating grids on M1 and M2. The signal wire width is 5 μm. A random grids structure is shown on the right.

to the return current and eddy currents in the dense grid or ground plane. Electromagnetic field solvers, such as FASTHENRY, can be used to simulate the eddy current effects based on constructed 3-D geometries of grids or ground planes. Fig. 4.23 compares the results of the conventional test chip with the results from a test chip which has coplanar waveguide structures on the fifth metal layer, and dense grids on the first and second metal layers across the chip. The chip is referred to as the random grid structure. For the conventional structure, inductance increases as the spacing to the nearest ground increases as shown in Section 4.4.2; while for the random grid structure, the inductance saturates around 20 μm and becomes independent of the spacing at larger spacings. The magnetic flux generated by eddy currents in the random grids opposes the magnetic field change, thus reducing the magnetic flux of the signal wires, and effectively reducing the inductance of the signal loop. The dense grids effectively change the electromagnetic field configuration in a manner similar to a continuous ground plane. As a result, wire inductance is primarily determined

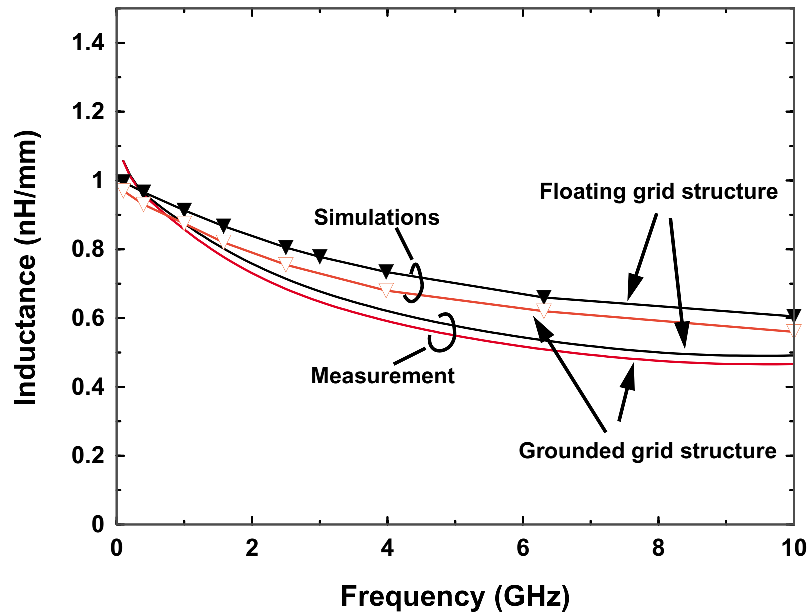


Figure 4.24: Frequency dependency of wire inductance with floating or grounded grids on M1 and M2 layers.

by the spacing from the wire to the grids. Each cell of the grids is about $15\mu m \times 15\mu m$. When the spacing between the signal wire and the nearest ground wire exceeds about 15 μm, the signal loop couples to the eddy current loops in the grids, and the effective magnetic flux is reduced. Fig. 4.24 shows the frequency dependency of the inductance. As the frequency goes up, the inductance decreases due to the time varying nature of the eddy currents. The same phenomena can be observed in the simulations and measurements if the grid structure is replaced by a continuous ground plane. Whether the grid structure is floating or grounded, it does not make much difference in the wire inductance due to the eddy current effects.

4.5 Conclusions for On-Chip Inductance Modeling

Results from both measurements and simulations show the growing impact of on-chip inductance for sub-0.25 μm VLSI. Inductance becomes a critical factor for intermediate (mm-scale) length wires. Simple RC models are no longer adequate for modern VLSI circuit analysis and simulation. Therefore, designs of high performance microprocessors and system-on-a-chip (SoC) need to account for inductance effects and inductive crosstalk. Since inductance is a function of the geometry layout of current-carrying conductors, automated geometry generation from layout needs to be integrated into CAD tools for accurate inductance extraction. In Sections 4.2-4.4, a new physical modeling approach is presented, which includes effects of 3-D geometry, as well as the overall complexity of multi-conductor environments, including consideration of substrate effects. For quick and accurate on-chip inductance estimation, analytical formulae have been derived for self- and mutual inductance calculation, and benchmarked with simulations and measurements. Excellent agreement between modeled and measured data is achieved for frequencies up to 10 GHz. These formulae are sufficiently accurate for circuit design as well as for screening of dominant inductance effects in CAD tools. To reduce the on-chip parasitic inductance of signal wires, nearby current return paths are needed. It is demonstrated, both in measurements and simulations, that coplanar waveguides can confine the magnetic fields, offer nearby return paths and reduce overall wire inductance for critical signals – for example, clock nets. Power/ground grids can also offer nearby current return paths for most of the signal wires. In addition, good conductivity of the substrate can reduce wire inductance. Detailed analysis shows

that, due to eddy current effects, densely populated grids including power/ground grids resulting from designs can reduce wire inductance significantly.

4.6 Capacitance Modeling of IC Structures

To model on chip interconnects as transmission lines, capacitance also needs to be accurately modeled [56]. Capacitance effects are well understood compared to on-chip inductance modeling. This section mainly focuses on capacitance extraction capabilities based on more realistic and geometrically complicated structures; this is especially important for MEMS, RF integrated circuits as well as on-chip ICs.

Accurate analysis of IC devices and interconnects in the deep submicron regime increasingly depends on the precise geometry of structures. Moreover, timely technology development requires the prediction of circuit performance based directly on the design data. Non-planar IC structures need to be modeled correctly in order to extract the accurate capacitance of these complex geometries. Many commercial tools often lack the ability to model and simulate IC structures with complex 3-D geometry. The 3-D simulation capabilities are described here, which directly link effects of layout and processing with the electrical characteristics of complex IC structures, especially for the interconnects. The 3-D modeling approach consists of three major components: geometry modeler, mesh generator, and electrical parameter extraction.

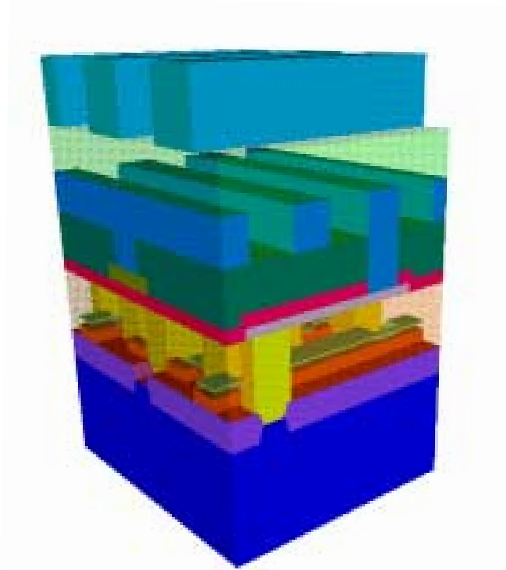


Figure 4.25: 3-D SRAM rendering with transparent layers.

4.6.1 Layout-Based 3-D Solid Modeling

Layout (GDSII files) and process (e.g., layer thickness or simulated bird's beak shape) information are incorporated using a custom C program. The control flow follows the actual processing sequence such as deposition and etching layer-by-layer. The geometry modeler is then used to generate the 3-D structures [82]. The description file for geometry is then converted to geometry files, readable for visualization. This object can be viewed from different angles or sliced by arbitrary cut-planes resulting in 2-D cross sections or 3-D slabs. The resulting geometric model has been represented in Virtual Reality Modeling Language (VRML) browsers. The device can be studied layer by layer or as a full image using a simple browser. The structures are both complex and realistic as shown in Fig. 4.25.

4.6.2 Level-Set Method for Surface Meshing of Complex Geometry

The mesh obtained by simply triangulating the geometric model from a solid modeler limits the accuracy of subsequent simulations. The level-set method [22] is adapted to generate a surface mesh of these 3-D structures. Octree grid and boundary surfaces are generated instead of using a quadtree grid with boundary curves. Surface polygons from the solid modeler are triangulated onto a coarse mesh. Octants containing the geometric model are then subdivided, recursively until a predefined refinement criterion is satisfied. The distance at each grid point is assigned a sign (+/- according to level-set 0). Octants intersecting the surface are segmented into triangles according to these signed distances. Local connectivity is extracted from the octree grid.

Details of a level set refinement for the wordline of an SRAM cell are demonstrated in Fig. 4.26 and Fig. 4.27. Fig. 4.26 shows a 2-D cross section for a 6 level-refined octree mesh as well as the contour values of distances; Fig. 4.27 shows the 3-D iso-surface at zero distance along with volume octree mesh. As a result of 3-D surface meshes, 1252 triangles are generated for the wordline and 5022 triangles for the substrate. A complete surface mesh includes a substrate (grey), the polysilicon layer (purple), and the two metal layers (blue and sky blue) shown in Fig. 4.28, where the polysilicon layer includes a wordline, a ground line and gate regions. The non-planar nature of the structures are fully captured with the solid modeling approach.

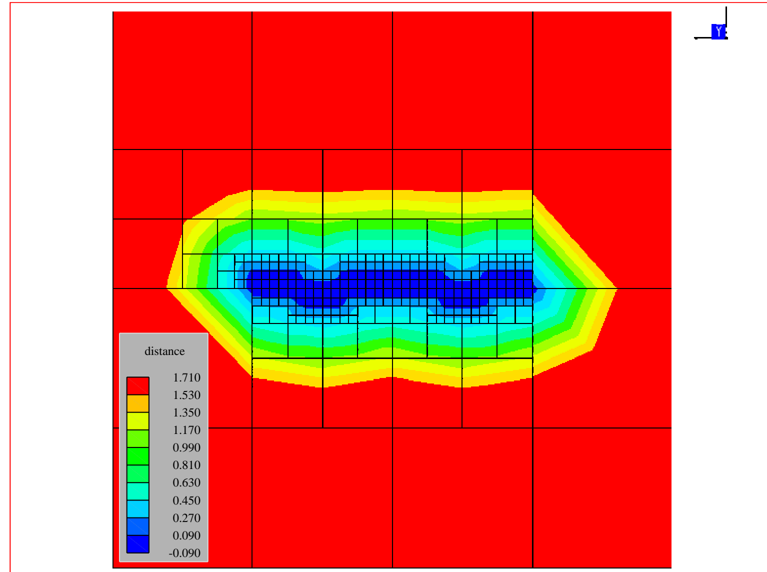


Figure 4.26: Mesh section and distance contour for the wordline.

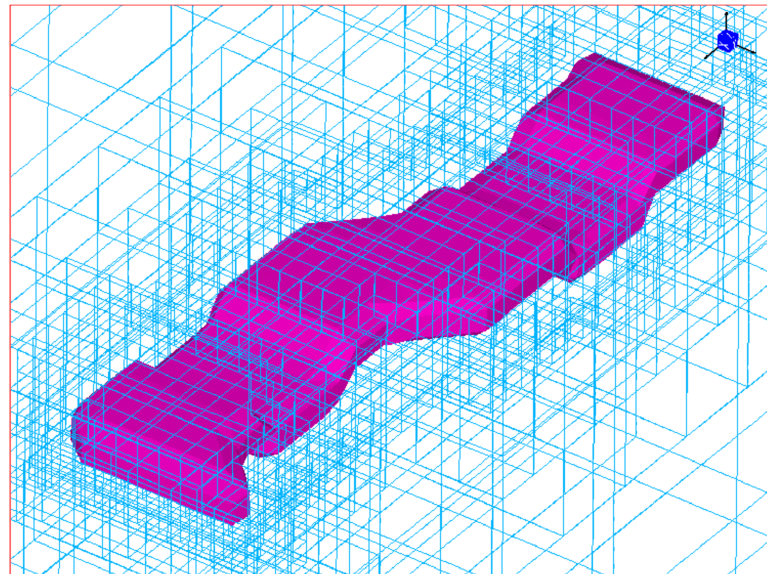


Figure 4.27: Iso-surface and octree mesh for the wordline.

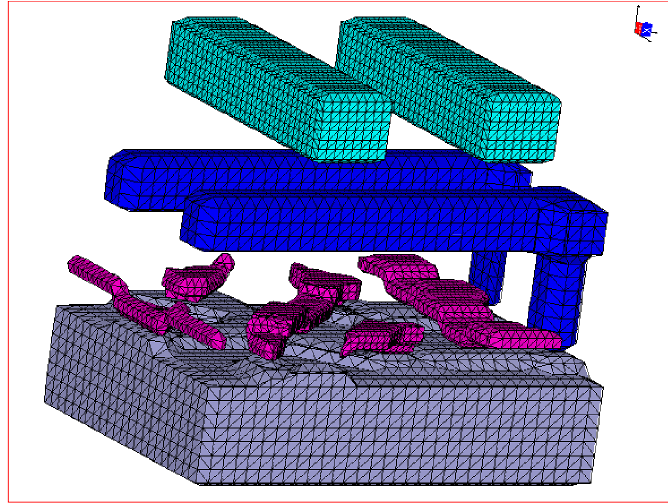


Figure 4.28: Silicon substrate, polysilicon layer, the first and second metal layers in surface mesh.

4.6.3 Capacitance Extraction for a Four-Transistor (4T) SRAM Cell

To analyze realistic structures, FASTCAP [50] is used, owing to its ability to handle complicated surface topologies. The 4T SRAM's wordline capacitance is first extracted. For a cell size of $5 \times 7.25\mu\text{m}^2$ (feature size is 0.6 μm), the resulting capacitance values are shown in Fig. 4.29. For the two bitlines, capacitance between one bitline and the substrate is 1.75 fF while capacitance between the other bitline and the substrate is 1.77 fF. The capacitance between two bitlines is 1.07 fF. One can simulate the wordline, bitlines and the substrate as a whole structure. Results of the calculations are summarized in Table 4.4.

Table 4.4: Capacitance among the wordline, bitlines and substrate

	substrate	wordline	bitline1	bitline2
substrate	11.4fF	4.96fF	1.42fF	1.41fF
wordline	-	6.14fF	0.48fF	0.52fF
bitline1	-	-	3.92fF	1.04fF
bitline2	-	-	-	3.97fF

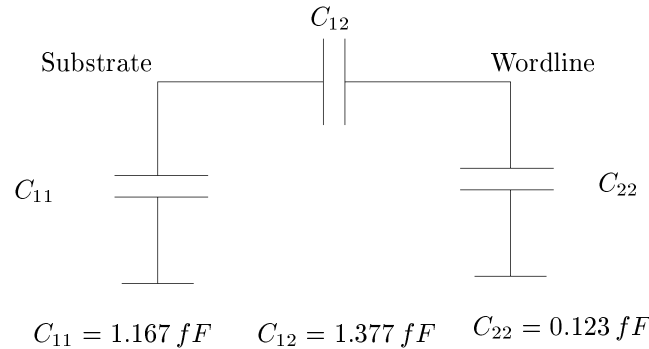


Figure 4.29: Capacitances for a single wordline.

4.6.4 Summary for On-Chip Capacitance Modeling

A technology-based interconnect modeling approach is presented in this section. Capabilities of this software allow more physically accurate parameter extraction for IC circuits and interconnects. Extracted electrical parameters provide essential design information with improved physical accuracy. Benchmark calculations of a simplified geometry model were also performed on a commercial simulator (Raphael from Avant!), which shows there are some differences between these results, owing to nonidentical geometries.

4.7 Summary

On-chip interconnect modeling is presented in this chapter, which includes both inductance and capacitance modeling. The 3-D geometry generation tools are developed and field solvers are used to extract accurate inductance values based on these geometries. Characterization of test structures and extracted RLC values were used in circuit simulation to show the impact of on-chip parasitic inductance on circuit performance and signal integrity including power/ground noise. Analytical formulae are provided to quickly estimate on-chip

inductance for design guidelines as well as to facilitate quick screening process in CAD tools. The modeling methodology and results are verified by experimental test chips. Modeling and measurement of test structures have shown good agreement up to 10 GHz.

On-chip capacitance modeling focuses on the link between the layout design data (and process information) and electrical parameters based on very accurate and realistic complex 3-D geometries. Generated non-planar 3-D geometries can be viewed and studied layer by layer as illustrated with the SRAM example.

Packaging parasitics (e.g. bonding wires) can also be modeled based on the same geometry information. For example, SEM photos can be used to extract geometry information. Inductance and capacitance analysis tools such as FASTHENRY and FASTCAP can be used to extract package inductance and capacitance which will be considered in the next chapter.

Chapter 5

RF IC Wire Bonds

In the last chapter, characterization and modeling of on-chip interconnects have been discussed. However, on-chip interconnects are finally connected to a board via off-chip interconnects, for example using bonding wires, to be grounded or powered on printed circuit board (PCB). Interconnect modeling of the IC packaging is essential in order to accurately simulate the entire IC sub-system. In this chapter, characterization and modeling of bonding wires for RF integrated circuits are studied. The RF IC package is chosen as the topic because radio frequency analog integrated circuits are more sensitive to parasitics in the package. Modeling for RF IC bonding wires is essential at gigahertz frequencies. All modeling methodology and results have been validated using test chip measurements.

5.1 Introduction

Because of growing concerns in high frequency design, consideration of parasitic effects for the bonding wires is essential in IC packaging of RF and deep submicron high speed VLSI circuits. As the frequency moves above several GHz, the parasitics caused by bonding wires, mainly inductance and capacitance, can no longer be ignored and require careful modeling. To predict the performance of packaged RF power devices, a compact model, including bonding wires, is desirable for circuit simulation. Bonding wires are sometimes also used in matching networks in RF ICs. Typically, to achieve good matching, adjustment of the bonding wires is required through empirical characterization, typically with little or no help from simulation results. Moreover, bonding wires are used in implementing high quality factor (Q) inductors as part of functional design of tuning networks in RF circuits, vis a vis on-chip spiral inductors. Therefore, for these applications, it is necessary that the electrical parameters of bonding wires be correctly extracted and their electrical performance be modeled accurately.

As circuits become more complex, the package and bonding wires become more difficult to model. Fig. 5.1 shows an SEM photo of an RF power transistor; complicated geometry of the package must be taken into account. The capture of sufficient bonding wire information depends on accuracy and automation of the 3-D geometry modeling process. In this chapter, a fast 3-D modeling approach is presented, which extracts the geometry from SEM photos, ultimately leading to extraction of electrical parameters. The input files for the field solvers, such as FASTHENRY [33] and FASTCAP[50], can be automatically generated

Figure 5.1: Inside look of the package of a 55 W bipolar transistor for 1.9 GHz PCS base stations.

based on this geometry. Electrical parameters (inductance, resistance and capacitance) and equivalent circuits are then obtained for circuit analysis. A carefully designed test structure has been fabricated and measured. The simulation results show excellent agreement with the measured data. The software is written in the Java programming language, offering potential use in remote and distributed design environments.

The chapter is organized as follows. In Section 5.2, a new geometry modeling method is introduced. In Section 5.3, the design of test structures is detailed along with a simple equivalent circuit for the bonding wires. In Section 5.4, the simulation and measurement results for the test structures are compared and finally conclusions are summarized in Section 5.5.

5.2 A Novel Geometry Extraction Method

5.2.1 Methodology

Physically-based simulation of interconnects is possible only when detailed knowledge of 3-D geometry is available. In many cases the structures can be defined from planes parallel to the coordinate planes (e.g., plane xy with $z = 0$, plane yz with $x = 0$, and plane zx with $y = 0$). Solid modeling tools have become popular in defining such geometries. The most common way of capturing geometry is based on projections of 2-D objects from respective coordinate planes (xy, yz and zx). If an object's projections to the coordinate planes are known, a 3-D geometry of the object can be constructed. This makes it possible to construct 3-D geometries, using conventional mechanical engineering drawing methodology.

To obtain the geometry of the wires, a new extraction method is developed. Even though shape can be controlled by the bonding machines with high accuracy and reproducibility, it is difficult to predict the shape of bonding wires in advance. SEM photos have a large depth of focus and are used to capture the shape of wires. Complete 3-D information can be obtained from several photos with known viewing locations and angles. In practice, however, it is sufficient to use a single properly positioned photo and to make the extraction unique by adding limited assumptions about the geometry. Since SEM photos are portable, using electronic transport formats, this geometry modeling method can be exploited in modeling a variety of wire shapes as long as we have the SEM photos.

A program has been written that can display the SEM photo, including the definition of

a reference coordinate system. A simplified drawing is superimposed on the photo interactively, and by moving the cursor on the screen the necessary depth information is captured which emulates 3-D movements and allows construction of the 3-D geometry [59][58].

5.2.2 Algorithm

The 3-D space and objects are described in a world coordinate system and a user defined reference coordinate system. The reference coordinate system can be considered as a result of two sequential rotations of the world coordinate system. The relationship between the two systems is described using transformation (rotation) matrices and one scaling matrix. The 3-D space is described in the world coordinate (x ,y ,z), which is defined, on the screen, that the x axis is always pointing to right, the y axis is always upright and the z axis points towards the user. The objects (bonding wires) are described in a user-defined reference system (x', y', z'). Fig. 5.2(a) shows the aligned world and reference coordinate systems. By assuming that the z' axis projection on the screen – the xy plane – is always parallel with the y axis (i.e. upright on screen), we do not have rotation around the y axis. This key assumption can always be made valid by an appropriately taken SEM photo. To transform the xyz system to the $x'y'z'$ system, we only need to first rotate the xyz system around the x axis and secondly, rotate around the new resulting z' axis. The rotation around x and the new z' axis are plotted in Fig. 5.2(b)(c) and the corresponding matrices can be obtained [1].

Users define the reference system by actually specifying the x' and y' axes projections on the screen in the xy plane. This is usually done by putting the origin on the corner of

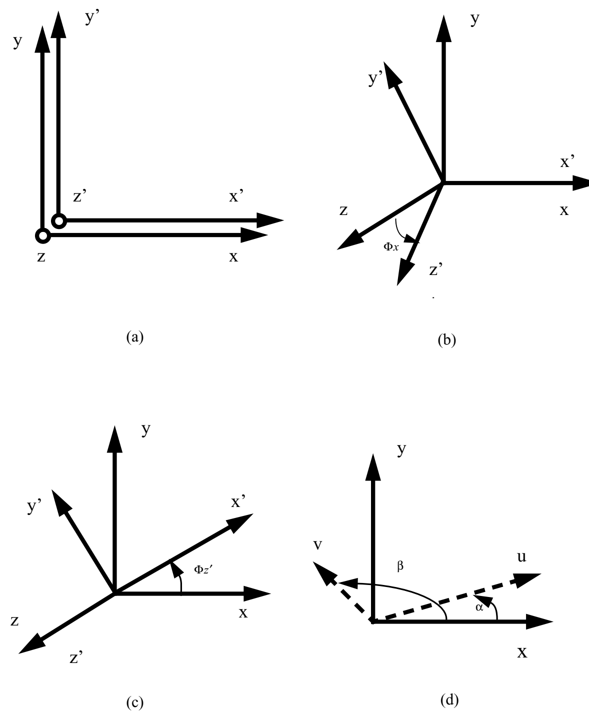


Figure 5.2: Translation of world coordinate system and reference coordinate system. (a) World coordinate system and reference coordinate system are aligned. (b) Rotation around x. (c) Rotation around z'. (d) Projections of x' and y' on xy plane. u and v are their projections.

a device and creating two projections along two selected edges of the device. As soon as the projections are drawn, the angle, α, between the x axis and the projection of x', and the angle, β, between the x axis and projection of y' are known (See Fig. 5.2(d)). The two rotation matrices can be used to derive the relationships between Φ_x, $\Phi_{z'}$, α and β based on the fact that (A) the x axis rotation yields the x' axis, the y axis rotation determines the y' axis and (B) the x' and y' axes can be represented by their projections on the xy plane:[1]

$$\tan\alpha = \frac{q_x}{q_y} \tag{5.1}$$

$$\tan\beta = \frac{r_x}{r_y} \tag{5.2}$$

where q_x and q_y are two scalars representing the x' axis projection on the screen (xy plane) – in other words, vector $\mathbf{u} = q_x\mathbf{x} + q_y\mathbf{y}$. Likewise, r_x and r_y are the components that represent the y' axis projection on the screen (xy plane). Vector $\mathbf{v} = r_x\mathbf{x} + r_y\mathbf{y}$.

With limited assumptions, once we define the x'y$'$ projections on the screen, a reference system is established which in turn defines its transformations with the world coordinate system. Whatever we draw on the screen can be converted to this system through two rotation matrices.

Programmed in Java, the tool can potentially be run across a network (or internet) using a Virtual Java Machine (VJM) available in Netscape and Internet Explorer browsers on most computer systems. The program automatically creates input files for the 3-D electromagnetic simulators such as FASTHENRY [33] and FASTCAP [50] to extract the

[1] The detailed transformation is shown in the Appendix B

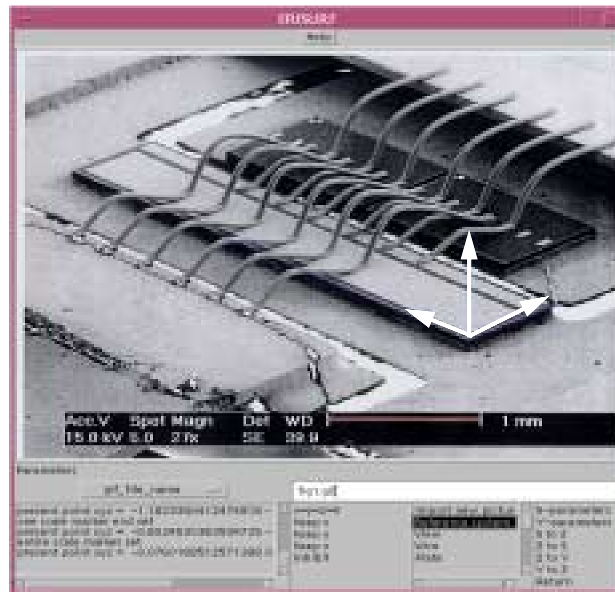


Figure 5.3: A program is developed to capture the 3-D bonding wire geometry and to generate input files for field solvers.

electrical parameters for the structure. Fig. 5.3 shows the user interface of the software used to capture 3-D geometry, and the extracted drawing is shown in Fig. 5.4. The axes of the reference system can be seen at the corner of the capacitor's plate. Users can easily choose functions from the menu shown below the SEM photo (i.e. Fig. 5.3).

To check the accuracy of the geometry modeling method, SEM photos are taken from different view angles (e.g. 180° rotation). Geometries are extracted from one SEM photo. If the extracted geometries are rotated 180°, to fit another SEM photo taken after 180° rotation, the extracted geometries fit the second SEM photo reasonably well as shown in Fig. 5.5. The primary error comes from neglecting the perspective factor which is usually small. The comparisons of the measurement and simulation of test structures in Section 5.4 further confirm the accuracy of the geometry extraction. One limit of this method could

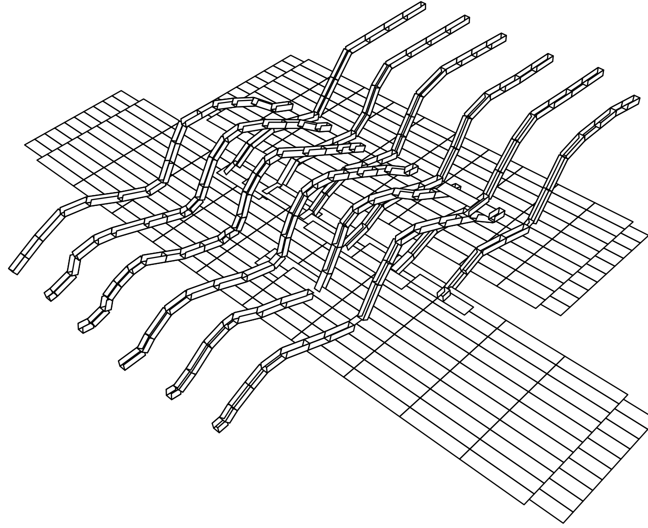


Figure 5.4: Extracted 3-D geometry model from the Java program for further electrical simulation.

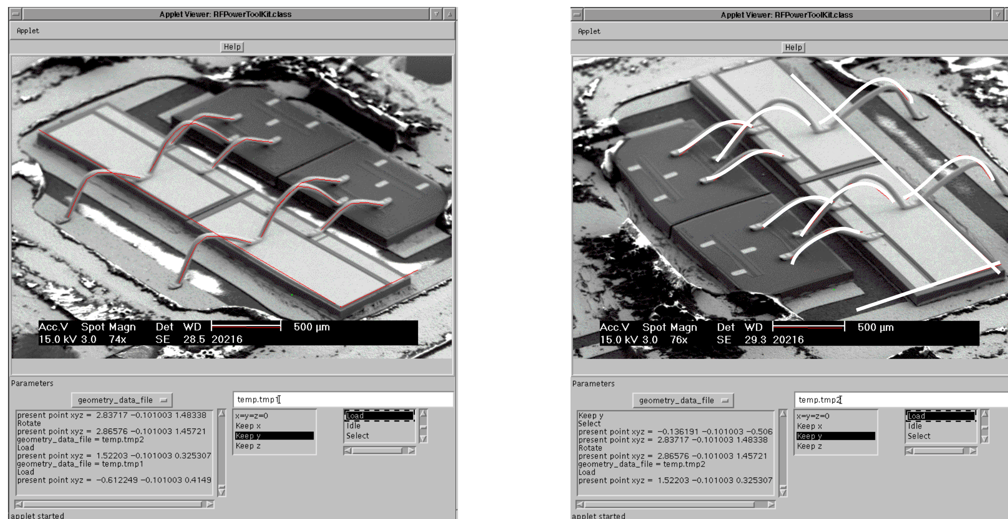


Figure 5.5: (a) Traces extracted from one angle. (b) Traces extracted from (a) is rotated 180° and fits the new SEM photo taken after 180° view angle rotation.

be the fact that geometry distortion will occur if the SEM photo is taken from an improper viewing angle.

5.3 Design of Test Structures and Model Parameter Extraction

5.3.1 Test Structures and Measurement

The accurate measurement of bonding wires for an entire RF circuit is difficult. Parasitics of the chip and coupling from other parts of the circuit are problematic, especially at high frequencies (GHz). To verify the accuracy of the modeling approach, test structures have been designed, targeted to enhance measurement accuracy. Two SEM photos of three test structures are shown in Figs. 5.6-5.7, which are referred as stra21 (two straight wires, each being 1 mm long) and curv31 (three curved wires, each being approximately 1 mm long), respectively. The other is curv22 (two curved wires, each being approximately 2 mm long). The bonding wires are made of gold with 99.99% purity and diameter of 0.7 mil (17.78 μm). On-wafer testing was performed with a HP8720B Network Analyzer and Cascade Microtech coplanar ground-signal-ground (GSG) probes. The measurement set-up is calibrated using the Cascade Impedance Standard Substrate (ISS). The shunt parasitics of the test structure were de-embedded using open calibration structures fabricated next to the device under test (DUT) [12] [45] [76]. An equivalent circuit for the two-port measurement set-up is shown in Fig. 5.8.[2]

[2] The DUT can also be extended to include the two on-chip ground return wires.

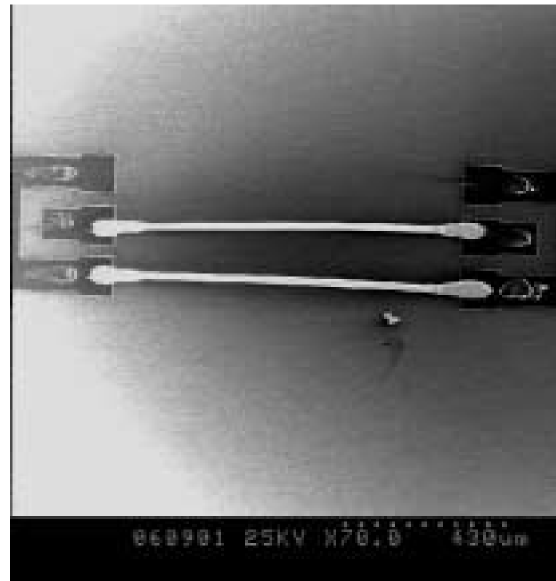


Figure 5.6: SEM photo for stra21 test structure.

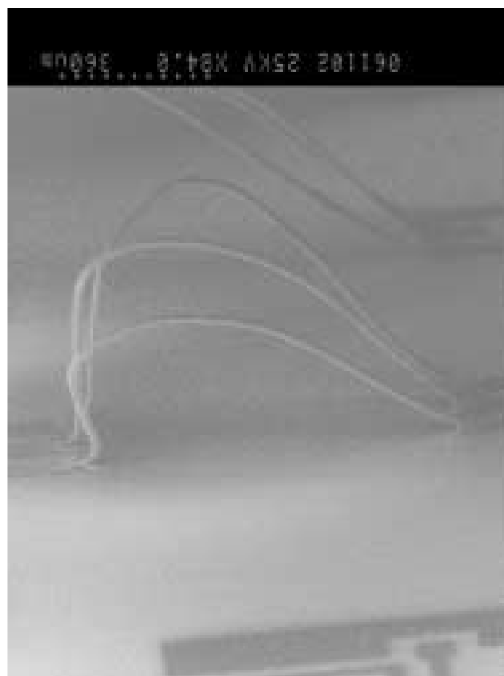


Figure 5.7: SEM photo for curv31 test structure.

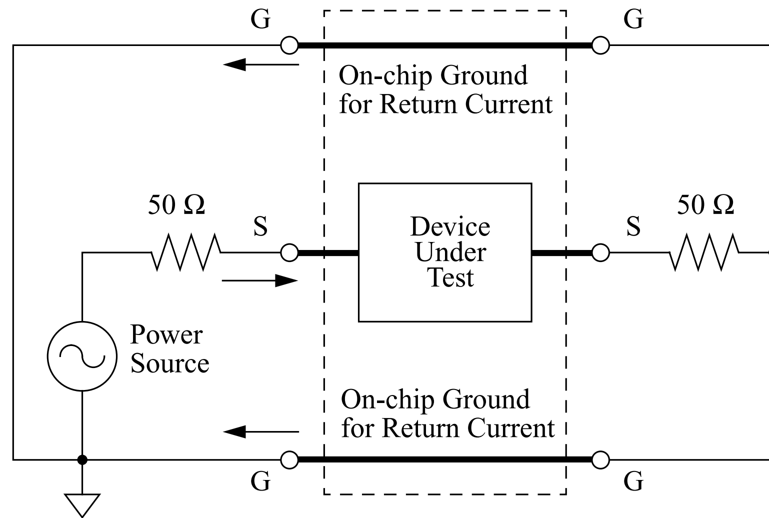


Figure 5.8: An equivalent circuit of a typical on-wafer measurement set-up to illustrate the series ground path parasitics.

Since the ground paths for return current appears in series with the DUT, the parasitic inductance and resistance of these ground paths should be made insignificant compared to the DUT impedance. Since the on-chip aluminum interconnect is much more resistive than the gold wire, the bonding wire resistance will be totally masked by the ground path resistance. To overcome this problem, the return path is implemented using bonding wires as well in the test structures. As a result, the parasitics due to the return interconnect to the ground pad is completely avoided. During these measurements, the backside of the silicon substrate was grounded through the testing chuck. Furthermore, the parasitics of the probe pads were de-embedded using open dummy structures.

5.3.2 Equivalent Circuit for the Bonding Wires

Input to the field solvers (i.e. FASTHENRY and FASTCAP) can be generated automatically based on the constructed geometries. Self- and mutual inductances and resistances of the

bonding wires are then extracted using FASTHENRY. To accurately model the skin effect, the resistance is calculated considering the frequency dependence. A similar dependence is used for the inductance. It is generally assumed that parasitic capacitance is negligible for bonding wires because of its small diameter. However, if bonding wires are used in higher frequency applications (above 6 GHz), the capacitance of the bonding wires to the substrate and the mutual capacitances of bonding wires must be considered for accurate modeling. Meshed input to FASTCAP is also supported and can be used to generate capacitance models as needed.

In addition, in order to compare the simulation results and measurement data, contact impedance of the test probes and the bonding wire's solder balls, which are frequency dependent, should be included in the model since it is extremely difficult to mask or decouple contact resistance in the measurements. The resistance of a straight bonding wire can be estimated as follows [40]

$$R \simeq \frac{l}{2\pi r \delta \sigma} \tag{5.3}$$

where δ is the skin depth and σ is the conductivity. For gold at 293 K, σ is 0.45 $\mu\mho$-cm at high frequencies [6]. r is the radius of the wire and l is its length. R is thus frequency dependent, owing to δ where for gold [6]:

$$\delta = \frac{75}{\sqrt{f}} \tag{5.4}$$

δ is in unit mm and f is frequency in unit Hz. The frequency dependent contact resistance can be deduced from the measured data by subtracting the resistance as expressed in

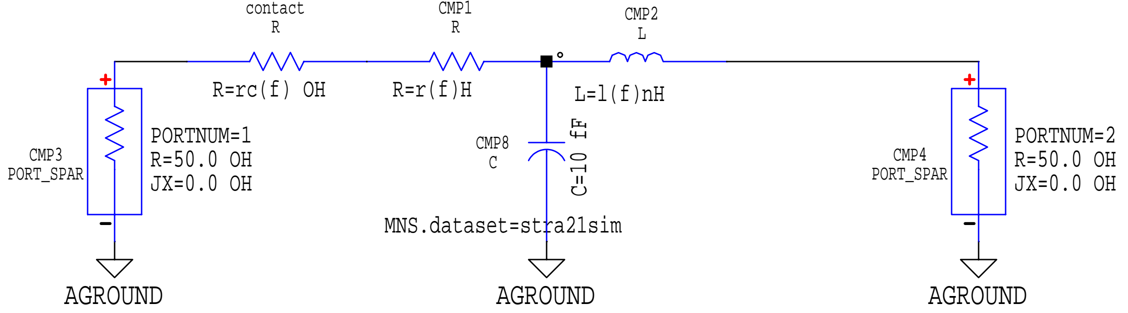


Figure 5.9: Equivalent circuit for the bonding wires.

Equation (5.3) at various frequencies. Regression data fitting is used to find an analytical expression for the contact resistance. For example, the contact resistance for the stra21 and curv22 test structure can be found to be

$$R_{contact}(\Omega) = -0.0053f^3 + 0.3888f^2 - 1.4735f + 1.0816 \tag{5.5}$$

where frequency f ranges from 1 GHz to 10 GHz.

To capture the skin effect in simulation, wires are divided into a number of filaments. Each filament's diameter should be smaller than the skin depth which is 2.37 μm at 1 GHz and varies according to Equation (5.4) for gold material. In our case, eight filaments are enough to accommodate the skin effect. More filaments entail increased computational complexity. The equivalent circuit for the entire test setup, including bonding wires, is shown in Fig. 5.9; the bonding wire's inductance, resistance, capacitance and contact resistance are all considered. Input and output ports are added for completeness.

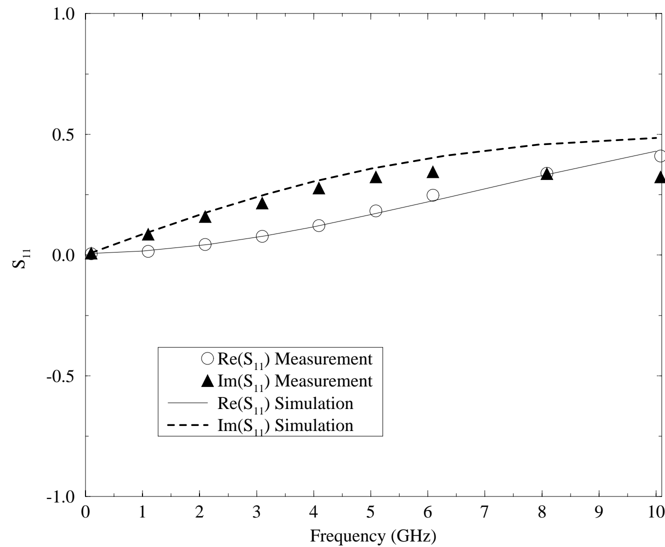


Figure 5.10: S_{11} for the stra21 structure: data points are from measurement and lines from simulation without capacitance included.

5.4 Simulation and Measurement

5.4.1 Results Comparison

In order to avoid the error induced by converting (via processing) the measurement data, S-parameters of the generated models were computed using HP-MDS or HSPICE and then compared directly to the measured S-parameters. In order to compare not only the magnitudes, but also their phases, real and imaginary parts are plotted and compared. Comparing only magnitudes of the S-parameters can lead to unconvincing conclusions about the phase, which is an equally important parameter. Figs. 5.10-5.11 show the comparison between the simulation and measurement of S_{11} of two different structures when only inductance and resistance are extracted. Since bonding wires are usually used around several GHz (where radiation is not a problem), the results are plotted up to 10 GHz. The agreement is excellent

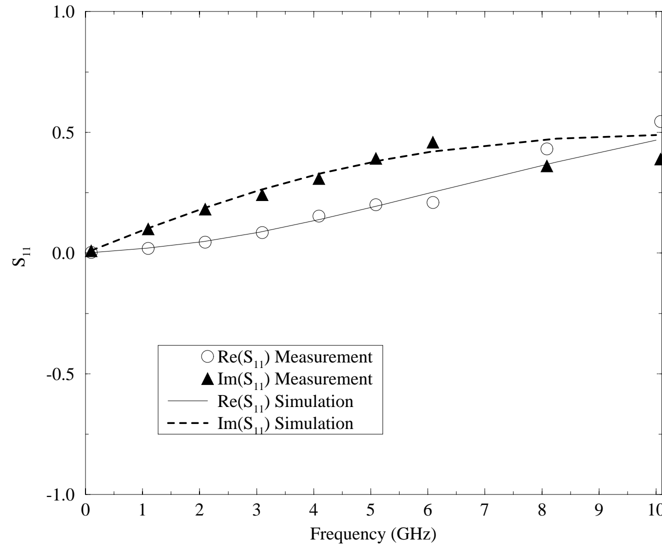
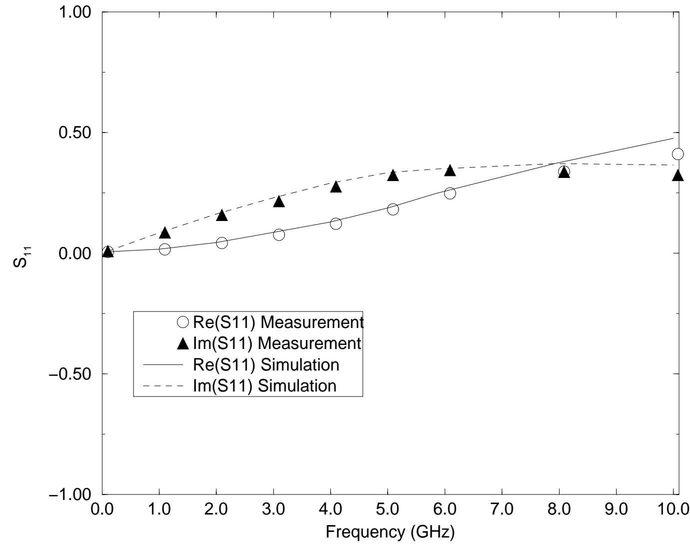


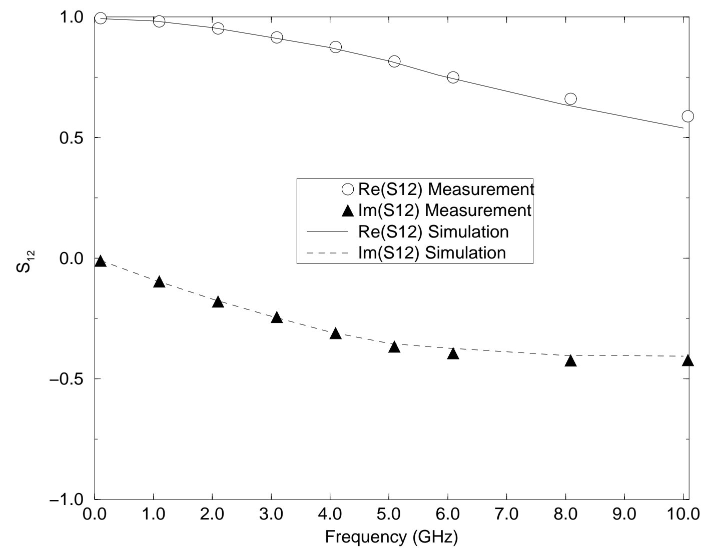
Figure 5.11: S_{11} for the curv31 structure: data points are from measurement and lines from simulation without capacitance included.

up to 5-6 GHz. From the figures, we can see that the real part of S_{11} increases as frequency increases, which is related to the resistance increase at higher frequencies. The imaginary part of the measurement, which is related to the reactance part, also increases up to 6 GHz and then decreases as frequency goes higher. While this differs from simulations at higher frequencies, the capacitance of the bonding wire brings down the S_{11} values. To model higher frequency bonding wires, capacitance should be taken into account. Figs. 5.12-5.14 show S_{11} and S_{12} comparisons of all the three structures with the bonding wire capacitances represented by the current model formulation. The agreement is then extended to 10 GHz, substantiating that parasitic capacitance plays an important role at higher frequencies. The relative simulation errors of the S-parameters usually are smaller than 5%.

Inductance values are also compared between simulations and measurements at a specific frequency based on the equivalent circuit which is shown in Fig. 5.9. S-parameters from

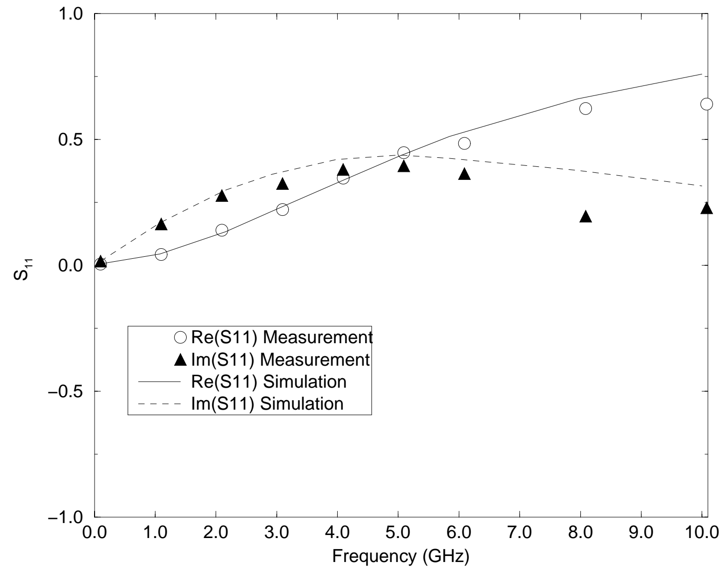


(a)

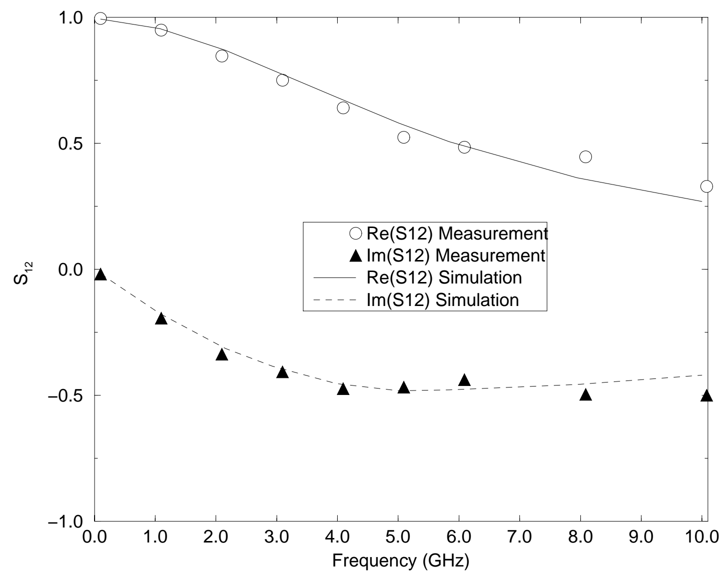


(b)

Figure 5.12: S-parameters comparison for stra21 structure: (a) S_{11} for the stra21 structure with capacitance included. (b) S_{12} for the stra21 structure with capacitance included.

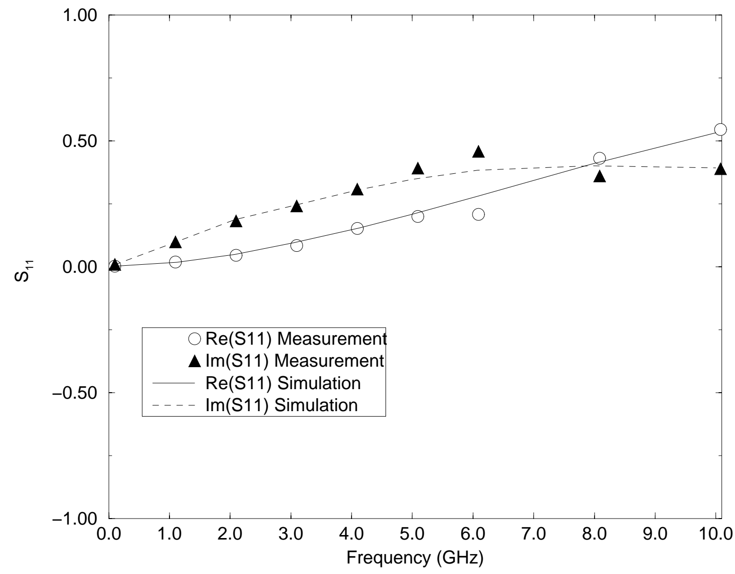


(a)

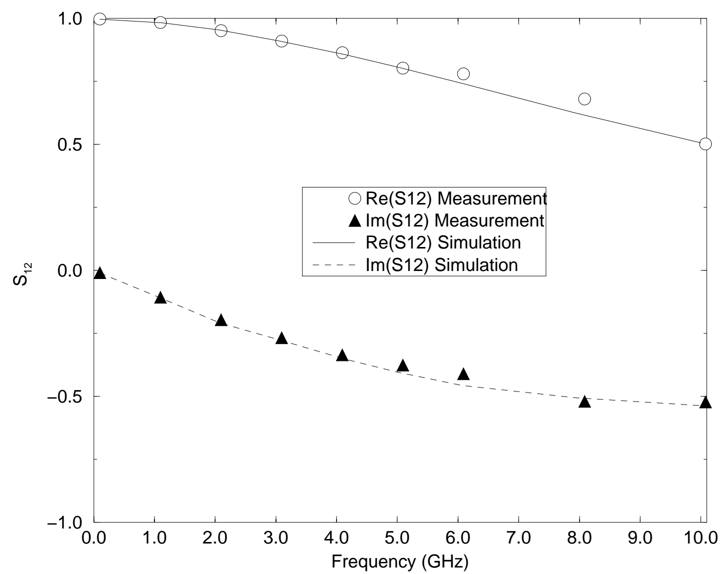


(b)

Figure 5.13: S-parameters comparison for curv22 structure: (a) S_{11} for the curv22 structure with capacitance included. (b) S_{12} for the curv22 structure with capacitance included.



(a)



(b)

Figure 5.14: S-parameters comparison for curv31 structure: (a) S_{11} for the curv31 structure with capacitance included. (b) S_{12} for the curv31 structure with capacitance included.

measurement can be converted to Y parameters and the inductance of the wire can be extracted from Y_{11} of the test structure. Table 5.1 shows the inductance from the simulations and measurements at 1.1 GHz. The simulation errors are rather small (i.e. below 4%).

Table 5.1: Inductance Comparison at 1.1 GHz (nH)

	Stra21	Curv22	Curv11
Measurement	1.377	2.802	1.546
Simulation	1.414	2.694	1.533
Simulation Error	2.69%	3.85%	0.84%
Analytical Calculation	1.233	N/A	N/A
Calculation Error	10.5%	N/A	N/A

RF designers usually use approximate analytical formulae[3] for straight wires to estimate bonding wire inductance L and mutual inductance M as shown below [40]:

$$L \simeq \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{r}\right) - 0.75\right] \tag{5.6}$$

$$M \simeq \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{d}\right) - 1 + \frac{d}{l}\right] \tag{5.7}$$

where μ_0 is the permeability in free space, l the wire length, r the radius of the wire, and d the center-to-center distance between two wires. The loop inductance of a two-wire structure can be estimated as:

$$L_{loop} = L_1 + L_2 - 2M \tag{5.8}$$

where L_1 and L_2 are the wire's self-inductance. Results from analytical calculations for

[3] They are similar to the formulae described in Chapter 4.

straight lines of bonding wires is also included for comparison. However, these formulae only apply for straight wires, which is usually not consistent with the shape of real wires. If we use these formulae to calculate the curv22 and curv31 structures, the inductance is 3.11 nH for curv22, 1.28 nH for curv31 and the relative error is 11.0% and 17.2%, respectively.

5.4.2 Inductance Shape Dependency

To investigate the shape dependence of inductance, further simulations and calculations were made assuming a wire with the same radius as that of the test structures. Three shapes are considered: a Π configuration, median curve (circle like) and straight line, all with the same length of 1.515 mm. The results are shown in Table 5.2. It is observed that

Table 5.2: Inductance comparison for three different wire shapes with the same wire length of 1.515 mm

	Straight wire	Curved wire		Π shape wire	
	Simulation result (nH)	Simulation result(nH)	Error if use straight wire	Simulation result (nH)	Error if use straight wire
100 MHz	1.192	1.011	17.9%	0.814	46.44%
1 GHz	1.160	0.979	18.49%	0.783	48.15%
10 GHz	1.152	0.970	18.76%	0.775	48.65%

the difference between the straight wire and the two curved wires cannot be ignored. While the difference are within 18% - 48%; the straight wire estimation, which circuit designers usually use, actually overestimates the inductance value and causes inaccurate modeling of the wires. The reason that curved wires have smaller inductance is due to the mutual inductance cancellation of the different segments of a single wire. The general trend is that the larger curvature a wire has, the smaller its inductance. Self-inductance of a wire

also has frequency dependence because of the skin effect. However, the resistance has little dependence on wire curvature if the wire length is fixed since the cross section of a wire does not vary with curvature. In terms of capacitance, the trend is that the more curved a wire is, the smaller capacitance it has since it has a larger distance to the substrate.

Examples of mutual inductance dependency on shape of the two wires are shown in Table 5.3. If the length of the two wires is kept constant, the more curved wires become, the smaller the mutual inductance. This is because the mutual inductance cancellation

Table 5.3: Mutual inductance simulation comparison for three different wire shapes with the same wire length of 1.515 mm. The distance of the two wires is 0.3 mm (nH)

	Straight wires	Curved wires	Π shape wires
100 MHz	0.457	0.305	0.176
10 GHz	0.457	0.305	0.176

from different segments of the two different wires. Mutual inductance has little frequency dependency. Calculation of mutual inductance without considering wire shape overestimates the mutual inductance. The curvature (or shape) of the wires makes a difference for a wire's self- and mutual inductances, in turn supporting the need for geometry modeling of bonding wire inductance.

5.5 Summary

A 3-D modeling approach for characterization (and design optimization) of bonding wires is presented. Test structures have been designed, fabricated and measured. A simple compact

model of bonding wires is proposed. Simulated electrical parameters show excellent agreement with measured data up to 10 GHz. The major electrical parameter of bonding wires is inductance while at higher frequencies, capacitance becomes important too. Simulation shows that the shape of bonding wires is an important factor to bonding wire inductance. The simulation methodology can be used in support of both RF device modeling and circuit simulation. It is well suited for the design and analysis of circuits for cellular phone communication (i.e. order of 2 GHz) and future wireless communication (i.e. order of 5 GHz).

Chapter 6

Ground Plane

In this chapter, ground plane effects on wire inductance are discussed. After the introduction, the relevant theory and methodology used to study ground plane effects are presented, followed by results with comparison between field solver simulations and analytical formulae. Design insights are obtained in using ground planes to reduce wire inductance.

6.1 Introduction

Ground planes are often used in both VLSI digital circuits as well as RF analog circuits. For VLSI chips, a ground plane sometimes is purposely designed and inserted between metal layers to shield electromagnetic waves in order to control the wire inductance of critical signal, clock and power nets. A densely populated grid structure, as seen in Chapter 4, also exhibits ground plane effects. For RF circuits and IC packaging, ground planes usually exist under bonding wires. Because of the presence of a ground plane, the electromagnetic field

configuration of the interconnects in IC chips as well as in package is changed, resulting in a different set of wire electrical parameters. A ground plane alters electromagnetic fields due to the boundary conditions at the surface of the plane which need to be satisfied. For example, the electric field **E** must be perpendicular to the ground plane in the case of a perfect conductor. One major ground plane effect is that wire inductance is significantly reduced because of a more confined electromagnetic field, resulting shielding of signals.

There are several previous studies of ground plane effects on wire inductance for PCBs. For example, microstrip lines have been studied by many groups. However, due to the nature of the problem, an exact analytical analysis is not possible for the general case of a microstrip of width w with finite thickness t [44]. Approximations have to be made to obtain a good estimation – for example the strip has to be assumed a very thin, perfect conductor carrying a transverse electromagnetic mode (TEM) wave. Some results for PCBs can not be directly used for on-chip interconnects because of geometry assumptions used in the derivation. Therefore, it is necessary to investigate the ground plane effects for the inductance of on-chip interconnects. This chapter focuses on the inductance simulation and analytical estimation for on-chip interconnects as well as wire bonds.

6.2 Theory and Methodology

6.2.1 Background

Suppose there is a signal wire over a ground plane. A current I goes into the wire, and there is a return current of I in the ground plane as shown in Fig. 6.1. Electromagnetic

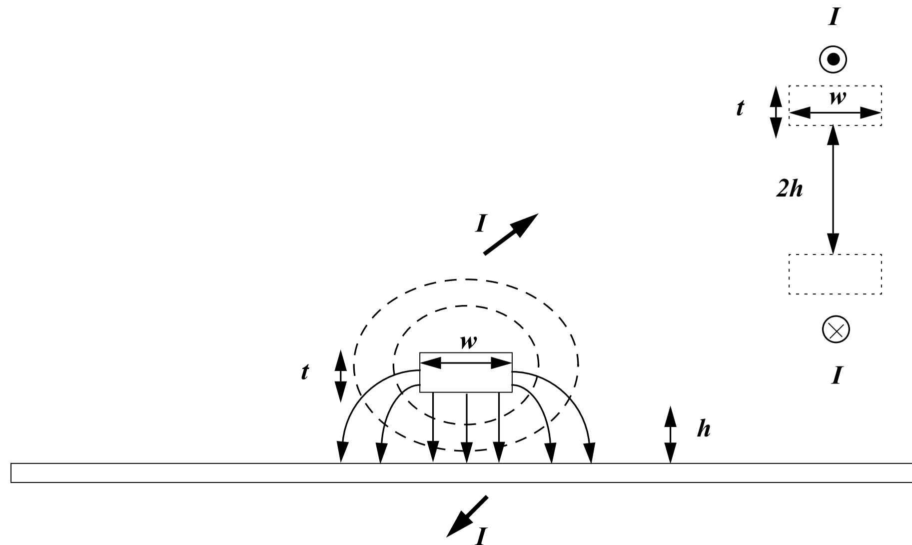


Figure 6.1: A signal wire over a ground plane: perfect conductors are assumed for both the wire and ground plane. Dotted lines show its equivalent geometry in terms of the equivalent electromagnetic field, see Section 6.2.3.

field solvers such as Maxwell [2] and FASTHENRY can be used to numerically extract the inductance of this structure. In order to obtain an analytical formula, perfect conductors are assumed for both the wire and ground plane. Hence, electric field lines are terminated perpendicularly at the surface of the ground plane. Also a simplification is made that a TEM wave propagates down the wire. Under the perfect conductor assumption, proximity and skin effects are not present, and currents follow on the surface of the conductors.[1] Currents return directly beneath the signal wire via the ground plane. Only external inductance exists, which is equivalent to the non-perfect conductor case when frequencies reach infinite values. Inductance in this case shows no frequency dependency. However, this is a very good approximation for many metallic conductors like copper at high frequencies (in or above the gigahertz range) as will be seen in Section 6.3. The inductance value obtained,

[1]Eddy currents do not exit in the perfect conductors. Equation (4.12) can be written as $\mathbf{E} = \frac{\mathbf{J}}{\sigma}$, and $\mathbf{E}$ can not be established in perfect conductors as $\sigma = \infty$.

in this circumstance, is frequency independent, and is the lower bound of a structure. To quickly estimate the inductance of wires over a ground plane and establish design insight, analytical formulae are desirable. Some simple and accurate inductance formulae for wires over a ground plane are presented in the Sections 6.2.2-6.2.4.

6.2.2 Formulae Derived from Characteristic Impedances

Inductance estimations can be obtained from formulations of the characteristic impedance for transmission lines and their relationship with distributed inductances. For a transmission line consisting of perfect conductors[2], the inductance of the transmission line with characteristic impedance Z_0 (in ohms) is [21]

$$L = KZ_0 = \frac{1}{3}\sqrt{\epsilon_r} \times 10^{-4} \mu\text{H/cm} \tag{6.1}$$

where ϵ_r is the relative dielectric constant of the uniform dielectric enclosed by the transmission line. The characteristic impedance of a pair of parallel wires over a ground plane have the same current direction is [21]

$$Z_{oe} = \frac{69}{\sqrt{\epsilon_r}} \log_{10}\left[\frac{4H}{d}\sqrt{1+\left(\frac{2H}{D}\right)^2}\right] \tag{6.2}$$

[2]So it is a lossless transmission line.

and two wires with current in the opposite direction is

$$Z_{oo} = \frac{276}{\sqrt{\epsilon_r}} \log_{10} \left[\frac{2D}{d} \frac{1}{\sqrt{1 + \left(\frac{D}{2H}\right)^2}} \right] \tag{6.3}$$

where H is the height of the wires over the ground plane (from the center of the wires), d is their diameter, and D is the center-to-center wire separation. The two equations hold when $d \ll D, H$.[3] Considering that the inductance of the transmission line is comprised of the inductance of the individual wires and of the mutual inductance M between wires, the transmission line inductance may be expressed as

$$L_{oo} = KZ_{oo} = 2L - 2M \tag{6.4}$$

$$L_{oe} = KZ_{oe} = \frac{L}{2} + \frac{M}{2} \tag{6.5}$$

L and M then can be solved from Equations (6.1)-(6.5),

$$L = 4.59 \log_{10} \frac{4H}{d} \text{nH/cm} \tag{6.6}$$

$$M = 2.30 \log_{10} \left[1 + \left(\frac{2H}{D} \right)^2 \right] \text{nH/cm} \tag{6.7}$$

Considering the rectangular cross section for on-chip wires instead of off-chip bonding wres, one obtains:

$$L = 0.2 \ln \frac{2\left(h + \frac{t}{2}\right)\pi}{w + t} \text{nH/mm} \tag{6.8}$$

[3]This assumption is remedied by adding a Δ term for small H case. See Equation (6.10) discussion.

$$M = 0.2 \ln \left[1 + \left(\frac{2\left(h + \frac{t}{2}\right)}{D} \right)^2 \right] \text{nH/mm} \tag{6.9}$$

where h is the wire height (from the bottom of the wire) to the ground plane, w and t are the width and thickness of the metal wire as shown in Fig. 6.1. To model the case when $h = 0$, an extra term Δ needs to be added in Equation (6.8). As $h = 0$, the magnetic flux enclosed by the loop consisting of the wire and ground plane is zero when L in Equation (6.8) should be equal zero. Δ can be solved by letting

$$\ln \frac{2(h + \frac{t}{2} + \Delta)\pi}{w + t} \mid_{h=0} = 0$$

and solve for $\Delta = \frac{w+t}{2\pi} - \frac{t}{2}$. Plug Δ back into Equation (6.8) to get

$$L = 0.2 \ln \left(\frac{2h\pi}{w + t} + 1 \right) \text{nH/mm} \tag{6.10}$$

6.2.3 Formulae Derived Using the Image Current Method

Since assumptions are made that all conductors are perfect conductors, the method of images can be applied [11] [15]. The method of images simply states that if a wire is carrying a current I with height h above a ground plane (The h is the distance from the bottom of the wire to the top of the ground plane), the electromagnetic field is equivalent to the *upper half* of the electromagnetic field of the case which two wires carrying opposite directional currents I with spacing $2h$ as the dotted lines shown in Fig. 6.1. So the inductance of a wire over a ground plane can be calculated by the two wire system, namely $L = 2(L_1 - M_{12})/2 =$

$L_1 - M_{12}$ where L_1 is the self-inductance of a wire and M_{12} is the mutual inductance of the two wires with spacing $2h$. The factor of $1/2$ needs to be taken into account because only half of the magnetic field is actually generated in the case of a wire over a ground plane. By using Equations (4.1) and (4.2), the formulae can be shown as

$$L = \frac{\mu_0}{2\pi}\left[\ln\left(\frac{2h+t}{w+t}\right) + \frac{3}{2}\right] \text{H/m} \tag{6.11}$$

where w and t are the width and thickness of the metal wire. Likewise, an extra term Δ can be added to model $h = 0$ case, and the finally formula is

$$L = \frac{\mu_0}{2\pi}\left[\ln\left(\frac{2h}{w+t} + 0.22\right) + \frac{3}{2}\right] \text{H/m} \tag{6.12}$$

Similarly, one can derive the formula for a round cross section observed in bonding wires by using Equations (3.11) and (3.12). Because of the varying heights of bonding wires above a ground plane, the average height can be used [42].

6.2.4 Formulae Derived from Geometrical Factor Concept

The self-inductance formula for a wire over a ground plane can also be derived based on a geometrical factor concept where self-inductance, capacitance, resistance and characteristic impedance are all represented by a geometrical factor Γ [77] [9]. In a homogeneous medium, the self-inductance per length can then be defined as $L = \frac{\mu}{\Gamma}$. μ is the permeability of the materials. In a non-homogeneous medium, a fringing factor needs to be included. For the case of a rectangular cross section wire over a ground plane, the geometrical factor $\Gamma = \frac{w}{h}$,

where w is the width of a wire and h is the wire height from the bottom of the wire to the ground plane. Thus,

$$L = \frac{\mu}{K_L}\left(\frac{h}{w}\right) \text{ H/m} \tag{6.13}$$

where K_L is an inductive fringing factor which can be curve-fitted as

$$K_L = -0.0264\left(\frac{h}{w}\right)^2 + 1.5618\frac{h}{w} + 1.3745$$

6.3 Simulation and Experiment

Electromagnetic field solvers such as Maxwell [2] can accurately simulate the ground plane effects on wire inductance. Results from the analytical calculations are validated by comparing them with simulations using Maxwell. Fig. 6.2 shows the self-inductance calculated from Equation (6.10) and the Maxwell results. An excellent agreement has been achieved with this formula. Fig. 6.3 shows self-inductance calculations from Equations (6.12) and (6.13). The comparison with the Maxwell results demonstrates the accuracy of these formulae. Wire inductance increases as the height of the wire to the ground plane increases because it results in larger current loop. According to on-chip interconnect geometries, the height is probably about 1 μm while for the off-chip bonding wires, the height (average height) could be as large as 100 μm. Simulation results at 3 GHz with a non-perfect conducting material (i.e., copper material) are also plotted in Fig. 6.3, showing that the perfect conductor material results give a very good approximation to the non-perfect metal conductor case at high frequencies.

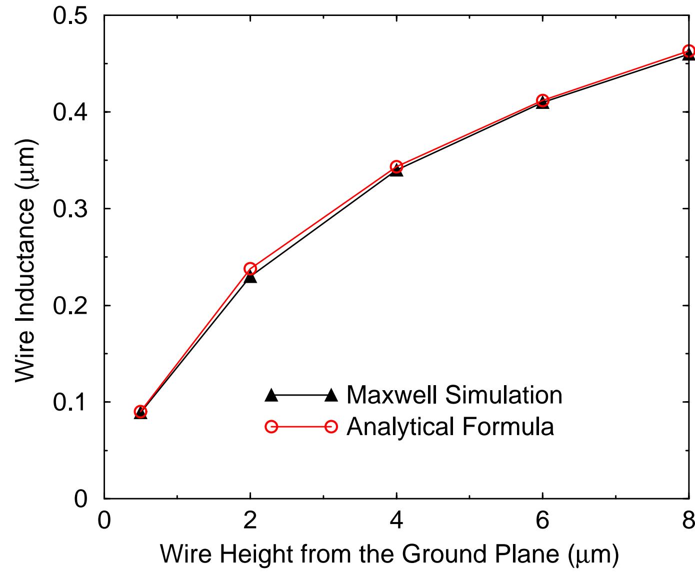


Figure 6.2: A wire over ground plane: Equation (6.10) results are compared with Maxwell simulation results. Wire height is the distance from the bottom of the wire to the top surface of the ground plane. The signal wire width is 5 μm and the thickness is 0.5 μm for both the signal wire and ground plane.

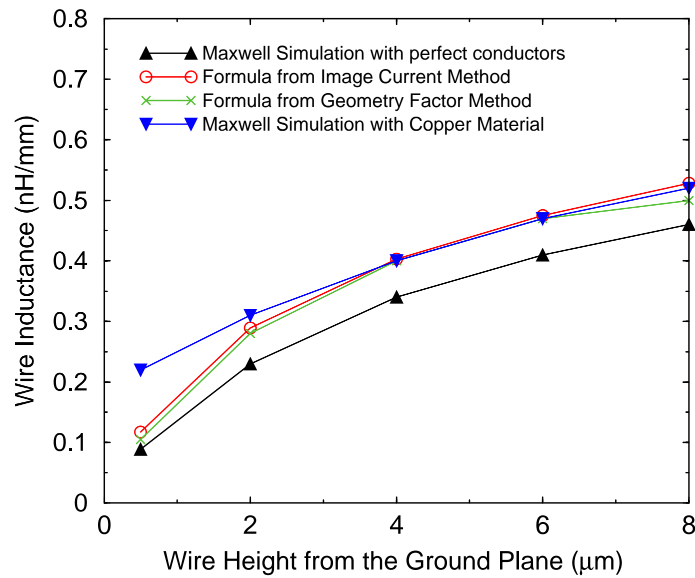


Figure 6.3: A wire over ground plane: Results from Equations (6.12) and (6.13) are compared with Maxwell simulation results. The signal wire width is 5 μm and the thickness is 0.5 μm for both the signal wire and ground plane. Simulations with copper material at 3 GHz are also plotted.

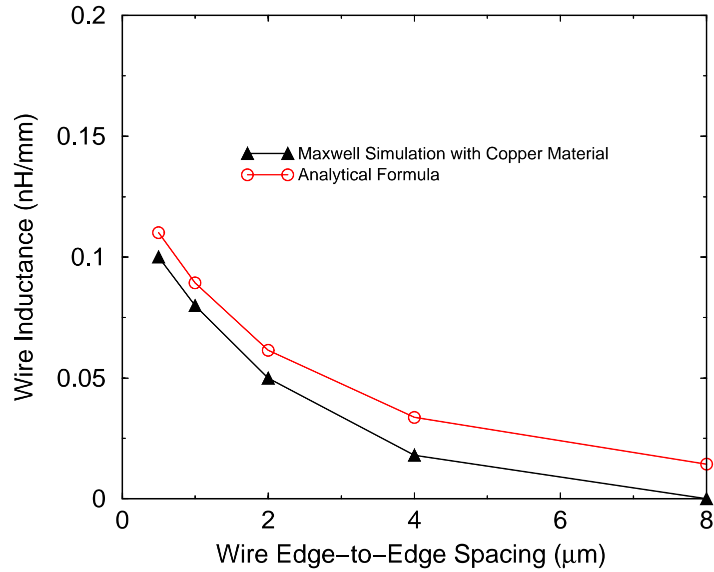


Figure 6.4: Two wires over a ground plane: Mutual inductance results from Equation (6.9) are compared with Maxwell simulations with copper material at 3 GHz. The width of the two wires is 5 μm.

Fig. 6.4 plots the mutual inductance calculated from Equation (6.9) and the Maxwell simulation results. The mutual inductance decreases quickly as wire separation increases – much faster than the mutual inductance of two wires without a ground plane. This is due to the fact that the mutual inductance of two wires over a ground plane is inversely proportional to the square of the wire separation D in Equation (6.9).

In terms of a co-planar waveguide structure over a ground plane, the loop inductance is no longer a function of the spacing between the signal wire and the nearest ground wire as presented in the Fig. 6.5 from test chip measurements. Because it forms a smaller loop, the inductance is mainly dictated by the height of the signal wire to the ground plane, not the spacing to the ground wires in the co-planar structure. In this case, controlling wire spacing can no longer control the loop inductance.

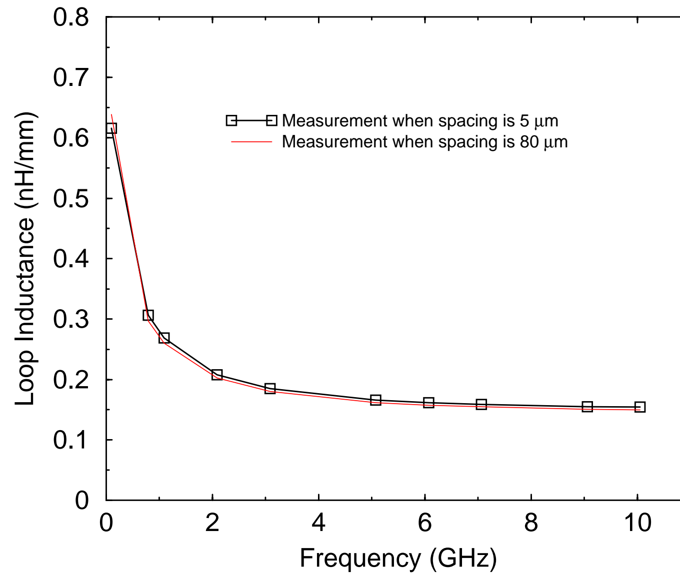


Figure 6.5: Loop inductance of a co-planar waveguide structure does not change with the spacing of the signal wire to the nearest ground wire. The signal wire width equals 5 μm. The width of the two ground wires is 16 μm.

6.4 Conclusion

Simulation and experiment results show that ground planes exhibit important effects on wire inductance both for VLSI on-chip interconnects and RF off-chip wire bonds. It is mainly due to the capability for a ground plane to shield the electromagnetic fields. Electromagnetic field solvers as well as analytical formulations have been used to simulate and analyze the ground plane effects on wire inductance. Analytical formulae, compared with simulation, have demonstrated the accuracy in modeling wire inductance with ground planes. They offer quick yet accurate inductance estimation and design guidelines for wires over a ground plane. As discussed in Section 6.2.3, the addition of the ground plane reduces wire inductance by

half.[4] At the same time, mutual inductance between two wires with an additional ground plane decreases much faster than that of two wires without a ground plane. The reduction of both self-inductance and mutual inductance with ground planes can be used to reduce wire inductance and inductive crosstalk for IC designs. The disadvantage of using a ground plane is that it consumes a substantial chip area.[5] As discussed in Subsection 4.4.3, ground plane simulations and analysis can also be used to analyze densely populated grid structures for on-chip interconnects.

[4]Compared with a loop consisting of two parallel wires with spacing $2h$, a loop consisting of one wire and a ground plane with spacing h reduces the inductance by half.

[5]Maybe a smaller local ground plane can be used to save routing area.

Chapter 7

Conclusions

This chapter firstly summarizes the contributions of this thesis to both digital on-chip interconnect modeling and RF IC packaging modeling. Possible future research areas are then discussed in the second section.

7.1 Summary

Because of the fundamental importance of the geometry on electrical parameters, this work starts with geometry modeling for both on-chip and off-chip interconnects followed by extensive electrical performance investigation. As an important modeling methodology adopted in this work, all major electrical modeling results are validated by test chip measurements.

The first part of this thesis work has been focused on on-chip inductance modeling of VLSI interconnects. With circuit clock and data frequencies operating in the gigahertz range and faster signal rise and fall times in modern IC technologies, on-chip interconnects now

show transmission line behavior. Simple RC models are no longer adequate for modern VLSI circuit analysis and simulation. On-chip inductive effects become increasing problematic for interconnect delay and signal integrity, and it is essential to model the parasitic inductance of on-chip interconnects. Modeling of on-chip inductance for real chips with power/ground wires and grids is presented in Chapter 4. Automated geometry extraction tools captures 3-D geometry and process technology effects directly from layout designs. Based on the PEEC method, analytical formulae suitable for design are developed to estimate the on-chip wire inductance. In addition, consideration of substrate effects may result in reduction of wire inductance when the spacing between the signal and ground wires becomes large. Simulation results and analytical calculations have been verified by S-parameter characterization of test chips up to 10 GHz. Detailed analysis of test chips also shows that eddy currents in ground planes or dense grids in a chip can significantly reduce wire inductance. Design insights and guidelines for minimizing interconnect inductance are demonstrated. Accurate capacitance modeling capabilities of IC on-chip structures is also presented.

The second part of this thesis is on geometry and electrical modeling for the bonding wires. Bonding wires are extensively used in IC packaging and circuit design in RF applications. An approach to fast 3-D modeling of the geometry for bonding wires in RF circuits and packages is demonstrated. The geometry can readily be used to extract electrical parameters such as inductance, resistance and capacitance. An equivalent circuit is presented to model the frequency response of bonding wires. To verify simulation accuracy, test structures have been created and characterized. Excellent agreement between simulated and measured data is achieved for frequencies up to 10 GHz.

Finally, ground plane effects on the on-chip and off-chip wire inductances are studied. Analytical formulae are derived to quickly estimate the inductance of wires over a ground plane. Simulation and analysis show that ground planes can reduce wire self- and mutual inductances which can be used in IC designs.

7.2 Future Research

Interconnect modeling remains one of the most active research areas due to its performance impact on future's high frequency ICs. Transmission line effects of on-chip interconnects and the associated inductive effects need to be fully understood. One obvious extension of this work is to develop full-chip inductance extraction and modeling capabilities. The speed and accuracy of this extraction should be efficient for very large scale integrated circuit designs. A commercial full-chip inductance extraction tool, similar to today's full-chip capacitance tools, is desirable. Another interesting area includes crosstalk analysis with simple analytical formulae. By understanding the inductive and capacitive couplings in complex wiring environment, such as multiple bus lines, crosstalk may be predicted based on geometry information, driver/loads and signal inputs. Guidelines may be provided based on wire geometries (e.g. wire separations, etc.) even without knowing the detail values of inductances and capacitances. Noise issues are especially important for mix-signal system-on-a-chip (SoC) where analog circuits are integrated with digital systems [81] [78]. Although wire inductance formulae with a ground plane of perfect conductors are obtained, more accurate formulae may still be needed for wires over a ground plane of non-perfect

conductors including proximity effects.

For package modeling, future studies can address radiation effects of bonding wires for microwave and millimeter-wave integrated circuits (above 30 GHz) including the impact of different wire shapes on the radiation. Mechanical reliability of packaging, for example, thermal expansion, can be an interesting topic [74]. Bonding wires combined with other packaging types, such as flip-chip mounting, need to be considered together because most of chip packagings may consist of more than one type of packaging.

Modern IC technology enables the construction of micro-electro-mechanical structures (MEMS) and the emergence of biomedical engineering (Bio-X[1]). The geometry modeling and extraction methodology can also be extended to the 3-D modeling of MEMS structures with electromagnetics analysis and Bio-X structures (e.g. molecules and organisms) with medical analysis.

[1]The Bio-X fosters the coming together of leading-edge research in basic, applied and clinical sciences to enable tomorrow's discoveries and technological advances across the full spectrum from molecules to organisms.

Appendix A

Derivation of Equation (4.6)

An on-chip co-planar waveguide structure is shown in the top part of Fig. A.1. Different from a normal co-planar waveguide, it has two ends connected by wires due to the ground grid in the test chip, which is the real case in IC chips. For the two-wire transmission line case (one signal and one current return), **B** field and its flux, Ψ, can be easily calculated. Ψ is then divided by current I to finally get the inductance, i.e. $L = \frac{\Psi}{I}$ [28]. For the co-planar structure, however, circuit techniques are employed to calculate the inductance because of the difficulties in defining a current I to be divided due to the two currents returning from *two* ground wires.

Suppose that the wires have same length of l. To extract only the inductance of this structure[1], the equivalent circuit of the structure is shown in the lower-left part of Fig. A.1, which is a two-port network.[2] With the port2 shorted, one can derive the $Z_{11} = j\omega L$ where

[1] Like a traditional transmission line case, e.g. a coaxial wire, inductance is calculated independent of capacitance calculation.

[2] The signal direction length, l, is much larger than the ground wire pitch, e.g. 4 mm vs. 300 μm, so that the inductance of the wires connecting the ground wires can be ignored.

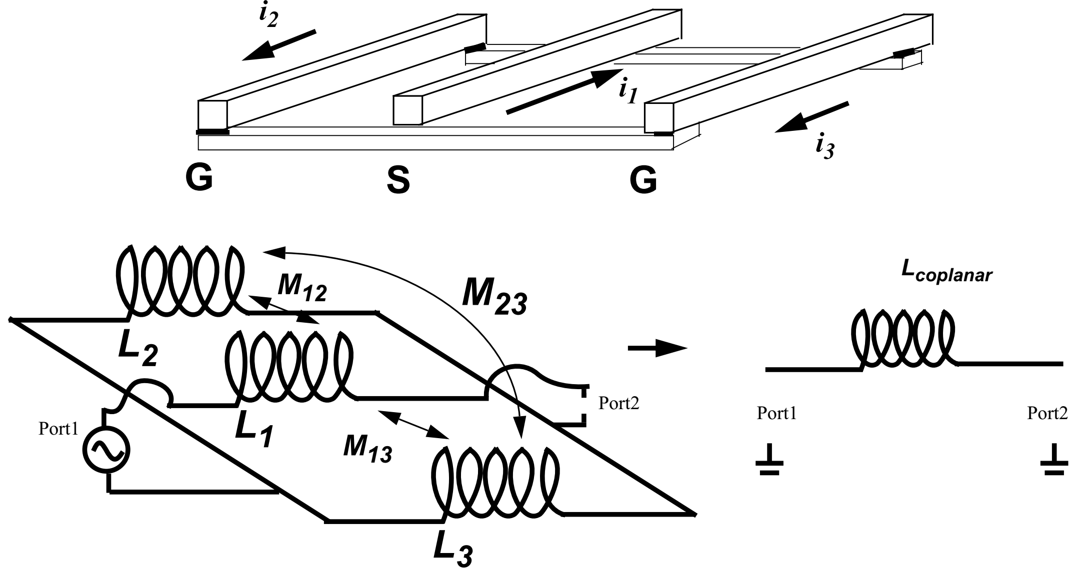


Figure A.1: The inductance equivalent circuit. The structure illustrated at the top is not drawn to scale.

L is the inductance of this co-planar structure, i.e., $L_{coplanar}$. A reduced equivalent two-port circuit is shown on the right next to the original one, with equal Z-parameters. L divided by l is the inductance per length of this co-planar transmission line.

Using circuit theory, namely, Kirchhoff's current and voltage laws, three equations can be obtained. Let $L_{coplanar}$ be the inductance of the structure. One can have

$$L_{coplanar}\frac{di_1}{dt} = L_1\frac{di_1}{dt} - M_{12}\frac{di_2}{dt} - M_{13}\frac{di_3}{dt} + L_2\frac{di_2}{dt} - M_{21}\frac{di_1}{dt} + M_{23}\frac{di_3}{dt} \tag{A.1}$$

$$L_2\frac{di_2}{dt} + M_{23}\frac{di_3}{dt} - M_{21}\frac{di_1}{dt} = L_3\frac{di_3}{dt} + M_{32}\frac{di_2}{dt} - M_{31}\frac{di_1}{dt} \tag{A.2}$$

$$i_1 = i_2 + i_3 \tag{A.3}$$

Solve Equations (A.2) and (A.3), and note that $L_2 = L_3$ and $M_{23} = M_{32}$, one can obtain

$$\frac{di_2}{dt} = \frac{(L_3 - M_{31} + M_{21} - M_{23})}{2(L_2 - M_{23})}\frac{di_1}{dt} \tag{A.4}$$

Similarly,

$$\frac{di_3}{dt} = \frac{L_2 - M_{23} + M_{31} - M_{21}}{2(L_2 - M_{23})}\frac{di_1}{dt} \tag{A.5}$$

Substitute Equations (A.4) and (A.5) into (A.1), and finally, $L_{coplanar}$ can be shown to be:

$$L_{coplanar} = (L_1 - M_{21}) + \frac{L_2 + M_{23} - M_{12} - M_{13}}{2} + \frac{(M_{21} - M_{31})(L_2 - M_{12} - M_{23} + M_{13})}{2(L_2 - M_{23})} \tag{A.6}$$

Assume that all wires have round cross sections for simplicity in the derivations, Equations (3.11) and (3.12) can be used. Also assuming the wire lengths are much longer than the cross sections and separations of the wires, i.e. $\frac{d}{l} \simeq 0$, $\frac{r}{l} \simeq 0$, and no internal inductance[3], Equations (3.11) and (3.12) can be simplified as

$$M = \frac{\mu_0}{4\pi} \times 2l \left[\ln\left(\frac{2l}{d}\right) - 1\right] \tag{A.7}$$

$$L = \frac{\mu_0}{4\pi} \times 2l \left[\ln\left(\frac{2l}{r}\right) - 1\right] \tag{A.8}$$

[3]Therefore, infinite frequency is assumed.

Substituting these two equations into Equation (A.6) and after suitable algebraic manipulations, one obtains,

$$L_{coplanar} = \frac{\mu_0 l}{2\pi}[\ln(\frac{d}{r_{sig}}) + \frac{1}{2}\ln(\frac{d}{r_{gnd}}) + \frac{1}{2}\ln(1-\frac{1}{\alpha}) + \frac{1}{2}\frac{\ln\frac{w_p}{(\alpha-1)r_{gnd}}}{\ln\frac{w_p}{r_{gnd}}}\ln(\alpha-1)] \qquad (A.9)$$

where r_{sig} and r_{gnd} are the equivalent radii of the signal and ground wires. Parameter w_p is ground wire pitch, and d is the center-to-center distance of the signal wire to the nearest ground wire. Parameter α is the ratio of ground wire pitch, w_p, to d, and $\alpha \geq 2$.

If an approximation is made that $2\pi r = 2(w+t)$ for all the wires, i.e., the perimeter of a rectangular wire cross section equals the circumference of the round cross section of the equivalent wire[4], the final formula becomes:

$$L_{coplanar} = \frac{\mu_0 l}{2\pi}[\ln(\frac{\pi d}{w_{sig}+t}) + \frac{1}{2}\ln(\frac{\pi d}{w_{gnd}+t}) + \frac{1}{2}\ln(1-\frac{1}{\alpha}) + \frac{1}{2}\frac{\ln\frac{\pi w_p}{(\alpha-1)(w_{gnd}+t)}}{\ln\frac{\pi w_p}{w_{gnd}+t}}\ln(\alpha-1)] \qquad (A.10)$$

and,

$$\hat{L}_{coplanar} = \frac{\mu_0}{2\pi}[\ln(\frac{\pi d}{w_{sig}+t}) + \frac{1}{2}\ln(\frac{\pi d}{w_{gnd}+t}) + \frac{1}{2}\ln(1-\frac{1}{\alpha}) + \frac{1}{2}\frac{\ln\frac{\pi w_p}{(\alpha-1)(w_{gnd}+t)}}{\ln\frac{\pi w_p}{w_{gnd}+t}}\ln(\alpha-1)] \qquad (A.11)$$

which was shown in Chapter 4.

The frequency dependent term can also be added to this formulae to model the skin effects and internal inductances as was provided in Chapter 4.

[4]This assumption is reasonable since external inductance is more related to the perimeter of a conductor other than the area of the cross section of a conductor [77].

Appendix B

Coordinate System Transformation

B.1 The Basics

The rotation of a coordinate system is used in Chapter 5. Generally, the coordinate system rotations are assumed in the following order, and the final position of the transformed coordinate axes is achieved in three steps [47].

1. Rotate the x, y, z system of axes through ϕ_z about the z axis. This moves the x axis to x_1 and the y axis to y_1. The z_1 axis is identical to the z axis.

2. Rotate the x_1, y_1, z_1 system of axes through ϕ_y about the y_1 axis. This moves the x_1 axis to x_2 and the z_1 axis to z_2. The y_2 axis is identical to the y_1 axis.

3. Rotate the x_2, y_2, z_2 system of axes through ϕ_x about the x_2 axis. This moves the y_2 axis to y_3 and the z_2 to z_3. The x_3 axis is identical to the x_2 axis.

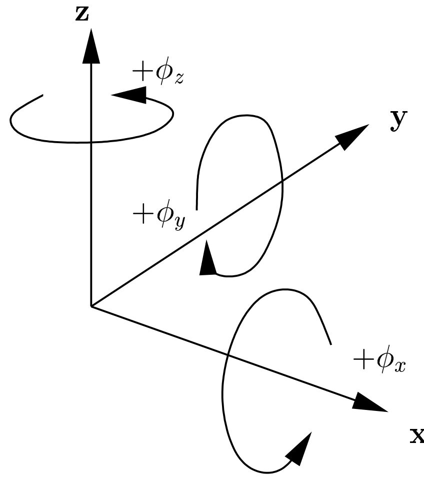


Figure B.1: The Rotation convention.

Apply the right-hand rule to define the algebraic sign of a rotation. Looking toward the origin from a point on the z axis, a positive rotation is counterclockwise; similarly for the x and y axes. See Fig. B.1.

The matrix of rotation around z is shown below.

$$\mathbf{R_z} = \begin{bmatrix} \cos\phi_z & \sin\phi_z & 0 \\ -\sin\phi_z & \cos\phi_z & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{B.1}$$

For rotation about the x or y axis, the matrices are

$$\mathbf{R_x} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos\phi_x & \sin\phi_x \\ 0 & -\sin\phi_x & \cos\phi_x \end{bmatrix} \tag{B.2}$$

and

$$\mathbf{R_y} = \begin{bmatrix} \cos\phi_y & 0 & -\sin\phi_y \\ 0 & 1 & 0 \\ \sin\phi_y & 0 & \cos\phi_y \end{bmatrix} \tag{B.3}$$

respectively.

For successive rotations, the total rotation matrix is

$$\mathbf{R_{total}} = \mathbf{R_x}(\phi_\mathbf{x})\mathbf{R_y}(\phi_\mathbf{y})\mathbf{R_z}(\phi_\mathbf{z})$$

It represents the rotation sequence as shown in the convention, i.e. first rotates about z, then rotates about y, and lastly about x. If the original coordinate system is $\mathbf{P}$, the final rotated coordinate system then is $\mathbf{P}' = \mathbf{R_{total}}\mathbf{P}$. For the backward rotation transformation, it is obvious that

$$\mathbf{R_{totalback}} = \mathbf{R_z}(-\phi_\mathbf{z})\mathbf{R_y}(-\phi_\mathbf{y})\mathbf{R_x}(-\phi_\mathbf{x})$$

B.2 Other Relationships Used in the Thesis

In Chapter 5, since assumption is made that there is no rotation about y axis, the sequence of rotations is made that the first rotation is about x axis, and the second rotation is about z axis.

As was explained in Chapter 5, the ϕ_x and ϕ_z needs to be solved based on α and β, see Fig. 5.2. By multiplying the backward rotation matrix[1] with a unit vector (100)

[1]The total backward rotation is rotation around z first and then rotation around x.

representing the x' axis, this vector's coordinates in the xyz coordinate system are obtained as a function of ϕ_x and ϕ_z. Using Equation (5.1), ϕ_x can be solved. Similar, By multiplying the backward rotation matrix with a unit vector (010) representing the y' axis and using Equation (5.2), ϕ_z can be derived.

For unit vector of x' axis,

$$\underbrace{\begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos\phi_x & -\sin\phi_x \\ 0 & \sin\phi_x & \cos\phi_x \end{bmatrix}}_{\text{Backward rotation around } x} \overbrace{\begin{bmatrix} \cos\phi_z & -\sin\phi_z & 0 \\ \sin\phi_z & \cos\phi_z & 0 \\ 0 & 0 & 1 \end{bmatrix}}^{\text{Backward rotation around } z} \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} q_x \\ q_y \\ q_z \end{bmatrix}$$

It is straight forward to solve for

$$\tan\alpha = \frac{q_y}{q_x} = \cos\phi_x \tan\phi_z \tag{B.4}$$

Likewise, for unit vector of y' axis,

$$\begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos\phi_x & -\sin\phi_x \\ 0 & \sin\phi_x & \cos\phi_x \end{bmatrix} \begin{bmatrix} \cos\phi_z & -\sin\phi_z & 0 \\ \sin\phi_z & \cos\phi_z & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} = \begin{bmatrix} r_x \\ r_y \\ r_z \end{bmatrix}$$

and solve for

$$\tan\beta = \frac{r_y}{r_x} = -\frac{\cos\phi_x}{\tan\phi_z} \tag{B.5}$$

Solve Equations (B.4) and (B.5), one can get

$$\cos\phi_x = \pm\sqrt{-\tan\alpha\tan\beta} \tag{B.6}$$

$$\tan\phi_z = \pm\sqrt{\frac{-\tan\alpha}{\tan\beta}} \tag{B.7}$$

Properly consider the signs, the rotated system can be finally defined.

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