AC and Noise Analysis of Deep-submicron MOSFETs

A DISSERTATION

SUBMITTED TO THE DEPARTMENT OF

ELECTRICAL ENGINEERING

AND THE COMMITTEE ON GRADUATE STUDIES OF

STANFORD UNIVERSITY

IN PARTIAL FULLFILLMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

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February 2004

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ABSTRACT

The *AC* and noise simulation of deep-submicron MOS device has emerged as a very important issue as device size scales down and the operational frequency of CMOS circuit rises. However, the quantum mechanical effects and high energy carriers in deep-submicron devices impede the accurate computer simulations.

As the MOSFET size scales down, the physical oxide thickness gets thinner, and the potential well under gate oxide splits the energy bands into subbands and causes quantum mechanical effects. Also, shorter channel lengths increase the electric field in the channel, invalidating the quasi-equilibrium condition. The carriers in the channel are accelerated to have several times more kinetic energy from the high electric field, the noise behavior of deep-submicron MOSFETs deviates from the long channel MOSFET noise model. This dissertation explores the computer simulation techniques to overcome those modeling obstacles and explaines the underlying physics of noise modeling.

The *density-gradient* model is an efficient approach to simulate the quantum mechanical effects without solving the complex multi-dimensional Schrödinger equations. The *density-gradient* model enables multi-dimensional *AC* simulation with quantum mechanical corrections, maintaining good accuracy and reasonable computational speed. From measurement and device simulations, it is shown that the substrate doping profile also has close relation with the quantum mechanical effects.

For noise simulations, the *impedance field* method with the *hydrodynamic* model is used to account for high energy carrier effects. A new local noise source model is developed based on the *hydrodynamic* carrier transport model. From measurement and simulations, the mechanisms of excess noise generation in deep-submicron MOSFETs are identified.

The high energy carriers and modified *impedance field* are both responsible for the excess noise generation. Contributions from the source side of the channel dominate drain current noise, indicating an accurate local noise source model is most important for drain noise simulation. On the contrary, the gate resistance and high energy electrons near the drain mainly create gate current noise. The gate voltage is also an important factor to gate current noise, controlling the number of high energy carriers contribute gate current noise. In addition, the correlation coefficient between gate and drain current noise in deep submicron MOSFET devices is determined by gate bias and gate resistance. Due to increased gate resistance with MOSFET scaling, consideration of gate resistance in RF front-end design has greater importance.

ACKNOWLEDGMENTS

My graduate student life in Stanford was the most exciting, joyful and rewarding experience in my life. Especially, those people who have ever accompanied me during my study are the most memorable parts. Hereby, I would like to show my best appreciation to the people who helped me to have this great time.

First of all, I would like to thank to my adviser, Professor Robert W. Dutton for his enthusiastic guidance throughout my Ph.D. study. He gave me such a great opportunity to participate in the TCAD group and let me purse my research interest. Under his passionate guidance, I was able to dedicate myself to the research and develop my specialty with comfort and confidence. Professor Robert is not only an outstanding scholar but also a great mentor with perspective and patience. I can't forget his continued support and care on my study and also career. Without his help, my Ph.D. thesis wouldn't be able to be completed so successfully.

Moreover, I would like to express my special thanks Professor Krishna Saraswat and Professor James Harris for serving on my oral committee members and careful review of Ph.D. Thesis. Professor Krishna Saraswat gave me great advices as associative adviser for my Ph.D. study and adviser for my master study. I am also grateful to Anthony E. Siegman who agreed to be the chairman of my oral committee in spite of his busy schedule. Their precious opinions and feedback make this thesis more completed and organized.

In addition, I am very fortunate to have the participation of Professor Christoph Jungemann, who gave me many critical advises at the final stage of my study. His profound knowledge and understanding on numerical simulation and physics enabled me to overcome many obstacles in device simulation and programming. He also spent huge effort and time to debug my C program codes. Because of his detailed review, I am able to avoid many mistakes in this research.

Also, I would like to show my appreciation to Professor Zhiping Yu in Ching-hwa university, who lead my study for a long time as a senior research scientist in Stanford. His hearty advice and discussion made my research on device simulation mature and concrete.

I would like to thank Andries J. Scholten of Philips, who kindly offered measured data of noise for my study.

I would like to thank to TCAD group staffs, Daniel Yergeau, Fely Barrera and Miho Nishi for always offering me excellent support. I would like to thank to my group mates, Li-chang, Chosu, Jae-wook, Reza, Eric, Jung-hoon and Hai.

Special thanks go to my former officemates, Kwang-hoon Oh and Chang-hoon Choi. Their abundant knowledge and experience always helped me when I met any difficulty in my study. Moreover, their sincere friendship always made my study in Stanford so enjoyable. I owe them so much.

I would like to acknowledge to my friends in Stanford, Ki-young, Dong-hyun, Jae-won, So-young, Jin-woong, Hyun-soo, Won-il and others. They have always been beside of me and the time I spent with them was always so refreshing and pleasant.

Finally, I would like show my sincerest appreciation to my family, my parents, my sisters and my wife for their support and love. Their encouragement is always my greatest motivation on study.

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INTRODUCTION

1. 1 Motivation

The demand for low-power and high-speed circuits, and development of device fabrication technology continue to drive the scaling down MOS devices under 0.1μm channel length. Currently, many CMOS circuits are operated with 1.2V supply voltage and some are running in GHz range of operating frequency. At this level of device scaling, some dimensions of the MOS device, such as gate thickness became comparable to atomic dimensions, therefore quantum mechanical corrections in device simulation are indispensable. Also, the operating voltage cannot be scaled down with the same ratio as that for the device in order to maintain adequate threshold voltage that limits leakage current within a reasonable level, hence the electric field in the device become so large that accelerated carriers can have kinetic energy more than ten times than that thermal energy.

There are two major problems that come with the quantum mechanical effects resulting from thin gate oxides. One is tunneling current through the gate oxide; the other is carrier energy quantization at the boundary between the oxide and silicon. Due to tunneling current, the minimum gate oxide thickness is kept to above 20Å where the tunneling current is not causing significant leakage current and oxide damage. The quantum confinement effect at the oxide boundary increases oxide thickness effectively, and the threshold voltage is shifted; capacitance and other device parameters are consequently changed.

The supply voltage also scales down with device scaling, however, it cannot follow the speed of channel length reduction. Therefore, the maximum electric field for a minimum size MOS transistor rises to the tens of volts/μm level. The carriers in the device are accelerated by this electric field and acquire excessive kinetic energy. These high energy carriers are called "hot-carriers" because they have effective temperatures of several thousands of carrier temperatures. The hot-carriers occur at the drain junction where the electric field is highest in a MOS device. To lose this excessive kinetic energy from scattering, the carrier needs to travel tens of nanometer s which is on the order of half the channel length of the smallest devices currently in mass production. This effect is also called velocity overshoot because the carriers travel at higher velocity than the scatter-limited saturation velocity. Therefore the carrier distribution along the channel is changed and more carriers are injected from the source. The high energy carriers also cause excess noise because of these high carrier temperatures and impedance field modification along the channel.

To extract parameters of such scaled devices for circuit simulations, *AC* simulations accounting for advanced transport effects are required. The *density-gradient* model is a first-order quantum-mechanical correction to the classical drift-diffusion transport formulation and faithfully describes the quantum mechanical effects at oxide boundaries. Without computing a rigorous solution of the Schrödinger equation, *Density-gradient* enables a simple extension of classical drift-diffusion; the same approaches can also be applied in *AC* simulations. The *hydrodynamic* model can illustrate the gain and loss of kinetic energy of carriers; they are also called the energy-balance equations. *Hydrodynamic* model is also useful for noise simulations, where the carrier energy has an important role in noise generation.

The noise parameters in a short channel MOS device are reported to increase as the channel length scales down. However, the amount and origin of the increased noise is still debatable. Full 2-D noise simulation based on the *hydrodynamic* model and impedance-field method can explain this effect. The impedance field method uses the same linear system as is used for *AC* simulation, therefore *AC* and noise simulation are closely related.

Prophet is a PDE level device simulator and provides a good platform to program simulation models for noise, based on its generality and flexibility. A user can implement his own carrier transport models in the C programming language. Also the post processing routine can be programmed as modules, thus enabling exploration of physical effects in the device.

1.2 Definition of noise

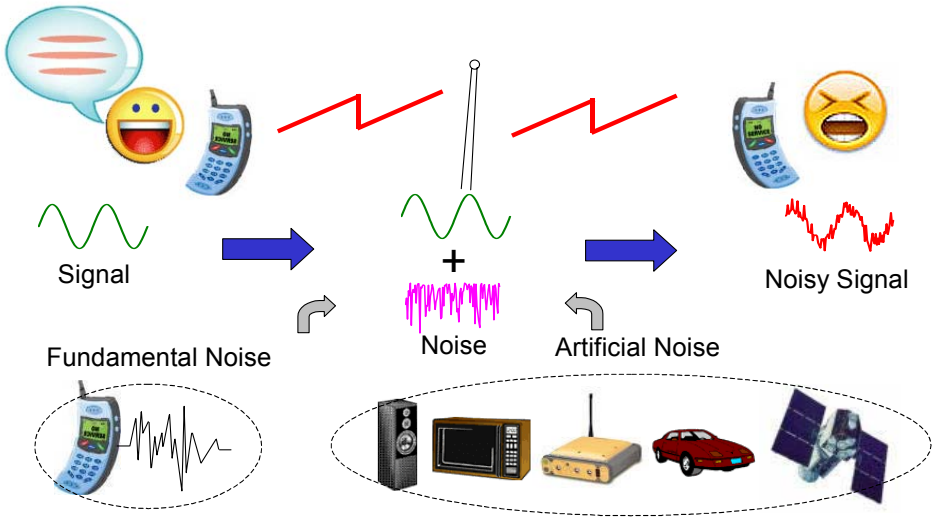


Fig 1.1 Definition of noise and various noise sources

The definition of noise is “A disturbance that obscures or reduces the clarity of a signal”. For an example, when we are doing wireless communications, the signal is always affected by noise, the receiver must cope with and overcome noisy signals. The source of this noise can be classified to two categories.

One is artificial noise created by numerous noise sources from the environment. Unwanted signals may enter the system together with our voice information. Also, the encoding and modulation circuits experience electromagnetic interference from other appliances. The transmitting signal is also mixed with other noise and becomes distorted. The effect from artificial noise can be reduced by choosing a less noisy environment or strengthen the signal power, there by improving the signal-to-noise ratio.

The other source of noise is fundamental noise created by the circuits or devices. Every electronic device generates its own intrinsic noise; other devices operating on the same chip also induce noise. The digitization and processing algorithm of signal inevitably creates noise. These effects from fundamental noise cannot be reduced unless we change the system architecture. Once we decide the fabrication process of our chip, the amount intrinsic device noise is fixed.

Modeling can provide understanding of this intrinsic noise and aid in design optimization of circuits.

Due to the randomness of noise, we need to use statistical approaches for its characterization. Generally, the average of noise current is zero, hence the power spectral density of noise per unit frequency is used for the expression of noise.

1.3 Intrinsic Noise Source in Semiconductor Device

The intrinsic noise in a semiconductor device is generated by several different mechanisms. Due to the difference of these mechanisms, the frequency behavior of noise becomes complex. Several major noise generation mechanisms in MOS transistors are reviewed here.

1.3.1 Thermal Noise

Thermal noise is also referred as Johnson-Nyquist noise from the name of researchers who first measured and empirically determined to the equation of thermal noise[1]. It is also called diffusion noise in non-equilibrium conditions. The scattering of electrons with the surrounding lattice makes them have random motion, and this randomness appears as thermal noise at electrodes. The power spectral density of this thermal noise in a resistance is well known as following voltage noise equation :

$$\overline{e_n^2} = 4k_B RT\Delta f \tag{1.1}$$

where k_B is the Boltzmann constant, R is the total amount of the resistance, Δf is the range of frequency in interest, and T is the temperature of the semiconductor device.

As shown in Equation 1.1, the power spectral density of thermal noise is independent of frequency and linearly proportional to resistance and temperature. However, it is expected that thermal noise may finally start to reduce above several terahertz, because the correlation between each scattering event of an electron will prevent generation of extremely high frequency thermal noise. Therefore, the total power of thermal noise cannot be infinite following the laws of physics.

However, thermal noise remains constant at the level predicted in Equation 1.1 for frequencies of interest for practical electric applications, and that is the reason engineers usually

regard the spectrum of thermal noise as “white”. This frequency independent property makes thermal noise a dominant noise source for RF applications.

1.3.2 Generation-Recombination Noise

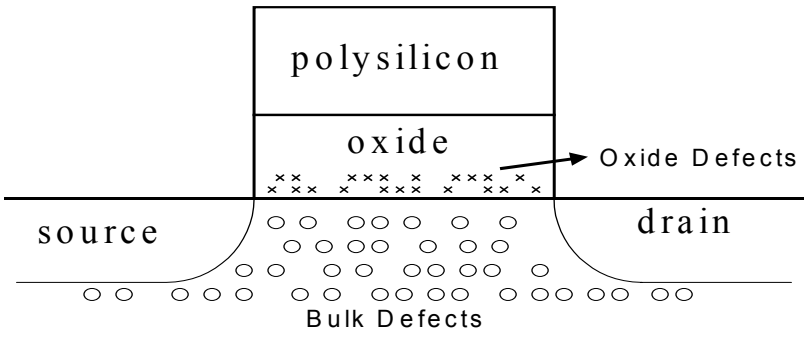


Fig 1.2 Low frequency noise sources in MOS structure. The bulk defects in silicon create generation-recombination noise and oxide defects at the oxide-silicon interface create flicker noise.

Carrier generation-recombination processes can fluctuate the number of carriers that participate in current flow, creating current noise. This noise is called generation-recombination noise and it cannot be detected in the equilibrium condition where there is no current. It usually has a low frequency noise behavior because the frequency is limited by physical generation-recombination processes. However, if impact ionization starts to occur, it is no longer a low frequency process.

The generation-recombination noise in MOS transistors originates from bulk silicon defects, especially in depletion region[2]. The defects create traps that capture or release carriers. The generation-recombination noise is known to have a correlation with diffusion noise[3]. Diffusion noise is generated by the scattering events of carriers; a carrier is trapped or another carrier is released if a trap participates in the scattering. Therefore, the velocity change of a carrier and the fluctuation of carrier number is created by a single event, thus creating correlation.

The magnitude of generation-recombination noise in MOS is usually much smaller than 1/f noise. The noise model of generation-recombination noise has the following form[4] :

$$S_I(f) = \frac{C\tau_0}{1+\omega^2\tau_0^2} \tag{1.2}$$

where τ_0 is time constant of the trapping process, and C is a constant related with defect concentrations. As seen in equation 1.2, the amount of generation-recombination noise is relatively constant at very low frequency and decrease rapidly above a certain frequency defined by $1/\tau_0$.

1.3.3 Flicker (1/f) noise

Although many researchers studied flicker noise for a long time, the exact mechanism is still uncertain. Flicker noise of a MOS transistor is assumed to originate from interfacial oxide traps[2]. At the interface between oxide and silicon, many dangling bonds appear creating available energy states. These interfacial oxide traps randomly trap and release charge in the channel. Flicker noise cannot be modeled easily because it is generated from surface defects which depend on the CMOS fabrication process. Also, PMOS transistors are generally observed to generate less flicker noise than NMOS transistors because the buried channel in PMOS transistors helps the holes to maintain some distance from interfacial traps.

Flicker noise also exists in bipolar transistors, where the defects at the base-emitter junction contribute to flicker noise. Generally, MOS transistors have higher flicker noise than bipolar transistors, because surface channel conduction property of MOS transistors dominates compared with the bulk conduction properties of bipolar transistors.

Flicker noise is also called 1/f noise because the magnitude is approximately inversely proportional to frequency. A typical 1/f noise model of a MOS transistor has following form[5].

$$S_I(f) = \frac{K}{WLC_{ox}^2}\frac{1}{f^\gamma} \tag{1.3}$$

where K is a device-specific constant, and γ is a constant typically between 0.8 and 1.2. Flicker noise does not strongly depend on temperature, and larger gate area and unit area oxide capacitance will reduce the flicker noise because larger gate capacitance smoothes the fluctuations of the channel charges. Therefore, sometimes the transistors in low-noise applications have large gate area to suppress 1/f noise.

The 1/f frequency property of flicker noise makes it the dominant noise source in low frequency applications. Fig. 1.3 shows the expected power spectral density of drain noise for a MOS transistor[3]. The frequency where the amount of flicker noise and thermal noise is equal is called “corner frequency”. The corner frequency of a MOS transistor is usually in the tens of kilohertz to megahertz range, which much higher than that of a bipolar transistor.

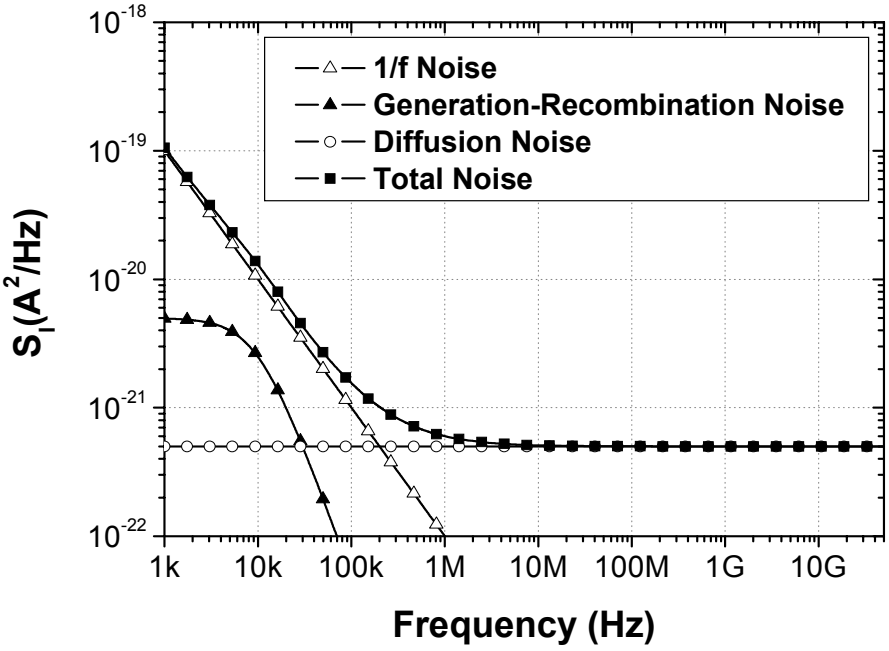


Fig 1.3 Expected frequency behavior of drain current noise in MOS transistors.

1.4 Thesis Outline

This dissertation provides detailed information and techniques for computer simulations and analyzes the *AC* and noise behavior to explain various phenomenon occurring in deep-submicron MOSFETs. The density-gradient model and hydrodynamic models have been implemented in a device simulator, Prophet; the computer simulations in this dissertation were performed using this code[6].

Chapter 2 presents the *AC* analysis method including quantum mechanical corrections. The quantum mechanical effects for thin gate oxide devices are demonstrated using the density-gradient model which can accurately describe the quantum mechanical effects in a device. The *AC* analysis method based on the *density-gradient* model is developed, and the simulation results are compared with measured data. Also, the change of device properties owing to physical parameters, such as channel doping and gate oxide thickness are simulated; reasons for device property changes are explained.

Chapter 3 gives an introduction to the *hydrodynamic* transport model and numerical techniques for its computer simulations. The discritization scheme and numerical method for equation coupling between carrier energy and momentum are discussed. Simulation results show the amount of kinetic energy a carrier acquires in the high electric field conduction, as well as effects on *DC* and *AC* characteristics of the device.

Chapter 4 presents the underlying theories of noise simulation. First a multi-dimensional noise simulation method, the impedance field method, is introduced. Second, the local noise source model is derived using a microscopic approach. Third, the corrections required to be applied in classical local noise source model are explained. Finally, numerically efficient techniques to save the computation time of impedance field are provided.

Chapter 5 illustrates noise simulation results based on the theories in chapter 3 and 4, and investigates the physics of noise generation in deep-submicron MOSFETs. Noise simulation results of drain and gate currents are shown and compared with measured data. The noise generation mechanism is explained, and the correlation between gate and drain current noise is explored. The results from long and short channel MOS transistors are contrasted, and the dependency on DC bias is explained. Finally, effects of parasitic resistance on noise behavior are discussed.

Finally, Chapter 6 summarizes the main results and contributions of this dissertation and gives suggestions for future work.

CHAPTER 2

AC analysis with Density-Gradient Model

For MOS technology in the deep submicron region, thinner gate oxides and higher substrate dopings are required to ensure proper device operation. However, combined with gate bias, they create a potential well at the oxide boundary. This well produces a quantization effect in the channel charge. The well splits the conduction band into discrete subbands, therefore the maximum electron concentration is located a few angstroms under the oxide as shown in Fig 2.1. This effect causes a deviation of effective oxide thickness from the physical oxide thickness which in turn reduces the gate capacitance and drain current with bias.

Calculation of gate capacitance including this quantum mechanical effect has been considered using various methods[7-10]. Most methods relies on finite difference formulations and do not separate the gate capacitance into its constitutive components, Cgs, Cgd, and Cgb, which are very important for circuit design.

In this chapter, an *AC* analysis using the density-gradient model is presented which includes previously described quantum mechanical effects with minimal corrections, using the classical drift-diffusion transport theory. The effects of oxide thickness and substrate doping on the threshold voltage and gate capacitance will also be explored.

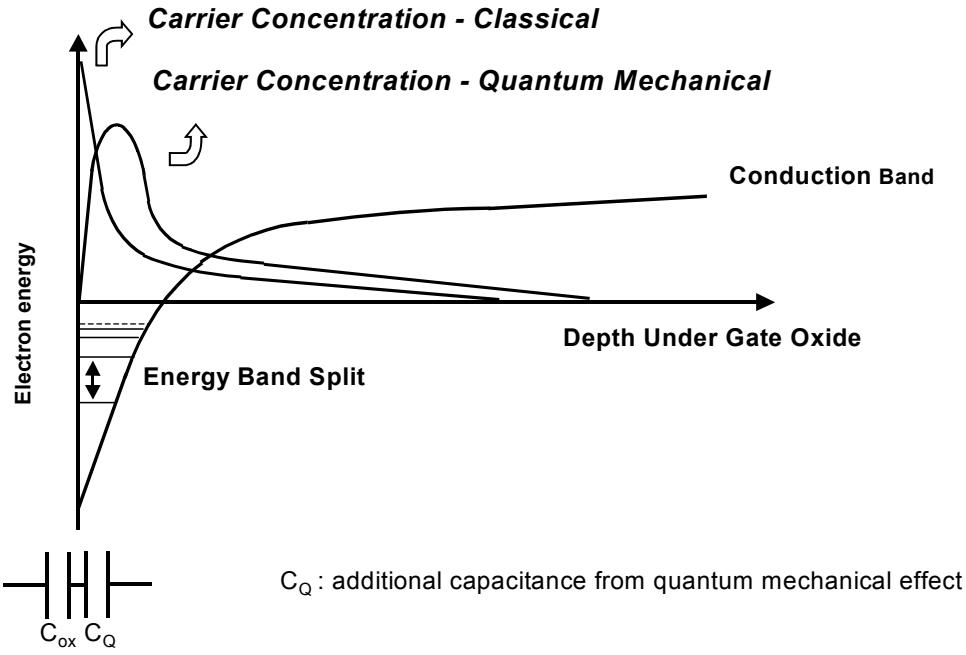


Fig. 2.1 Quantum mechanical effects under thin gate oxide and additional capacitance from carrier distribution change.

2. 1 Density-Gradient Method

The aggressive scaling of MOS transistors makes quantum mechanical effects have an important role in device operation, for example quantum confinement effects and gate tunneling current. The most physically accurate way to simulate these quantum mechanical effects is based on solving the Schrödinger equation self-consistently.

There have been many attempts to solve the Schrödinger equation using a one-dimensional simplification, perpendicular to the oxide-silicon surface. However, there has been no significant progress in multi-dimensional simulation with Schrödinger equation solver. The Schrödinger equation is mathematically complex and requires a long time to obtain a solution. Also the non-local nature of the wave equations create direct coupling between all grid points, making the Jacobian matrix non-sparse. This property slows down the iteration process to get a solution, and

requires huge memory allocations for multi-dimensional simulations. Currently, a full multi-dimensional Schrödinger equation solver for semiconductor device simulation is impractical

Various researchers have developed approximation methods for multi-dimensional device simulation with quantum mechanical corrections. One of the popular methods is one suggested by van Dort et al.[10], which describes the quantum mechanical effect using a band edge shift due to electric field. This method is created from the lowest eigenenergy of a particle in a triangular potential well. However, it gives only a solution with limited accuracy, and its generalization is difficult due to the case specific nature of its derivation.

The density-gradient method is a generalization of the classical drift-diffusion method including first-order quantum effects. An additional term with the gradient of carrier density enables the system to model the quantum mechanical effects with good accuracy. Moreover, the numerical approaches used to solve the classical drift-diffusion model still can be applied due to the simplicity of the method. Semiconductor engineers can easily gain a useful insight from density-gradient method, because the variables are familiar. For example, carrier concentration and mobility are still used for simulation. The density-gradient method can also be used for multi-dimensional simulation with reasonable additional computational cost compared to the drift-diffusion method.

In a region of quasi-equilibrium the electron and hole fluxes are expressed as

$$\overrightarrow{F_n} = \mu_n n \nabla \phi_n \tag{2.1}$$

$$\overrightarrow{F_p} = -\mu_p p \nabla \phi_p \tag{2.2}$$

where ϕ_n and ϕ_p are quasi-Fermi potentials for electrons and holes, respectively. In the classical regime, the quasi-Fermi potentials under isothermal conditions are calculated by Fermi-Dirac statistics, or its approximation, as a Maxwell-Boltzmann distribution. In Maxwell-Boltzmann case, the quasi-Fermi potentials are expressed as :

$$\phi_n = \Phi_n + \frac{kT}{q} \ln\left(\frac{n}{n_c}\right) \tag{2.3}$$

$$\phi_p = -\Phi_p + \frac{kT}{q} \ln\left(\frac{p}{n_v}\right) \tag{2.4}$$

Φ_n and Φ_p are energy levels of conduction and valence bands respectively. n_c and n_v are effective density of states of conduction and valence bands, repectively

When the carrier concentration is very high and the gradient is large such as in the inversion layer of the MOS transistor, an additional density-gradient term is required for the first-order approximation to the nonlocality of quantum mechanics[11]. Although, it is a first-order approximation, it is still capable of describing quantum mechanical effects such as quantum confinement and tunneling. The generalized quasi-Fermi potentials are as following :

$$\phi_{n\,DG} = \phi_n + \frac{2\nabla \cdot (b_n \nabla \sqrt{n})}{\sqrt{n}} \tag{2.5}$$

$$\phi_{p\,DG} = \phi_p - \frac{2\nabla \cdot (b_p \nabla \sqrt{p})}{\sqrt{p}} \tag{2.6}$$

where b_e and b_h are constants which control the strength of the gradient effects. They are represented as

$$b_n = \frac{\hbar^2}{4qm_n^*\gamma} \tag{2.7}$$

$$b_p = \frac{\hbar^2}{4qm_p^*\gamma} \tag{2.8}$$

γ is a dimensionless statistical parameter for averaging the quantum phenomenon, and they approach three in high temperature and carrier density conditions. Therefore, the flux equation terms of the density-gradient method become:

$$\overrightarrow{F_n} = -\mu_n n \nabla \psi - D_n \nabla n - 2\mu_n b_n \nabla \left(\frac{\nabla^2 \sqrt{n}}{\sqrt{n}} \right) \tag{2.9}$$

$$\overrightarrow{F_p} = \mu_p p \nabla \psi - D_p \nabla p - 2\mu_p b_p \nabla \left(\frac{\nabla^2 \sqrt{p}}{\sqrt{p}} \right) \tag{2.10}$$

where ψ is the electric potential.

Taking the divergence of flux in Equations 2.9 and 2.10 creates a forth order spatial differentiation of $\sqrt{n}$ and $\sqrt{p}$; higher order spatial differentiations are not suitable for numerical

simulations because large numerical errors are generated by the discrete nature of numerical simulations. Therefore, the flux equations of the *density-gradient* model are usually separated into two equations. Finally, the full equations of the *density-gradient* model become:

$$\nabla \cdot (\varepsilon \nabla \psi) + q(p - n + N_D^+ - N_A^-) = 0 \tag{2.11}$$

$$\nabla \cdot (b_n \nabla \sqrt{n}) + \frac{\sqrt{n}}{2}(\psi - \frac{kT}{q} \ln \frac{n}{n_i} - \phi_n) = 0 \tag{2.12}$$

$$\nabla \cdot (b_p \nabla \sqrt{p}) - \frac{\sqrt{p}}{2}(\psi + \frac{kT}{q} \ln \frac{p}{p_i} - \phi_p) = 0 \tag{2.13}$$

$$\nabla \cdot (\mu_n n \nabla \phi_n) - \frac{\partial n}{\partial t} - r = 0 \tag{2.14}$$

$$\nabla \cdot (\mu_p p \nabla \phi_p) + \frac{\partial p}{\partial t} + r = 0 \tag{2.15}$$

Maxwell-Boltzmann distributions are assumed for electron and hole densities. All symbols have their conventional meaning; and the r term represents net recombination rate.

2. 2 Formulation of *AC* system

The technique used for sinusoidal *AC* analysis is basically the same as that for the drift-diffusion model presented by S. E. Laux[12]. To run *AC* analysis, $\frac{\partial n}{\partial t}$ and $\frac{\partial p}{\partial t}$ are replaced with $j\omega n$ and $j\omega p$, respectively where n and p are complex values. The $j\omega$ term appears in order to represent the carrier density as $ne^{j\omega t}$ and $pe^{j\omega t}$. Differentiating them by t and dropping the $e^{j\omega t}$ yields the above terms involving $j\omega$. The system variables are $\sqrt{n}$ and $\sqrt{p}$ instead of n and p. Applying the chain rule to $\frac{\partial n}{\partial t}$ and $\frac{\partial p}{\partial t}$, the results are :

$$\frac{\partial n}{\partial t} = \frac{\partial n}{\partial(\sqrt{n})}\frac{\partial(\sqrt{n})}{\partial t} = 2\sqrt{n}\,\frac{\partial(\sqrt{n})}{\partial t} \tag{2.16}$$

$$\frac{\partial p}{\partial t} = \frac{\partial p}{\partial(\sqrt{p})}\frac{\partial(\sqrt{p})}{\partial t} = 2\sqrt{p}\,\frac{\partial(\sqrt{p})}{\partial t} \tag{2.17}$$

Substituting 2.16 and 2.17 into the density-gradient equations sets, the *AC* system becomes

$$\begin{pmatrix} J & -\omega D \\ \omega D & J \end{pmatrix}\begin{pmatrix} x_r \\ x_i \end{pmatrix} = \begin{pmatrix} B \\ 0 \end{pmatrix} \tag{2.18}$$

$$D = \begin{pmatrix} D_1 & 0 & \cdots & 0 \\ 0 & D_2 & & 0 \\ \vdots & & \ddots & \vdots \\ 0 & 0 & \cdots & D_n \end{pmatrix} \tag{2.19}$$

$$D_k = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & -2\sqrt{n_k} & 0 & 0 & 0 \\ 0 & 0 & 2\sqrt{p_k} & 0 & 0 \end{pmatrix} \tag{2.20}$$

where k is the node number. Equation 2.18 is the same as the equation system used for the classical model [12]; however, the matrix D in 2.18 is changed as shown in 2.19. B is a voltage drive vector which has non-zero real values in the rows corresponding to the rows of potential and quasi-Fermi level in nodes of the contact where *AC* signal is applied. The system variable for Equation 2.12 is $\sqrt{n}$ and its time derivative is determined using Equation 2.14. Also, the system variable for Equation 2.13 is $\sqrt{p}$ and its time derivative comes from Equation 2.15. Therefore, D_k has non-zero elements only in the 3rd lower diagonal

To solve the *AC* system, a preconditioning method based on the work Ke-chih Wu[13] was used. The preconditioner moves the off-diagonal elements in D into the diagonal, introducing ω^2 terms. This preconditioning process makes the *AC* system simple and saves memory usage. The ω^2 terms increase the diagonal dominance with higher frequencies. The current at each contact is calculated by summing the flux through edges which contain nodes in the contact. The DC simulation at each bias point is performed in a script-level partial differential equation solver,

PROPHET[14] and the *AC* analysis was coded in the C language as a post-processing plug-in module.

2. 3 Density-gradient simulation results

AC simulations for different gate oxide thickness and doping level were performed. 1-D MOS capacitors were simulated and compared with measured data. Then, 2-D MOS transistors were simulated to separate the gate capacitance into the respective components: Cgs, Cgd and Cgb. 2-D MOS transistor simulations also provide current-flow related information, such as transconductance.

2.3.1 1-D MOS simulation

Fig. 2.2 is the gate capacitance extraction result of a MOS capacitor with 21Å gate oxide thickness. The simulation results agree with measured data in all regions. The *AC* analysis of the classical drift-diffusion model predicts much higher capacitance in the accumulation and inversion regions, because of the well, created by band bending, and occurs close to the surface. The energy levels in the quantum well are quantized, therefore, the electron concentration under the gate oxide peaks a few angstroms from the surface. This effect is shown in Fig. 2.4. The device structure is the same as the one in Fig. 2.2; 1.0V gate bias voltage was applied. The maximum of electron concentration is located approximately 0.001 μm under the oxide, which correspondsabout 20% of the oxide thickness.

Fig. 2.3 shows the *AC* analysis result of a MOS transistor with 31Å gate oxide thickness. The simulation results also agree well with measured data. Compared with Fig. 2.2, Fig. 2.3 predicts a noticeably lager threshold voltage (V_{th}) shift from the classical model. The substrate doping is lager in the MOS device used for Fig. 2.3, which accounts for the shift.

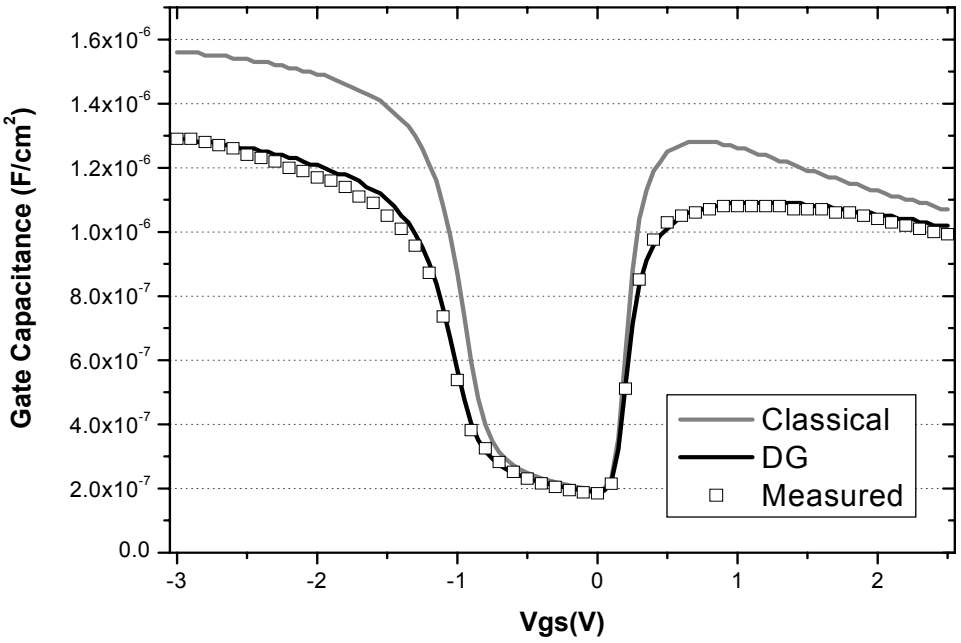


Fig 2.2 Gate capacitance simulation result and measured data of 21Å gate oxide thickness NMOS transistor.

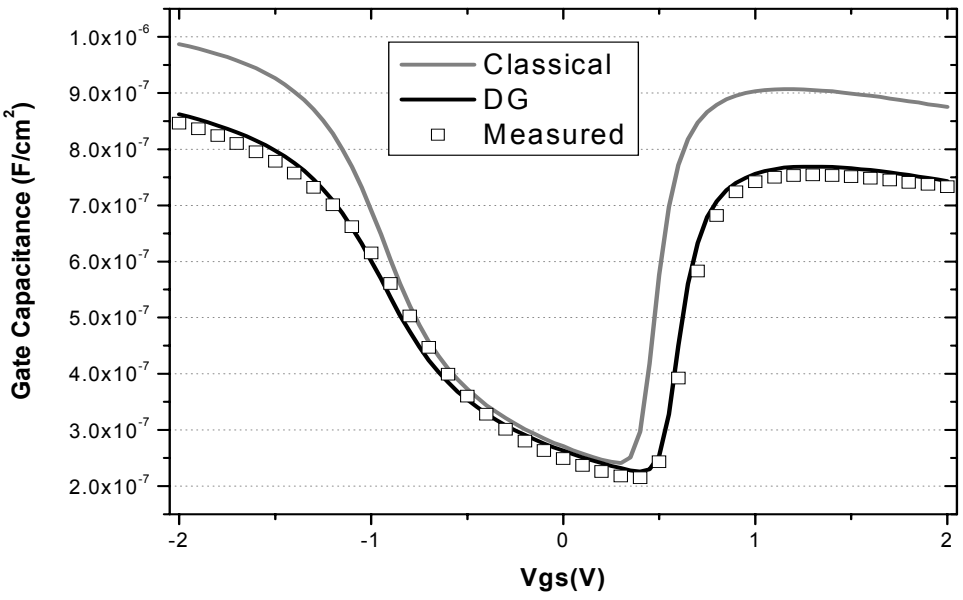


Fig 2.3 Gate capacitance simulation result and measured data of 31Å gate oxide thickness NMOS transistor.

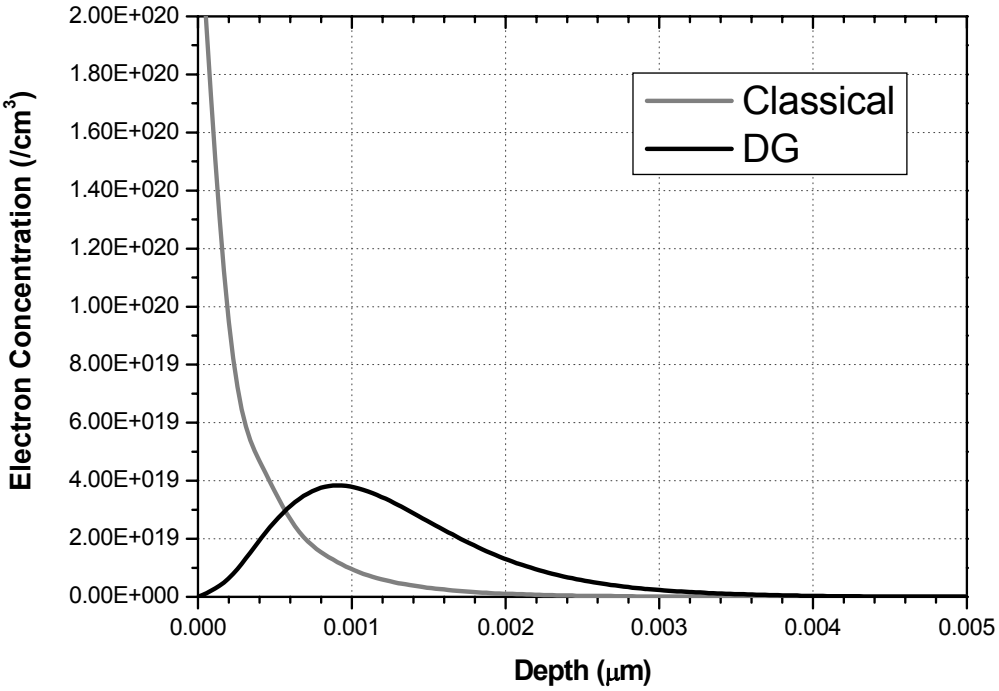


Fig 2.4 Electron concentration distribution under gate oxide in inversion region. 21Å gate oxide thickness NMOS transistor was used.

2.3.2 2-D MOS simulation

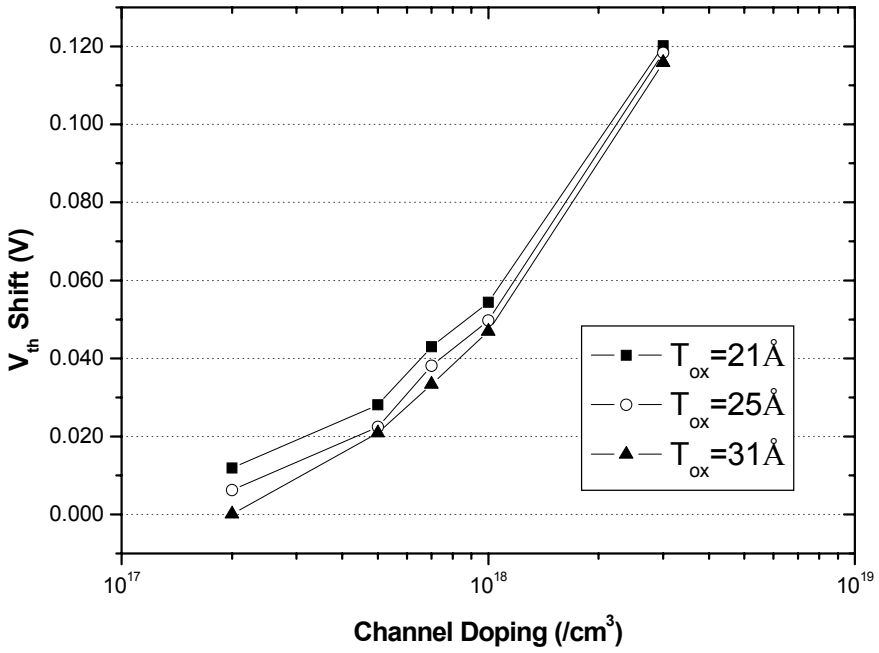


Fig 2.5 Threshold voltage shift(=$V_{th\ DG}$-$V_{th\ Classical}$) with different substrate doping concentration and oxide thickness

The V_{th} shift with substrate doping has been reported [10] and explained using various quantum-mechanically corrected models by Hareland and others [8-9]. The density-gradient method also predicts this trend of V_{th} shift in a physically consistent manner. Fig. 2.5 shows the amount of V_{th} shift predicted by the density-gradient method. 100mV was applied to the drain and the V_{th} was defined as the gate voltage when the drain current reaches 100nA/μm. The V_{th} for the density-gradient model is larger than the classical model, and the amount of shift increases as the gate oxide thickness reduces and the substrate doping increases. The band bending is steeper for MOS devices with higher doping concentrations, therefore the quantum confinement effect starts to occur at earlier stages of inversion. Also, the ratio of effective oxide thickness and physical oxide thickness is larger for thinner oxide devices, and as a result, the V_{th} shift is also larger, though the effect is not so obvious as that due to substrate doping.

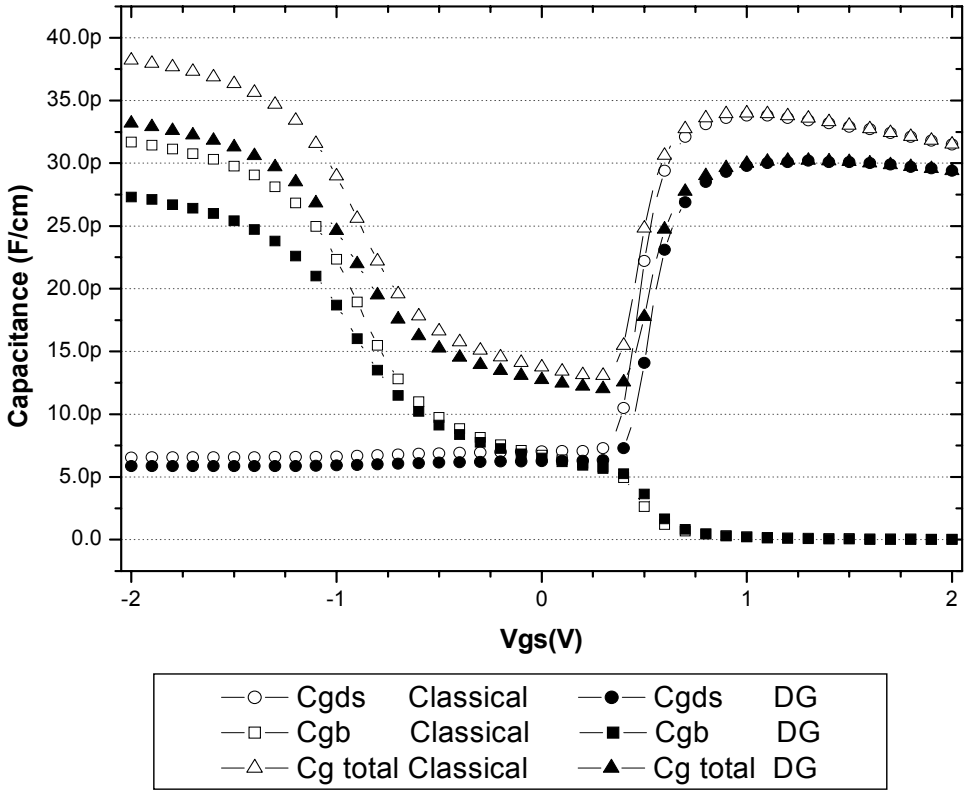


Fig 2.6 2D simulation of a 25Å gate oxide thickness MOS and comparison with classical model. The source, drain and substrate are tied to ground and gate voltage was swept.

The change of Cgds (Cgd+Cgs) with gate bias voltage is plotted in Fig. 2.6. Fig. 2.6 also includes the capacitance between gate and bulk. In the accumulation region, the total gate capacitance consists of Cgds and Cgb. The quantum confinement phenomenon doesn't have any effect on the overlap capacitance, therefore Cgds is the same as in the classical case. However, the Cgb is a series connection of Cgc and Ccb, and the quantum confinement phenomenon in the poly region reduces Cgc, resulting in a reduced size of Cgb. In the depletion region, the density gradient model predicts almost the same result. In the inversion region the shielding effect by the inversion layer makes Cgb go to zero in both models and only Cgds is different

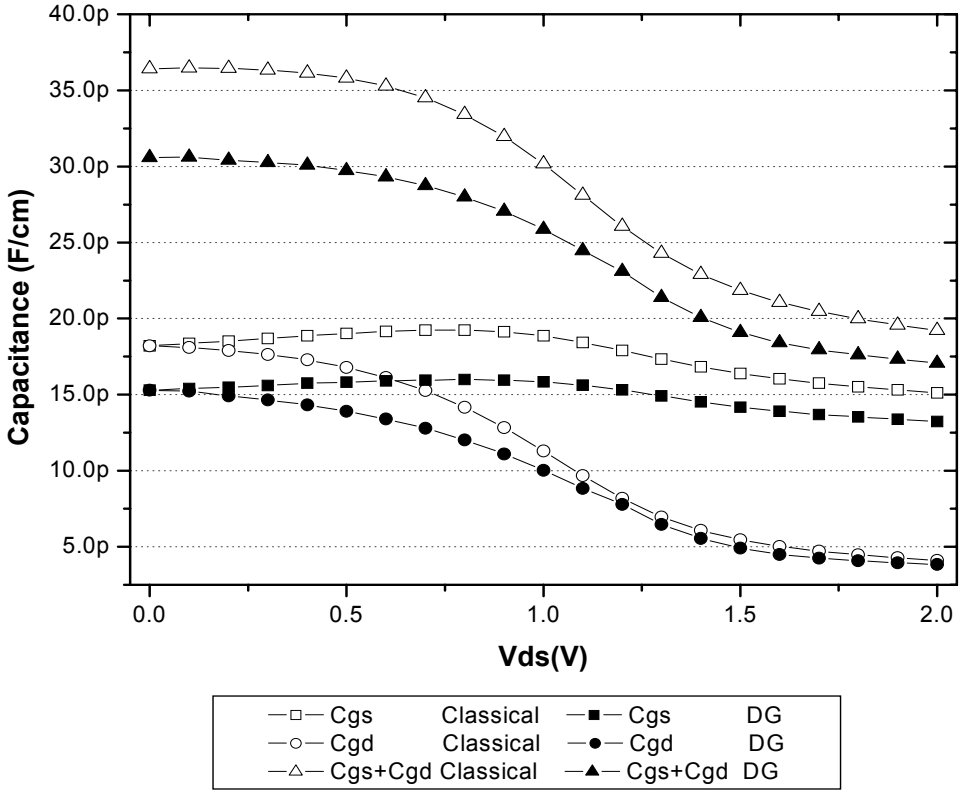


Fig 2.7 2D simulation of a 25Å gate oxide thickness MOS and comparison with classical model. The gate voltage is 1V and the drain voltage was swept from ground to 2V.

When a MOS transistor is turned on, the gate capacitance is the sum of Cgs and Cgd. The size of Cgs and Cgd are equal without drain bias. However, as the device moves into saturation with high drain bias, the source region dominates in controlling channel charge and Cgd reduces to the overlap capacitance between gate and drain. Fig. 2.7 shows the change Cgg (=Cgs+Cgd), Cgs and Cgs and Cgd with drain bias. The gate voltage is 1V and 1M Hz *AC* signals were applied to the source and drain to calculate the *AC* current to the gate.

The transconductance of a MOS transistor can be calculated simply by applying an *AC* signal to the gate and computing the drain current at a given bias condition. The transconductance calculation results for a 25Å oxide thickness MOS transistor is shown in Fig. 2.8. The gate bias point was set to 0.5 V higher than the threshold voltage of the density-gradient model case, which was obtained by plotting Fig. 2.5. Drain voltage was set to 1.5V which make the device operate in the saturation region.

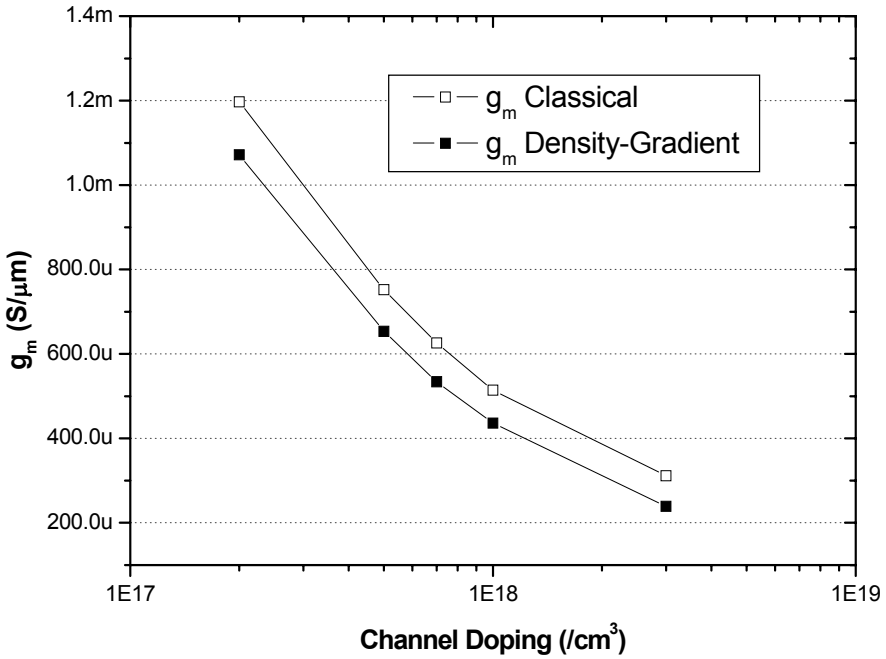


Fig 2.8 25Å gate oxide thickness NMOS transistor transconductance calculation result at different channel doping.

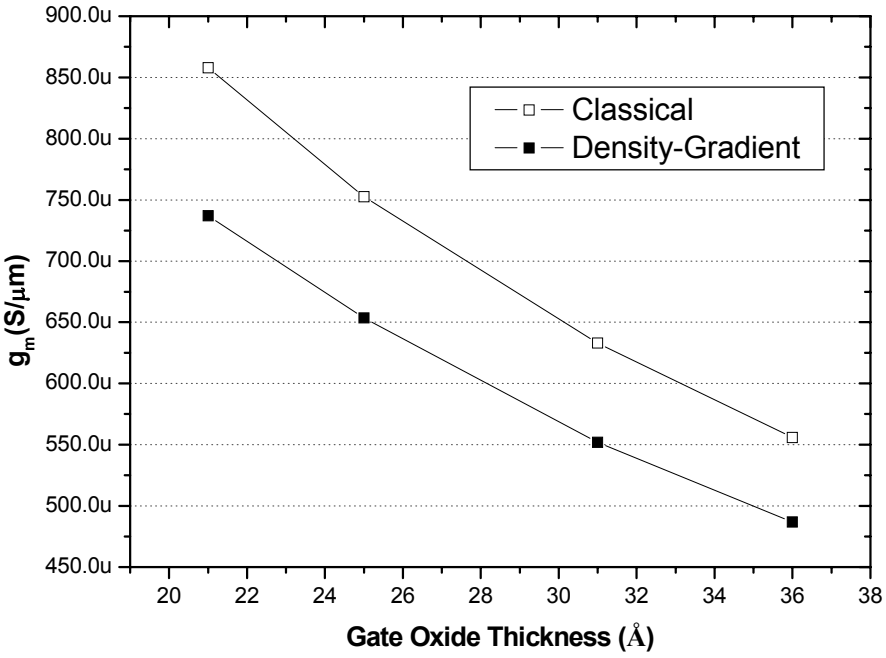


Fig 2.9 Transconductance calculation result with various oxide thickness. Substrate doping is p-type 5e17cm^3.

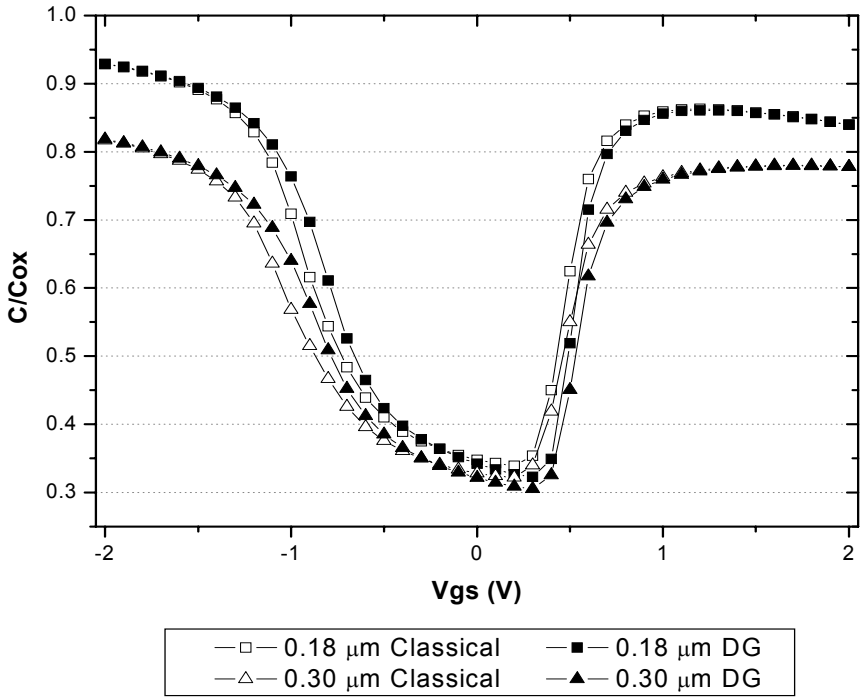


Fig 2.10 Effects from channel length reduction on the C-V curve. C-V curves were extracted with two different channel length, 0.18 μm and 0.30 μm..

The classical model predicts higher transconductance than the density-gradient model because the g_m is proportional to gate oxide capacitance.

Fig. 2.9 illustrates the effect of gate oxide thickness reduction on the transconductance. When the gate oxide thickness decreases, the g_m increases and the deviation of the classical model from the density-gradient model increases, as well.

The effect of channel length reduction on the C-V curve is shown in Fig. 2.10. Simulations were done with two different channel length NMOS transistors, 0.18μm and 0.30μm with the same doping profile. There is a shift to the left in the C-V curve because of the depletion effects due to source and drain electric fields. Source and drain regions help the formation of the depletion layer under the gate oxide, which becomes more obvious with reduced channel length. The amount of shift calculated by the density gradient method is almost the same as for the classical model. The depth of the area where quantum confinement phenomenon appears is several angstroms, so it is still much smaller than the channel length.

2.4 Summary

A new macroscopic model, using the density-gradient, to account for the quantum mechanical effects, was described and the *AC* system was developed. The density-gradient system was simulated using a partial differential equation solver, PROPHET, and the *AC* analysis was implemented as a plug-in post-processor based on the DC-simulation results. Computer simulations were performed for 1D and 2D devices with different conditions and the result agrees very well with measured data. The density-gradient model predicts the quantum mechanical effects in scaled MOS transistors, the *AC* analysis of this model enables device parameter extraction for circuit and device designers efficiently and accurately. The simulation results also indicate that the deviation from the classical model becomes more important as the gate oxide becomes thinner and the substrate doping increases.

CHAPTER 3

Hydrodynamic Simulation

In the classical drift-diffusion transport model, we solve the device system with three variables: potential, electron and hole concentrations. This assumes that the carrier temperature is identical to the lattice temperature. However, in advanced MOS devices, the local carrier heating from electric field in the channel is so large that the carrier temperatures are significantly higher than the lattice temperature. Therefore it is indispensable to include carrier temperature calculation for device simulations.

In the *hydrodynamic* transport model, we do not use the thermal equilibrium approximation. The *hydrodynamic* model includes the carrier energy balance equations to calculate carrier temperature. The spatial difference of the carrier temperature creates a gradient, resulting in thermal diffusion current. Therefore, the thermal diffusion current term is added to the classical drift-diffusion current equations. Moreover, the carrier velocity is controlled by the energy-relaxation time rather than limited by saturation velocity. This requires a carrier-temperature dependent mobility model for high electric field region. As a result, the carrier and electric field distributions are influenced and the terminal current-voltage characteristics change.

This chapter introduces the equation sets for *hydrodynamic* simulations and the required discretization scheme for numerical simulation. The simulation results are compared with the drift-diffusion model in deep-submicron MOS case and the results will also be compared with commercial device simulations using MEDICI.

3. 1 Energy Balance Equations

In the *hydrodynamic* model, the energy of carriers is calculated from energy balance equations. From the energy conservation law, the incoming energy flux has to be balanced with an outgoing energy flux. Carrier temperature is a parameter to measure the kinetic energy of carriers. The electron energy flux is expressed as following[15]:

$$\vec{s_n} = n\vec{v_n}\omega_n + \vec{v_n}P + \vec{Q} \tag{3.1}$$

where $\vec{v_n}$ is average electron velocity, ω_n is electron kinetic energy, P is kinetic pressure of electron gas and $\vec{Q}$ electron heat flux.

The kinetic pressure has the following relation with kinetic energy:

$$P = \frac{2}{3} n\omega_n \tag{3.2}$$

From the heat flux law, the electron heat flux becomes

$$\vec{Q} = -\kappa \nabla T_n \tag{3.3}$$

where κ is thermal conductivity, and T_n is electron temperature. From the approximation of Wiedemann-Franz law between thermal and electric conductivity, the thermal conductivity is given as[16]

$$\kappa = \sigma_n L T_n = q\mu_n n L T_n \tag{3.4}$$

$$= \frac{5}{2}\left(\frac{k_B}{q}\right)^2 q\mu_n n T_n$$

The constant of proportionality, L , is called Lorenz number.

Inserting Equations 3.2 and 3.3 to Equation 3.1 and using relation $v_{nT} = \frac{k_B T_n}{q}$ and $\omega_n = \frac{3}{2} k_B T_n$ leads

$$\vec{s_n} = n\vec{v_n}\omega_n + \vec{v_n}P + \vec{Q} = n\vec{v_n}\omega_n + \frac{2}{3}n\vec{v_n}\omega_n + \vec{Q} \tag{3.5}$$

$$= \frac{5}{3}n\vec{v_n}\omega_n - \frac{5}{2}\left(\frac{k_B}{q}\right)^2 q\mu_n n T_n \nabla T_n$$

$$= \frac{5}{2}qn\vec{v_n}v_{nT} - \frac{5}{2}q\mu_n n v_{nT}\nabla v_{nT}$$

$$= -\frac{5}{2}v_{nT}(\vec{j}_n + q\mu_n(T)n\nabla v_{nT})$$

The carriers with high kinetic energy eventually experience scattering and lose their kinetic energy. The lost kinetic energy is transferred to the lattice and transforms to heat, however the lattice heat flow is not modeled here. The loss of carrier kinetic energy through scattering processes can be written as,

$$\frac{3}{2}nk_B\frac{T_n - T_0}{\tau_{n\varepsilon}} = \frac{3}{2}qn\frac{(v_{nT} - v_{T0})}{\tau_{n\varepsilon}} \tag{3.6}$$

where $\tau_{n\varepsilon}$ is energy relaxation time of electrons.

Therefore, the divergence of carrier energy flux becomes,

$$\nabla \cdot \vec{s}_n = -\vec{j}_n \cdot \nabla\psi - \frac{3}{2}qn\frac{(v_{nT} - v_{T0})}{\tau_{n\varepsilon}}$$

where $-\vec{j}_n \cdot \nabla\psi$ represents Joule heat generated by electron current and electric field.

3. 2 *Hydrodynamic* Model implementation in PROPHET

3.2.1. *Hydrodynamic* Equation Sets

The *hydrodynamic* carrier transport model implemented in PROPHET consists of the following equations[17] :

$$\nabla \cdot (\varepsilon \nabla \psi) = -q(p - n + N_D^+ - N_A^-) \tag{3.7}$$

$$\nabla \cdot \vec{j}_n = -q(G - R)$$

$$\vec{j}_n = -q\mu_n(T)(n\nabla\psi - \nabla(nv_{nT})) \tag{3.8}$$

$$\nabla \cdot \vec{j}_p = q(G - R)$$

$$\vec{j}_p = -q\mu_p(T)(p\nabla\psi + \nabla(pv_{pT})) \tag{3.9}$$

$$\nabla \cdot \vec{s}_n = -\vec{j}_n \cdot \nabla\psi - \frac{3}{2}qn\frac{(v_{nT} - v_{T0})}{\tau_{n\varepsilon}}$$

$$\vec{s}_n = -\frac{5}{2}v_{nT}(\vec{j}_n + q\mu_n(T)n\nabla v_{nT}) \tag{3.10}$$

$$\nabla \cdot \vec{s}_p = -\vec{j}_p \cdot \nabla\psi - \frac{3}{2}qp\frac{(v_{pT} - v_{T0})}{\tau_{p\varepsilon}}$$

$$\vec{s}_p = \frac{5}{2}v_{pT}(\vec{j}_p - q\mu_p(T)p\nabla v_{pT}) \tag{3.11}$$

In the above equations $v_T = k_B T_c / q$ where T_c is the carrier temperature. The vector $\vec{j}$ is carrier current density. Equations 3.8 and 3.9 are different from classical drift-diffusion carrier flux equations only in the last thermal diffusion term. $\vec{s}$ is a vector describing the flux of carrier energy and τ_ε is the ensemble average of the time a carrier loses its energy from collision and is called the energy relaxation time.

The mobility model depends on the carrier temperature in the following way :

$$\mu(T) = \frac{\mu_0}{1 + \alpha(v_T - v_{T0})} \tag{3.12}$$

μ_0 is the low-field mobility and $v_{T0} = kT_0 / q$ where T_0 is the lattice temperature. The constant α is determined by the low-field mobility, saturation velocity, and energy relaxation time.

$$\alpha = \frac{3\mu_0}{2v_s^2\tau_\varepsilon} \tag{3.13}$$

In the *hydrodynamic* simulation, the mobility model is not an explicit function of local electric field as in the drift-diffusion simulation. However, the mobility actually decreases in the high electric filed region because high electric fields accelerate carriers and raise the carrier temperature.

The carrier temperature is assumed to be the same as the lattice temperature at the contacts. Hence, the boundary conditions for the *hydrodynamic* model at the contacts are as follows:

$$n = \frac{N_D - N_A}{2} + \sqrt{(\frac{N_D - N_A}{2})^2 + n_i^2} \tag{3.14}$$

$$p = -\frac{N_D - N_A}{2} + \sqrt{(\frac{N_D - N_A}{2})^2 + n_i^2}$$

$$v_{nT} = v_{nT0}$$

$$v_{pT} = v_{pT0}$$

3.2.2 Discretization Scheme

The discretization and implemented strategies developed by Meinerzhagen and Engl[16] were used for numerical method in PROPHET. This discretization scheme is similar to the Scharfetter-Gummel method[18] and shows good convergence properties.

$$-\vec{j}_n \cdot \vec{t} = q\mu_n(T)(n(\nabla\psi - \nabla v_{nT}) \cdot \vec{t} - v_{nT}\nabla n \cdot \vec{t}) \tag{3.15}$$

$$\vec{s}_n \cdot \vec{t} = \frac{5}{2} q\mu_n(T)(nv_{nT}(\nabla\psi - \nabla v_{nT}) \cdot \vec{t} - v_{nT}\nabla(nv_{nT})) \tag{3.16}$$

The above equations are electron current density and electron energy current density equations on an edge, where $\vec{t}$ means the unit vector in the direction of the edge. Assuming that ψ and v_{nT} vary linearly through the edge and $\vec{j}_n \cdot \vec{t}$, $\vec{s}_n \cdot \vec{t}$ and μ_n are constants,

$$\nabla\psi \cdot \vec{t} = \frac{\psi(w) - \psi(z)}{\Delta l} = \frac{\Delta\psi}{\Delta l} = const \tag{3.17}$$

$$\nabla v_{nT} \cdot \vec{t} = \frac{v_{nT}(w) - v_{nT}(z)}{\Delta l} = \frac{\Delta v_{nT}}{\Delta l} = const \tag{3.18}$$

3.15 and 3.16 can be rewritten in a common form

$$C_1(1 + \alpha(v_{nT} - v_{nT0}) = UC_2 - v_{nT}U' \tag{3.19}$$

where $C_1 = -\frac{\vec{j}_n \cdot \vec{t}}{q\mu_0}$, $U = n$ and $U' = \nabla n \cdot \vec{t}$ for the electron current density case, and $C_1 = -\frac{\vec{s}_n \cdot \vec{t}}{2.5q\mu_{n0}}$, $U = nv_{nT}$ and $U' = \nabla(v_{nT}n) \cdot \vec{t}$ for the electron energy current density case. $C_2 = \frac{(\Delta\Delta - \Delta v_{nT})}{\Delta l}$ for both cases.

Multiplying both sides of 3.19 with $v_T^{\beta-1}$ where $\beta = -C_2 \frac{\Delta l}{\Delta v_{nT}}$, and integration of that result gives

$$C_1 = (U(z)v_{nT}(z)^{\beta} - U(w)v_{nT}(w)^{\beta}) \cdot X \tag{3.20}$$

$$X = \left[\frac{(1 - \alpha v_{nT0})}{\Delta v_T - \Delta\psi}(v_{nT}(w)^{\beta} - v_{nT}(z)^{\beta}) + \frac{\alpha\Delta l}{2\Delta v_{nT} - \Delta\psi}(v_{nT}(w)^{\beta+1} - v_{nT}(z)^{\beta+1}) \right]^{-1}$$

In the case of hole current density and hole energy current density,

$$-\vec{j}_p \cdot \vec{t} = q\mu_p(T)(p(\nabla\psi + \nabla v_{pT}) \cdot \vec{t} + v_{pT}\nabla p \cdot \vec{t}) \tag{3.21}$$

$$\vec{s}_p \cdot \vec{t} = \frac{5}{2}q\mu_p(T)(-pv_{pT}(\nabla\psi + \nabla v_{pT}) \cdot \vec{t} - v_{pT}\nabla(pv_{pT})) \tag{3.22}$$

Therefore, only ψ is needed to be replaced with $-\psi$ in Equations 3.15 and 3.16.

3.2.3 Joule Heat

In Equations 3.10 and 3.11 the left hand side, $\nabla \cdot \vec{s}$ can be calculated following the method described in Section 3.2.1, however the right hand side also includes $-j \cdot \nabla \psi$ which needs to be dealt with carefully. The term $-j \cdot \nabla \psi$ represents the inner product between current density and electric field, and which implies Joule heating. To evaluate this term at each node, the following transform is applied:

$$\vec{j} \cdot \vec{E} = -\vec{j} \cdot \nabla \psi = \psi \nabla \cdot \vec{j} - \nabla \cdot (\psi \vec{j}) \tag{3.23}$$

From carrier continuity equations,

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot \vec{j}_n - r \tag{3.24}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \cdot \vec{j}_p - r \tag{3.25}$$

where r is the recombination rate of carriers.
Inserting 3.24 and 3.25 into 3.23, the Joule heat term of the carrier energy current equations can be rewritten as:

$$\vec{j}_n \cdot \vec{E} = -\vec{j}_n \cdot \nabla \psi = q\psi \left(\frac{\partial n}{\partial t} + r\right) - \nabla \cdot (\psi \vec{j}_n) \tag{3.26}$$

$$\vec{j}_p \cdot \vec{E} = -\vec{j}_p \cdot \nabla \psi = -q\psi \left(\frac{\partial p}{\partial t} + r\right) - \nabla \cdot (\psi \vec{j}_p) \tag{3.27}$$

Transforming 3.23 to 3.26 and 3.27 gives two benefits for numerical calculation. First, the computation time and memory for the additional vector $\vec{E}$ is removed. Second, direct computation of the inner product $\vec{j} \cdot \vec{E}$ is erroneous in the case that the current density or electric field varies rapidly because the direct computation has to assume that $\vec{j}$ and $\vec{E}$ are constant through the edge with which we are dealing.

3. 3 DC *Hydrodynamic* Simulation Results

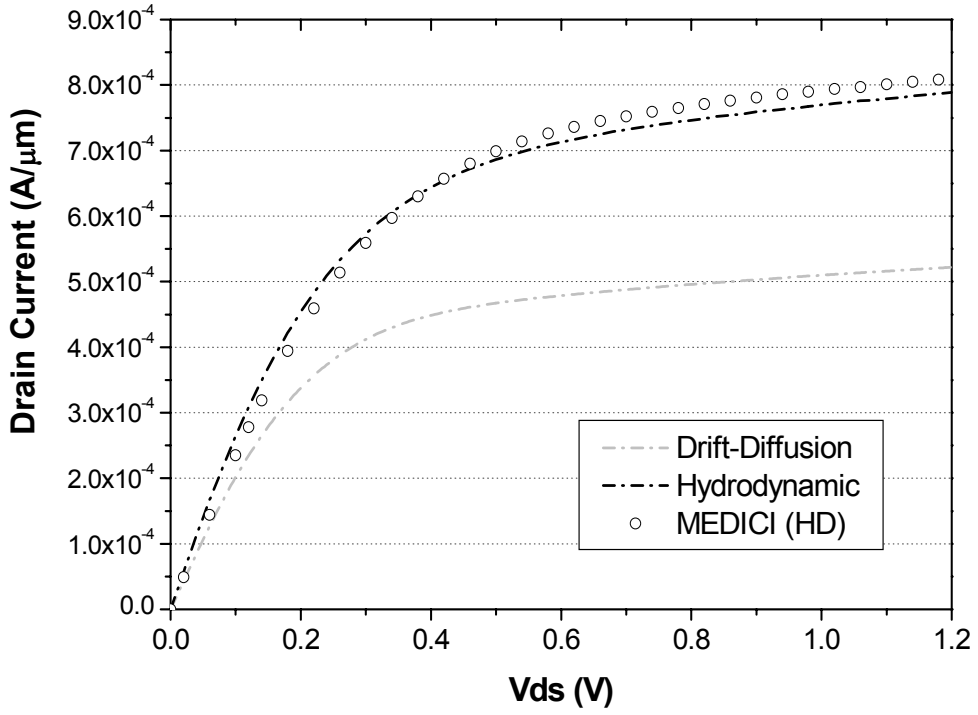


Fig 3.1 Drain current simulation result of 50nm channel length NMOS transistor. Gate voltage is fixed to 1.2V.

The difference between hydrodynamic method and classical drift-diffusion method is more obvious in deep submicron devices. A 50 nm channel length device with super-halo channel was used for DC simulations[19]. Only Equations 3.7-3.10 are solved in the simulation because the hole temperature is unimportant in n-MOS device operation.

Fig. 3.1 shows the drain current vs. V_{ds}. The Lombardi model[20] was used for low-field mobility for both *hydrodynamic* and drift-diffusion simulations. The results of *hydrodynamic* simulation in a commercial simulator, MEDICI, were also shown for comparison. The *hydrodynamic* simulation result predicts significantly higher current than that from drift-diffusion simulation because the carrier velocity is not saturated. Also, the predicted current from the hydrodynamic implementation in this work agrees well with MEDICI results.

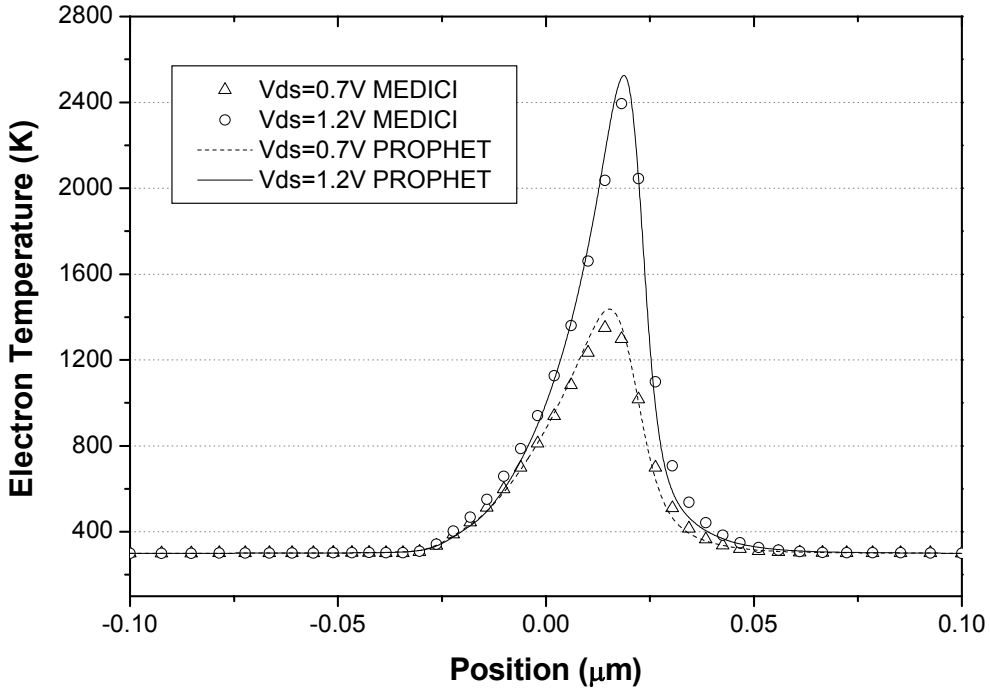


Fig 3.2. Electron temperature under gate oxide simulation result for 50 nm channel length NMOS transistor. The source is to the left of –0.025μm and the drain to the right of +0.025μm.Drain voltage is 1.2 V

The electron temperature is drawn in Fig. 3.2. The high electric field at the drain side raises the electron temperature to 2500K with 1.2V drain bias. MEDICI simulation results are shown again and the PROPHET simulation agrees well with MEDICI.

The electric field in the channel is reduced with HD transport model because the electric field is overestimated in the classical drift-diffusion case due to the velocity saturation. The electric field in the channel is plotted in Fig. 3.3.

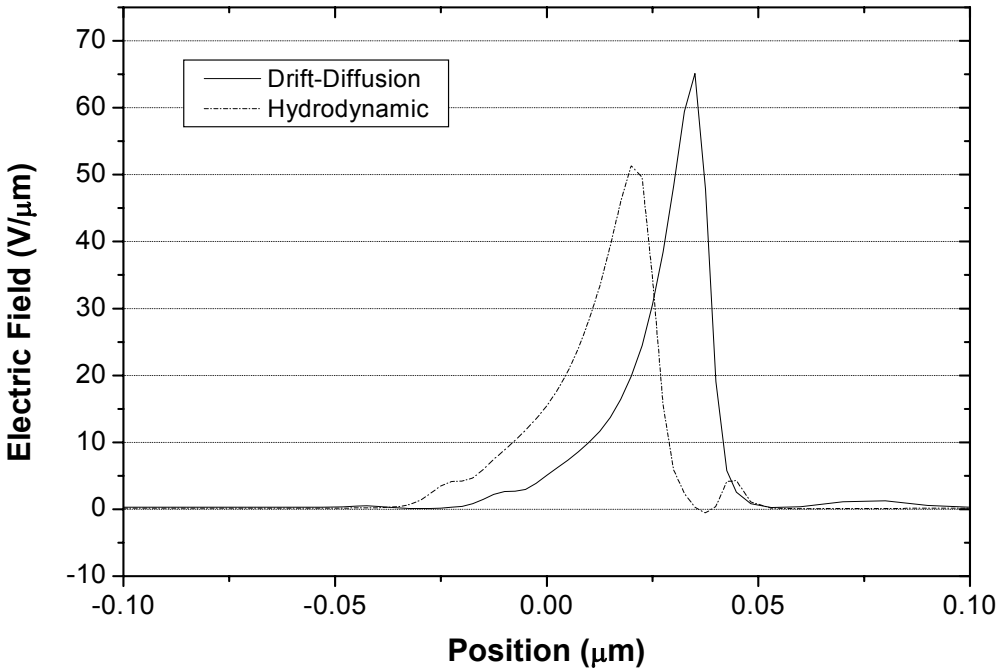


Fig 3.3. Electric field under gate oxide simulation result for 50 nm channel length NMOS transistor. Drain voltage and gate voltage are 1.2 V

3.4 Cut-off frequency calculation result

To calculate the cutoff frequency, *AC* analysis was performed at 3 GHz. An *AC* signal with 3GHz was applied at a gate electrode, and the current at the drain electrode which was DC biased at 1.2V was computed. The following equation was used to approximate the cut-off frequency:

$$\text{Approx. cutoff frequency} = 3GHz \times \left| \frac{i_d}{i_g} \right| \tag{3.28}$$

Where i_d and i_g mean the *AC* current at drain and gate electrode, respectively.

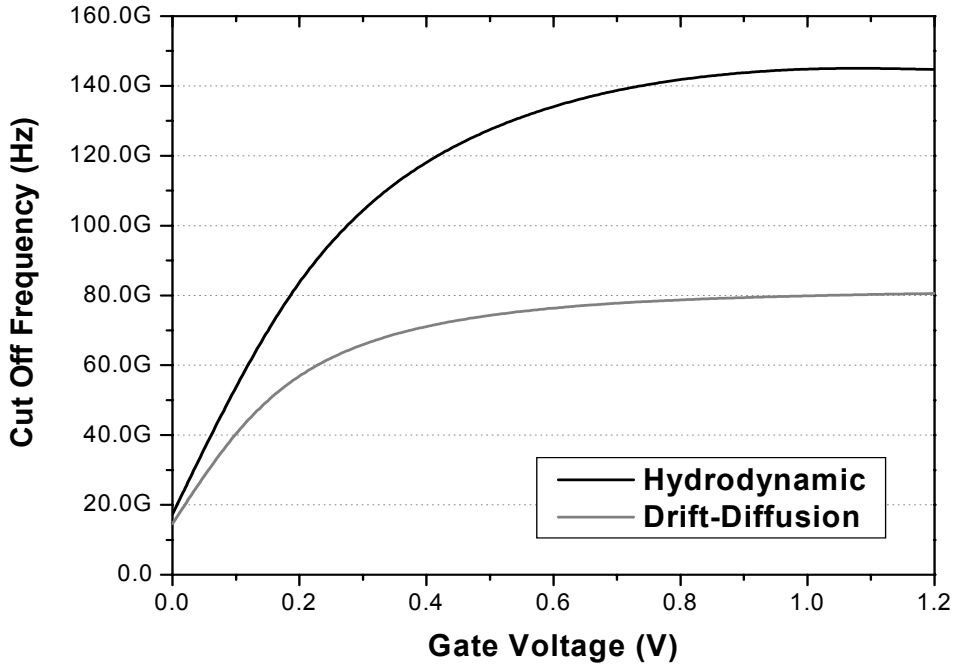


Fig 3.4. Cut-off frequency simulation result for 90 nm channel length NMOS transistor. Gate voltage is 1.2 V

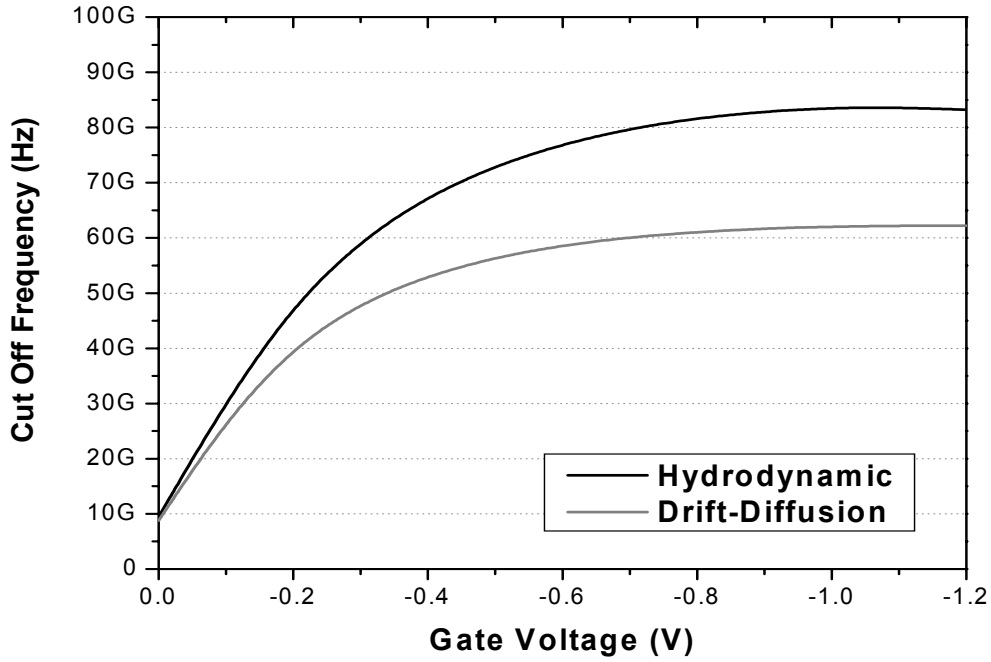


Fig 3.5. Cut-off frequency simulation result for 90 nm channel length PMOS transistor. Gate voltage is -1.2 V

The approximated cutoff frequencies for the 90nm channel length MOSFETs are drawn in Fig.3.4 and Fig. 3.5. Fig. 3.4. shows that the approximated cutoff frequency changes for the NMOS with gate voltage; the drift-diffusion model predicts maximum cutoff frequency of 80.7GHz with 1.2V gate bias while the *hydrodynamic* model predicts maximum cutoff frequency of 145.2GHz with 1.08V gate bias. The cutoff frequency of a MOS transistor is approximately calculated as $\frac{g_m}{2\pi C_{gs}}$. The *Hydrodynamic* model predicts a larger drain current level than drift-diffusion model and, consequently, higher transconductance. Also the gate-to-source capacitance is reduced in the *hydrodynamic* model because the portion that contributes gate source capacitance in the channel is reduced due to carrier velocity overshoot. Therefore, the *hydrodynamic* model generally predicts higher cutoff frequencies.

Fig. 3.5. shows that the approximated cutoff frequency changes for a PMOS with gate voltage; the drift-diffusion model predicts maximum cutoff frequency of 62.4GHz with –1.1V gate bias and the *hydrodynamic* model predicts maximum cutoff frequency of 83.7GHz with –1.07V gate bias. The expected cut-off frequency is lower for PMOS due to its lower carrier mobility.

3.5 Summary

This chapter introduces basic idea of *hydrodynamic* transport model and explorers numerical techniques for implementation in a device simulator. For accurate simulation of deep-submicron MOS transistors, the *hydrodynamic* model is necessary, because we can no longer assume quasi-equilibrium. High electric fields in the channel create velocity overshoot near the drain, and this also changes the carrier injection conditions at the source. As a result, the *hydrodynamic* model predicts larger currents than for the drift-diffusion model. From the *hydrodynamic* simulations, it appears that the high energy electrons near drain acquire up to 10 times more kinetic energy than an electron in thermal equilibrium for a 90nm channel length NMOS transistor.

The cut-off frequency simulation results from *AC* analysis show that *hydrodynamic* simulations predict much higher cut-off frequencies. The cut-off frequency is mainly determined by the transconductance and gate-to-source capacitance. The tranconductance from the *hydrodynamic* model is larger due to larger current levels. Also the gate-to-source capacitance is smaller in the *hydrodynamic* model because the velocity overshoot reduces the carrier concentrations near the drain.

CHAPTER 4

2-D Noise Simulation Theory

With the fabrication and circuit design development, CMOS technology is now widely used for RF applications. CMOS RF circuits are inexpensive and can be easily integrated with digital circuit on a single silicon chip.

For the design of optimal CMOS RF circuits, accurate modeling of RF noise is crucial. The noise in long channel MOSFETs is analytically analyzed with 1D transmission line approach by van der Ziel[21]; the results show good agreement with measurement data. As the fabrication technology develops, the channel length is reduced into the deep-submicron range, and now the cut-off frequency of the latest MOSFET generations is reported as over a hundred gigaHertz[22], which is well above the operation frequency requirements for any RF applications. However, short channel effects make the noise behavior of deep-submicron MOSFET deviate from van der Ziel's analytical result, and poor understanding and modeling of this noise behavior of deep-submicron MOSFETs is a major obstacle for RF CMOS circuit designers.

For accurate computer simulation of deep-submicron MOSFETs, full two dimensional simulation is indispensable. A popular method for 2D noise simulation is the impedance field method, which was developed by Shockley et al[23]. This method calculates the noise at an electrode using a transfer function from every point of a device to an electrode, based on local noise sources at every point. Therefore, the transfer function has to be defined at every point of the device, which requires substantial computational cost.

Also, the accuracy of the local noise source model is very important. Generally, the thermal noise is directly proportional to temperature. In thermal equilibrium, the lattice temperature and carrier temperature are identical. However, a large electric field in a deep-submiron device accelerates the carriers, and they acquire significant temperature compared to the lattice temperature as described in Chapter 3. This discrepancy between carrier and lattice temperature makes development of local noise sources very complex. Recently, C. Jungemann developed a hydrodynamic noise model for bulk-transport-dominated devices. In this work a *hydrodynamic* noise model for Si MOSFETs is presented, which includes a model for surface transport. The *hydrodynamic* model is the one developed by [17] and in contrast to that of [24] this model is based on an analytical formulation of the microscopic noise sources, which are readily extended to the case of surface transport.

This chapter is constructed as follows: Section 4.1 shows how the impedance field is defined and integrated with local noise sources to calculate the noise at the electrodes. Section 4.2 derives a new hydrodynamic local noise source model with analytical formulation. Finally, Section 4.3 presents an efficient numerical method for impedance field calculation based on the AC analysis algorithm.

4. 1 Impedance Field Method

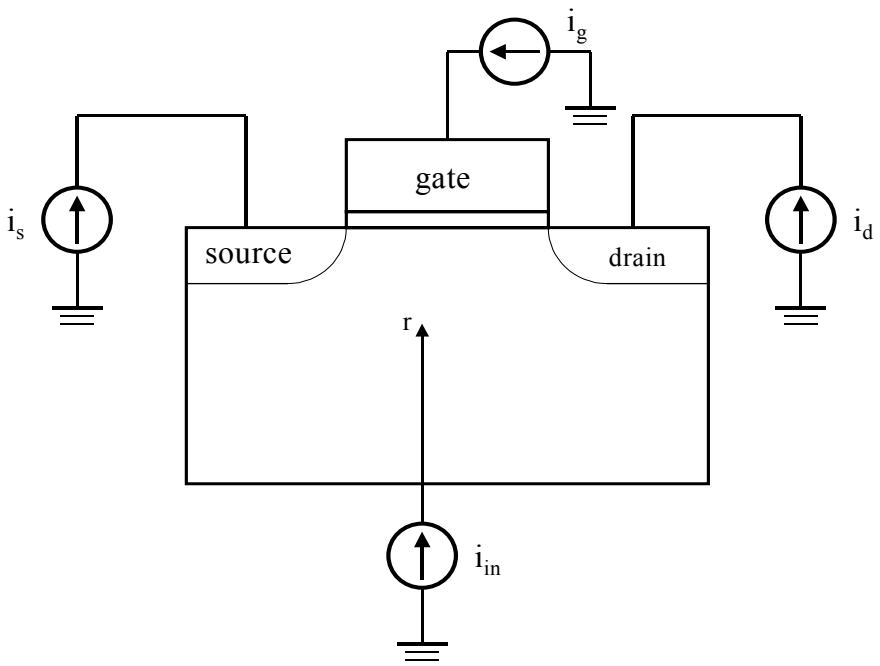


Fig 4.1 Definition of impedance field from transfer function between injected and output current.

The impedance field originally defined by Shockley[23] is

$$Z_{k\vec{r}} = \frac{\text{Voltage fluctuation at } k\text{th electrode}}{\text{Injected Current at } \vec{r} \text{ in the device}} \tag{4.1}$$

Assume that there is a current injection at the location $\vec{r}$ in the device as in Fig 4.1, and the voltage fluctuations at the electrodes are calculated. In this case, the boundary conditions for the electrodes are open circuited for AC because the output is a voltage. Also, this is called the impedance field from the $Z_{k\vec{r}}$ perspective. However, in this work, using injected current :

$$A_{k\vec{r}} = \frac{\text{Current fluctuation at } k\text{th electrode}}{\text{Injected Current at } \vec{r} \text{ in the device}} \tag{4.2}$$

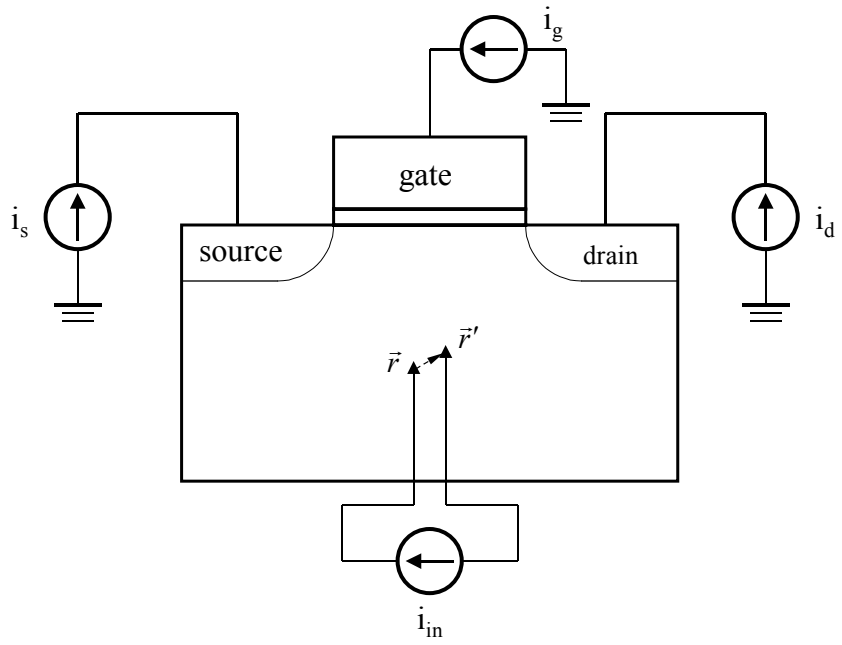


Fig 4.2 Equivalent current source to local noise source.

The reasons the current-current transfer function is preferred are: first, we are more interested in current noise at the electrodes than voltage noise, second, PROPHET has short-circuited boundary conditions of electrodes for *AC* analysis.

The local noise generation can be modeled by injecting a current at a location $\vec{r}$ and pulling out that current from another location $\vec{r'}$ near $\vec{r}$. The contribution to noise at the k-th electrode from location $\vec{r}$ becomes:

$$\left|\nabla A_k\right|^2 S_{in} \tag{4.3}$$

where S_{in} is the power spectral density of the local noise source. The gradient of the impedance field in Equation 4.3 is squared because we are calculating the power spectral density of current noise at the electrodes.

Finally, integrating 4.3 over the whole area of the device gives the total noise at the k-th electrode. Electrons and holes have their own transfer function respectively, and the integration must be done for each carrier type:

$$S_{ik} = \int \left|\nabla A_{nk}\right|^2 S_{in} dv + \int \left|\nabla A_{pk}\right|^2 S_{ip} dv \tag{4.4}$$

The first term in the above equation represents the contribution to noise from electrons, and the second term the contribution from holes. (In the case of the HD model a more general definition of the transfer function must be used [24].)

4.2 Local Noise Source

4.2.1 Local Noise Source in Thermal-equilibrium

Thermal noise in a semiconductor device is created by Brownian motion of electrons. The scattering of electron with the surrounding lattice make the electron have a random motion, and this randomness appears as thermal noise at the electrodes. Johnson in 1928 first measured this thermal noise in resistances and Nyquist derived an equation using a transmission line and black-body radiation theory[22]. Following their name, this thermal noise is also called Johnson-Nyquist noise.

The local noise source model in thermal-equilibrium is derived as follows. We imagine an infinitesimal cube which has length l to each side. The current from an electron crossing a gap l with velocity $v(t)$ is derived as:

$$I(t) = \frac{qv(t)}{l} \tag{4.5}$$

Thermal noise is a stationary random process, therefore its autocorrelation function depends only on the time difference. As a result, the autocorrelation function of the above current is:

$$R_I(\tau) = \int_{-\infty}^{\infty} I(t)I(t+\tau)d\tau = \frac{q}{l^2}^2 \int_{-\infty}^{\infty} v(t)v(t+\tau)d\tau \tag{4.6}$$

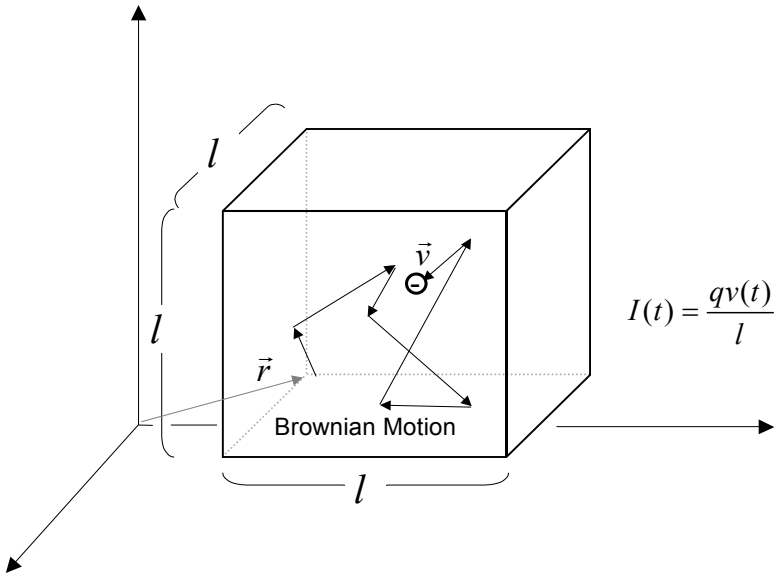


Fig 4.3 Random Brownian motion of an electron in a infinitesimal cube. The scattering events in each cube are assumed to have no correlation.

The probability that an electron does not experience scattering for a time duration τ is $e^{-\tau/\tau_{cn}}$, where τ_{cn} is the mean time between collisions. After an electron experiences scattering, the new velocity is completely uncorrelated with old velocity, hence contributing nothing to the autocorrelation.

Therefore, the autocorrelation function becomes:

$$R_I(\tau) = \frac{q}{l^2}^2 \int_{-\infty}^{\infty} v(t)v(t+\tau)d\tau = \frac{q^2}{l^2}\left\langle v^2 \right\rangle e^{-|\tau|/\tau_{cn}} \tag{4.7}$$

From the equipartition theorem of statistical mechanics, the mean square velocity has the following relation with absolute temperature:

$$\frac{1}{2} m_n^* \left\langle v^2 \right\rangle = \frac{1}{2} k_B T \tag{4.8}$$

where m_n^* is effective mass of conduction band electrons and k_B is Boltzmann's constant.

Inserting the above equation to Equation 3 results :

$$R_I(\tau) = \frac{q^2 k_B T}{l^2 m_n^*} e^{-|\tau|/\tau_{cn}} \tag{4.9}$$

The number of electrons that exist in the cube is $nl^3 = n\,d\mathrm{vol}$, therefore we multiply this to get the total contribution

$$R_{I\,total}(\tau) = \frac{q^2 n k_B T}{l^2 m_n^*} e^{-|\tau|/\tau_{cn}} d\mathrm{vol} \tag{4.10}$$

The Fourier transform pair for $e^{-|\tau|/\tau_{cn}}$ is

$$F(e^{-|\tau|/\tau_{cn}}) = \frac{2/\tau_{cn}}{(2\pi f)^2 + 1/\tau_{cn}^2} \tag{4.11}$$

Therefore, using the Wiener-Khintchine theorem, the contribution from this cube to the power spectral density of current noise at the kth electrode becomes:

$$\left|A_k(r+l) - A_k(r)\right|^2 2\frac{q^2 n k_B T}{l^2 m_n^*}\left(\frac{2\tau_{cn}}{1+(2\pi f)^2\tau_{cn}^2}\right) d\mathrm{vol} \tag{4.12}$$

$$= \left|\frac{A_k(r+l) - A_k(r)}{l^2}\right|^2 4k_B q n \mu_n T \left(\frac{1}{1+(2\pi f)^2\tau_{cn}^2}\right) d\mathrm{vol}$$

$$= \left|\nabla A_k(r)\right|^2 4k_B q n \mu_n T \left(\frac{1}{1+(2\pi f)^2\tau_{cn}^2}\right) d\mathrm{vol}$$

where $A_k(r)$ is the impedance field of position r. In the above equations, a factor 2 was multiplied, accounting for frequencies f and $-f$. Also the relation between mobility and mean time between collisions $\mu_n = \frac{q\tau_{cn}}{m_n^*}$ is used.

From Section 4.1, the contribution to noise at the k-th electrode from location $\vec{r}$ is

$$\left|\nabla A_k\right|^2 S_{in} \tag{4.13}$$

Finally, comparing above expression with 4.13 shows that the local noise source is

$$S_{in}(f) = 4k_B qn\mu_n T\left(\frac{1}{1+(2\pi f)^2\tau_{cn}^2}\right) \tag{4.14}$$

The mean time between carrier collisions is about 100fs, and the local noise source $S_{in}(f)$ is constant up to several THz. This frequency is well above conventional IC electronic applications, and the spectrum of thermal noise is usually regarded as white by engineers.

$$S_{in}(f) \approx 4k_B qn\mu_n T \tag{4.15}$$

4.2.2 Corrections on local noise model for Hydrodynamic simulation

In Section 4.2.1, the local noise source model was derived in the thermal-equilibrium condition, however, under quasi-equilibrium, the local noise source model still can be used with the following correction:

$$S_{in} = 4qnk\mu_{n\vec{E}}T \tag{4.16}$$

where $\mu_{n\vec{E}}$ is electric field dependent mobility, and T is lattice temperature which is assumed to be equal to carrier temperature due to quasi-equilibrium assumption. This noise model has to be modified to include the effect of high energy carriers in non-equilibrium conditions for the *hydrodynamic* model.

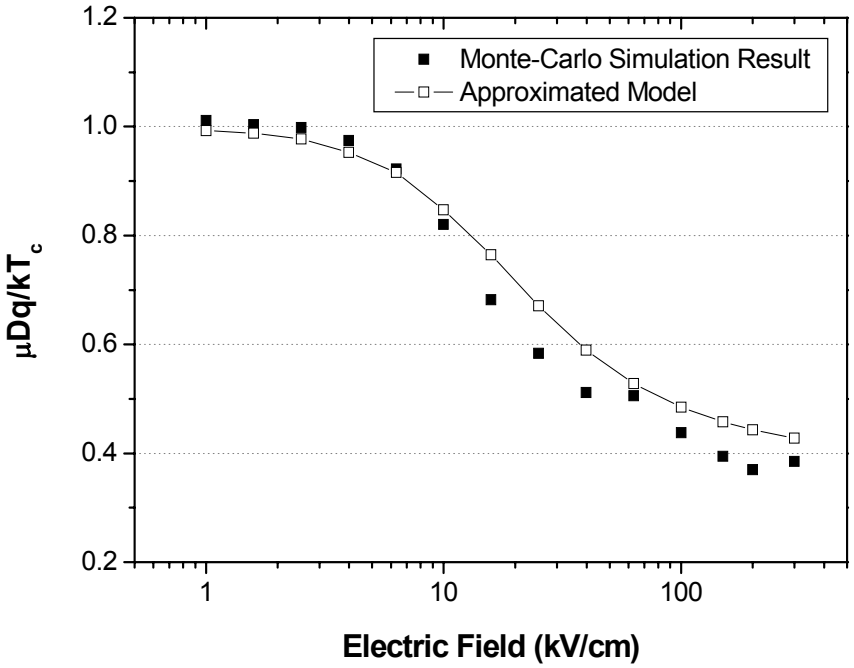


Fig 4.4 Monte-Carlo simulation result of Einstein relation in high electric field. Bulk silicon with n-type 1e17 doping concentration was used.

In regions where the electric field is very high, the Einstein relation is not correct because we can no longer assume quasi-equilibrium. Fig 4.4 shows Monte-Carlo simulation results for the Einstein relation in high electric field, performed by Jungemann[25]. According to the simulation result, a corrected model of Einstein relation in high electric field is created as:

$$D = \frac{kT_c}{q}\mu(0.4 + 0.6\frac{\mu}{\mu_0}) \tag{4.17}$$

where μ is carrier-temperature-dependent mobility and μ_0 is the low-field mobility. T_c denotes the local carrier temperature.

The coupling of energy and velocity fluctuations through the Joule term also creates a correction to the local noise source in case of the HD model [24]. In homogeneous conditions, the divergence of energy current density is zero, therefore the energy current equation becomes :

$$\nabla \cdot \vec{s}_n = \vec{j}_n \cdot \vec{E} - \frac{3}{2} qn \frac{\left(v_{Tn} - v_{T0}\right)}{\tau_{\varepsilon n}} = 0 \tag{4.18}$$

$$\vec{j}_n = qn\mu_n \vec{E} \tag{4.19}$$

Inserting Equation 4.18 into 4.19 becomes,

$$\vec{E} \cdot \vec{E} = \left|\vec{E}\right|^2 = \frac{3}{2} \frac{\left(v_{Tn} - v_{T0}\right)}{\mu_n \tau_{n\varepsilon}} \tag{4.20}$$

Jungemann et al[24] have shown that the fluctuation of carrier velocity and local carrier temperature have the following relations with Lagenvin forces of carrier velocity($\vec{\xi}_{\vec{v}_n}$) and local carrier temperature(T_n) :

$$\hat{I}\delta\vec{v}_n + \frac{\partial \mu_n}{\partial T_n} \vec{E} \delta T_n = \vec{\xi}_{\vec{v}_n} \tag{4.21}$$

$$q\vec{E}\delta\vec{v}_n + \frac{3k_B}{2\tau_{n\varepsilon}} \delta T_n = 0 \tag{4.22}$$

Removing T_n from Equation 4.21 and 4.22 yields,

$$(1 - \frac{\partial \mu_n}{\partial T_n} \frac{2}{3} q \left|\vec{E}\right|^2 \frac{\tau_{\varepsilon n}}{k_B}) \delta\vec{v}_n = \vec{\xi}_{\vec{v}_n} \tag{4.23}$$

and inserting $\vec{E}$ from Equation 4.18 and 4.19 becomes:

$$\hat{S}_{\vec{\xi}_{v_n}\vec{\xi}_{v_n}} = (2 - \frac{\mu(T_n)}{\mu_0})^2 \hat{S}_{\vec{v}_n\vec{v}_n} \tag{4.24}$$

Including this coupling effect, the local noise source with those corrections becomes:

$$S_{in} = 4q^2 n\mu v_{T_n}(0.4+0.6\frac{\mu}{\mu_0})\times\left(2-\frac{1}{1+\alpha(v_{T_n}-v_{T_0})}\right)^2 \qquad (4.25)$$

$$v_{T_n} = \frac{kT_n}{q}\ ,\ v_{T_0} = \frac{kT_0}{q}$$

where T_n and T_0 represent the electron and lattice temperature, respectively.

4.3 Numerical Method

4.3.1 General Method for Impedance Field Calculation

The general method for the impedance field calculation is based on *AC* analysis. An *AC* analysis is performed by solving the following matrix system [12].

$$\begin{pmatrix} J & -\omega D \\ \omega D & J \end{pmatrix}\begin{pmatrix} x_r \\ x_i \end{pmatrix} = \begin{pmatrix} B \\ 0 \end{pmatrix} \qquad (4.26)$$

where J is the Jacobian matrix from the DC solution, D is from the time-dependent terms, and B is the stimulus. In the *AC* analysis case, the stimulus B has non-zero elements only for the Poisson's equation of nodes in the contact where the stimulus is applied. The current injection creates nonzero terms in electron and hole current density equations:

$$\nabla\cdot\vec{j}_n = q(\frac{\partial n}{\partial t}+r)+i_{n\vec{r}} \qquad (4.27)$$

$$\nabla\cdot\vec{j}_p = -q(\frac{\partial p}{\partial t}+r)+i_{p\vec{r}} \qquad (4.28)$$

where $i_{n\vec{r}}$, $i_{p\vec{r}}$ means injected electron and hole currents at location $\vec{r}$ and scalar r is recombination rate. We usually assume that the correlation between electron noise and hole noise is small enough to be neglected because generally the scattering between two different carriers is negligible for diffusion noise. Therefore the noise contribution from electrons and holes are calculated independently.

Applying 4.27 and 4.28, B has non-zero elements for the carrier continuity equations of the node where the current source of stimulus is applied. Also, it can be noted that the sum of the impedance field over all electrodes becomes

$$\sum_{i=1}^{n} A_i = 1 \tag{4.29}$$

because the input current we applied at location $\vec{r}$ should go out through the electrodes.

If the device has N nodes, we need to run AC analysis $2 \times N$ times to get the impedance field for electrons and holes and that requires an unreasonable computation time. An efficient numerical method, which reduces the computation to two AC analyses, has been developed to improve efficiency. This numerical approach is similar to the Bonani's work[27].

The matrix system to calculate the entire impedance is

$$J_{AC} Y = P \tag{4.30}$$

where J_{AC} is the matrix in equation 4.26, Y is a matrix with $2N$ columns that contains the solution from the current stimulus at each node, and P has $2N$ columns which represent the current stimulus.

The computed Y can then be transformed to the final impedance field A by

$$IY = A \tag{4.31}$$

I is a matrix with two rows and $2N \times N_s$ columns, and it calculates the resulting current at a given terminal electrode (N_s is the number of system variables). A is the final impedance field calculated and has two rows for the real and imaginary parts, respectively, and $2N$ columns.

Inserting Equation 4.31 in 4.30 to eliminate Y results in,

$$IJ_{AC}^{-1} P = A \tag{4.32}$$

Let $IJ_{AC}^{-1} = T$ and T can be acquired easily by solving

$$\left(J_{AC}^{T}\right)^{-1} T^{T} = I^{T} \tag{4.33}$$

Equation 4.33 needs two AC analyses since I^T has only two columns. Inserting T into equation 4.32 and the final impedance field A can be achieved in a negligible computation overhead.

4.3.2 Corrections for *Hydrodynamic* Simulation

The transformation to compute the Joule heat in Section 3.2.2 changes matrix D and vector B in Equation 4.26. The Joule heat term has a divergence of current density through the following transformation and the divergence has to include the effect of current injection.

$$\vec{j}_n \cdot \vec{E} = -\vec{j}_n \cdot \nabla\psi = \psi\nabla \cdot \vec{j}_n - \nabla \cdot (\psi \vec{j}_n) = q\psi(\frac{\partial n}{\partial t} + r) + \psi i_{n\vec{r}} - \nabla \cdot (\psi \vec{j}_n) \tag{4.34}$$

$$\vec{j}_p \cdot \vec{E} = -\vec{j}_p \cdot \nabla\psi = \psi\nabla \cdot \vec{j}_p - \nabla \cdot (\psi \vec{j}_p) = -q\psi(\frac{\partial p}{\partial t} + r) + \psi i_{p\vec{r}} - \nabla \cdot (\psi \vec{j}_p) \tag{4.35}$$

The time dependent term in Equation 4.34 and 4.35 changes matrix D as ollows;

$$D = \begin{bmatrix} D_1 & 0 & \cdots & 0 \\ 0 & D_2 & \ddots & \vdots \\ \vdots & \ddots & \ddots & 0 \\ 0 & \cdots & 0 & D_n \end{bmatrix} \tag{4.36}$$

$$D_k = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \\ 0 & -\psi_k & 0 & 0 & 0 \\ 0 & 0 & \psi_k & 0 & 0 \end{bmatrix}$$

where ψ_k means the potential at kth node.

Also, the vector B in Equation 4.26 becomes

$$B = \begin{bmatrix} 0 \\ \vdots \\ 0 \\ B_l \\ 0 \\ \vdots \\ 0 \end{bmatrix} \tag{4.37}$$

where $B_l = \begin{bmatrix} 0 \\ 1 \\ 0 \\ \psi \\ 0 \end{bmatrix}$ for electrons and $B_l = \begin{bmatrix} 0 \\ 0 \\ 1 \\ 0 \\ \psi \end{bmatrix}$ for holes. l is the node where the current is injected.

4.4 Summary

The impedance field method calculates the noise at electrodes by using transfer functions from each point in the device to an electrode with local noise sources. It is well suited for multi-dimensional device simulation, because of its simplicity and generality.

The coupling of carrier energy and momentum makes the local noise source as a complex function. The Einstein relation between the carrier diffusion constant and mobility is not valid when high electric fields exist, because the Einstein relation is based on thermal-equilibrium. Therefore, a local noise source model with an analytical formulation is developed for accurate noise simulation.

Usually, device simulation requires calculation of thousands or more node points. Computing the transfer function from each point to an electrode for the impedance field simulation requires enormous computational cost. A numerical technique based on *AC* simulation is presented to reduce this computational cost. The impedance field noise simulation can be performed with negligible overhead using a single *AC* analysis with this technique.

CHAPTER 5

Noise Simulation and Analysis

The noise simulation results from the drift-diffusion model do not show satisfactory agreement to measured data for deep-submicron MOSFETs. The high energy carriers created from large electric fields near the drain change the impedance field, and also the size of local noise source. As a result, the hydrodynamic model which includes a carrier energy relation is necessary for accurate noise simulation.

The theories presented in Chapter 3 and 4 were implemented in a multi-dimensional device simulator, PROPHET, as modules. Hydrodynamic noise simulations were performed with n-channel and p-channel MOSFETs with various channel lengths and the results were compared with those from drift-diffusion model.

In this chapter, the noise simulation results will be shown and the noise generation mechanism will be explained. Good understanding of the noise generation mechanisms is very important for creating a physically sound circuit noise model and noise performance estimation of future technology scaling. Also the effect of noise from gate resistance, which is one of major noise generation sources in deep-submicron MOSFETs, will be illustrated.

This chapter is constructed as follows : Section 5.1 shows the local noise source dependency on carrier temperature and the transport model. Sections 5.2 and 5.3 present noise simulation results and measured data, and explain generation mechanisms for drain and gate noise respectively. Section 5.4 presents correlation coefficient simulation results and also explains the

mechanism of its dependency on channel length and bias. Finally, Section 5.5 shows the effects of gate resistance on noise.

5.1 Local Noise Source

In contrast to the drift-diffusion model *hydrodyanmic* MOSFET simulations yield a carrier velocity overshoot for large drain voltages near the drain. This velocity overshoot changes the carrier distribution in the device and the impedance field (A). The maximum carrier temperature also rises to more than 3000K, which means that the carrier in the velocity overshoot region acquires about 10 times more energy than a normal carrier near equilibrium condition. The local noise generation is also increased by these high energy carriers, and the relation follows Equation 4.25.

Fig. 5.1 illustrates the relation between the local noise source and carrier temperature. The new local noise source model predicts a fast increment with carrier temperature until 1000K and becomes saturated beyond that point. This implies that the reduction of diffusion constant under high electric field suppress the rise of local noise source. In the calculations for Fig 5.1., $n=5\times10^{17}/cm^3$ and $\mu_0=800\,cm^2/Vs$ were used. Fig. 5.2 and Fig. 5.3 show the simulation result of local noise source under gate oxide for 1.0μm and 0.18μm channel length NMOS transistor. This is a two dimensional noise simulation, and the vertical profile of the local noise source is also important. However, the noise source profile under the gate oxide more clearly shows the difference between drift-diffusion and *hydrodynamic* models. The *hydrodynamic* model predicts much larger local noise source near the drain, and the difference is larger in 0.18μm channel length NMOS transistors.

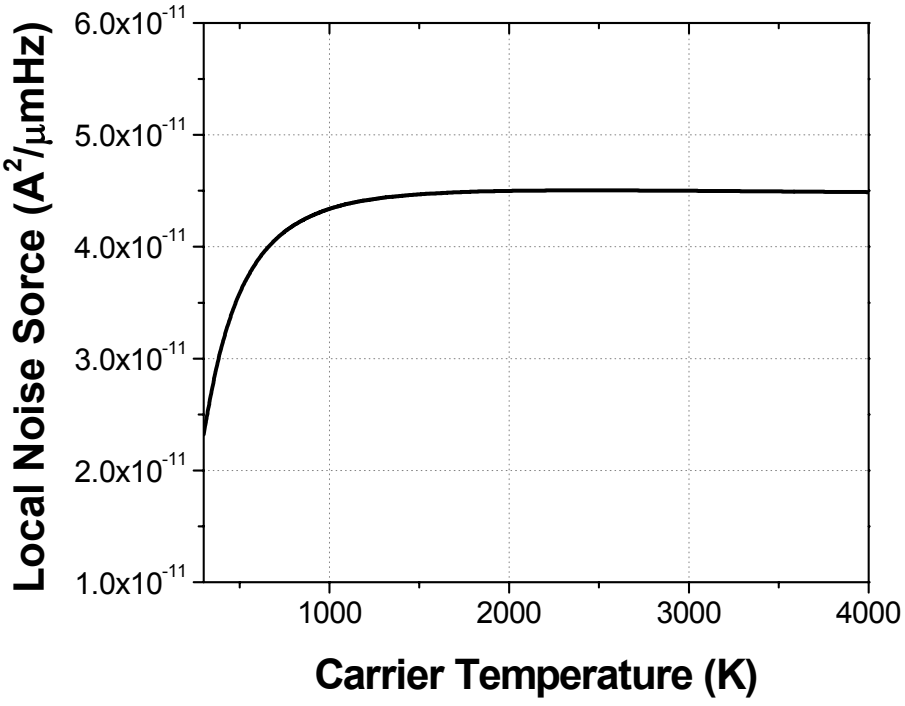


Fig 5.1 Local noise source in bulk silicon vs. carrier temperature. $n=5\times10^{17}/cm^3$ and $\mu_0=800\,cm^2/Vs$ is used.

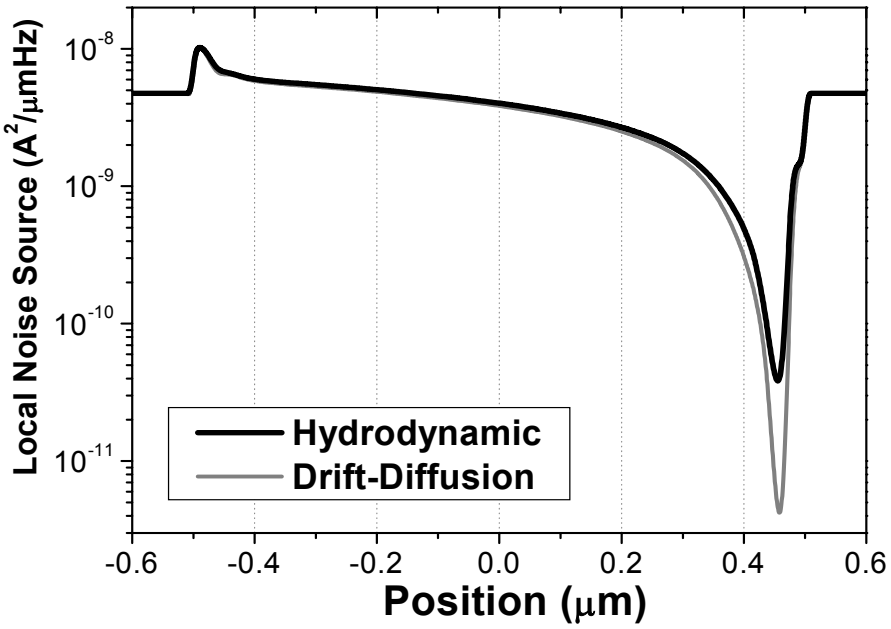


Fig 5.2 Local noise source under gate oxide in 1.0μm channel length NMOS transistor. Gate voltage is 1.0V and drain voltage is 1.8V.

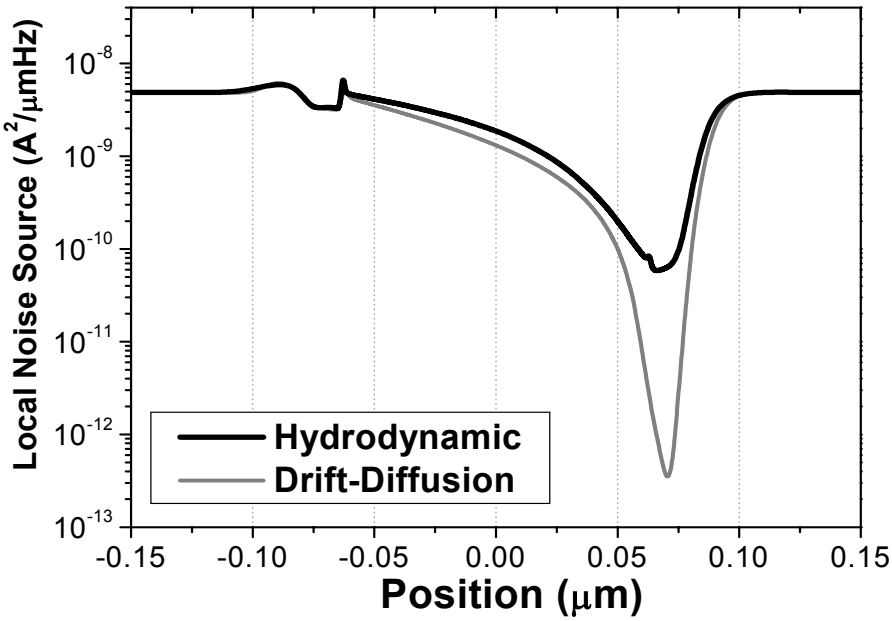


Fig 5.3 Local noise source under gate oxide in 0.18μm channel length NMOS transistor. Gate voltage is 1.0V and drain voltage is 1.8V.

5.2 Drain Noise Simulation

The impedance field for drain noise of an ideal long channel MOS transistor is determined by transistor action. Fig 5.4 illustrates how the shape of the impedance field is determined intuitively. We can divide a MOS transistor in saturation into three regions - linear, saturation and pinch-off. In Fig. 5.4 from 0 to x, is modeled as a transistor in linear region. Here, x is a variable which moves from 0 to L'. The region from xL' to L' is modeled by a transistor in the linear region. The pinch-off region from L' to L is removed from our model, because it does not have any effect on the current-voltage characteristics of an ideal long channel MOS device.

Therefore, a MOS transistor in the saturation region is modeled as two MOS transistors in a common gate configuration. For impedance field calculations, we inject current between those two transistors, and calculate the output current of the total transistor. Impedance field analysis is based on small signal perturbations at each point, therefore, we use the small signal MOS model for our investigation. The small signal model of the two transistors in common gate configuration is illustrated in Fig 5.4. The drain currents of both transistors have to be equal in this configuration and it is still the same as the drain current of the whole transistor before splitting it. Therefore, from simple MOS current equations,

$$I_D = \mu_n C_{ox} \frac{W}{L'x}\left((V_G - V_t)V_{ds1} - \frac{V_{ds1}^2}{2} \right) \tag{5.1}$$

$$= \frac{1}{2}\mu_n C_{ox} \frac{W}{L'(1-x)}\left(V_G - V_{ds1} - V_t\right)^2$$

$$= \frac{1}{2}\mu_n C_{ox} \frac{W}{L'}\left(V_G - V_t\right)^2$$

where V_{ds1} means drain-to-source voltage of the left side transistor in the linear region.

The output resistance of the transistor in the linear region is,

$$R_s = \frac{\partial V_{ds1}}{\partial I_D} = \frac{1}{\mu_n C_{ox} \frac{W}{L'x}\left((V_G - V_t) - V_{ds1}\right)} \tag{5.2}$$

From the current equation of the right side transistor in saturation and the entire transistor,

$$\frac{1}{1-x}\left(V_G - V_{ds1} - V_t\right)^2 = (V_G - V_t)^2 \tag{5.3}$$

Inserting Equation 5.3 to Equation 5.2 yields

$$R_S = \frac{1}{\mu_n C_{ox} \frac{W}{L'}(V_G - V_t)\frac{\sqrt{1-x}}{x}} \tag{5.4}$$

The transconductance of the transistor in the saturation region is derived as:

$$g_m = \frac{\partial I_D}{\partial V_G} = \mu_n C_{ox} \frac{W}{L'(1-x)}(V_G - V_{ds1} - V_t) \tag{5.5}$$

$$= \mu_n C_{ox} \frac{W}{L'\sqrt{1-x}}(V_G - V_t)$$

Organizing Equation 5.4 and 5.5 leads to the impedance field

$$A(x) = \frac{R_s}{R_s + \frac{1}{g_m}} = \frac{\frac{x}{\sqrt{1-x}}}{\frac{x}{\sqrt{1-x}} + \sqrt{1-x}} = \frac{x}{x + (1-x)} = x \tag{5.6}$$

Hence, the expected impedance field for an ideal long channel MOS transistor is simply linear before the pinch-off region, and remains a constant value of units. The contribution to noise at electrodes is determined by $|\nabla A_k|^2 S_{in}$, and from previous calculation, we expect that $|\nabla A_k|^2$ is a constant in the channel before the pinch off-region and 0 in pinch-off. This implies that pinch-off region near the drain does not have any impact on the noise at electrodes because $|\nabla A_k|^2$ is zero there.

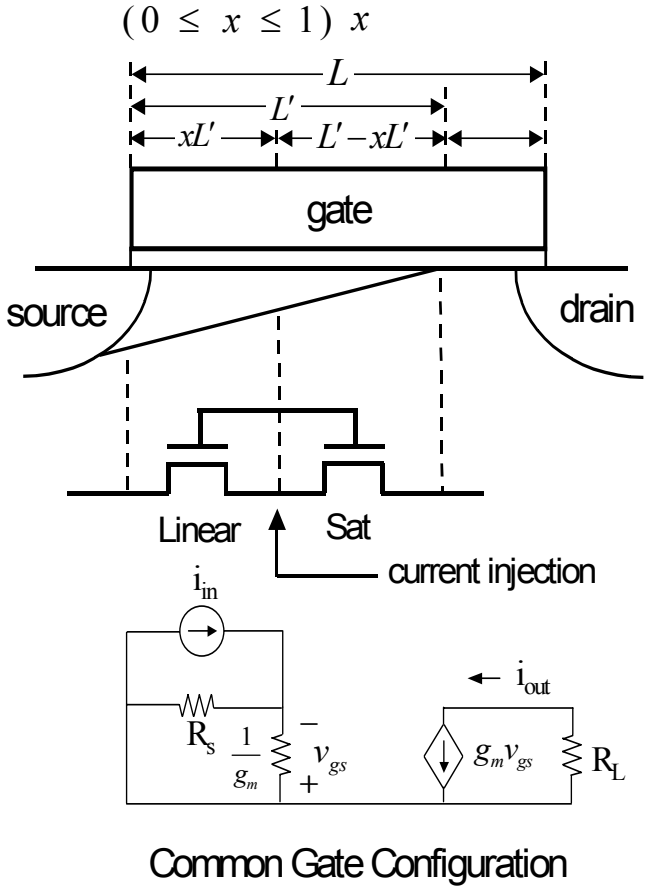


Fig 5.4 Modeling of a MOS transistor in saturation region for simple impedance field calculation. Bottom figure is the ac small signal model of top circuit.

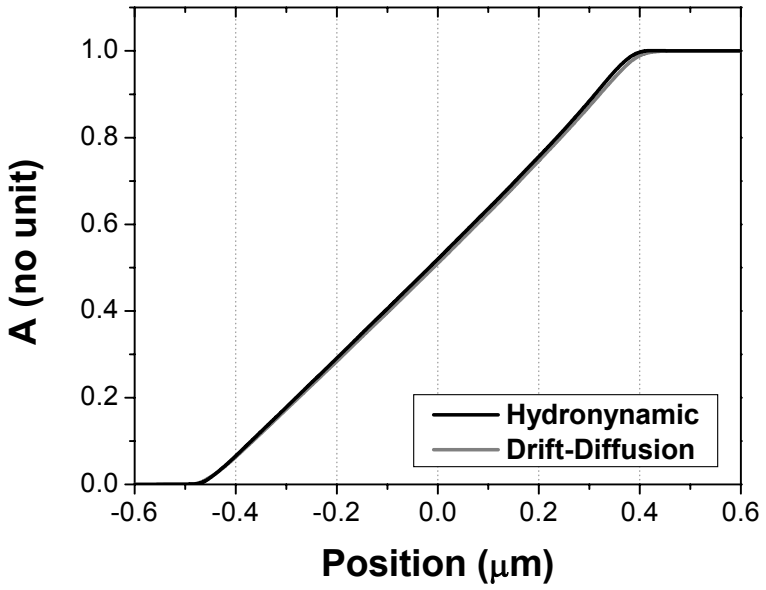


Fig 5.5 Impedance field to drain current noise at each channel position in 1.0μm channel length NMOS transistor. Gate voltage is 1.0V and drain voltage is 1.8V.

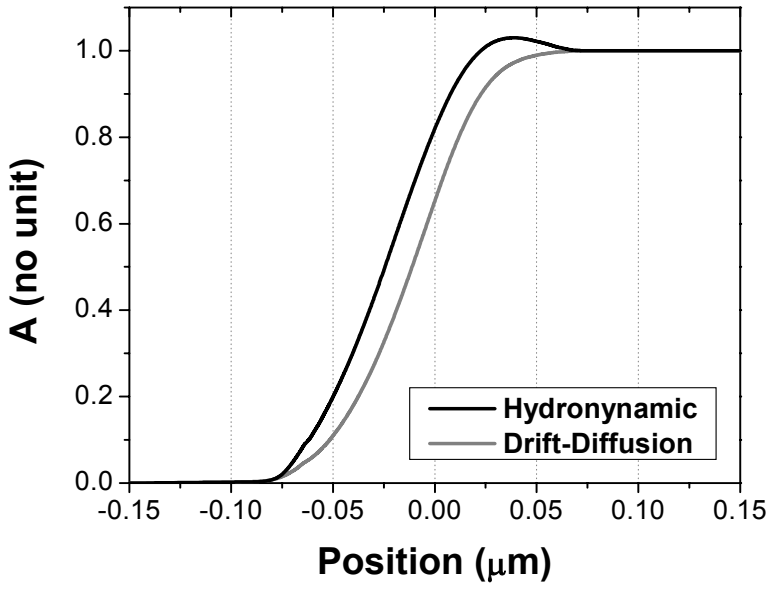


Fig 5.6 Impedance field to drain current noise at each channel position in 0.18μm channel length NMOS transistor. Gate voltage is 1.0V and drain voltage is 1.8V.

The impedance field A was calculated for 1.0μm and 0.18μm channel length devices in Fig. 5.5 and 5.6 using the *hydrodynamic* and drift-diffusion models respectively. The velocity overshoot of electrons near the drain pushes the impedance field to the source side, because the area near the drain which does not contribute to drain noise is widened. As a result, the calculation results from *hydrodynamic* model are shifted relative to the drift-diffusion model towards the source side. Fig. 5.7 and 5.8 show $|\nabla A_k|^2$ calculation results for the same device. $|\nabla A_k|^2$ reaches its maximum between the source and middle of the channel, creating the greatest contribution to drain noise. The contribution to drain noise at each channel position is drawn in Fig 5.9 and 5.10. The contribution at each channel position was integrated in the vertical direction to calculate this result. The *hydrodynamic* model predicts much higher drain noise than the drift-diffusion model. The maximum of $|\nabla A_k|^2$ from the *hydrodynamic* model is greater close to the source, where the carrier concentration is higher and local noise generation is larger. Also, for the drift diffusion case, the carrier mobility decreases rapidly with electric field and the contribution of local noise source is also reduced. As a result, the noise calculation results are much smaller compared to the *hydrodynamic* case.

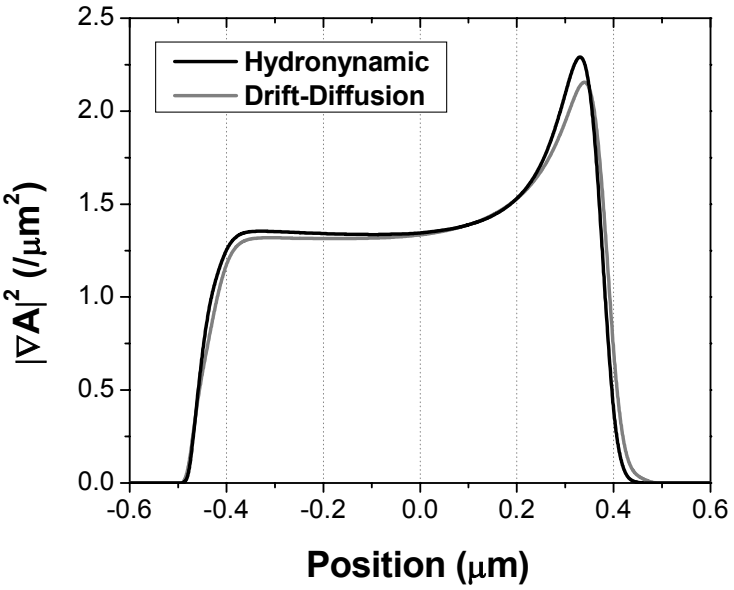


Fig 5.7 $|\nabla A|^2$ to drain current noise at each channel position in 1.0μm channel length NMOS transistor. Gate voltage is 1.0V and drain voltage is 1.8V.

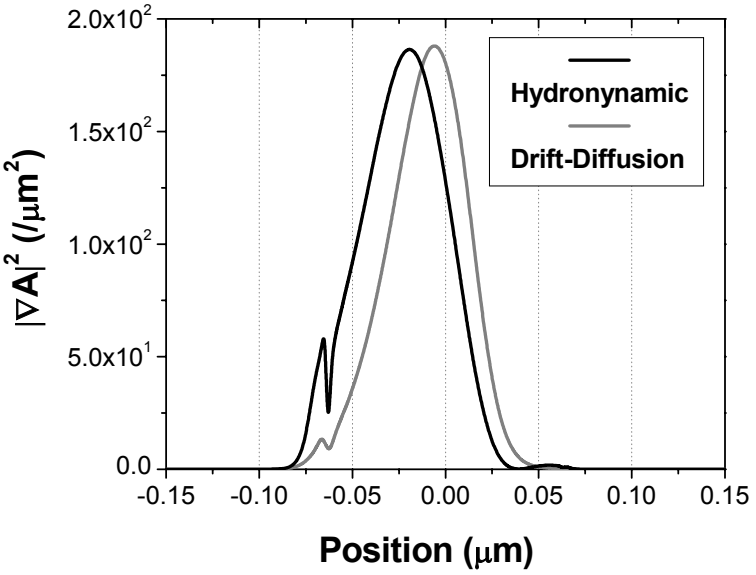


Fig 5.8 $|\nabla A|^2$ to drain current noise at each channel position in 0.18μm channel length NMOS transistor. Gate voltage is 1.0V and drain voltage is 1.8V.

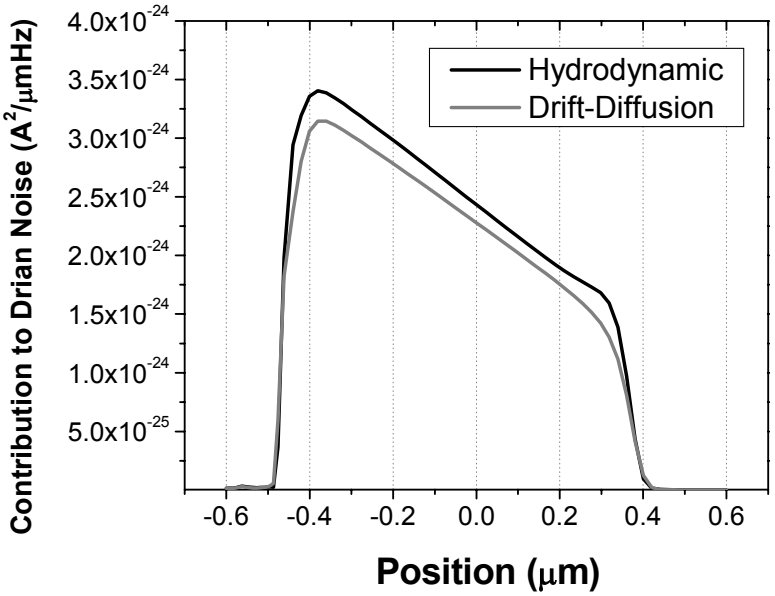


Fig 5.9 Contribution to drain current noise at each channel position in 1.0μm channel length NMOS transistor. Gate voltage is 1.0V and drain voltage is 1.8V.

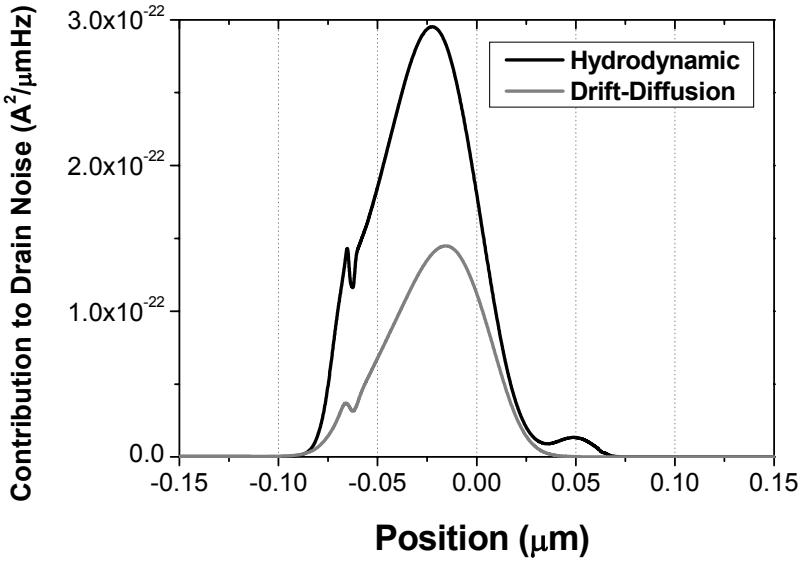


Fig 5.10 Contribution to drain current noise at each channel position in 0.18μm channel length NMOS transistor. Gate voltage is 1.0V and drain voltage is 1.8V.

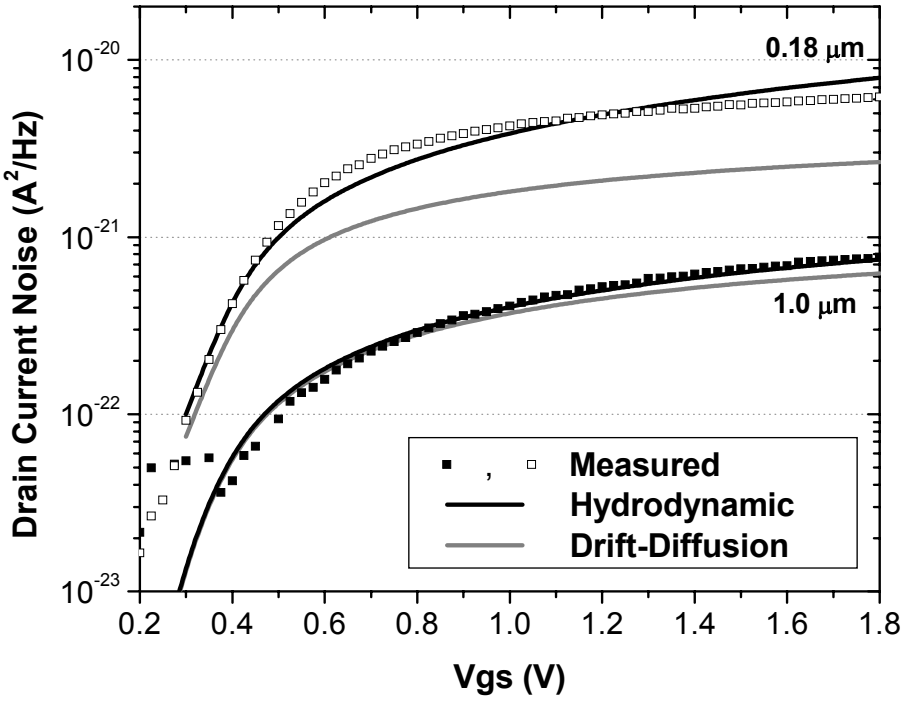


Fig 5.11 Simulation result and measured data for drain current noise. Drain voltage is 1.8V and gate voltage was swept.

The drain noise calculation results are compared with measured data in Fig 5.11. The measured data are from Scholten et al[28] of Philips. Drain voltage was 1.8V and gate voltage was swept. Simulation and measurement were performed at 2.475GHz for 1.0μm channel length device and 5.0 GHz for 0.18μm channel length device. The *hydrodynamic* model predicts about three times larger drain noise with all gate bias for and for 0.18μm channel length device agrees well with measured data.

The *hydrodynamic* and drift-diffusion simulations have been performed for MOS transistors with metallurgical channel lengths ranging from 90nm to 10μm. These MOS transistors have the same doping profiles except for variations in the channel length. To compare MOS transistors with exactly the same profile except the channel length, the MOS transistors in this simulation has a $5\times10^{17}/cm^3$ uniform channel doping and 20 Å gate oxide thickness. The gate bias was set to 1.08V for the NMOS transistor and –1.07V for the PMOS transistor where they have maximum cutoff frequency.

The excess drain noise parameter (γ) is defined as :

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f + \frac{K_1}{f}\Delta f \tag{5.7}$$

where $\overline{i_{nd}^2}$ is the power spectral density of the drain noise and g_{d0} is the drain to source conductance under zero drain bias. K_1 is a constant for flicker noise.

The drain excess noise parameter (γ) for NMOS and PMOS transistors with various channel lengths is shown in Figs. 5.12 and 5.13.

For a frequency of 1MHz and a channel length of 10μm, both simulation models reproduce the analytical results (γ=0.66) for long channel devices in saturation[21],[28]. For 2.5GHz nonquasistatic effects occur in the long channel devices and the drain noise increases[28]. In the case of the short channel devices these effects occur at much higher frequencies and no differences are found for the two frequencies shown. For channel lengths below 1μm the noise increases for short channels. The maximum drain noise parameter is 1.76 for NMOS and 1.53 for PMOS from *hydrodynamic* simulations and are in good agreement with recent experimental results[24]. While the results from the *hydrodynamic* model increase for shorter channels, compared to that from the drift-diffusion model while slightly decreases, this indicates that excess noise is generated by nonequillibrium effects.

The frequency behavior of drain noise is also calculated and shown in Fig 5.14 to illustrate the nonquasistatic effects at high frequencies. The drain noise is independent of frequency until the frequency reaches the cutoff frequency of the MOS transistor, and increases rapidly thereafter

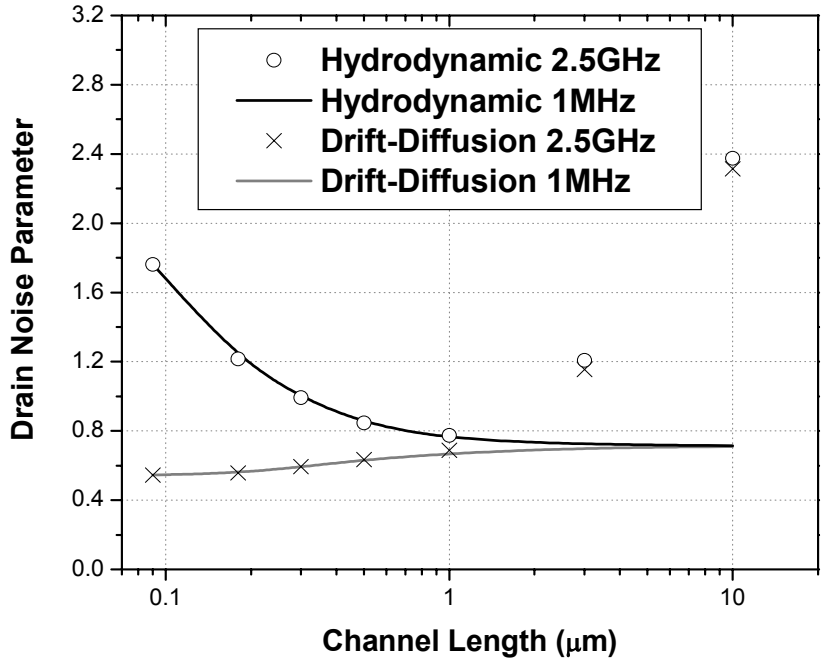


Fig 5.12 Drain noise parameter(γ) dependence on channel length reduction for NMOS transistors. Vg=1.08V and Vd=1.2V

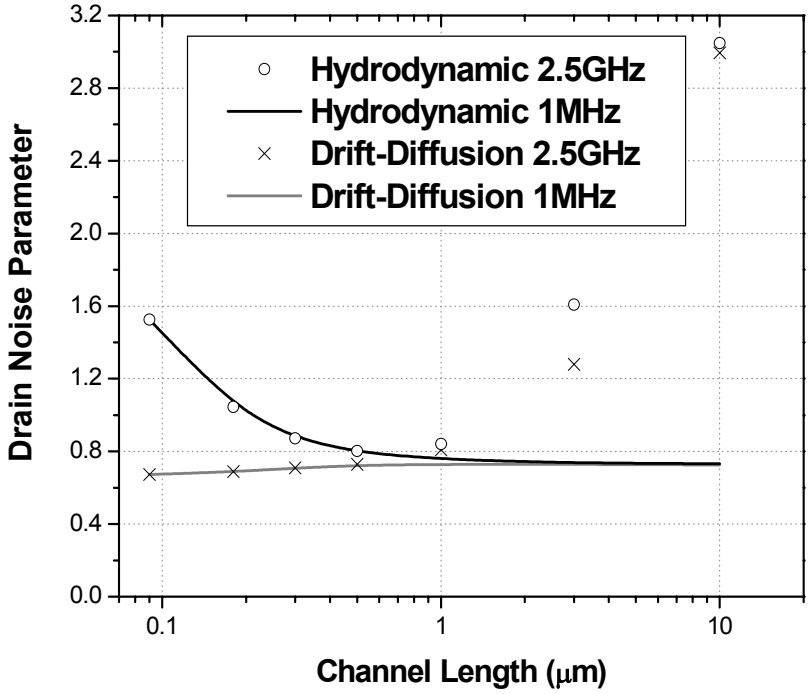


Fig 5.13 . Drain noise parameter (γ) dependence on channel length reduction for PMOS transistors. Vg=-1.07V and Vd=-1.2V

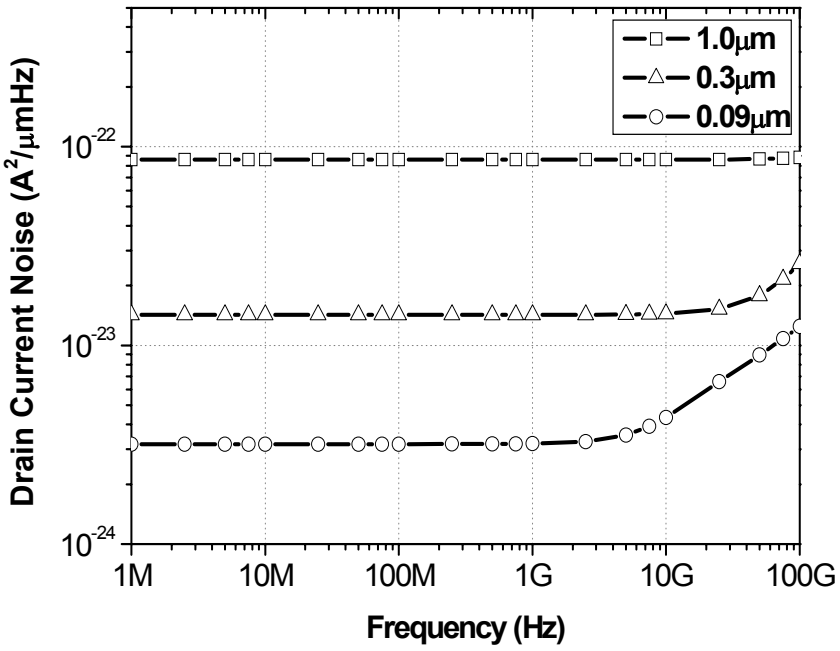


Fig 5.14 Frequency behavior of drain current noise of NMOS transistors with various channel length. Vg=1.08V and Vd=1.2V

5.3 Gate Noise Simulation

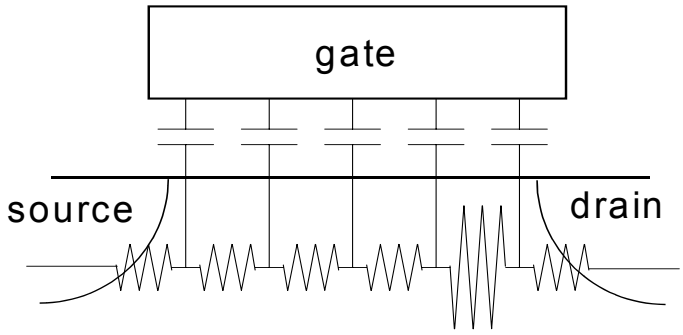


Fig 5.15 Circuit modeling of impedance field generation mechanism for gate current noise

While there is only one peak of $|\nabla A_k|^2$ in the channel for drain noise, there are two peaks of $|\nabla A_k|^2$ for gate noise. Fig 5.16 and 5.17 show the impedance field (A) for gate current noise in 1.0μm and 0.18μm channel length NMOS transistors, and Fig. 5.18 and 5.19 show $|\nabla A_k|^2$ for same devices. In Figs. 5.18 and 5.19, $|\nabla A_k|^2$ becomes zero in the middle of the channel, where the impedance field (A) starts to decrease. Among the two peaks of $|\nabla A_k|^2$, the one near the drain is always larger because the local *AC* resistance is smaller from low carrier concentrations as shown Fig. 5.15. In the 0.18μm channel length NMOS device, the $|\nabla A_k|^2$ calculation results from the drift-diffusion model is much higher because high electric field reduces electron mobility and local ac resistance near the drain.

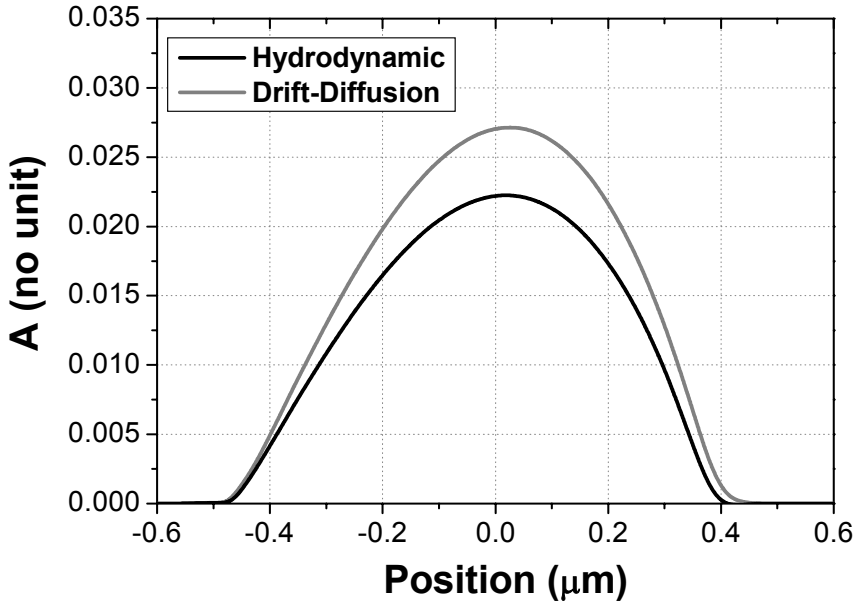


Fig 5.16 Impedance field to gate current noise at each channel position in 1.0μm channel length NMOS transistor. Gate voltage is 1.0V and drain voltage is 1.8V.

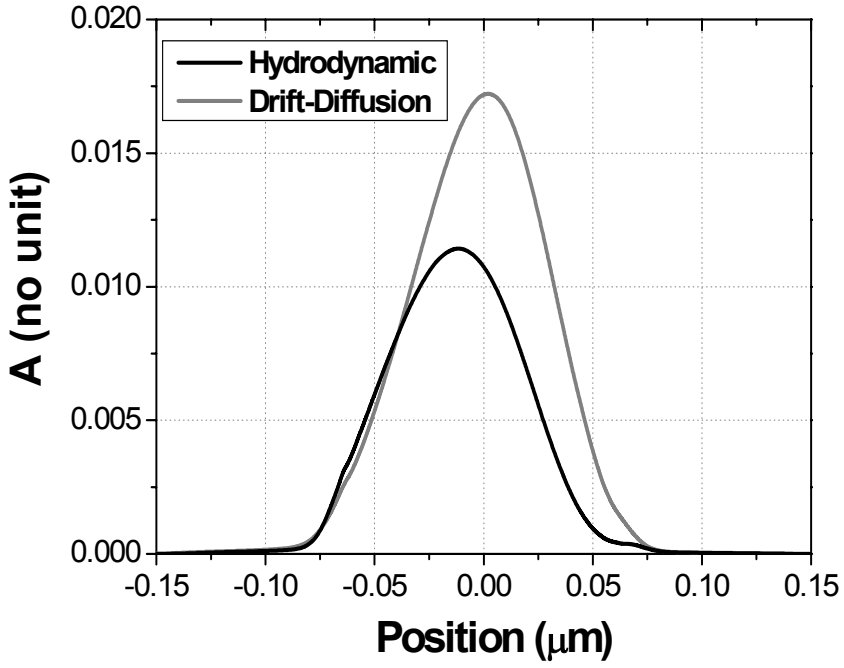


Fig 5.17 Impedance field to gate current noise at each channel position in 0.18μm channel length NMOS transistor. Gate voltage is 1.0V and drain voltage is 1.8V.

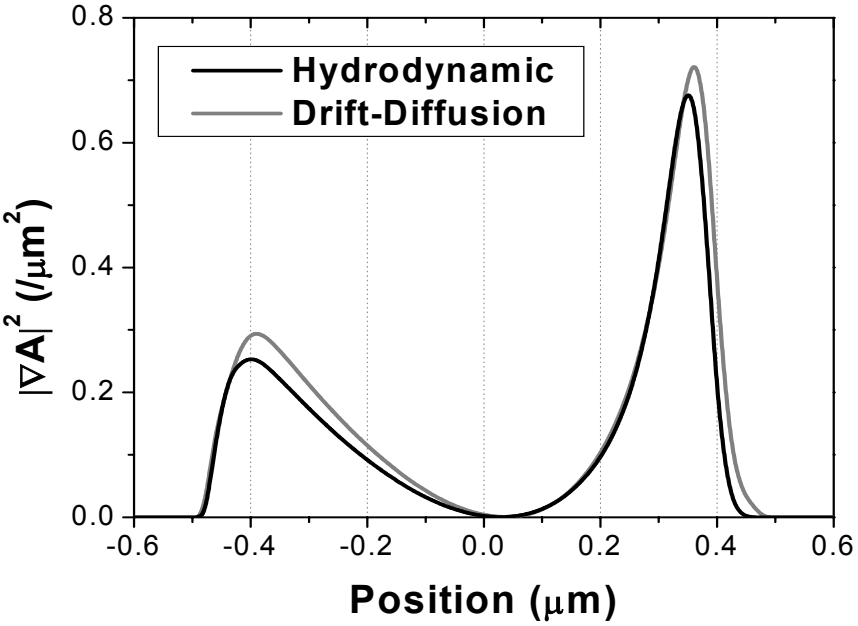


Fig 5.18 $|\nabla A|^2$ to gate current noise at each channel position in 1.0μm channel length NMOS transistor. Gate voltage is 1.0V and drain voltage is 1.8V.

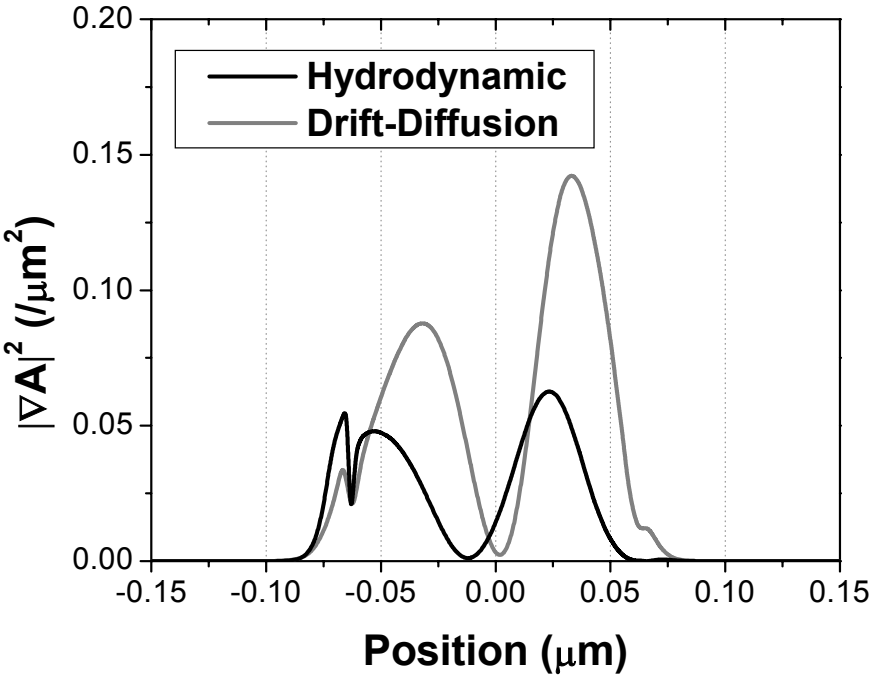


Fig 5.19 $|\nabla A|^2$ to gate current noise at each channel position in 0.18μm channel length NMOS transistor. Gate voltage is 1.0V and drain voltage is 1.8V.

Although, $|\nabla A_k|^2$ is larger near the drain, the local noise source is larger near the source due to higher carrier concentrations as shown in Fig 5.2 and 5.3. Therefore, in long channel MOS transistors(Fig. 5.20), the contribution to gate current noise is larger near the source. In short channel MOS transistors, the *hydrodynamic* model predicts that the contribution to gate noise near the drain is equal or higher than the contribution near the source while the drift-diffusion model still predicts a larger contribution near the source. The mobility used in the drift-diffusion model decreases near the drain due to high electric fields, and reduces the size of local noise sources. On the contrary, the high electron temperature from the *hydrodynamic* model increases the size of local noise sources near the drain.

The vertical carrier distribution changes also have an effect on the gate current noise. Fig. 5.22 and 5.23 show the electron concentrations under the gate oxide for a 0.18μm channel length NMOS transistor calculated using drift-diffusion and *hydrodynamic* models respectively. The results from the *hydrodynamic* model show a spread of electron concentration near the drain owing to the scattering of high energy carriers. As a result, the depth contributes to gate noise, and creates a larger contribution because the contribution is integrated in vertical direction. Therefore, the carrier concentration spread becomes a factor that increases the gate current noise.

In Fig. 5.24, graphs are the impedance field calculation result from the *hydrodynamic* model, however, for the gray colored line, the electron temperature is artificially flattened to lattice temperature when the local noise source is calculated. This result clearly shows how the high carrier temperature increases gate current noise.

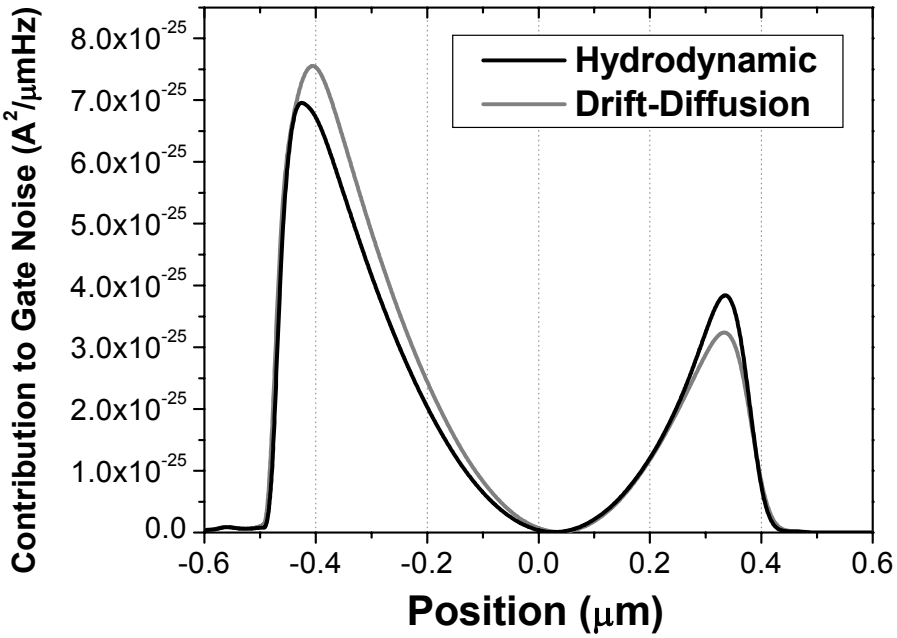


Fig 5.20 Contribution to gate current noise at each channel position in 1.0μm channel length NMOS transistor. Gate voltage is 1.0V and drain voltage is 1.8V.

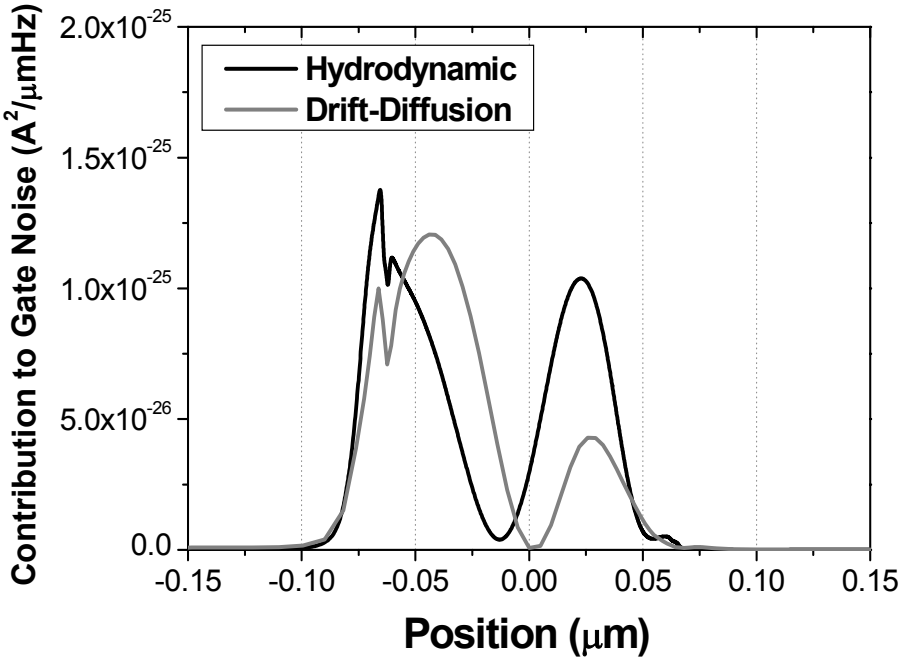


Fig 5.21 Contribution to gate current noise at each channel position in 0,18μm channel length NMOS transistor. Gate voltage is 1.0V and drain voltage is 1.8V.

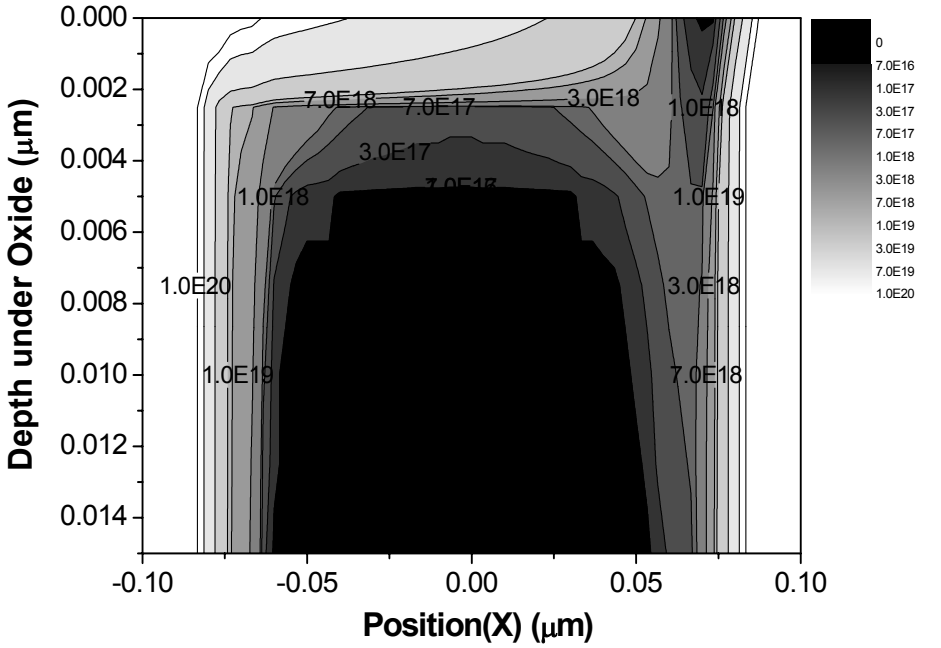


Fig 5.22 Electron concentration calculation result under gate oxide of 0.18μm channel length NMOS transistor from drift-diffusion model. Gate voltage is 1.0V and drain voltage is 1.8V.

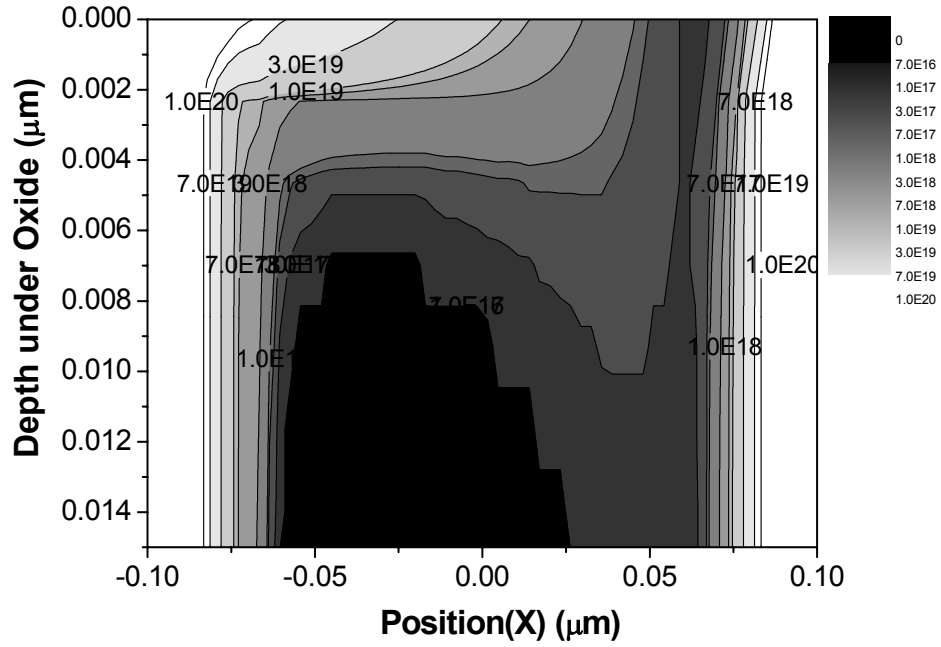


Fig 5.23 Electron concentration calculation result under gate oxide of 0.18μm channel length NMOS transistor from hydrodynamic model. Gate voltage is 1.0V and drain voltage is 1.8V.

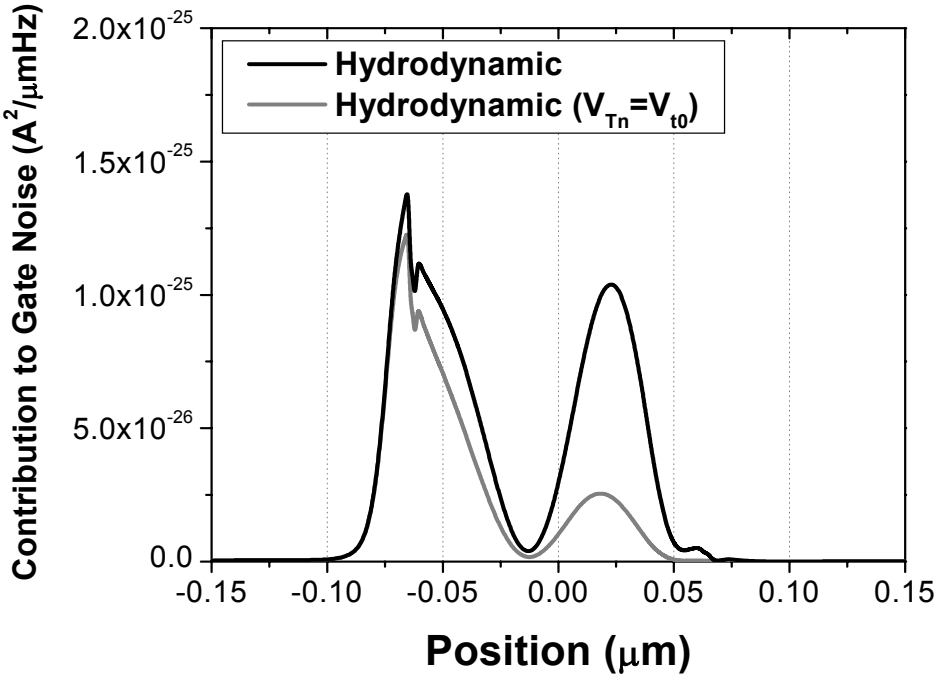


Fig 5.24 Effect of carrier temperature on contribution to gate current noise in 0.18μm channel length NMOS transistor. Gate voltage is 1.0V and drain voltage is 1.8V.

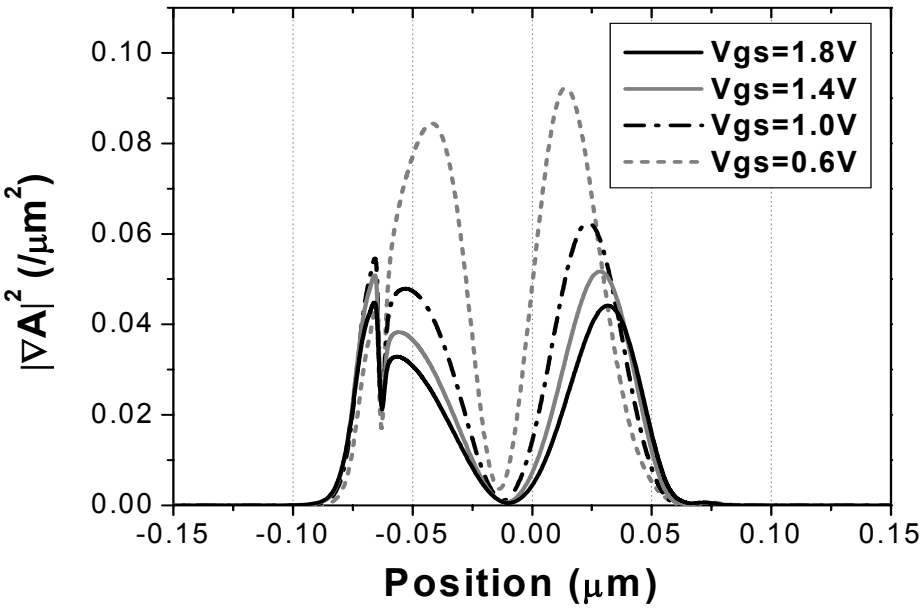


Fig 5.25 $\left|\nabla A\right|^2$ dependency on gate voltage in 0.18μm channel length NMOS transistor. Drain voltage is 1.8V.

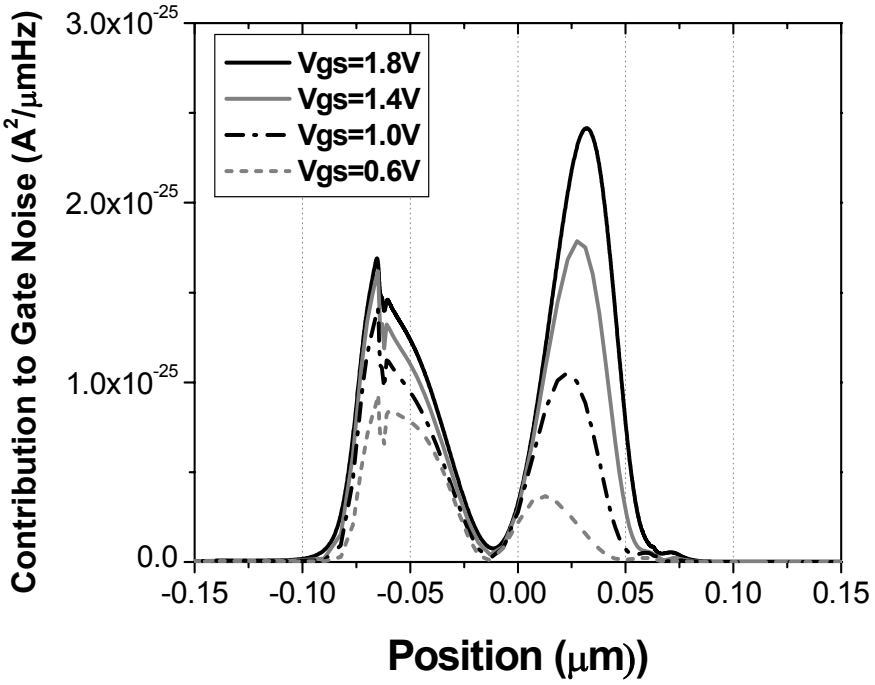
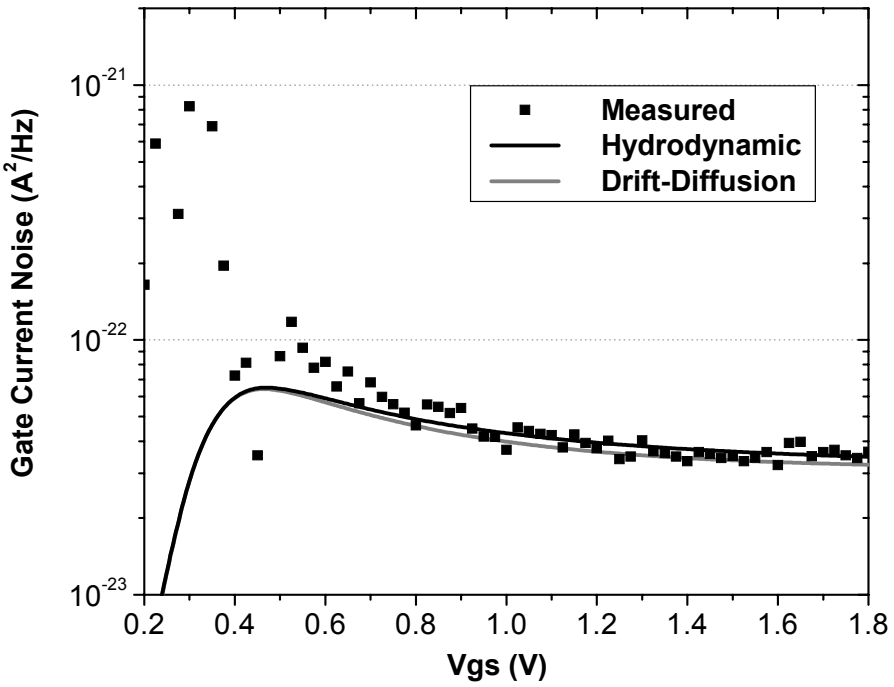


Fig 5.26 Contribution change to gate current noise on gate voltage in 0.18μm channel length NMOS transistor. Drain voltage is 1.8V.

The shape of contribution to gate noise and total gate noise depends on gate bias. Figs. 5.25 and 5.26 show $|\nabla A_k|^2$ and the contributions to gate noise at each channel position of the 0.18μm channel length NMOS transistor using the *hydrodynamic* model with various gate bias. As the gate bias increases, $|\nabla A_k|^2$ decreases because the carrier concentration decreases and resistance is reduced. However, the contributions to gate current noise increase because larger carrier concentrations increase the amount of the local noise source. Fig 5.26 shows that the contributions to gate current noise from the drain side in the channel increases rapidly with gate bias, and the total gate noise increases consequently. The local noise source near the drain increases faster, because the high carrier temperature accelerates the increment of local noise sources.

(a)



(b)

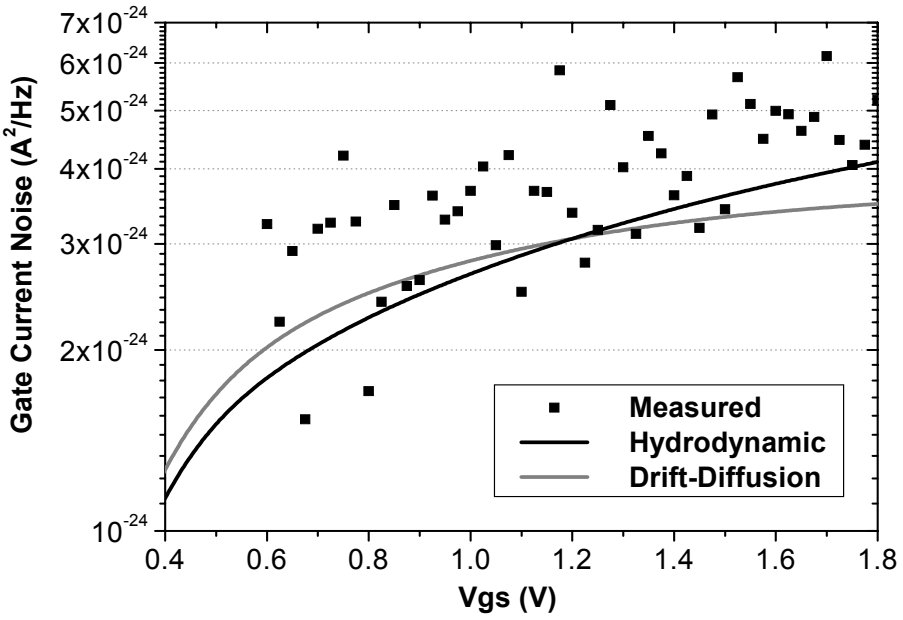


Fig 5.27 Simulation result and measured data for gate current noise. Drain voltage is 1.8V and gate voltage was swept. (a) 1.0 μm Channel Length. (b) 0.18 μm Channel Length.

The measured data and total gate noise calculation results are shown in Fig 5.27. For the 1.0μm channel length device, both *hydrodynamic* and drift-diffusion models show good agreement with measured data. However, in 0.18μm channel length device the results from drift-diffusion model do not show a rapid increment with gate bias. Also we can notice that the gate current noise measured data for 1.0μm channel length NMOS transistors remain constant with gate bias while it shows a steady increase for 0.18μm channel length MOS transistors. This also proves that the gate current noise increases from high energy carriers in short channel MOS transistors.

The gate excess noise factor (δ) is defined as follows:

$$\overline{i_{ng}^2} = 4kT\delta g_g \Delta f \tag{5.8}$$

where $\overline{i_{ng}^2}$ is power spectral density of gate current noise and g_g is the real part of gate to the source admittance.

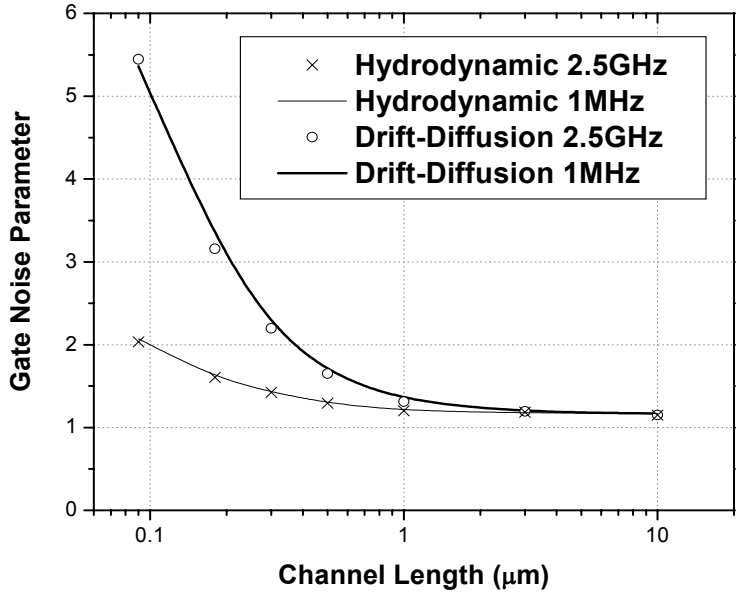


Fig 5.28 Gate noise parameter (δ) dependence on channel length reduction for NMOS transistors. Vg=1.08V and Vd=1.2V

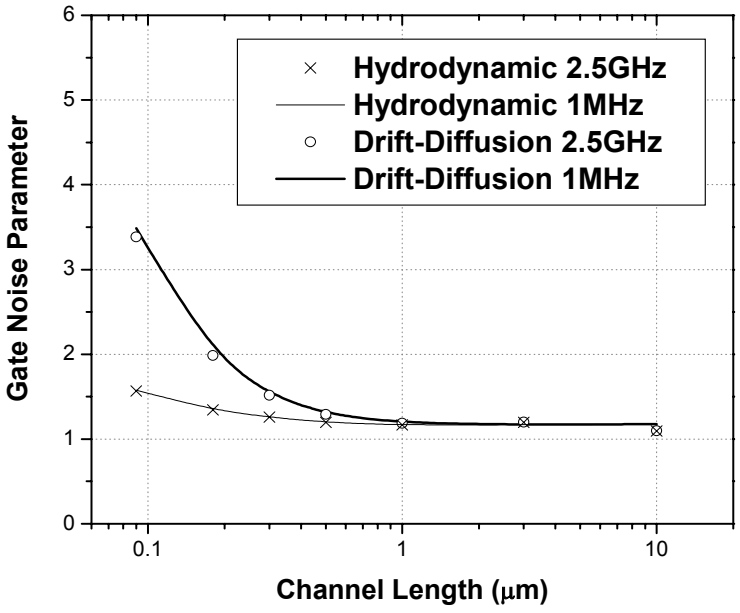


Fig 5.29 Gate noise parameter (δ) dependence on channel length reduction for PMOS transistors. Vg=-1.07V and Vd=1.2V

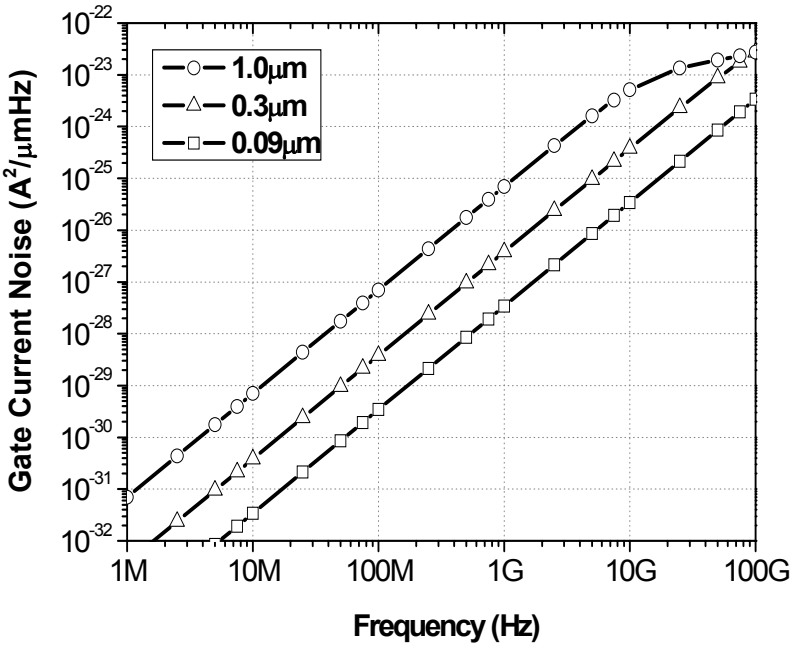


Fig 5.30 Frequency behavior of gate current noise of NMOS transistors with various channel length. Vg=1.08V and Vd=1.2V

In Figs. 5.28 and 5.29 the gate excess noise factor (δ) for various channel lengths is shown. The gate noise parameter increases rapidly in short channel devices. For the 90nm channel length devices, the *hydrodynamic* model predicts 5.36 for NMOS and 3.49 for PMOS transistors.

In the van der Ziel model, g_g is approximated by following equation[21]

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}} \tag{5.9}$$

Therefore, the power spectral density of gate current noise is proportional to the square of frequency and gate to source capacitance. As frequency and capacitance increase, the gate to channel impedance decreases and induces more gate current noise. This frequency behavior of gate current noise is shown in Fig 5.30.

5.4 Correlation Coefficient Simulation

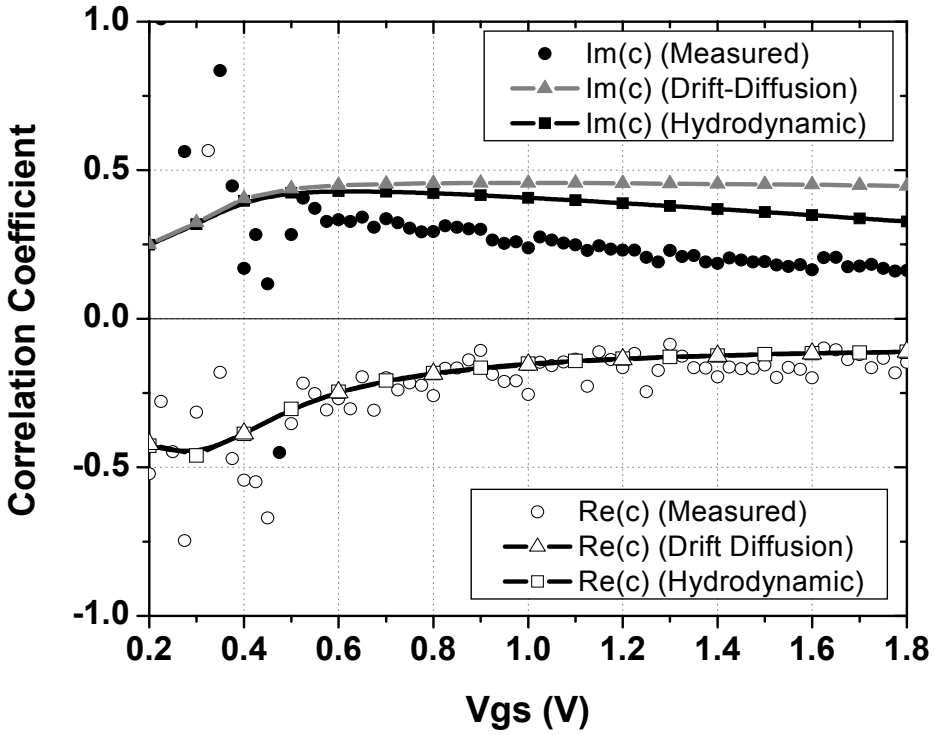


Fig 5.31 Simulation result and measured data for correlation coefficient between gate and drain current noise in 1.0μm channel length NMOS transistor. Simulation and measurement frequency is 2.475GHz and drain voltage is 1.8V.

The correlation coefficient between gate and drain current noise is defined by the following equation:

$$c = \frac{\overline{i_{ng} i_{nd}^{*}}}{\sqrt{\overline{i_{ng}^{2}}\,\overline{i_{nd}^{2}}}} \tag{5.10}$$

This correlation coefficient provides very important information to RF circuit designers because the noise in a CMOS RF circuit can be minimized by exploiting that correlation[30].

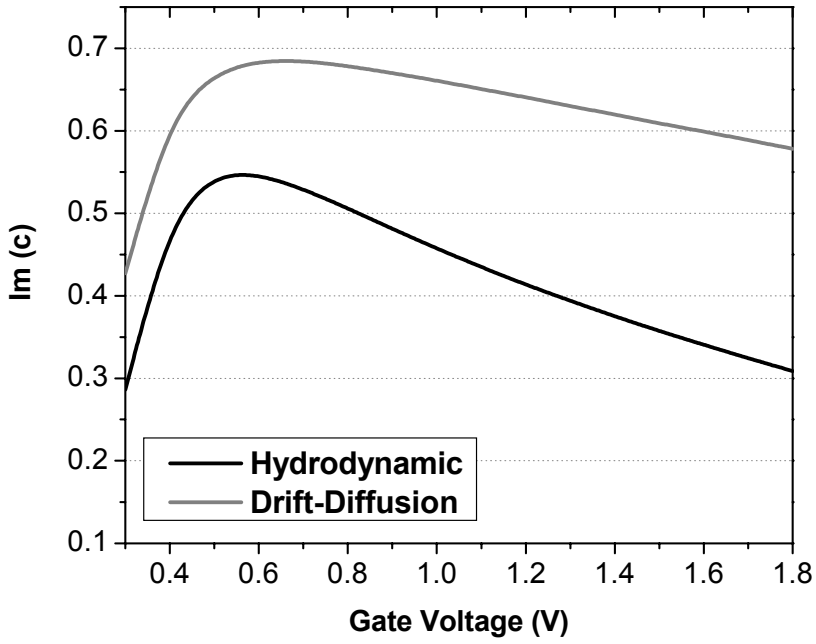


Fig 5.32 Simulation result for correlation coefficient between gate and drain current noise in 0.18μm channel length NMOS transistor. Simulation and measurement frequency is 5.0GHz and drain voltage is 1.8V.

Fig 5.31 shows the measured data and simulation results for extracted +correlation coefficient between gate and drain current noise components in 1.0μm channel length NMOS transistors. For the real part of correlation coefficient, both drift-diffusion and *hydrodynamic* models give good agreement with measured data. However, for the imaginary part of correlation coefficient, only the *hydrodynamic* model shows a slight decrease with gate bias as reflected in measured data.

The same simulations were performed for 0.18μm channel length NMOS transistors and plotted in Fig 5.32. The real part of the correlation coefficient is omitted because the value is virtually zero at the simulation frequencies, 5GHz, due to the high cut-off frequency of 0.18μm channel length NMOS transistor. While the correlation coefficient becomes a constant of 0.395j[21] in the analytical calculation of van der Ziel, it is a strong function of gate bias in short channel MOS transistors. After the gate bias is above threshold, the correlation coefficient decreases rapidly, and the decrease is much faster in *hydrodynamic* model case.

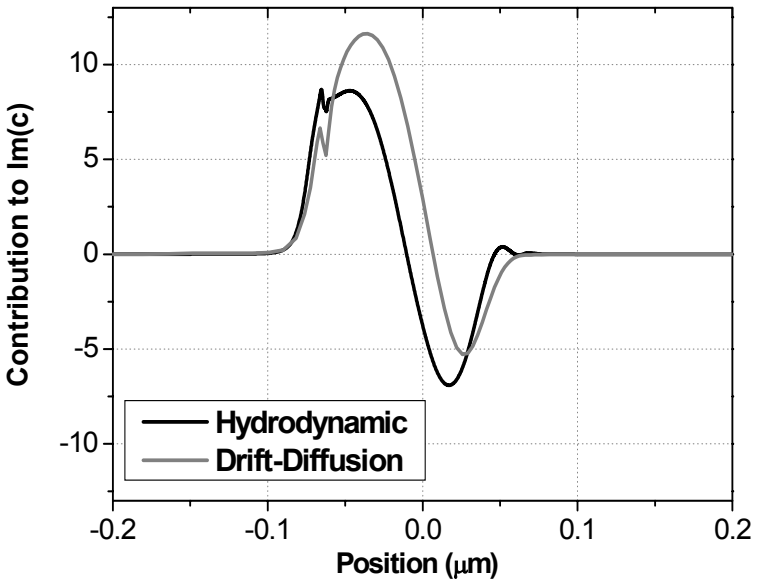


Fig 5.33 Contribution to imaginary part of correlation coefficient between gate and drain current noise in 0.18μm channel length NMOS transistor. Simulation and measurement frequency is 5.0GHz. Gate voltage is 1.0V and drain voltage is 1.8V.

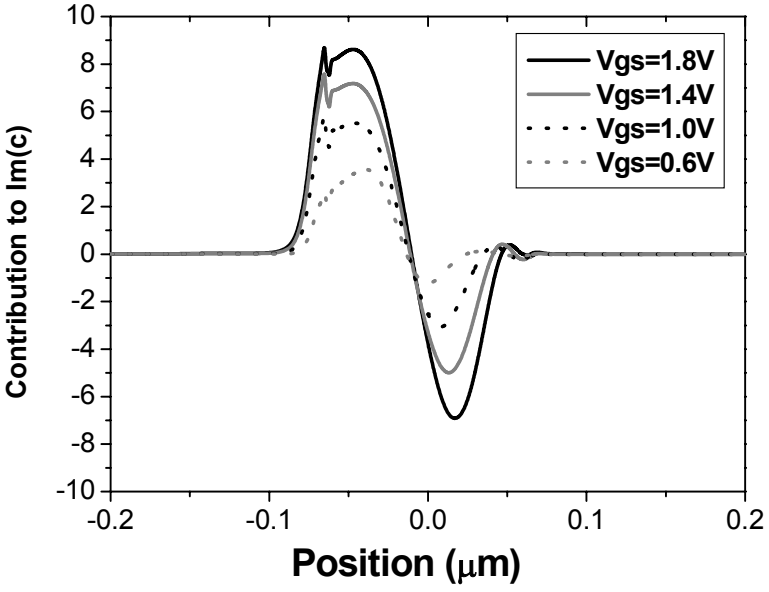


Fig 5.34 Gate bias effect on the change of contribution to imaginary part of correlation coefficient between gate and drain current noise in 0.18μm channel length NMOS transistor. Simulation and measurement frequency is 5.0GHz. Gate voltage is 1.0V and drain voltage is 1.8V.

The difference of the excess noise mechanisms for drain current noise and gate current noise create this reduction of the correlation coefficient. Fig. 5.33 shows the contribution to the imaginary part of the correlation coefficient(Im(c)) from the channel. The source side has a positive sign contribution and the drain side has a negative sign contribution. In the *hydrodynamic* simulation case, the contribution to gate noise from drain side is far larger than for the drift-diffusion simulation case, creating more negative contributions to Im(c). Therefore, those two opposite contribution to Im(c) cancel each other and Im(c) decreases. Also, as we can see in Fig. 5.34, higher gate bias creates more negative contribution to Im(c) from drain side due to larger gate noise generation and Im(c) decreases with gate bias.

Figs. 5.35 and 5.36 show the calculation results of Im(c) with different channel lengths. Im(c) decreases with channel length in the *hydrodynamic* model, while it increases slightly in the drift-diffusion model. The result from the *hydrodynamic* model agrees well with experimental results[31]. From the simulation results, only Im(c) in NMOS transistors start to rise again at extremely short channel lengths under 0.1μm. The stronger high energy electron effects in NMOS device even start to increase the gate noise generation near the source and in turn increases Im(c).

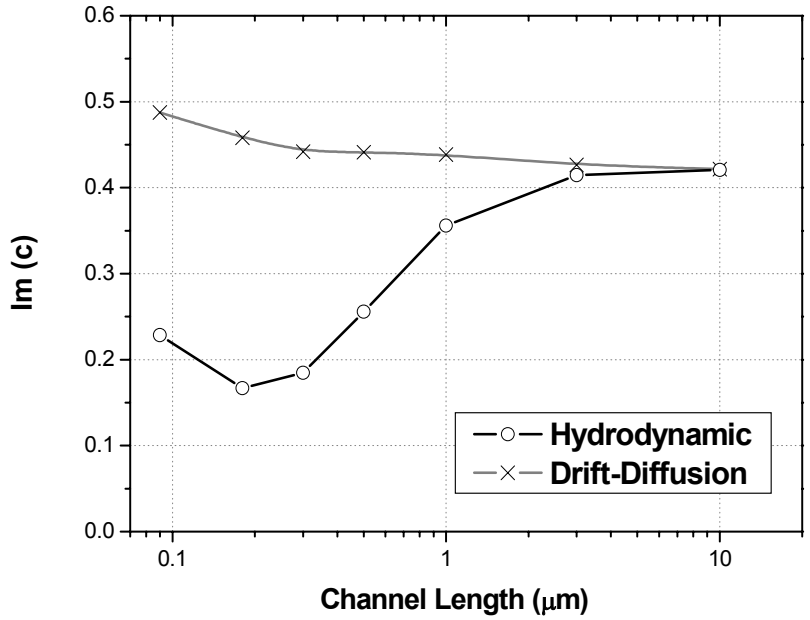


Fig 5.35 Relation of imaginary part of correlation coefficient between gate and drain noise (Im(c)) with channel length for NMOS transistor. Vg=1.08V and Vd=1.2V

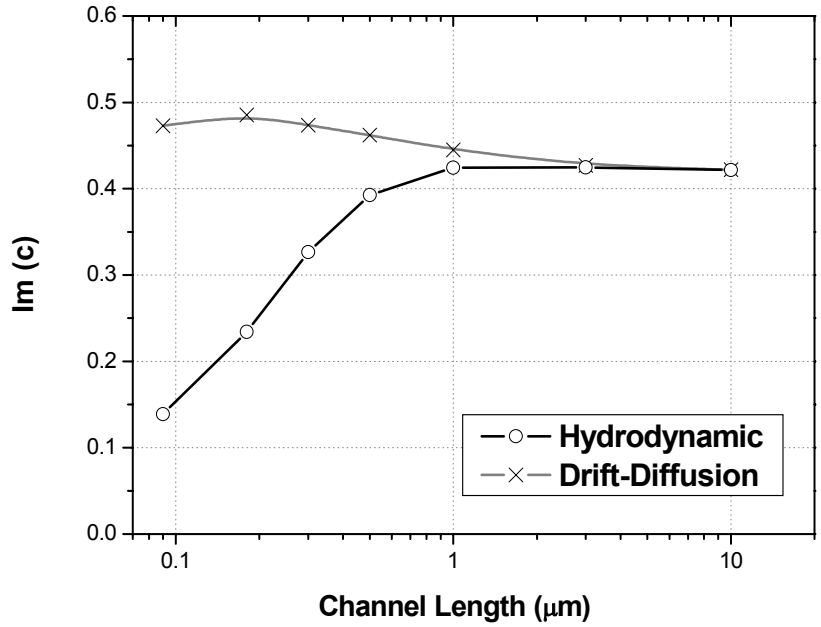


Fig 5.36 Relation of imaginary part of correlation coefficient between gate and drain noise (Im(c)) with channel length for NMOS transistor. Vg=1.08V and Vd=1.2V

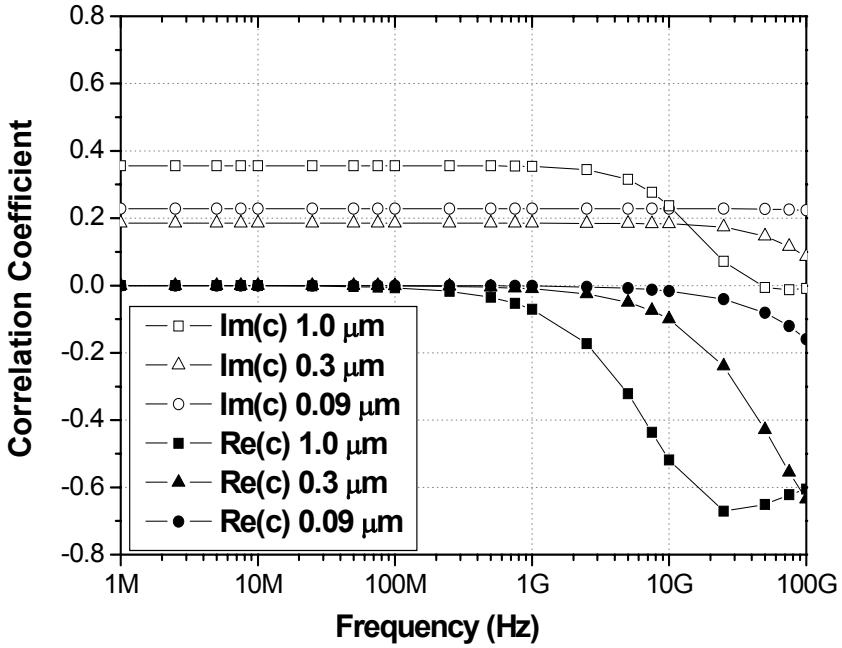


Fig 5.37 Frequency behavior of correlation coefficient between gate and drain noise with various channel length. Vg=1.08V and Vd=1.2V

The frequency behavior of the correlation coefficient between gate and drain current noises is illustrated in Fig 5.37. At low frequency, the gate to channel capacitance dominates the impedance between gate and source and Im(c) is much larger than Re(c). As the frequency is increased to gigaHertz levels, the channel resistance starts to dominate the impedance and Im(c) is reduced to zero and Re(c) becomes larger.

5.5 Noise generation from gate resistance

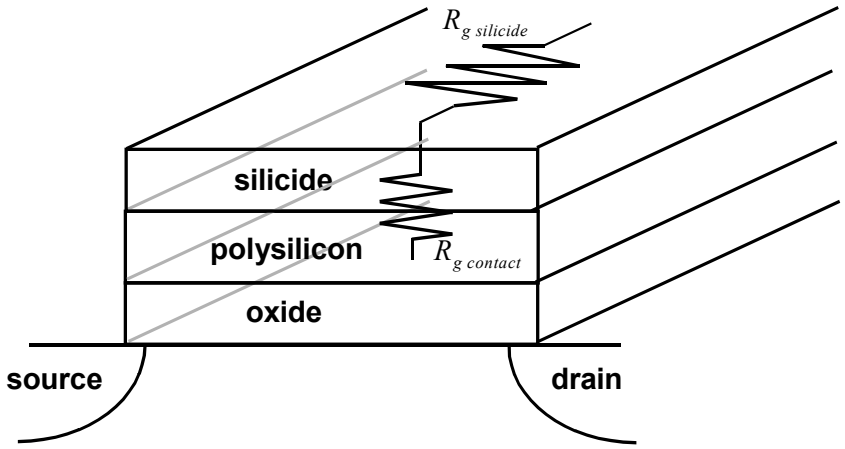


Fig. 5.38 Parasitic gate resistance in MOS transistors

Another important noise source in short channel MOS transistors is the gate resistance. A 0.5μm thickness polysilicon film is known to have about 20Ω/□ with practical doping concentrations. Usually metal silicides, such as $TiSi_2$, are placed over the poly-silicon film to reduce the sheet resistance to 2-3Ω/□ range, while keeping the properties of oxide silicon characteristics the same[32]. However, the interface between polysilicon and silicide form a Schottky contact and contribute significantly to gate resistance with a typical value of about 25Ωμm^2[33]. The gate resistance from the silicide sheet, when gate is connected only on one side, is expressed as

$$R_{g\ silicide} = \frac{R_{\square} W}{3 L_g} \tag{5.11}$$

where $R_{\square}$ is the sheet resistance of the silicide layer, W is the gate width, and L_g is the gate length. Also the resistance from the contact is

$$R_{g\,contact} = \frac{r_c}{WL_g} \tag{5.12}$$

where r_c is the contact resistivity between the silicide and polysilicon.

As the device size shrinks, the gate length is reduced, and both $R_{g\,silicide}$ and $R_{g\,contact}$ are inversely proportional to the gate length. Therefore the total gate resistance increases, and this resistance can be modeled as an additional noisy resistance which is externally connected to the gate as illustrated in Fig 5.39. In the case of 0.18μm channel length MOS devices used in this simulation, the total gate resistance was extracted to be about 74.8 Ω/ μm. This resistance has to be included in the noise simulation self-consistently, because it has an effect on not only gate current noise but also drain current noise. The noise from this gate resistance causes fluctuation in the gate potential and consequently changes drain noise values. Therefore, it also has effect on the correlation coefficient between gate and drain current noises.

The simulation results shown in Section 5.1~5.4 all include this gate resistance to compare the results with measured data. From the simulation results, the gate resistance increase drain current noise about 5%, which means significant drain current noise is still generated in the channel. However, for gate noise, about 43% of gate noise is generated from gate resistance when the gate voltage is 1.0V, as shown in Fig. 5.40. This ratio is reduced to 19% when the gate voltage is increased to 1.8V, since the intrinsic gate noise of the MOS transistor increases with gate voltage.

From simulation results, it appears that the gate resistance increases the imaginary part of the correlation coefficient between gate and drain current noise about 0.1. The extra gate current noise and drain current noise are generated from the same source, gate resistance, and coupled by gate capacitance. Therefore, it increases the imaginary part of correlation coefficient. Fig. 5.41 shows the effect of gate resistance on the imaginary part of correlation coefficient in 0.18μm channel length NMOS transistors is illustrated. The increment does not depend on gate bias after the transistor fully turns on, because it is from external resistance, not from the channel.

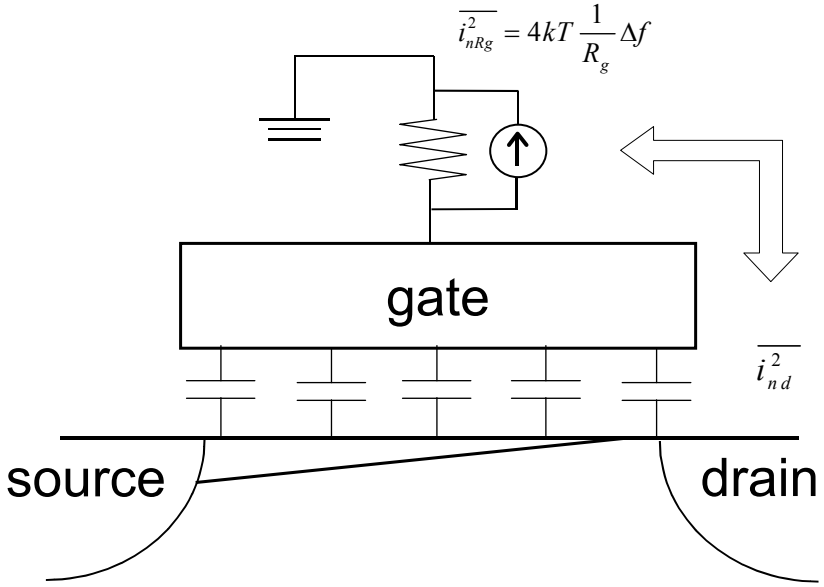


Fig. 5.39 Modeling of gate parasitic resistance to external noisy resistance

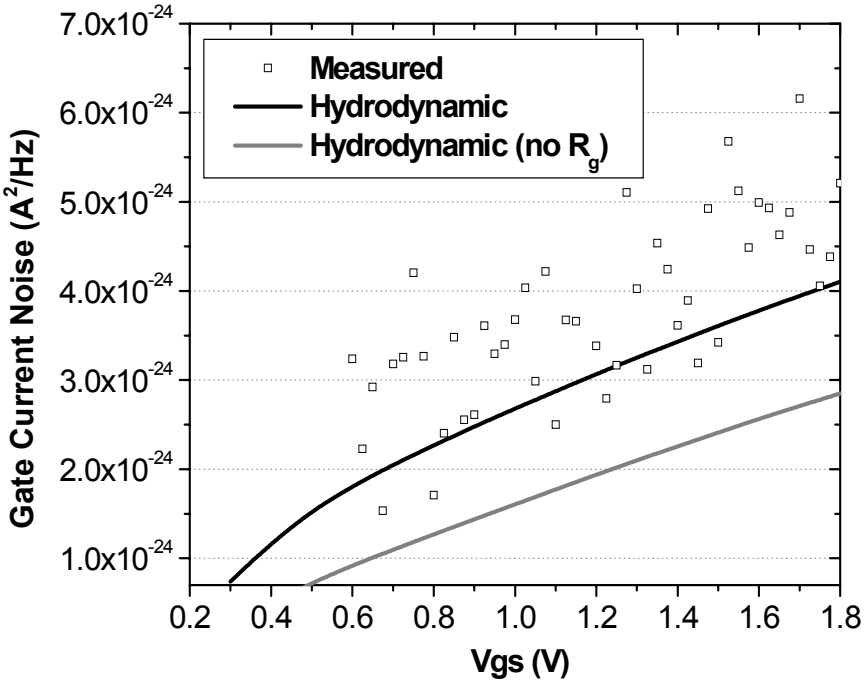


Fig. 5.40 Gate resistance effect on gate current noise

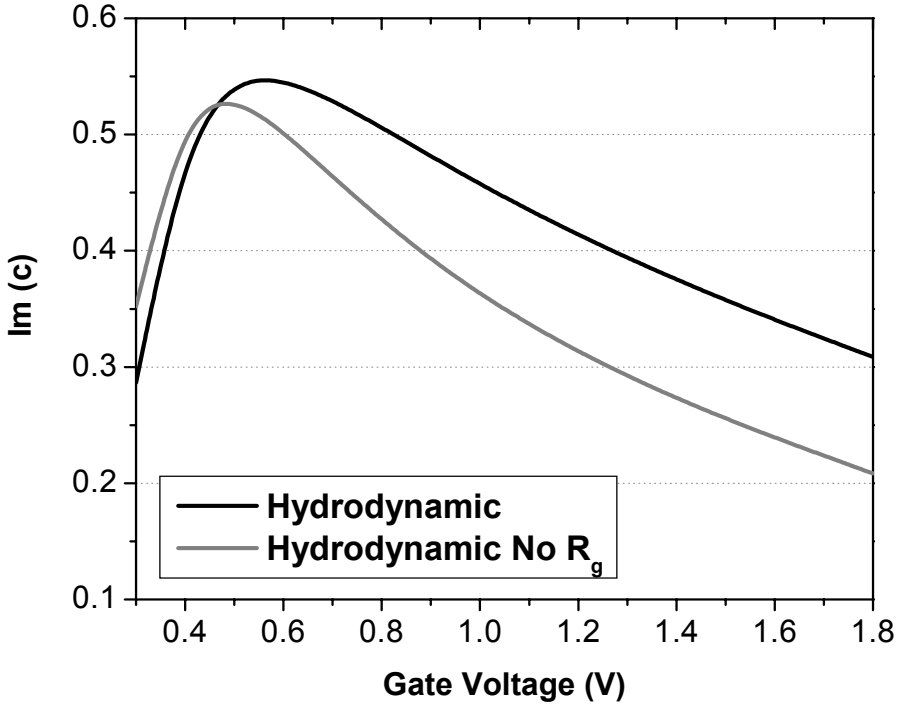


Fig. 5.41 Gate resistance effect on imaginary part of correlation coefficient between gate and drain noise

5.6 Summary

The *Hydrodynamic* transport model using impedance field method developed in chapter 3 and 4 has been implemented in a PDE-based simulator, PROPHET, using the theories developed and the post-processing modules were used for noise simulation. The noise simulation results were compared with classical calculation results and measured data, and the simulation results agree well with measured data.

Drain noise simulation results show that the middle of the channel near source has the greatest contribution to drain current noise, due to the shape of the impedance field. Although, the electric field near the drain is high and accelerates carriers to have large kinetic energy, it has minimal impact on drain noise because the gradient of impedance field is zero near the drain. The *hydrodynamic* noise simulation results predict drain noise parameters for 90nm channel length devices to be 1.76 and 1.52 for NMOS and PMOS transistors respectively. *Hydrodynamic* simulations predict larger drain current noise than drift-diffusion simulation and the difference mainly comes from the local noise source model; creating an accurate local noise source model is most important for drain noise simulation.

For the gate noise parameter, the *hydrodynamic* model predicts 5.36 and 3.48 for 90nm channel length NMOS and PMOS transistors, respectively. Electron mobility in the channel is higher than hole mobility, making NMOS have less voltage drops until velocity overshoot region. Therefore, NMOS transistors suffer from high energy carrier effect more than PMOS transistors. The square of the gradient impedance field has ‘M’ shape and the contribution to gate noise has two peaks in the channel. In long channel MOS transistors, the high carrier concentration near the source contributes substantially to gate noise. However, as the channel length shrinks, the peak near the drain also becomes a major contributor for gate noise because the high electric field near the drain generates high energy carriers and more noise.

The correlation coefficient between gate and drain noise also changes as the drain side creates more noise. The source side has a positive sign contribution to the imaginary part of correlation coefficient between gate and drain noise, while drain side has a negative sign contribution. Therefore, the contribution to the imaginary part of the correlation coefficient starts to cancel as more gate noise is generated near drain.

The gate bias also has a large influence on gate noise and the correlation coefficient between gate and drain noise in short channel MOS transistors. Although in long channel MOS transistors the amount of gate current noise does not change with gate bias, it increases rapidly in short channel MOS transistors. The carrier concentration near the drain increases with gate bias, and

generates more gate noise. The correlation coefficient between gate and drain noise also reduced by this effect.

As the MOS transistor size scales down, the parasitic gate resistance becomes noticeable. The contact resistance between silicide and polysilicon is also a major source for the parasitic gate resistance. This parasitic gate resistance also generates noise, and additional drain noise is also induced. This induced drain noise creates increased correlation between gate and drain current noise, making the noise modeling of short-channel transistors more complex. The gate resistance is another important performance limiting factor for CMOS RF circuits.

CHAPTER 6

Conclusions

The *AC* and noise simulation of deep-submicron MOS device has emerged as a very important issue as device size scales down and the operation frequency of CMOS circuits rise. However, the quantum mechanical effects and high energy carriers in deep-submicron device impede the accurate computer simulations. This dissertation has explored the computer simulation techniques to overcome those obstacles and explained the underlying physics. The presented contents should help TCAD engineers to achieve accurate computer simulation, and develop improved circuit models. This also should help circuit designers to create advanced RF circuits with better insight using circuit simulators. This chapter summarizes the contributions of this dissertation and proposes future work as extensions of this research.

6.1 Summary

As the MOS device size scales down, the physical oxide thickness gets thinner, and the potential well under gate oxide splits the energy bands into subbands and cause quantum mechanical effects. Due to these quantum mechanical effects, the maximum of carrier concentration is located several angstroms under the gate oxide causing increase in effective oxide thickness. The *density-gradient* model is an efficient approach to simulate this without solving the complex multi-dimensional Schrödinger equations. In Chapter 2, an *AC* analysis

method using the density-gradient model was presented and the simulation result with measured data were illustrated. *AC* analysis based on the *density-gradient* method can be solutions for a device with small additional computation cost compared to the classical method, and results show good agreement with measured data.

Shorter channel lengths increase the electric field in the channel, invalidating the quasi-equilibrium assumption. The carriers in the channel are accelerated to have several times more kinetic energy from the high electric field, and the *hydrodynamic* model is required to simulate this accurately. Chapter 3 explains how the *hydrodynamic* model can be implemented in a device simulator, and the numerical techniques of discritization for energy transport. The high energy carriers cause velocity overshoot near the drain, changing the carrier injection condition at the source. Therefore, the current lever becomes higher than values predicted by classical methods.

For the noise simulation of deep-submicron channel length MOS devices, a full 2D simulation is necessary, because secondary effects from scaling gets more important. A popular method for multi-dimensional noise simulation is the impedance field method. This method describes the noise at each electrode by a transfer function and local noise sources. In deep-submicron MOS devices, noise simulation based on the classical model does not give satisfactory results, because the transfer function local noise source size changes due to high energy carriers. Chapter 4 delivers the basic idea of the impedance field method and a new local noise source model based on the *hydrodynamic* model.

Chapter 5 presents the noise simulation results based on the theory explained in Chapter 3 and 4, and the noise generation mechanism analyzed. The middle of channel near source has the most contribution to drain current noise, due to the shape of the impedance field. The high energy carriers have minimal impact on drain noise because the gradient of impedance field is zero near the drain. The difference between noise simulation results of hydrodynamic and drift-diffusion models mainly comes from the local noise source model; creating an accurate local noise source model is most important for drain noise simulation.

The contribution to gate noise has two peaks in the channel. In the long channel MOS transistor, the peak near source is larger since the local noise source is larger from higher carrier concentrations. As the channel length shrinks, the peak near drain rises due to high energy carriers which are generated near the drain, and becomes a major contributor to gate noise. This phenomenon also has impact on the correlation coefficient between gate and drain noise. As the drain side generates more gate noise, the correlation coefficient cancels out and decreases.

While the gate current noise for long channel MOS transistors does not change with gate bias, it increases rapidly with gate bias for short channel MOS transistors. In short channel MOS transistors, the local noise source size near the drain rises quickly with gate bias, generating more gate noise. This also causes a reduction of the correlation coefficient between gate and drain noise.

Another major source of noise generation is the gate contact resistance. This contact resistance is an external noise source to the gate, in creating noise. By changing the effective gate voltage, gate resistance also generates drain current noise. Therefore, this gate contact resistance will be another important factor that limits noise performance of CMOS RF circuits.

6.2 Suggested Future Work

This thesis has presented the *AC* and noise behaviors of deep-submicron MOS transistors, however, as the size of the MOS devices continue scale down aggressively, there are still many challenging topics for research. Several recommendations for future research will be discussed here.

A simple extension of this study will be 1/f and generation-recombination noise. The impedance field method also can be used with other types of local noise sources. Therefore, if we can model the local noise source accurately, it is straight forward to expand this work to 1/f and generation-recombination noise sources.

The channel length of a MOS transistor will eventually be reduced to tens of nanometer range. This size of short channel length will be comparable to the carrier mean free path, which is in the several nanometer range. Therefore, the local noise at each point will have a correlation with that of another location. This effect creates another uncertainty of noise performance in MOS transistors. Currently, no significant investigation or measurement has been performed on this matter.

Another interesting noise source is gate tunneling noise. If the gate oxide thickness is reduced to under 20 angstroms the tunneling current through the gate oxide can not be ignored. This tunneling current has 1/f properties, because this is a current through a potential barrier. Already, some measurements were performed on this noise source, however it hasn't been imported to device simulator and circuit model yet.

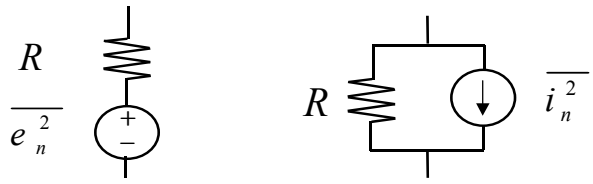
There are other suggested future works as expansion of this work. One is simulation of other structures such as SOI or SiGe HBT. Especially, noise modeling of SiGe HBTs are gaining

attention because it has major applications in RF circuits. SiGe HBT is superior to homojunction BJT in almost every aspect, and still can be integrated with CMOS circuits. Currently, the noise simulation of SiGe HBT devices at devices simulator level is studied by researchers[34]. This will help circuit engineers to optimize for their applications.

Appendix A

Modeling of Noise Source

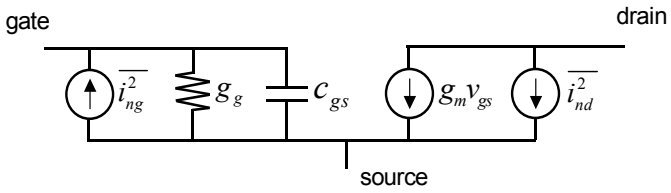
- Resistor Noise Models :



$$\overline{e_n^2} = 4kTR\Delta f \qquad \overline{i_n^2} = \frac{\overline{e_n^2}}{R^2} = \frac{4kT\Delta f}{R}$$

The thermal noise of a resistance can be modeled as voltage noise source or current noise source. Both models are equivalent and can be transformed to each other for convenience. The power spectral density of thermal noise voltage is as shown above and independent of frequency until several THz.

● MOS Noise Model :



• Drain Noise : $\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f + \frac{K_1}{f}\Delta f$ γ : drain noise parameter

• Gate Noise : $\overline{i_{ng}^2} = 4kT\delta g_g \Delta f$ δ : gate noise parameter

g_{d0} : Drain output conductance under zero drain bias

g_g : Real part of gate to source admittance

• Correlation Coefficient between gate and drain noise :

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2}\,\overline{i_d^2}}}$$

The noise in MOS transistor is usually modeled as current noise source because electric engineers are usually more interested in current characteristic of a device at given voltage bias. The analytic calculation result from A. van der Ziel suggests

$$\gamma = 2/3$$

$$\delta = 4/3$$

$$c = 0.395j$$

Appendix B

List of Symbols

Symbol	Meaning
k_B	Boltzmann's constant : $1.38\times10^{-23}JK^{-1}$
W	MOSFET width
L	MOSFET length
C_{ox}	MOSFET Gate Oxide Capacitance
C_{gs}	MOSFET Gate to Source Capacitance
$\hbar$	Planck's constant : $h/2\pi = 1.05459\times10^{-34}Js$
m_n	Electron Effective Mass
N_D	Concentration of Donor Type Dopant Atoms
N_A	Concentration of Acceptor Type Dopant Atoms
N_D^+	Concentration of Ionized Donor Type Dopant Atoms
N_A^-	Concentration of Ionized Acceptor Type Dopant Atoms
n	Electron Concentration
p	Hole Concentration
n_i	Intrinsic Carrier Density
Φ_n	Energy Level of Conduction Band
ϕ_n	Fermi Potential of Electrons
$\vec{s}_n$	Electron Energy Flux
$\vec{Q}$	Electron Heat Flux
$\vec{j_n}$	Electron Current Density
$\vec{E}$	Electric Field
ω_n	Electron Kinetic Energy

Symbol	Meaning
$\vec{v}_n$	Average Electron Velocity
v_s	Saturation Velocity of Carrier under High Electric Field
κ	Thermal Conductivity
σ_n	Electron Conductivity
T_n	Electron Temperature
v_{nT}	$= k_B T_n / q$
T_0	Lattice Temperature
v_{T0}	$= k_B T_0 / q$
$\tau_{n\varepsilon}$	Energy Relaxation Time of electrons
r	Recombination Rate of Carriers
τ_{cn}	Mean Time between Collisions for Electrons
$\vec{\xi}_{\vec{v}_n}$	Lagenvin Forces of Electron Velocity

∗ If subscript n is replaced with p in above table, the symbol is related with holes, rather than electrons.

Symbol	Meaning
μ_0	Mobility at Zero Electric Field Condition
D	Carrier Diffusion Constant
$A_{k\vec{r}}$	Impedance Field to kth Electrode at Location $\vec{r}$
S_{in}	Power Spectral Density of Local Noise Source
$\overline{i_{nd}^2}$	Power Spectral Density of Drain Noise
γ	Excess Drain Noise Parameter
g_{d0}	Drain to Source Conductance under Zero Drain Bias
$\overline{i_{ng}^2}$	Power Spectral Density of Gate Noise
δ	Excess Drain Noise Parameter
g_g	Real Part of Gate to Source Admittance
c	Correlation Coefficient between Gate and Drain Current Noise

∗ The subscript n in above table denotes noise, not electrons.

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