SMALL-SIGNAL MODELING OF RF CMOS

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Abstract

Continuous scaling of CMOS technology has now reached a state of evolution, in terms of both frequency and noise, where it is becoming a serious contender for radio frequency (RF) applications in the GHz range. Cutoff frequencies of about 50 GHz have been reported for 0.18 µm CMOS technology, and are expected to reach above 100 GHz for the feature size of 90 nm within a few years. This translates into CMOS circuit operating frequencies well into the GHz range, which covers the frequency range of many of today's popular wireless products. While complete broadband characterization and accurate modeling of the MOSFETs are critical requirements for circuit designs, the RF behavior and physics are not well understood. This dissertation explores the physical origins of small-signal characteristics of RF MOSFETs and discusses many of the challenges facing the CMOS RF circuit designer in terms of device modeling and characterization, which are crucial issues in circuit simulation and design.

An often mentioned problem seems to be the Non-Quasi Static (NQS) phenomena. A distributed NQS model is discussed and an estimation of the theoretical limit up to which quasi-static MOSFET models are reasonable is presented. The NQS frequency (f_{NQS}) is defined as the frequency when NQS effects start to occur. Bias dependency of the NQS frequency is examined for critical modeling parameters (i.e., C_{gg}, C_{gs}, and C_{gd}); the strong bias dependency of the parameters is due to the charge sharing between source and drain, and mobility. At high frequencies, the existence of substrate network cannot be ignored. The substrate network is modeled as parallel R_{sub} and C_{sub}, and the product ($R_{sub}C_{sub}$) shows conservative behavior (i.e., dielectric relaxation time constant of Si). The existence of substrate resistance impacts terminal admittances, even at low frequencies, and this fact suggests that the QS model needs to include substrate components in order to achieve accurate terminal characteristics. In addition, the negative capacitance (NC) effect of a diode is discussed and the corresponding compact model is developed. Instead of analyzing a small-signal

model from measurement data alone, two-dimensional simulation is employed in order to develop a physically acceptable small-signal model of RF MOSFETs.

When dealing with small-signal equivalent circuits, the extraction of parameters is of great importance. Accurate extraction of parasitics is critical in RF circuit simulation and accurate modeling of intrinsic device. Characterization of RF MOSFETs is often done using two-port s-parameter measurements, where the source and bulk are tied together. A compact model of MOSFETs for the common source configuration is developed to identify two-port characteristics and the model is used to effectively de-embed extrinsic parasitics with good accuracy. The extraction of gate resistance is particularly important. The de-embedding methodology is capable of isolating gate resistance (e.g. poly resistance and gate contact resistance) from the channel resistance (i.e., component of gate induced noise), which is crucial in accurate noise modeling of MOSFETs.

Acknowledgments

I would like to thank many people who made my life at Stanford valuable and memorable. First and foremost, I wish to acknowledge my advisor, Professor Robert W. Dutton for his support, guidance and encouragement in this work.

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Contents

List of Figures

1 Introduction

1.1 Background

Since the invention of the transistor more than fifty-years ago, solid-state electronics has developed rapidly and has transformed the meaning of device technology into a new dimension. Today, deep-submicron CMOS processes typically reach the 50 GHz cut-off frequency (f_T) region and offer low noise figures, making them a serious alternative for RF circuit integration. In general, CMOS offers VLSI capabilities allowing for a high level of integration. The feasibility of RF CMOS circuit integration has clearly been demonstrated. Radio frequency integrated circuits (RFIC's) based on CMOS processes are currently receiving a significant amount of attention due to the low cost, low-power characteristics of CMOS technology, availability of passive components, and possibilities for System-on-Chip (SoC) integration. Nevertheless, the design of RF CMOS circuits in real products remains a challenge due to the strong constraints on power consumption and noise that leave very little design margin. It is therefore crucial to be able to accurately predict the performance of RF CMOS circuits. Although current IC design tools are well suited for digital and baseband analog design, they fail for RF designs at frequencies > 1 GHz due to lack of accurate modeling of device behavior.

1.2 Thesis Outline

This thesis is organized into nine chapters of which this is the first.

Chapter 2 presents general issues of y-parameter network analysis. No assumptions will be made as to the physics of the device. The only restriction we will place on the device is that it has four terminals. This y-parameter network is the basis of the small-signal equivalent circuit modeling that follows.

Chapter 3 discusses non-quasi-static (NQS) effects and related modeling. An often mentioned problem in RF modeling seems to be non-quasi static phenomena. A distributed NQS model is discussed and an estimation of the theoretical limits up to which quasi-static MOSFET models are reasonable is presented.

Chapter 4 discusses negative capacitance (NC) effects in silicon devices. It will be shown that the conventional method for calculating capacitance based on the incremental charge method is not suitable, using a diode as an example.

Chapter 5 discusses source-to-drain coupling effects and the substrate network. As operating frequency increases, substrate effects can not be ignored and strong channel length dependency on output characteristics is discussed. It will be shown that the source to drain coupling effects are a dominant factor compared to the substrate network; a new model describing the substrate network is presented.

Chapter 6 discusses 2-D devices simulation of RF MOSFETs. Application of the two-dimensional device simulator gives excellent insight into the modeling of high frequency behavior of MOSFET, while modeling through s-parameter measurements of MOSFET at high frequency can result in inaccurate models due to erroneous measurement and difficulties in parameter de-embedding.

Chapter 7 discusses extraction of intrinsic parameters. The analytical methodology of extracting small-signal parameters from either device simulation or s-parameter measurements are introduced.

Chapter 8 discusses extraction of extrinsic parasitics. A general network of extrinsic parasitics are assumed and the de-embedding of the parasitics are achieved through analytic calculation and curve fitting. This method is shown to be accurate to within 2% compared to device simulation.

Chapter 9 discusses RF LDMOS characterization and its compact modeling. The unique features of the LDMOS, such as graded channel and quasi-saturation effect are demonstrated, including peculiar behavior of capacitance and non-linear LDD resistance. These effects are analyzed and modeled using device simulation.

Finally, Chapter 10 concludes with a summary and suggestions for future work.

Several appendices provide more detailed explanation of certain subjects. Appendix A introduces capacitances of MOSFET that are derived from charge-based approach. Appendix B describes frequency response of all sixteen y-parameters of MOSFET, in linear and saturation region. Appendix C describes the network parameter conversion table. Finally Appendix D validates the assumption of the properties of lossy silicon substrate.

2 y-parameter based Small-Signal model for RF CMOS

In this chapter we will consider the case where the terminal voltage variations are sufficiently small so that the resulting small current variations can be expressed using linearized relations. We will derive such linear relations and develop equivalent circuits to represent them. When excited by voltages equal to the small variations of the actual terminal voltages, these circuits will produce currents equal to the small variations of the actual transistor currents. Such models find wide use in analog circuit design, and have been studied since the early days of MOS transistors. In most of this chapter, we will concentrate on the intrinsic part of the transistor.

Figure 2.1 shows a conventional small signal model for the MOSFET, which has been widely used for modeling and parameter extraction. However this simple small-signal model has limits in predicting high frequency behavior of the MOSFET.

2.1 General y-parameter model

Design of very-high-frequency circuits (not necessarily using MOS transistors) is often done by using the so-called “y-parameters”. In this section we will first show the general form of such mod-

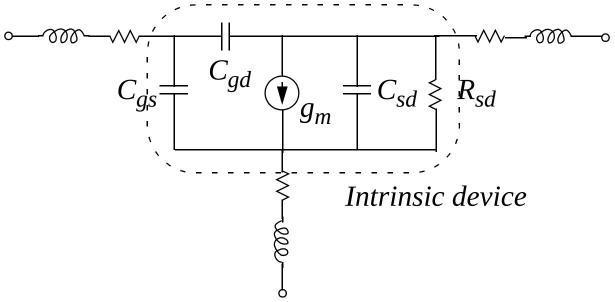


Figure 2.1. Conventional simplified small-signal model.

els. In doing so, no assumptions will be made about the physics of the device. In fact we do not even have to assume that the device is a MOS transistor. The only restrictions we will place on it is that it has four terminals and that linear superposition can be applied.

The y-parameter set, which is also called the admittance matrix, is defined as the ratio of current phasor to the voltage phasor when a small-signal voltage is applied to one of the terminals, while the rest of the terminals are grounded; the induced current signal is detected at a specific terminal as shown in Figure 2.2 for y_{sd}.

Small-signal equivalent circuits are linear circuits, representing the fact that in an actual transistor with vanishingly small signals the quantities I_d, I_g, I_b, and I_s are linear functions of V_d, V_g, V_b, and V_s. One can thus use superposition to find I_d when all four of the small-signal voltages are active (nonzero). This is done by considering one voltage at a time, evaluating the resulting current, and then adding up the currents:

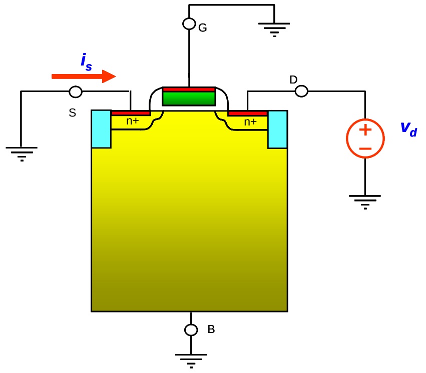
$$I_d = y_{dd}V_d + y_{dg}V_g + y_{db}V_b + y_{ds}V_s \tag{2.1}$$

Similarly the rest of the terminal currents can be written as follows:

$$I_g = y_{gd}V_d + y_{gg}V_g + y_{gb}V_b + y_{gs}V_s \tag{2.2}$$

$$I_s = y_{sd}V_d + y_{sg}V_g + y_{sb}V_b + y_{ss}V_s \tag{2.3}$$

$$I_b = y_{bd}V_d + y_{bg}V_g + y_{bb}V_b + y_{bs}V_s \tag{2.4}$$



$$y_{sd} = \left.\frac{i_s}{v_d}\right|_{v_g,\, v_s,\, v_b\, =\, 0}$$

Figure 2.2. Definition of y parameters.

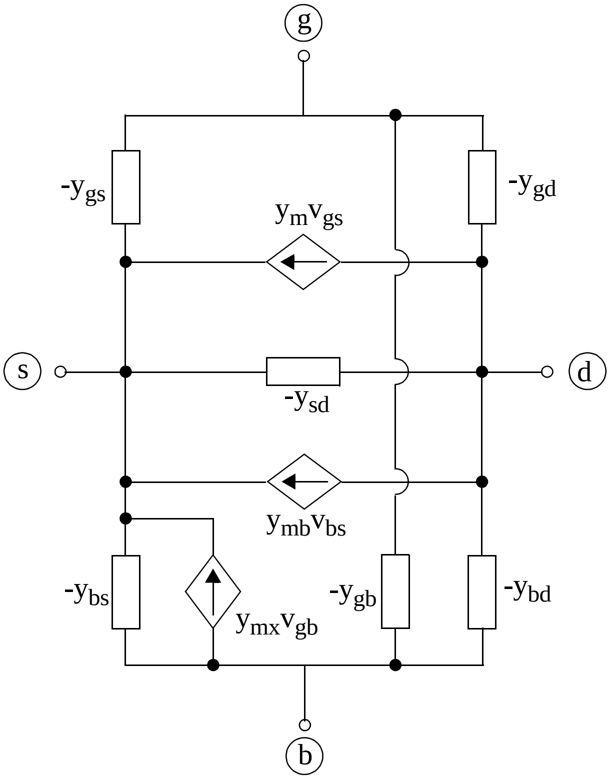


Figure 2.3. General y-parameter model for 4 terminal device.

We now go one step closer in relating current and voltage using y-parameters and can rewrite the above equations without losing information as follows [29]:

$$I_d = -y_{gd}V_{dg} - y_{sd}V_{ds} - y_{bd}V_{db} + y_m V_{gs} + y_{mb}V_{bs} \tag{2.5}$$

$$I_g = -y_{gd}V_{gd} - y_{gb}V_{gb} - y_{gs}V_{gs} \tag{2.6}$$

$$I_b = -y_{bd}V_{bd} - y_{gb}V_{bg} + y_{mx}V_{gb} - y_{bs}V_{bs} \tag{2.7}$$

where

$$y_m = y_{dg} - y_{gd} \tag{2.8}$$

$$y_{mb} = y_{db} - y_{bd} \tag{2.9}$$

$$y_{mx} = y_{bg} - y_{gb} \tag{2.10}$$

The above set of equations can be represented by the circuit of Figure 2.3. Each y_{gs}, y_{gd}, y_{sd}, y_{bs}, y_{bd}, y_m, y_{mb}, y_{mx} and y_{gb} are represented only symbolically for the moment. We will derive actual parameters and represent them in circuit form in the following sections. Note that the development of this model is general without any assumptions except that it has four terminals and obeys superposition (of linearized terms). There can be many configurations of y-parameter networks to represent a 4 terminal device (i.e., y-parameter model using the substrate terminal as a reference, y-parameter model using the source terminal as a reference). Figure 2.3 is just one of the many possible forms for the y-parameter network for a 4 terminal device.

As a special case of this model, a simple quasi-static small-signal model is shown in Figure 2.4, which is the same topology as used for most commercial quasi-static models (e.g., BSIM4). By comparing the two circuits in Figure 2.3 and Figure 2.4 we can define following quantities:

$$-y_{gd} = j\omega C_{gd} \tag{2.11}$$

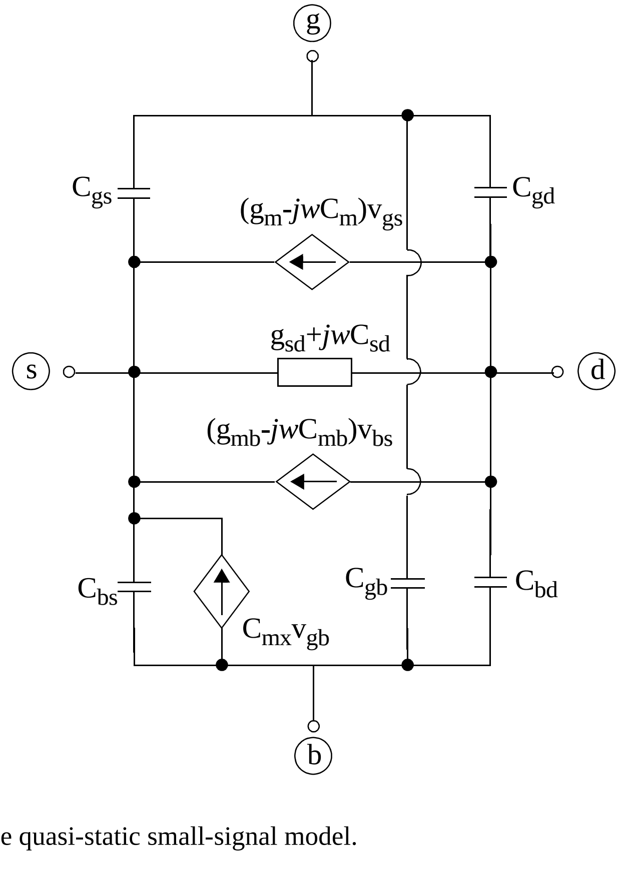


Figure 2.4. A simple quasi-static small-signal model.

$$-y_{gs} = j\omega C_{gs} \tag{2.12}$$

$$-y_{bd} = j\omega C_{bd} \tag{2.13}$$

$$-y_{bs} = j\omega C_{bs} \tag{2.14}$$

$$-y_{gb} = j\omega C_{gb} \tag{2.15}$$

$$-y_{sd} = g_{sd} + j\omega C_{gd} \tag{2.16}$$

$$y_m = g_m - j\omega C_m \tag{2.17}$$

$$y_{mb} = g_{mb} - j\omega C_{mb} \tag{2.18}$$

$$y_{mx} = g_{mx} - j\omega C_{mx} \tag{2.19}$$

In the above equations, note that y_{gd}, y_{gs}, y_{bd}, y_{bs}, and y_{gb} have no real part. However this is not physically correct. At very high frequencies (i.e., near f_T), all the assumptions that C_{gd}, C_{gs}, C_{bd}, C_{bs}, C_{gb}, and g_m are constant over frequency do not hold. To explain such phenomena, the quasi-static assumption must be abandoned, as discussed in the next section.

3 Non-Quasi-Static (NQS) Effects

Due to continuous device scaling, CMOS technologies are playing a more important role in RF systems, mostly driven by significant cost reduction advantages while maintaining equivalent performance compared to other compound material FET (III-V) or Bipolar Junction Transistor (BJT) devices. Therefore, there is a strong demand for compact small-signal models that accurately describe the high frequency region of behavior in MOS devices. An often mentioned problem seems to be non-quasi static phenomena. In this chapter, a distributed NQS model is discussed and an estimation of the theoretical limit up to which quasi-static MOSFET models are reasonable is presented.

3.1 Introduction on NQS Effect [13]

Consider the intrinsic transistor shown in Figure 3.1.; assume that, in general, each terminal voltage consists of a DC bias and a small-signal sinusoidal component, as shown. Assume further

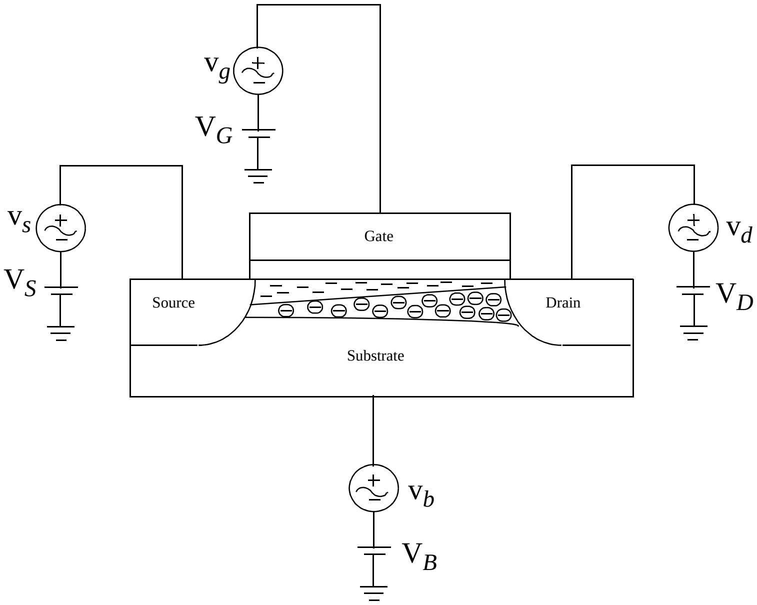


Figure 3.1. A transistor with bias and small-signal voltage.

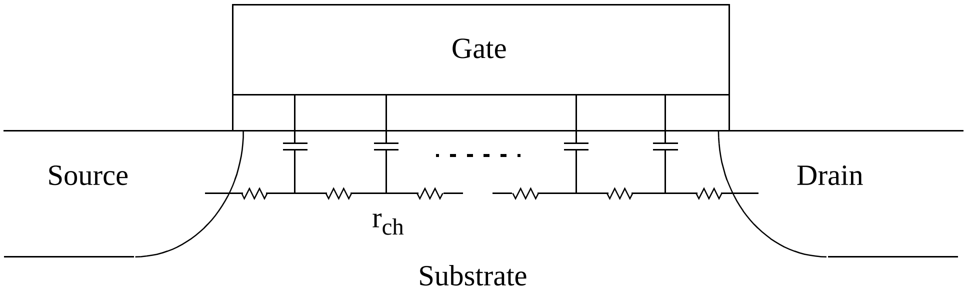


Figure 3.2. A simple quasi-static small-signal model.

that only one small-signal voltage is nonzero at a time. If v_s is varying very slowly, the inversion layer charge has time to follow the input with practically no delay. However, if the variation of v_s is fast, the "inertia" of the inversion layer becomes non negligible, and the effect (gate charge change) will lag behind the driving force (source voltage). A similar effect will be observed between drain and gate; similar conclusions can be drawn for the effects of the source and of the drain on the substrate (the "back gate"). Consider now the effect of the gate voltage. If v_g is varying rapidly, the inversion layer charge does not have enough time to respond fully, and thus $|y_{dg}|$, which models this response, will be small. Also, the conduction angle of y_{dg} should be significant and negative, because of the delay between the cause (the variation in the gate voltage) and the effect (the variation in the drain current). Finally, similar observations hold for the effect of the substrate voltage on the inversion layer charge. Measurements [33] on both long- and short-channel devices do, in fact, verify that such effects can influence transistor behavior. These effects are broadly categorized as non-quasi static (NQS) behavior.

3.2 Compact Model of Distributed Channel

One way to model the NQS effect in the high frequency regime is to split the channel into sections [37]. The length of each section is chosen such that a quasi-static model can be used. The combination of the models of all sections will then be a valid model for the entire transistor at the high frequencies of interest. The higher the frequency, the smaller the length needed for each section. However, such a modeling approach is complex and requires substantial simulation time. Furthermore, it is fairly difficult to model the short channel effects separately.

This distributed effect along the channel length can be modeled as a bias-dependent *RC* distributed transmission line as shown in Figure 3.2. *Under the assumption of the gradual channel approximation*, the equivalent input impedance Z_{gs} seen between the gate and source can be written as:

$$z_{gs} = r_{ch} \frac{coth(\gamma L)}{\gamma L} \tag{3.1}$$

where,

$$\gamma = \sqrt{\frac{j\omega r'_{ch} C'_{gs}}{L^2}}$$

L is the channel length, γ is the propagation constant, and $r'_{ch} = r_{ch}/L$, $C'_{gs} = C_{gsi}/L$. C_{gsi} is the total gate to source capacitance.

The first order approximation of z_{gs} in Equation 3.1 is:

$$z_{gs} = r_{ch} \frac{coth(\gamma L)}{\gamma L} \approx \frac{r_{ch}}{3} + \frac{1}{j\omega C_{gsi}} \tag{3.2}$$

As a result, the z_{gs} can be expressed as a *series RC circuit* as shown in Figure 3.3 a), which consists of $r_{gs} = r_{ch}/3$ and C_{gsi}. Physically the resistance, r_{ch}, is the bias-dependent channel resistance. The resistance is insignificant and almost invisible from the gate terminal perspective at low frequencies. As the frequency increases the conductance seen from the gate can be comparable or significantly larger compared to the imaginary part.

The corresponding conductance and capacitance can be represented in terms of the admittance as follows:

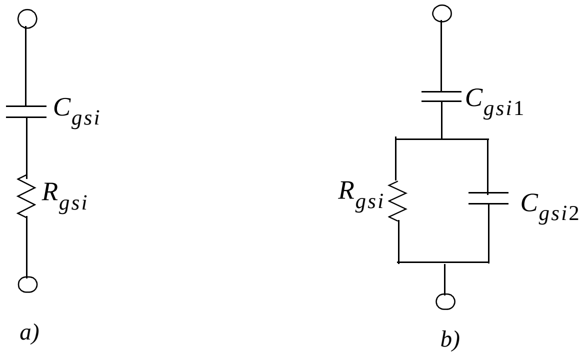


Figure 3.3. Gate to drain impedance approximated by transmission line equivalent circuit. a) First order approximation. b) Second order approximation.

$$-y_{gs} = \frac{R_{gsi}C_{gsi}^2\omega^2}{D_{gsi}} + j\omega\frac{C_{gsi}}{D_{gsi}} = G_{gs} + j\omega C_{gs} \tag{3.3}$$

The C_{gs}, and G_{gs} terms are introduced to represent the conductive and capacitive parts of the -y_{gs} and -y_{gd} respectively. The extension ‘i’, as in C_{gsi} R_{gsi}, is used in referring to the compact model parameter to differentiate from the terminal conductance and capacitance, C_{gs} and G_{gs}. Between the gate and drain terminals, an analogous approach can be applied.

$$-y_{gd} = \frac{R_{gdi}C_{gdi}^2\omega^2}{D_{gdi}} + j\omega\frac{C_{gdi}}{D_{gdi}} = G_{gd} + j\omega C_{gd} \tag{3.4}$$

where

$$D_{gsi} = 1 + (\omega C_{gsi}R_{gsi})^2, D_{gdi} = 1 + (\omega C_{gdi}R_{gdi})^2$$

Equation 3.3 predicts that the conductance is zero when $\omega = 0$ and as frequency increases the conductance increases proportionally with ω^2 until $\omega \approx 1/(C_{gsi}R_{gsi})$. Also, the capacitances C_{gd} and C_{gs} become frequency dependent when $\omega > 1/(C_{gsi}R_{gsi})$. In fact, device simulation (see Chapter 6 for detailed device simulations) shows that the frequency dependence of y_{gg} for various channel lengths (L=0.3 um, 0.6 um, 1.2 um, 2.5 um, 10 um and 50 um) as reflected in Figure 3.4. As expected, the longer the channel length, the smaller the fall off frequency becomes (i.e., the C_{gg} starts to fall off at ~10 MHz for L = 50 um device, and at ~30 GHz for L = 0.3 um device).

For the 50 um device, the C_{gg} does not fall off indefinitely and becomes zero as Equation 3.3 predicts, rather the capacitance becomes a constant greater than zero at infinite frequency. This is because an approximation is used in calculating the z_{gs} in Equation 3.2. Some improvement can be achieved as a result of the second-order approximation of z_{gs} as follows:

$$z_{gs} = r_{ch}\frac{\coth(\gamma L)}{\gamma L} \approx \frac{r_{ch}}{3}\Big/\left(1 + j\omega\frac{r_{ch}}{3}C_{gsi2}\right) + \frac{1}{j\omega C_{gsi1}} \tag{3.5}$$

As a result, the z_{gs} can be expressed as a combination of two capacitors and a resistor as shown in Figure 3.3 b), which consists of $r_{gs} = r_{ch}/3$, C_{gsi1}, and C_{gsi2} ($C_{gsi1} = 5C_{gsi2}$).

The corresponding conductance and capacitance can be represented in terms of admittances as:

$$-y_{gs} = \frac{R_{gsi}C_{gsi1}^2\omega^2}{D_{gsi}} + j\omega\frac{C_{gsi1}(1 + \omega^2 C_{gsi1}(C_{gsi1} + C_{gsi2}))}{D_{gsi}} = G_{gs} + j\omega C_{gs} \tag{3.6}$$

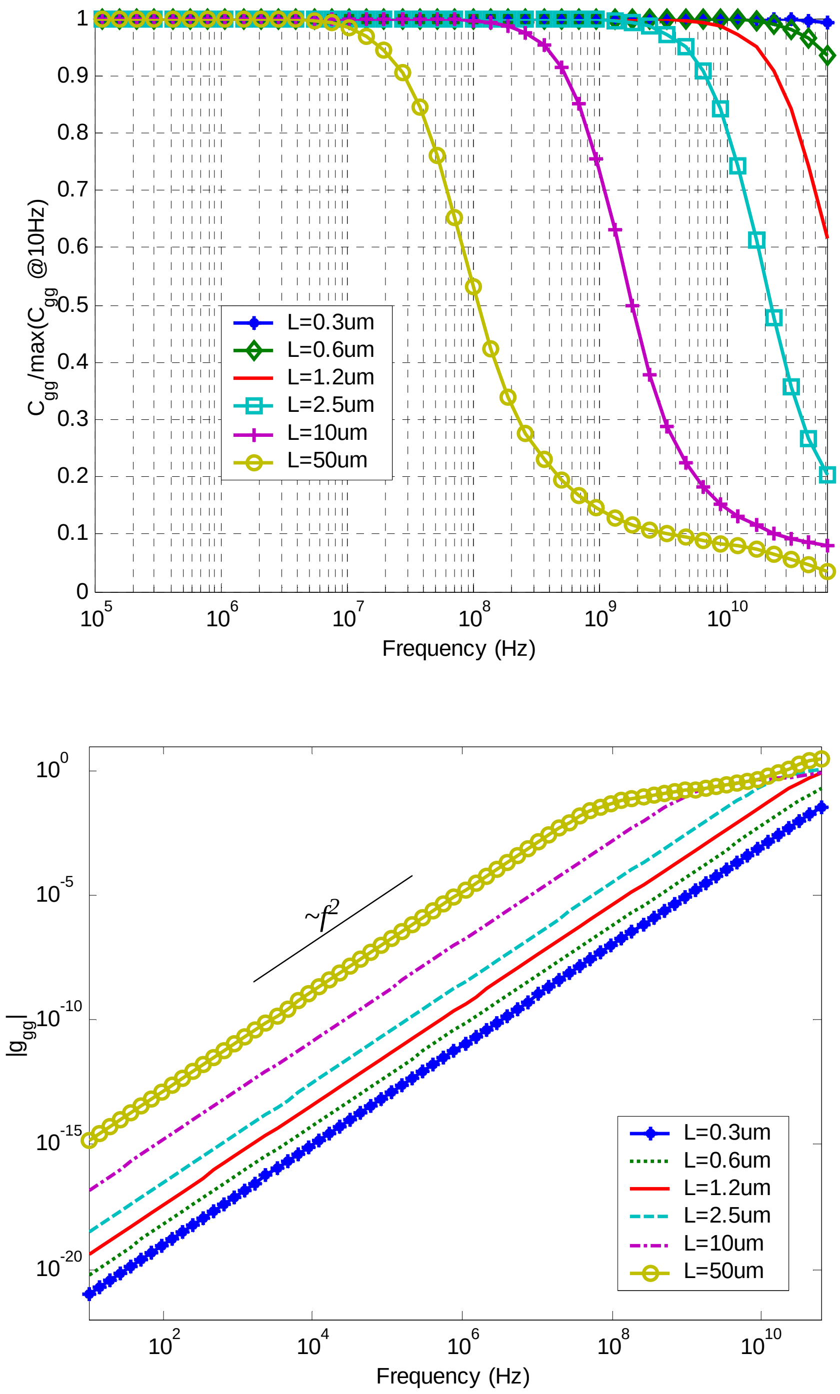


Figure 3.4. Simulated C_{gg} and G_{gg} vs. frequency for various channel lengths at $V_{DS} = 0$ and $V_{GS} = 3$ V. The C_{gg} is normalized by the maximum C_{gg} at 10 Hz for each device. In this bias condition, $C_{gg} \approx C_{gs} + C_{gd}$ and $G_{gg} \approx G_{gs} + G_{gd}$, and due to the symmetry $C_{gs} = C_{gd}$ and $G_{gs} = G_{gd}$.

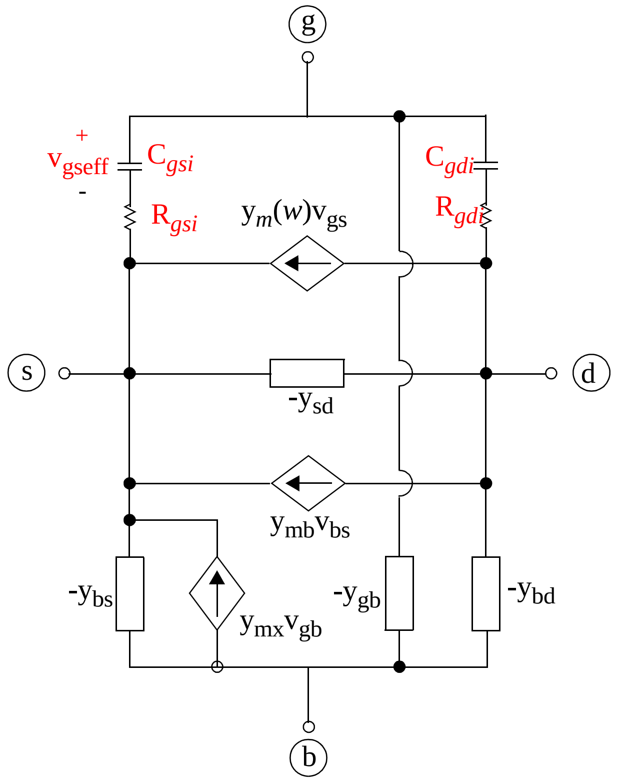


Figure 3.5. y-parameter network of MOSFET. The y_{gs} and y_{gd} are replaced with series RC circuit element.

$$-y_{gd} = \frac{R_{gdi}C_{gdi1}^2\omega^2}{D_{gdi}} + j\omega\frac{C_{gdi1}(1+\omega^2 C_{gdi1}(C_{gdi1}+C_{gdi2}))}{D_{gdi}} = G_{gd} + j\omega C_{gd} \qquad (3.7)$$

where

$$D_{gsi} = 1+\omega^2 R_{gsi}^2(C_{gsi1}+C_{gsi2})^2, D_{gdi} = 1+\omega^2 R_{gdi}^2(C_{gdi1}+C_{gdi2})^2$$

Equations 3.6 and 3.7 correctly predict the frequency response of the total capacitive term (C_{gs} and C_{gd}) by introducing additional capacitance (introduces a zero that compensates the pole due to the capacitance). Nevertheless, this is not important in most practical situations because these changes take place in a range near or above the cutoff frequency, f_T. Hence, the first order approximation is sufficient in most RF applications.Figure 3.5 shows the MOSFET y-parameter network with y_{gs} and y_{gd} parameters represented as circuit elements.

The conductance (G_{gg}) in Figure 3.4 directly translates into gate current noise, which can be significant in RF applications since it is proportional to f^2.

3.3 Bias Dependence of NQS Effect

From the discussion so far, we expect that the quasi-static model will be valid if the terminal voltage varies sufficiently slowly so that the charge distribution in the channel can follow with negligible inertia. A quantitative definition of the term “sufficiently slowly” is difficult to quantify. There have been reports, [41][40] and [39], to show the criteria for the onset of NQS effects derived from *time transient device simulation* and s-parameter measurements. However these works are mainly focused on one specific bias condition. From the modeling point of view, it will be more appropriate to define at what frequency each model parameter is appreciably affected by NQS behavior. Furthermore, the bias dependency of the onset of NQS effects need to be quantified.

In this section, the bias dependency of the NQS effect on critical small-signal model parameters are studied. Since gate capacitance is one of the most critical parameters in terms of device modeling, the bias dependency on the NQS effect for C_{gs}, C_{gd}, and C_{gb} is discussed.

3.3.1 On Set of NQS Effect of C_{gs}, C_{gd}, and C_{gb}

The NQS effect on gate capacitance is strongly correlated with how the charge is divided between the source and drain terminals. When there is a small signal change at the gate, assuming other nodes are small-signal grounded, the signal gets modulated by channel charge when there is an inversion layer. The modulated channel charge has to come from either the source or drain since the channel itself cannot generate charge fast enough from the bulk node to follow the gate signal (i.e., the characteristic time to form an inversion layer at the surface of an MOS system biased to

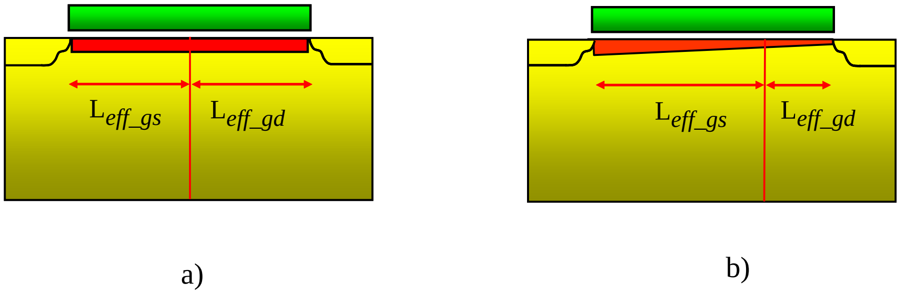


Figure 3.6. Charge split a) when $V_{DS} = V_{SS} = 0$ and $V_{GS} > V_{th}$ where $L_{eff\_gs} = L_{eff\_gd}$, b) $V_{DS} > V_{SS}$ and $V_{GS} > V_{th}$, where $L_{eff\_gs} > L_{eff\_gd}$.

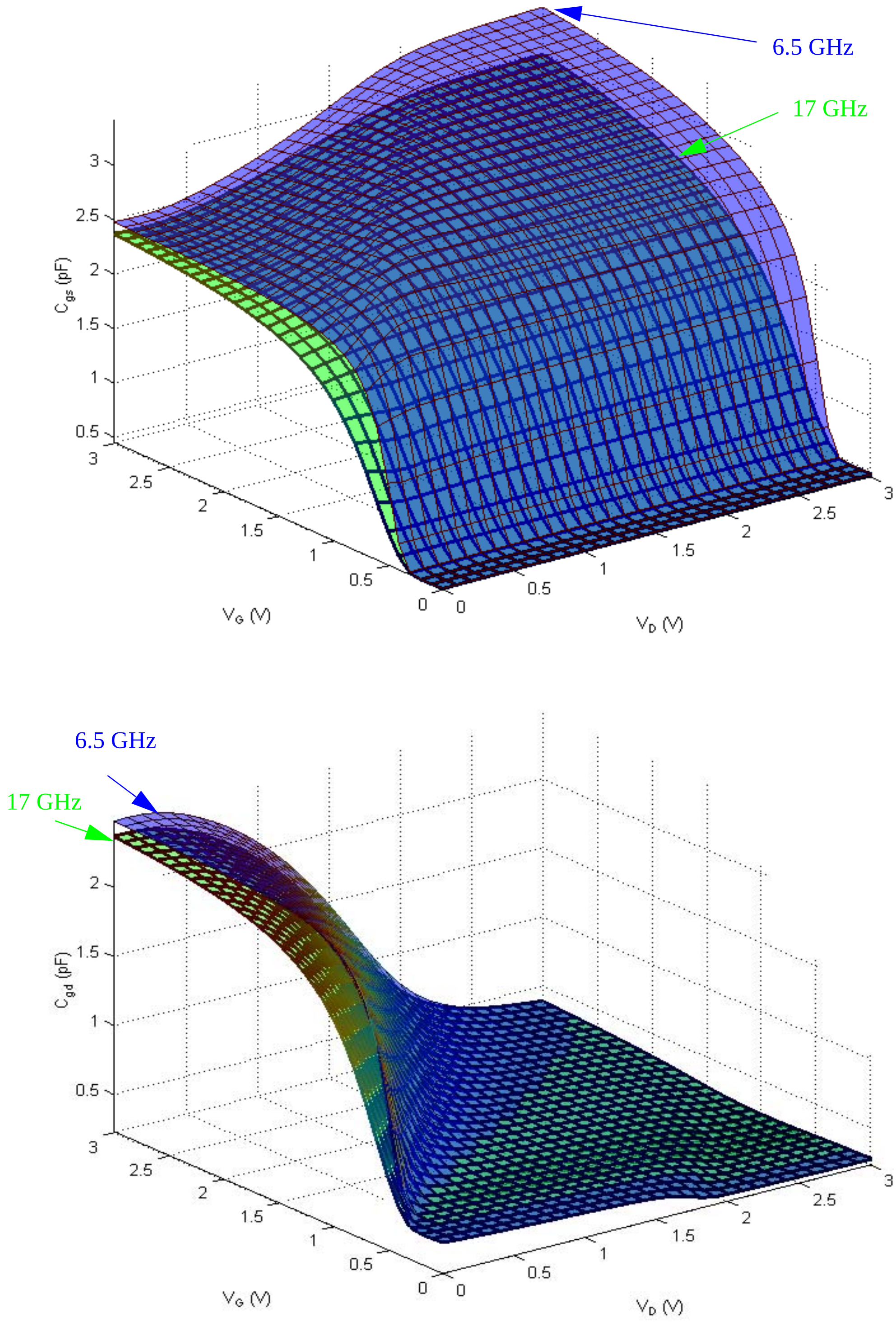
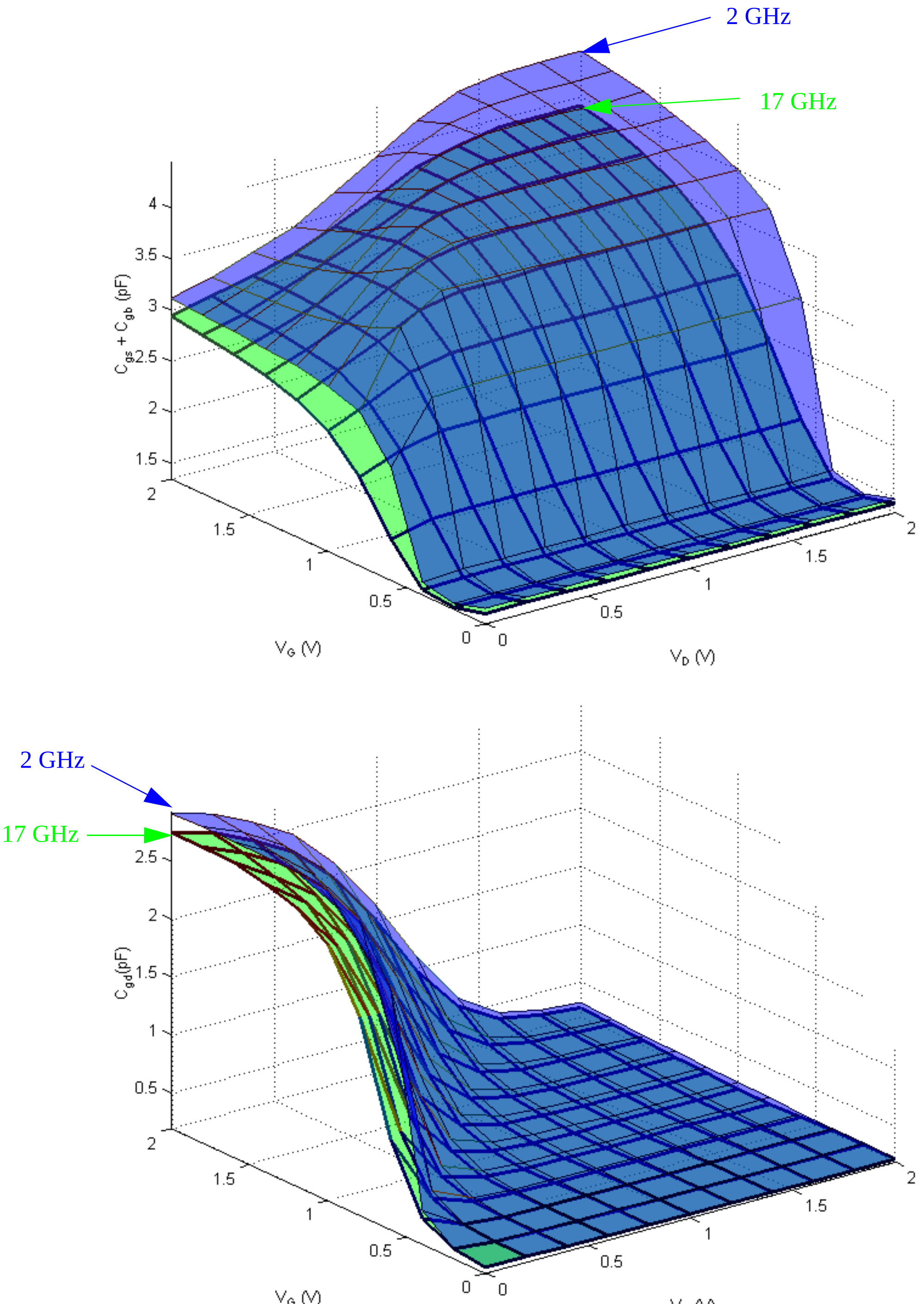


Figure 3.7. a) Simulated C_{gs} and C_{gd} at 6.5 GHz and 17 GHz for L = 1.2 um. In saturation region (i.e. $V_{DS} = V_{GS} = 3$ V) the degradation of C_{gs} between 2 frequencies is higher compared to C_{gd}, while the degradation of the C_{gs} and C_{gd} is similar in linear region (i.e., $V_{DS} = 0$ V and $V_{GS} = 3$ V).



b)

Figure 3.8. a) Extracted C_{gs} and C_{gd} from s-parameter measurement at 6.5 GHz and 17 GHz for L = 1.2 um device. The NQS effect is stronger in C_{gs} compared to C_{gd} in saturation region and becomes strong in weak inversion region and linear region. This is due to the effective channel length is longest in linear region (no pinch off) and transit time is higher in weak inversion region.

inversion is of the order of $2Na \cdot \tau_0 / n_i$ where τ_0 is the minority -carrier lifetime at the surface. For a typical value of lifetime (1us) and dopant concentrations (10^{15} cm^{-3}), this time is roughly 0.2 s). When V_{DS} equals 0, the channel charge is equally divided and results in equal C_{gs} and C_{gd} values. This means that the effective channel length seen from gate-to-source and by gate-to-drain (L_{eff_gs} and L_{eff_gd}) terminal are equal as shown in Figure 3.6 a). In the saturation bias condition as shown in Figure 3.6 b), the source terminal has more control over channel charge and results in $L_{eff\_gs} > L_{eff\_gd}$. If we formulate the bias dependency of L_{eff_gs} using a capacitance point of view,

$$L_{eff-gs} \cong L \cdot \frac{C_{gs}}{C_{gs} + C_{gd}} \tag{3.8}$$

and for L_{eff_gd},

$$L_{eff-gd} \cong L \cdot \frac{C_{gd}}{C_{gs} + C_{gd}} \tag{3.9}$$

Another factor that determines the on-set of NQS effects is mobility. Mobility determines the transit time between source and drain. When the transit time is longer due to decreased mobility along the channel, the response time of the channel charge due to the input signal change becomes slower, resulting in a NQS effect that occurs at lower frequencies.

The onset frequency of NQS effects can be approximated [29] by

$$f_{NQS} = n\left[\frac{\mu(V_{GS} - V_T)}{2\pi L^2}\right] \tag{3.10}$$

where n is a fitting parameter and L is channel length. The f_{NQS} for C_{gd} and C_{gs} can be expressed by substituting L in Equation 3.10 from L_{eff_gs} and L_{eff_gd} of Equations 3.8 and 3.9.

In the case of deep sub-micron devices, the f_{NQS} was shown to be proportional to velocity saturation [40] as given by:

$$f_{NQS} = n\frac{v_{sat}}{2\pi L} \tag{3.11}$$

Figure 3.7 shows the frequency dependence of C_{gs} and C_{gd} for a MOSFET device (L = 1.2 um) for all bias regions. Both the device simulation, Figure 3.7, and measurements, Figure 3.8, show the same frequency response; when the device operates in saturation, most of the channel charge belongs to the source side (i.e., evidenced by the higher C_{gs}) resulting in a larger degradation of C_{gs}. In other words, the gate-to-source node sees a larger portion of the channel charge, resulting in lower on-set frequency of the NQS effect in the saturation region compared to the linear region.

To find out when the gate capacitances start to degrade, we define the on-set frequency (f_{NQS}) of the NQS effect as the frequency when the gate capacitance (C_{gg}, C_{gd}, C_{gs}, and C_{gb}) degrades by 10 % from the low frequency value. Figure 3.9 shows the f_{NQS} of an L = 1.2 um device for C_{gg}, C_{gd}, C_{gs} and C_{gb} for various operating bias. For the C_{gg}, the highest f_{NQS} is at $V_{DS} = V_{SS} = 0$ and $V_{GS} = 3$ V, where the transit time delay is lowest due to low channel resistance. For C_{gs}, the highest f_{NQS} occurs when there is no inversion charge (bulk charge modulates). The maximum f_{NQS} is clamped at 60 GHz since simulations are only valid to that frequency. For C_{gd}, the highest f_{NQS} occurs when the device operates in saturation and subthreshold. When the device operates in saturation, the effective channel length seen by the gate-to-drain terminal becomes significantly smaller than the total device channel length, which is proportional to the reduction of C_{gd} from linear to saturation

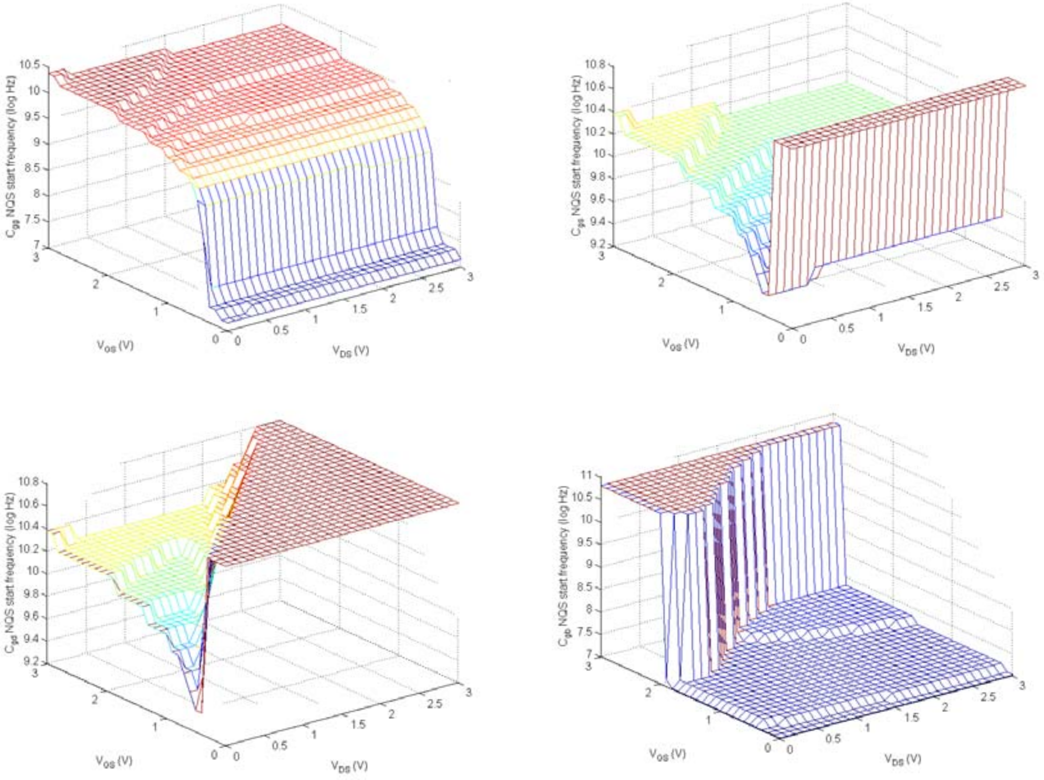


Figure 3.9. f_{NQS} (L = 1.2 um device) vs. V_{DS} and V_{GS} for C_{gg}, C_{gs}, C_{gd}, and C_{gb}.

operation. For C_{gb}, the highest f_{NQS} occurs when the device operates in the linear and strong inversion regions (inversion charge modulation).

It is interesting to note that the f_{NQS} of C_{gg} for the 1.2um device occurs at a fairly low frequency (~50 MHz) when the device operates near threshold voltage. In many RF CMOS applications the devices are operated near the threshold voltage. This means that circuit simulation with a QS model at 1 GHz can be quite off near threshold voltage, even though the maximum f_T of the device is rated as 9 GHz.

3.3.2 Unity Gain Frequency and Maximum Power Gain Frequency

The unity current gain frequency (or cutoff frequency), f_T, is defined when the current gain of the device equals one; f_T is often used to measure the speed of the device. The value of f_T can be approximated as

$$f_T \approx \frac{g_m}{2\pi C_{gg}} \tag{3.12}$$

where second order terms and parasitics are ignored. An important observation that comes from Equation 3.12 is that the current gain is independent of the gate resistance of the device. To find a more accurate expression for f_T, the current gain, |h21| is converted from the s-parameters using the transformation:

$$. \qquad |h_{21}| = \left|\frac{-s_{21}}{(1-s_{11})(1+s_{22})+s_{12}s_{21}}\right| \tag{3.13}$$

The |h21| method extracts f_T by plotting the |h21| vs. frequency in the log scale. The resulting plot is then curve-fit by linear regression

$$f_T = 10^{-intercept/slope} \quad \text{(Hz)} \tag{3.14}$$

The slope and intercept is calculated by using two data points, (f_1, h_1) and (f_2, h_2) as shown in Figure 3.10 as follows:

$$slope = (h_2-h_1)/(f_2-f_1) \tag{3.15}$$

$$intercept = -f_1(slope+h_1) \tag{3.16}$$

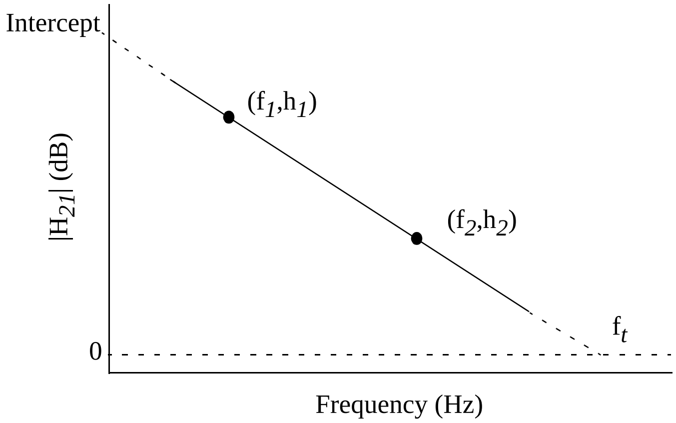


Figure 3.10. $|h_{21}|$ vs. frequency.

The |h21| method assumes that the roll-off of the |h21| in the |h21| vs. frequency plot is constant at -20 dB per decade of frequency. Figure 3.11 shows extracted f_T using the |h21| method. The result shows an increase in f_T with drain and gate bias. The f_T saturates at approximately 40 GHz for the 0.3um device and 9 GHz for a 1.2 um device. Beyond this point, g_m becomes independent of bias, thus making f_T independent of bias. However in the linear region, an increase of V_{GS} decreases f_T since increasing V_{GS} decreases the effective mobility.

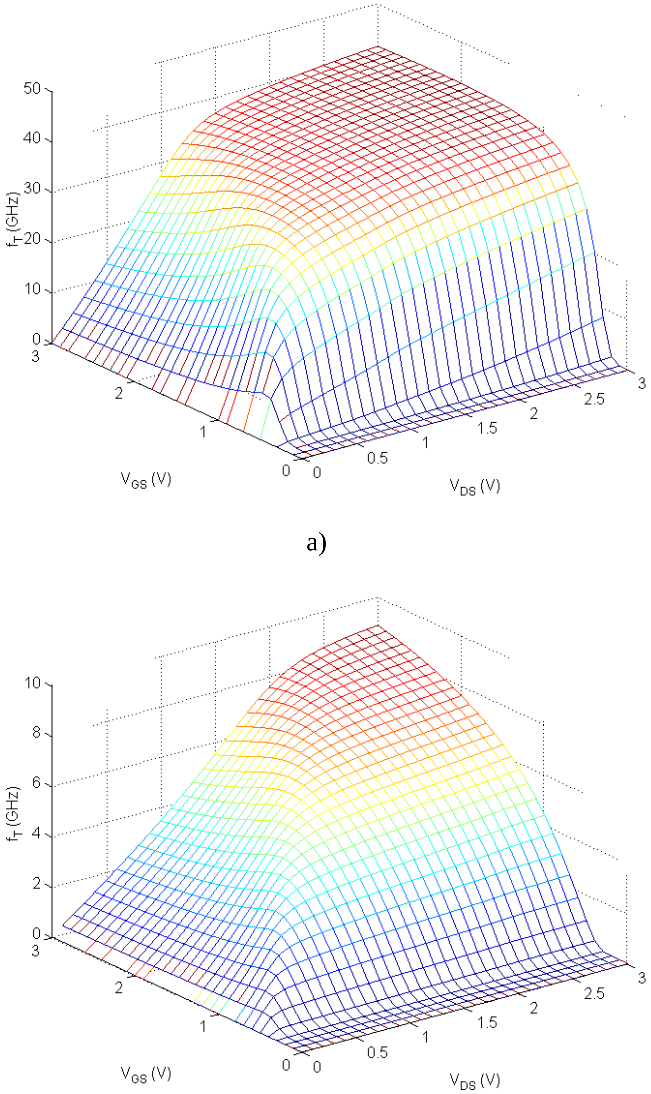
The maximum power gain of a device G_{max} is defined as the power gain delivered by a device when both input and output ports are matched to the impedance of the source and load, respectively. This figure of merit provides a fundamental limit on how much power gain can be achieved from a device. For any two-port network, G_{max} is described by

$$G_{max} = \frac{1}{4} \times \frac{|y_{21} - y_{21}|^2}{Re(y_{11})Re(y_{22}) - Re(y_{21})Re(y_{12})} \tag{3.17}$$

A common figure of merit for RF application is the maximum frequency of oscillation f_{max}, also called the unity power gain frequency. By setting G_{max} =1, an expression for the maximum oscillation frequency f_{max} can be derived. Using circuit theory, one can calculate f_{max} for a given model as

$$f_{max} \approx \sqrt{\frac{f_T}{8\pi r_g C_{gs}}} \tag{3.18}$$

Where r_g is gate resistance. The f_{max} is proportional to square root of f_T and can be higher than f_T by minimizing the gate resistance.



a)

b)

Figure 3.11. f_T vs. V_{DS} and V_{GS} for a) L = 0.3 um device, and b) L = 1.2um device.

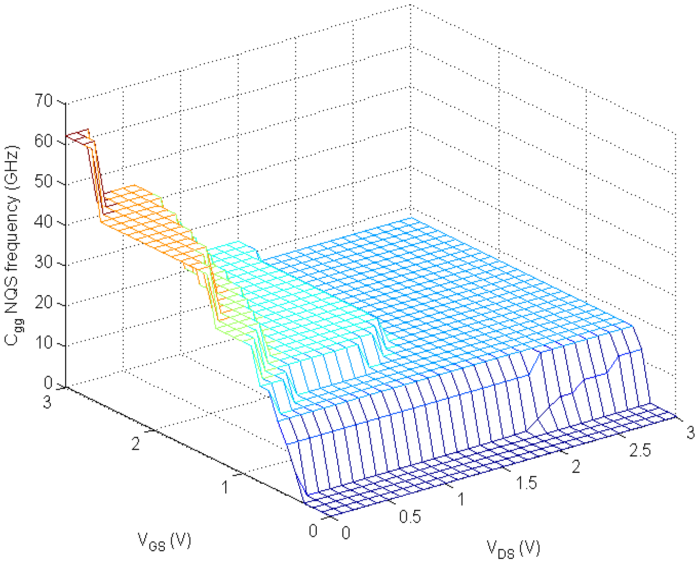
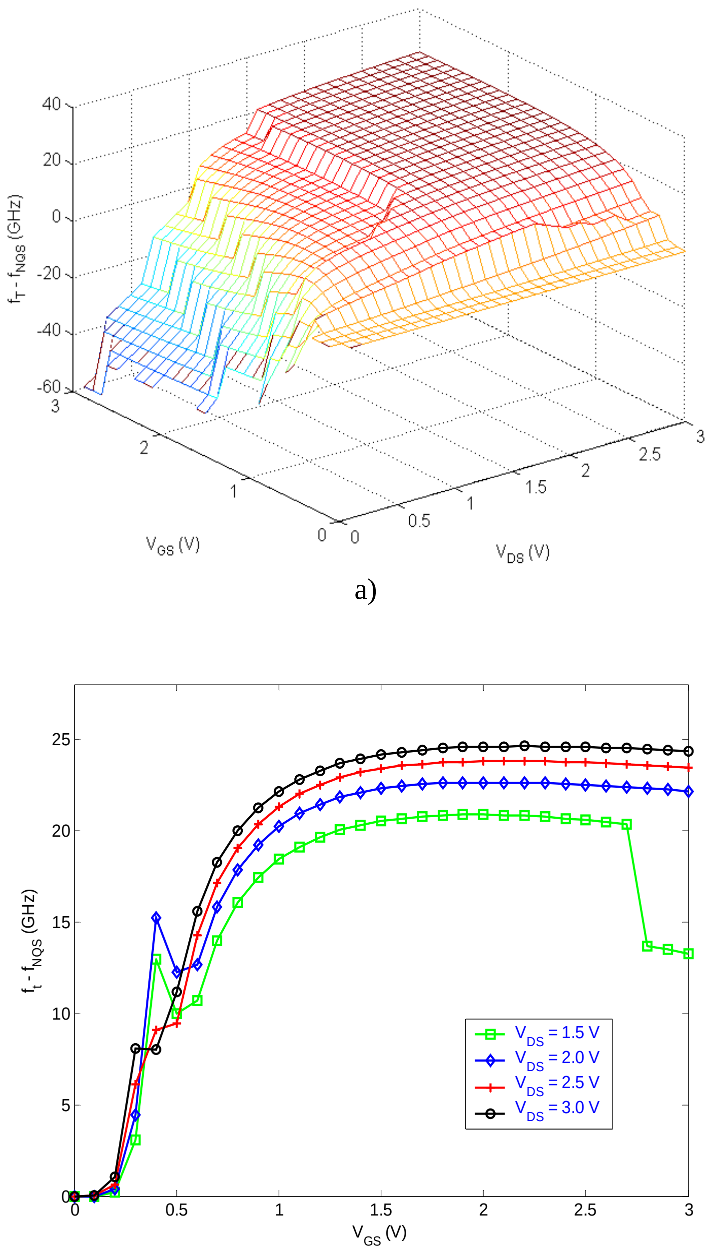


Figure 3.12. f_{NQS} of C_{gg} for L = 0.3 um device.

3.3.3 f_T vs. f_{NQS}

In previous sections, we have defined f_{NQS} and f_T. RF Circuit designers are often interested in f_T of MOSFET device at operating bias condition. However, f_{NQS} should be also considered in the circuit design since it can impact circuit performance dramatically. In this section, the relationship between f_T and f_{NQS} is discussed.

NQS frequency (f_{NQS}) is defined as the frequency when NQS effect starts to occur in terms of modeling parameters (i.e., C_{gg}, C_{gs}, C_{gd}, and C_{gb}). Figure 3.12 shows the extracted f_{NQS} of C_{gg} for L = 0.3 um device. Since $C_{gg} = C_{gs} + C_{gd} + C_{gb}$, f_{NQS} of C_{gg} is the lowest f_{NQS} of the capacitance elements (i.e., C_{gs}, C_{gd}, and C_{gb}) at a bias condition. The f_{NQS} of C_{gg} is the highest in linear region since charge under the gate is equally shared between source and drain, while f_T is the highest in saturation region due to the highest g_m as shown in Figure 3.11a. Figure 3.13a shows f_T - f_{NQS} of C_{gg} for L = 0.3 um device for all biasing regions. In linear region, f_{NQS} dominates while f_T dominates in saturation region. Figure 3.13b shows the bias dependency of f_T - f_{NQS} in 2-D for various drain bias. The gap between f_T and f_{NQS} decreases as V_{GS} decreases.



a)

b)

Figure 3.13. a) f_T - f_{NQS} of C_{gg} for L = 0.3 um device and b) f_T - f_{NQS} for various bias for the same device.

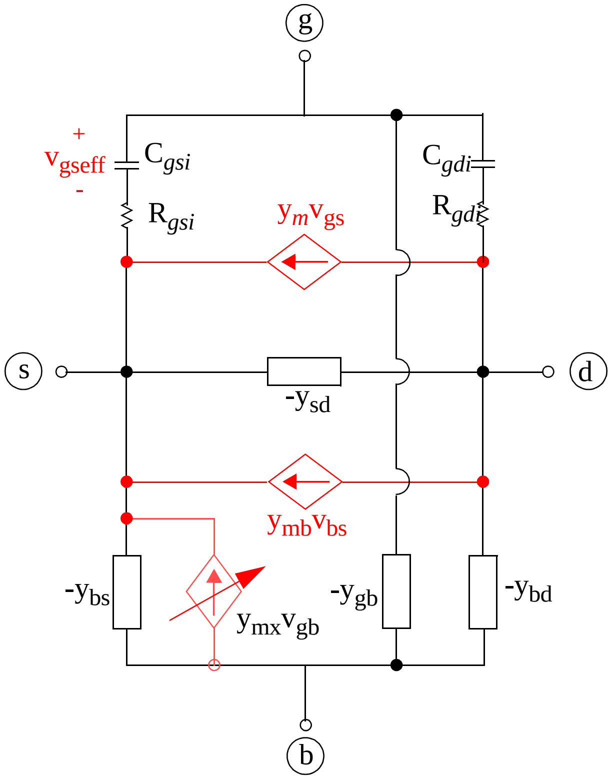


Figure 3.14. General y-parameter network. The y_{mb} and y_{mx} can be ignored in RF.

3.4 Transconductance g_m and g_{mb}

One particular interest in analog circuit design is the accurate fitting of g_m, and g_{mb}. The mutual transconductance measures the amount by which drain current increases for a given increment in the gate bias:

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS},\, V_{BS} = const} \tag{3.19}$$

The substrate transconductance reveals the effect of back-gate bias on the drain conduction:

$$g_{mb} = \left.\frac{\partial I_D}{\partial V_{BS}}\right|_{V_{GS},\, V_{DS} = const} \tag{3.20}$$

The g_m and g_{mb} correspond to y_m and y_{mb} respectively in the general y-parameter network as shown in Figure 3.14.

The most notable difference between the QS and NQS models appears to be the specific dependence of the g_m on frequency. The g_m shows similar frequency dependency as C_{gs} and C_{gd} (in fact, the time constant is identical to that for C_{gg}). This effect can be formulated using the fact that effective v_{gs} (v_{gseff} in Figure 3.14) is decreasing with increasing frequency due to the pole at the gate to source node (i.e., a greater portion of V_{gs} drops in the channel resistance, r_{gs}, with increasing frequency) as

$$g_m(\omega)= \frac{|g_m(0)|e^{-j\omega\tau}}{1 + j\omega r_{gs}C_{gs}} \tag{3.21}$$

where τ is the intrinsic channel transit time. Note that both the real and imaginary part becomes frequency dependent and $g_m(\omega)$ has the same fall-off frequency ($1/R_{gsi}C_{gsi}$) as C_{gs}. Figure 3.15 shows the frequency vs. g_m for various devices. As expected, g_m starts to fall off around 20 MHz for long channel devices (L = 50 um) while g_m falls off at 30 GHz for short channel device (0.3 um). Also note that short channel devices have higher g_m due to a higher electric field between source and drain.

In a similar way, g_{mb} can be represented by

$$g_{mb}(\omega)= \frac{|g_{mb}(0)|e^{-j\omega\tau}}{1 + j\omega\tau_1} \tag{3.22}$$

where τ_1 is $r_{sub}C_j$ (product of substrate resistance and junction capacitance). Hence as frequency increases a greater portion of V_{bs} drops along the substrate rather than in the source-to-substrate junction. This is because the source and drain junctions start to be shorted out at frequencies in the range of $1/(2\pi r_{sub}C_j)$ as shown in Figure 3.16. In this simulation, source/drain junction area and the substrate doping are kept the same for various devices. Thus all the devices show the same general fall off frequency. It is interesting to note that the g_{mb} for a 0.3 um device is lower than that for a 0.6um device. This is because of the Drain Induced Barrier Lowering (DIBL) effect which becomes significant for 0.3 um devices and thus provide effectively less potential drop in the source/drain-to-substrate junctions.

At low frequencies, g_{mb} can be as high as 10 % to 30 % of g_m. However with increasing frequency, g_{mb} tends to fall off at lower frequencies than g_m for short channel devices as shown in Figure 3.16. For RF devices, the following relationship holds (assuming the width of the device is relatively large compared to the channel length, which is true in most RF applications):

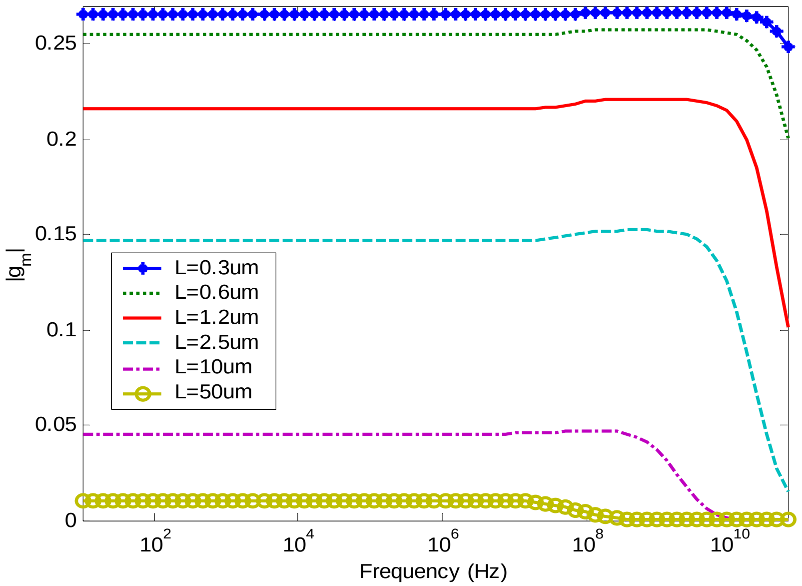


Figure 3.15. The simulated g_m at $V_{DS} = V_{GS} = 3$ V for various channel lengths. Note that the fall off frequency of the g_m is proportional to ~1/L.

$$\tau_1 \approx r_{sub} C_j \gg r_{gs} C_{gs} \tag{3.23}$$

At $f_t/10$, *g_{mb} becomes less than 1 % of g_m* so that the $y_{mb}v_{bs}$ term can be ignored at RF frequencies. However, the g_{mb} has a significant impact at lower frequencies due to the existence of substrate resistance, which is discussed in Chapter 5.

Another transconductance in the y-parameter model is g_{mx} (shown as y_{mx} in Figure 3.14). This is the source to substrate conductance due to V_{GB} as given by:

$$g_{mx} = \left.\frac{\partial I_B}{\partial V_{GB}}\right|_{V_{GS},\, V_{DS} = const} \tag{3.24}$$

The y_{mx} term is very small at low frequencies but increases with frequency as shown in Figure 3.18. However it is insignificant even at RF frequencies compared to g_m and g_{mb} as shown in Figure 3.17. Hence y_{mx} is ignored in the general y-parameter network as shown in Figure 3.14.

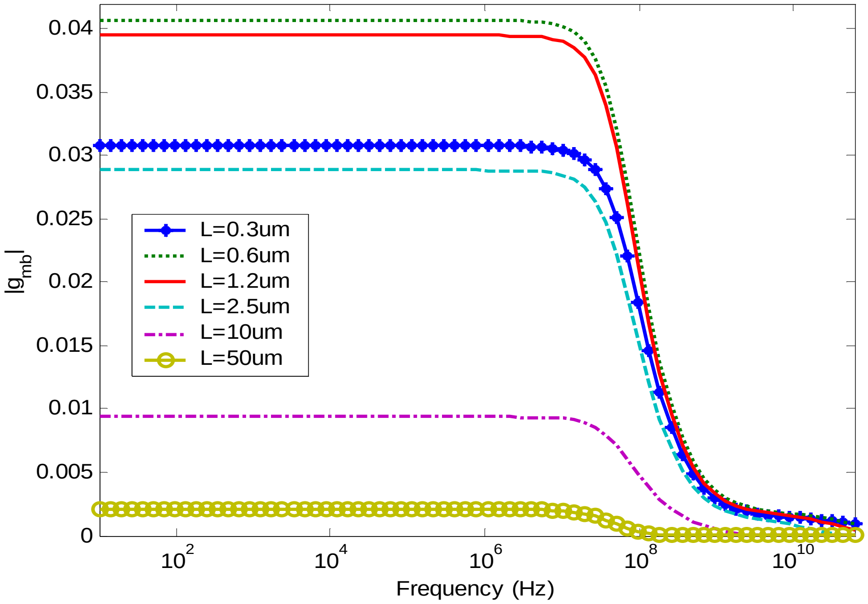


Figure 3.16. The simulated g_{mb} at $V_{DS} = V_{GS} = 3$ V for various channel lengths. Note that g_{mb} starts to fall when the junction capacitance becomes shorted out (~ 20 MHz).

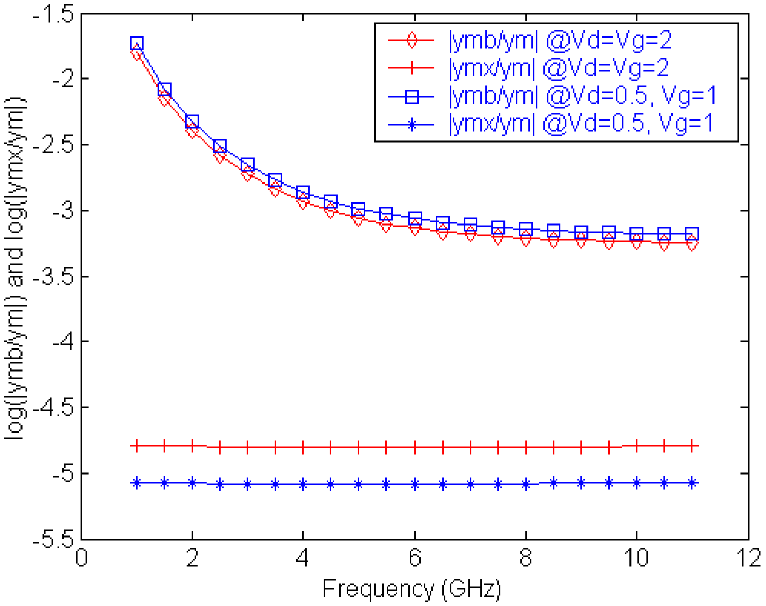


Figure 3.17. The frequency response of simulated y_m, y_{mb} and y_{mx} for a device (L = 0.13 um W = 25 um). Note that g_{mb} becomes insignificant in GHz range compared to g_m.

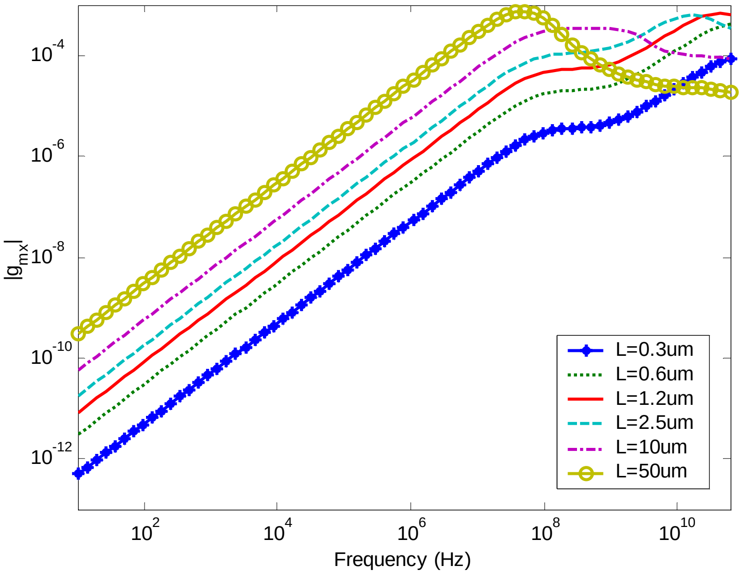


Figure 3.18. The simulated g_{mx} at V_{DS} = V_{GS} = 3 V for various channel lengths. Note that g_{mb} increases proportional to frequency.

3.5 C_{gb} and g_{gb}

The y_{gb} term becomes a significant portion of y_{gg} in the region below threshold voltage. The frequency response of y_{gb} is similar to y_{gg} except the corner frequency is independent of channel length as shown in Figure 3.19. This is due to the existence of substrate resistance, R_{sub} (Both C_{gb} and $1/R_{sub}$ are proportional to L, resulting in the same corner frequency for devices with various channel lengths).

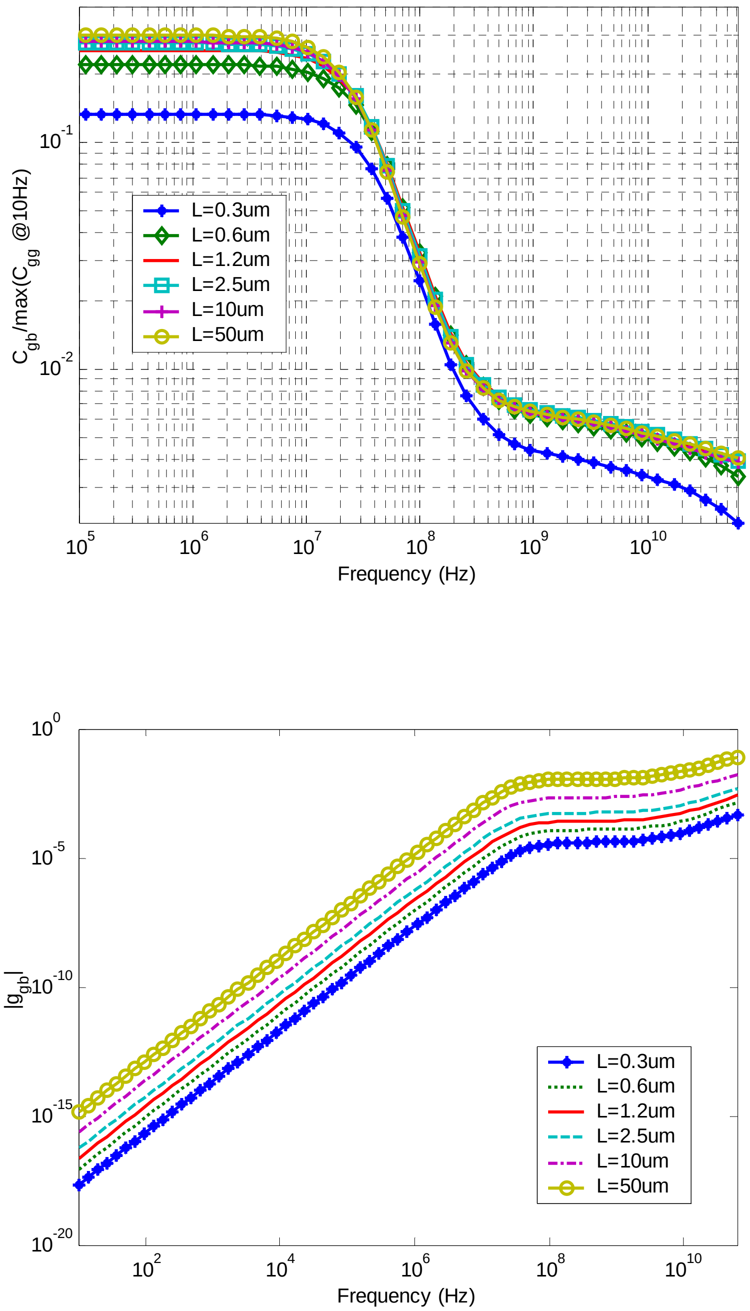


Figure 3.19. The simulated C_{gb} and g_{gb} at $V_{DS} = V_{GS} = 0$ V for various channel lengths. Note that both C_{gb} and g_{gb} degrade when s/d junction becomes shorted around 10 MHz regardless of channel length.

4 Negative Capacitance Effect in Silicon Device

Effective circuit simulation requires accurate models for active devices. These models determine simulated circuit behavior just as the devices which they represent determine the behavior of the actual circuit. The primary focus in this work is on capacitive effects, these being a dominant factor in circuit timing and ac behavior.

Capacitance or admittance spectroscopy gives insight into the underlying device physics. Also it is an important building block of small-signal models. Quite often the capacitance exhibits highly non-trivial characteristics, for example the phenomenon of negative capacitance (NC).

The NC effect reported in the literature has often been referred to as “anomalous” or “abnormal.” NC behavior measured, experimentally, has been some times attributed to instrumentation problems, such as parasitic inductance or poor measurement equipment calibration. Regrettably, in many cases experimental NC data were not reported in the literature due to the confusion caused by the effect. On the other hand, theoretical interpretations of the NC phenomenon were often based on considerations of purely electrostatic charge distributions inside the device.

4.1 Negative Capacitance Effect of a Diode

In this section, we examine one of the basic building blocks of analog circuit, the junction diode, and its small-signal model.

The AC characteristics of a diode at zero and negative bias voltages are well explained by Shockley’s theory. But in the measurements at forward bias voltages, it is found that the capacitance is negative, and thus the experimental results deviate from the Shockley’s theory [70][71].

Figure 4.1 shows the widely used small-signal model of a diode. It is comprised of a series resistance R_S, a diode conductance g_d, a junction capacitance C_j, and a diffusion capacitance C_d. It can be expressed using y-parameters in the form of

$$y_{diode} = G_{diode}(\omega) + j\omega C_{diode}(\omega) = \frac{g_d + j\omega C_t}{1 + R_S g_d + j\omega C_t R_S} \tag{4.1}$$

Where C_t is the summation of C_j and C_d. If we separate y_{diode} into the conductive and capacitive parts;

$$G_{diode}(\omega) = \frac{g_d(1 + R_S g_d) + \omega^2 C_t^2 R_S}{(1 + R_S g_d)^2 + (\omega C_t R_S)^2} \tag{4.2}$$

$$C_{diode}(\omega) = \frac{C_t}{(1 + R_S g_d)^2 + (\omega C_t R_S)^2} \tag{4.3}$$

The Equation 4.3 suggests that the admittance of the diode is always positive (capacitive) and frequency dependent with the following limiting values:

$$C_{diode}(0) = \frac{C_t}{(1 + R_S g_d)^2} \tag{4.4}$$

$$C_{diode}(\infty) = 0 \tag{4.5}$$

In the case of a reverse biased diode, $C_{diode}(0) \approx C_t$ since $g_d \approx 0$. As the bias increases from reverse bias to forward bias, the C_t becomes larger with the increasing junction capacitance due to a narrower depletion width with the following DC characteristics.

$$C_j(V) = BottomWallArea \times \frac{C_J}{\left(1 - \frac{V}{P_B}\right)^{M_j}} \tag{4.6}$$

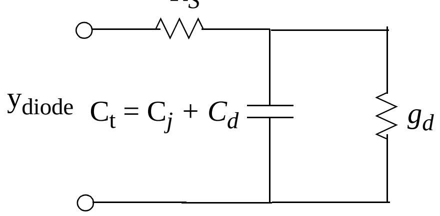


Figure 4.1. The “standard” small signal model of a diode.

Similarly, side-wall junction capacitance exhibits the same characteristics as given in Equation 4.6.

However, measured diode characteristics show a significantly different admittance characteristic as illustrated in following section.

4.1.1 Experimental Data

The results presented here were obtained on a large area n^+-pwell diode. All measurements are performed at a temperature of 25 ° C. HP4284A (20 Hz - 1 MHz) LCR meter was used for the C-V measurement. The parasitic elements were checked carefully in order not to influence the measurement data.

Figure 4.2 shows the C-V characteristics measured at different frequencies. As frequency increases, capacitance decrease as predicted by Equation 4.3. The bias dependency is correctly described by Equation 4.6 from V = - 2 V up to V = 0.5 V. Further increases in forward bias makes

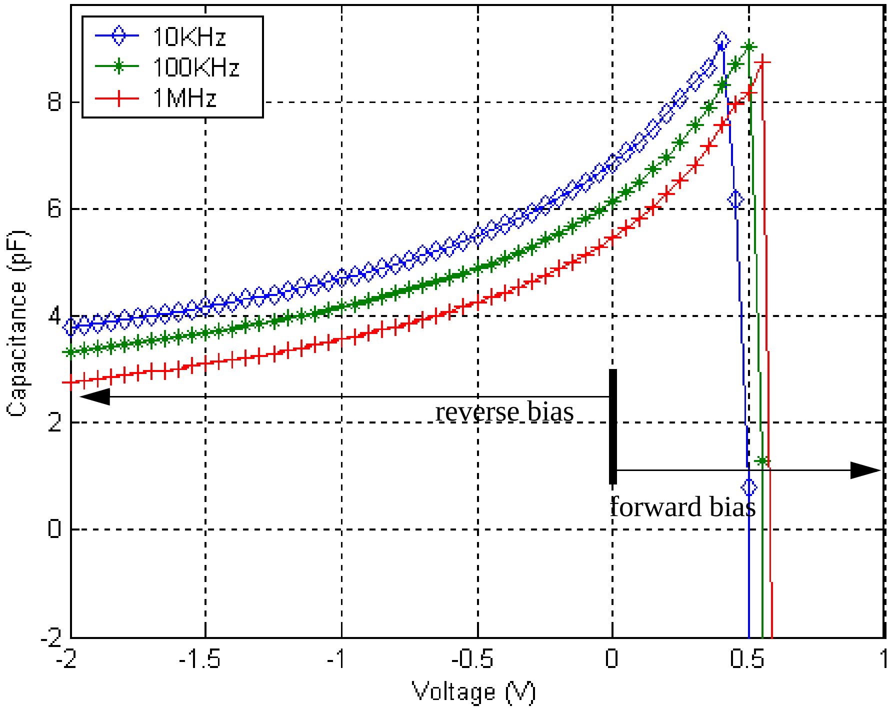


Figure 4.2. Measured capacitance of a n^+-pwell diode. When there is a large conduction current flowing in the diode, the capacitance of a diode becomes negative.

the measured capacitance values negative. The transition from the positive capacitance to negative capacitance occurs when the diode starts to draw large conduction currents. This behavior can not be explained using the simple diode model described in the previous section.

Further increases in forward bias make the measurement unstable due to the large conduction currents. Since there are limitations in characterizing the frequency response of a diode from measurements, device simulation is performed as illustrated in following section.

4.1.2 Device Simulation

A n^+-pwell diode, source/drain of a n-type MOSFET, is simulated using the device simulator, Atlas. The structure is obtained from the calibrated process simulation, Athena, for a 0.13um technology. Figure 4.3 shows C-V characteristics simulated at different frequencies. The simulations show the same negative capacitance in the strongly forward biased region as in the measurement

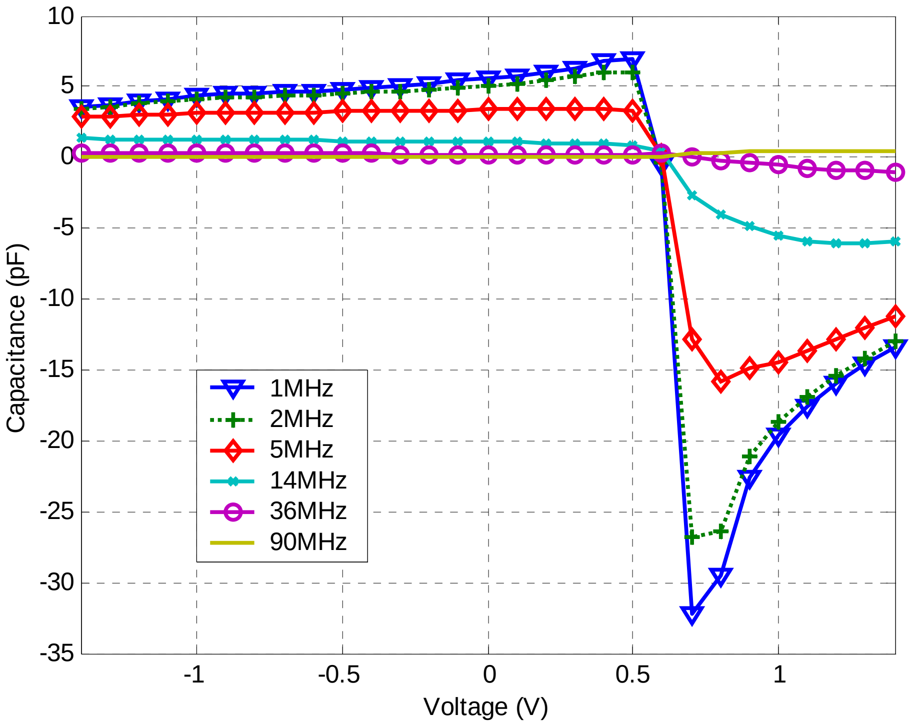


Figure 4.3. Simulated capacitance of a n^+-pwell diode. When there is a large conduction current flowing in the diode, the capacitance becomes negative.

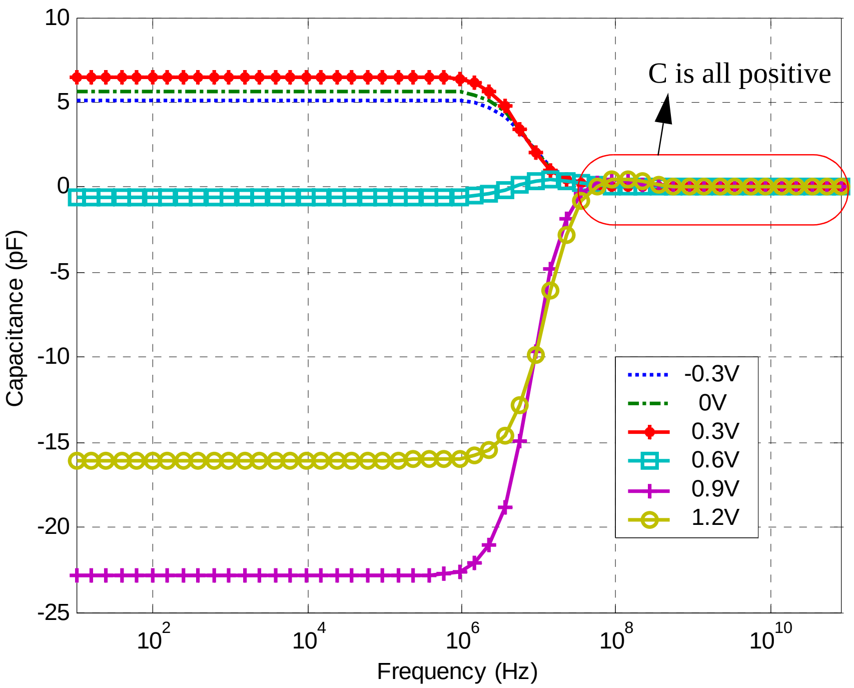


Figure 4.4. Simulated capacitance of a n^+-pwell diode. Capacitance vs. frequency for various bias. When there is a large conduction current flowing in the diode, the capacitance becomes negative. As frequency goes above 100 MHz, all capacitance becomes positive and approaches geometric C_{diode} regardless of bias conditions.

results, with the polarity transition of the capacitance occurring near the on-set of strong current flow (high level injection).

To determine the frequency dependence of the capacitance, capacitance vs. frequency plots for various DC conditions are shown in Figure 4.4. When there is low conduction current, V_{diode}= - 0.3 V ~ 0.6 V, the capacitance behaves as expected from the small-signal model (i.e., capacitance is constant up to the pole frequency as illustrated in Equation 4.3, Equation 4.4). However, when there is a large component of conduction current (V_{diode} > 0.6 V), the capacitance becomes negative at low frequencies and tend to be strongly bias dependent; the magnitude of the negative capacitance at 0.9V is as much as 5 times the magnitude of its value at reverse bias. It is interesting to note that as frequency increases even higher, the capacitance in all DC operating regions becomes positive-valued, approaching the geometric capacitance value (i.e. substrate capacitance value). The physical origin of the NC effect of a diode is explained in detail by T. Misawa [71]. In short, it is because the diffusion capacitance of the junction takes time to be charged up (by minority carriers) for a step response of voltage, while the drift component (majority carriers) can respond to the potential change in a very short time by an inertia-less characteristic when the diode is biased at those high current levels.

4.2 Small-Signal Model of a Diode Including NC Effect

The above results clearly show that the small-signal model of a diode fails to describe its frequency behavior when there are strong conduction currents. This is because the capacitance model is based on an incremental charge approach. The incremental charge approach is only valid in the case of very low conduction currents under DC bias conditions [68].

To account for the NC effect, a new small-signal model of the diode is proposed as shown in Figure 4.5. The model also includes the substrate effect at RF expressed using a parallel resistance (g_s) and capacitance (C_s). The substrate capacitance is usually very small (100 ~ 1000 times less than that of the junction capacitance) and the resistance of the highly doped region (n^+) is ignored since substrate resistance dominates. Series inductor (l_f) and resistor (r_f) are introduced to model the NC effects for high current levels. The admittance representation for a diode then becomes:

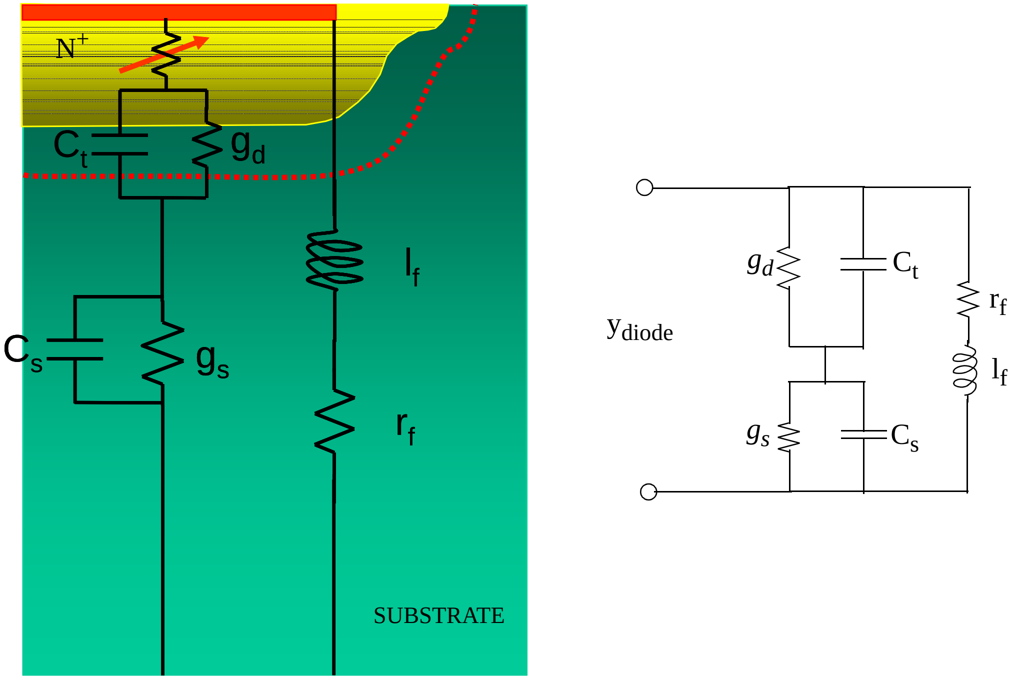


Figure 4.5. Small-signal model of source/drain to substrate diode. $C_s << C_g$ and L_f and r_f is to model the NC effect.

$$G_{diode}(\omega) = \frac{g_d^2 g_s + g_d g_s^2 + \omega^2(c_s^2 g_d + c_t^2 g_s)}{(g_d + g_s)^2 + \omega^2(c_t + c_s)^2} + \frac{r_f}{r_f^2 + (\omega l)^2} \tag{4.7}$$

$$C_{diode}(\omega) = \frac{g_d^2 c_s + c_t g_s^2 + \omega^2 c_t c_s(c_s + c_t)}{(g_d + g_s)^2 + \omega^2(c_t + c_s)^2} - \frac{l/r_f^2}{1 + (\omega l/r_f)^2} \tag{4.8}$$

Although the capacitance is small compared to the conductive part of the admittance, it can be comparable to the junction admittance and makes the admittance of the whole diode reactive, as the injection level rises. Figure 4.6 shows the frequency response of the conductance and capacitance term, based on device simulation. The checked mark represents the NC bias condition. Equation 4.7 and Equation 4.8 correctly predict the frequency response at reverse and forward bias. Note that at very high frequencies (> 100 MHz) the NC effects dies out and both conductance and capacitance saturates as given by:

$$G_{diode}(\infty) = \frac{(c_s^2 g_d + c_t^2 g_s)}{(c_t + c_s)^2} \approx g_s \tag{4.9}$$

$$C_{diode}(\infty) = \frac{c_t c_s}{(c_t + c_s)} \approx c_s \tag{4.10}$$

The diode example, using both the measurements and simulations, shows that the capacitance model based on incremental charge method does not hold. It is therefore necessary to consider a more general definition of a capacitance and a methodology for its calculation.

4.3 Definition of Capacitance and Method of Its Calculation

For simplicity, we consider two-terminal semiconductor devices. Capacitance is defined as

$$C(\omega) = \frac{1}{\omega} Imag[Y(\omega)] \tag{4.11}$$

where

$$Y(\omega) = \frac{\delta I(\omega)}{\delta V(\omega)} \tag{4.12}$$

is the device admittance relating the small-signal harmonic current flowing through the terminals and small-signal voltage. The real part of the complex admittance is called conductance

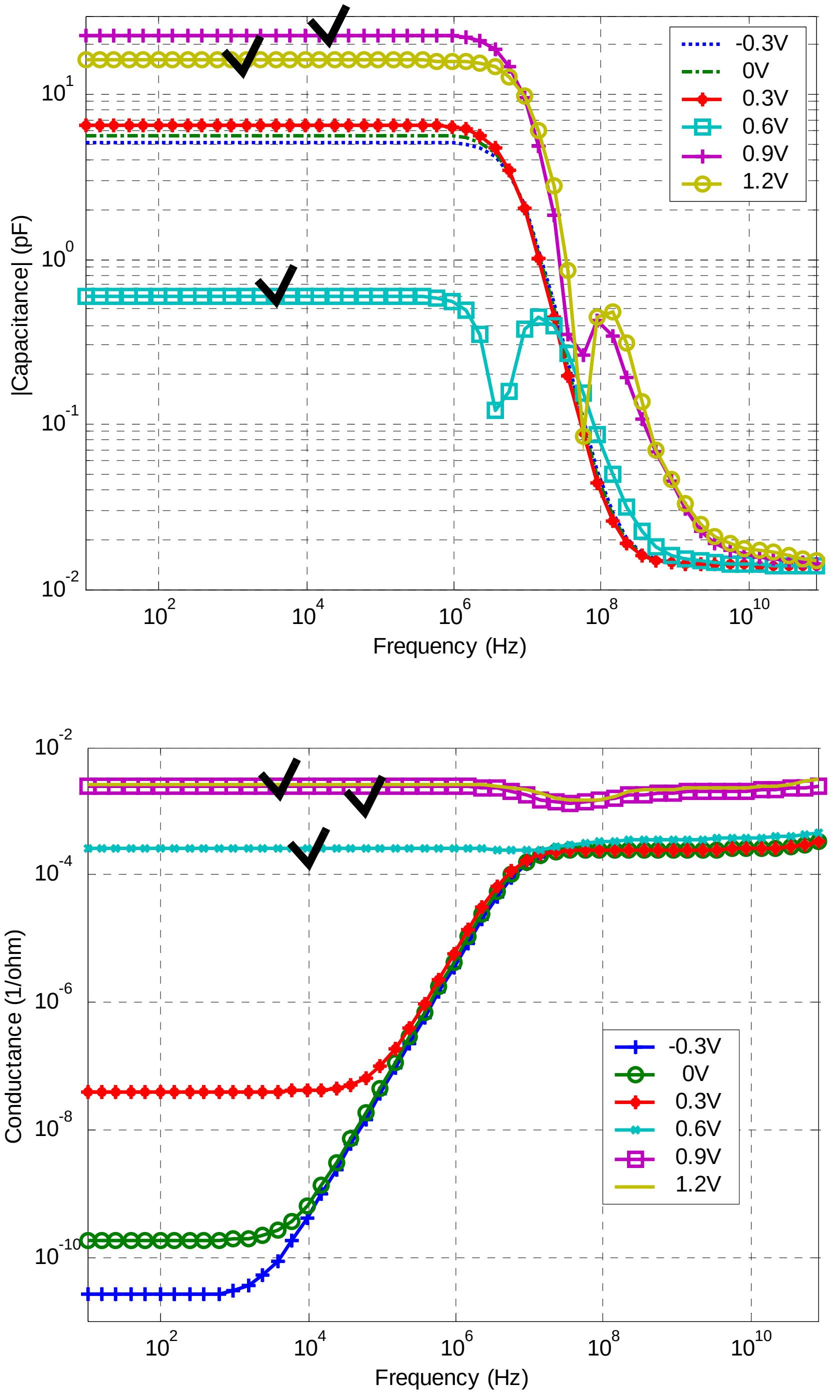


Figure 4.6. The simulated capacitance of a n^{+}-pwell diode for various bias. When there is a large conduction current flowing in the diode, the capacitance becomes negative. As frequency goes above 100 MHz, all capacitance becomes positive number and approaches geometric C_{diode} regardless of bias conditions.

$G(\omega) = Real[Y(\omega)]$. In general, capacitance calculations should involve the solution of the system of equations describing device operation (Poisson equation, current continuity equation, etc.) in the time or frequency domain. There are several established methods for calculation of the capacitance (and, more generally, of the admittance) using:

- Incremental Charge Method -- The capacitance is calculated as $C = \frac{\Delta Q}{\Delta V}$. The main advantage of this method is its simplicity, as it requires only a steady-state simulation program for the calculation.
- Sinusoidal Steady-State Analysis (SSSA) -- The system of the time-dependent equations is linearized around a steady-state solution for harmonic small-signal quantities, and then solved for a particular frequency. The SSSA method is rigorous, rather simple to carry out, and fast. The disadvantage is that it requires solution of a system of equations for each frequency to obtain the frequency dependence of capacitance.
- Method Based on Fourier Analysis -- The method based on the Fourier analysis involves calculation of the transient response of the device to a small time-dependent voltage excitation (usually in the form of a step-function) applied at time t=0. Admittance is calculated as the ratio of the Fourier components of the transient current

The first case, the incremental charge method of capacitance calculation, is absolutely inapplicable for handling the case of large conduction currents in the device, which is often the case when the capacitance is negative [68]. Conventionally, capacitance is associated with the accumulation of charges and electric field energy with the change of the voltage on contacts. This concept comes from electrostatics, when conduction current is zero and the total electric current is due to the displacement component, related to the redistribution of charges inside the structure. However the capacitance is determined by the reactive part of the total current, which comprises both conduction and displacement components. The incremental charge method only considers the displacement component. Regrettably many of the capacitance values obtained using device modeling are based on the incremental charge method. One of them is the diode model as illustrated in previous section.

The second case, SSSA, corresponds to device simulation. It is shown in the previous section that the device simulation shows very similar NC characteristic in terms of frequency and bias. The device simulation can be quite useful in calculating nodal capacitance when capacitance measurements are limited by instrumentation capabilities, when large conduction currents involved.

The third case, Fourier analysis, is employed by M. Ershov [68]. It is shown that the NC can have the following theoretical frequency dependence:

$$C(\omega) = C_o + \frac{a_1\tau_1}{1+(\omega\tau_1)^2} - \frac{a_2\tau_2}{1+(\omega\tau_2)^2} \tag{4.13}$$

where C_o is the normal geometric capacitance, obtained using the incremental charge method, and a_1, a_2, τ_1, and τ_2 are additional model parameters. It can be seen that, depending on the values of the parameters, the frequency dependence of capacitance can be either negative or positive. It is interesting to note that Equation 4.8 has a similar frequency dependence to that given in Equation 4.13. The high frequency capacitance value is equal to the geometric capacitance:

$$C(\infty) = C_o \tag{4.14}$$

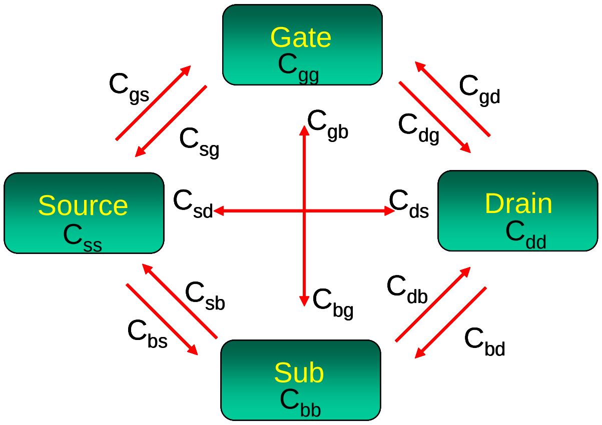
This diode example also shows that the negative capacitance approaches the geometric capacitance as frequency increases. From the physical modeling viewpoint, this is due to the fact that at high frequencies the physical processes related to electron transport are “frozen” due to finite carrier inertia, and the total small-signal current at high frequencies contains only the displacement component associated with the charging of the geometric capacitance [68].

4.4 Capacitance Model of MOSFET

The capacitor model of the MOSFET has been extensively studied since its invention. The first derivative of such a capacitance model for MOSFET was represented in the Meyer model [27]. Although the model generally gave accurate capacitance characteristics, the model had fundamental problems, e.g. non conservation of charge. The Ward and Dutton model [32] used a charge-based approach, which conserves charge correctly, and showed a number of unique characteristics, for example, the non reciprocal property between any pair of terminals and the negative drain-source capacitances. Since then, there have been refinements of the charge based model (i.e., refinement of non-linear capacitance, charge split method, etc.). The capacitance based on incremental charge method is defined as:

$$C = \frac{\partial Q}{\partial V} \tag{4.15}$$

In this section, the characteristics of terminal capacitance of MOSFETs is examined in terms of geometry (i.e. long channel vs. short channel). The main focus will be to consider characteristic of frequency response rather than the accuracy of existing models (i.e. BSIM4 and MOS 11).



$$C_{ii} = \frac{-\partial Q_i}{\partial V_i}$$

$$C_{ij} = \frac{\partial Q_i}{\partial V_j}$$

Figure 4.7. Conventional 16 capacitances of MOSFET. 9 or them are linearly independent.

4.4.1 Capacitances of MOSFET

The MOSFET has four terminals and thus has 16 capacitances, 9 of which are linearly independent, as shown in Figure 4.7. Each of the capacitances is defined in following way.

Junction and overlap capacitances are modeled separately; this analysis applies only to the intrinsic capacitances associated with the channel charge. Device structures are created in a way that the MOSFET capacitance is mainly intrinsic - the area of source and drain is reduced significantly compared to channel length so that the extracted capacitance is mainly from intrinsic capacitances.

In the following we present the simulation data from Atlas simulations. The doping profiles used are from SUPREM simulations, whose simulation parameters have been calibrated with experimental data of the dopant profiles. Once the simulation parameters have been properly tuned, a low frequency (10 Hz) AC simulation is performed to extract CV characteristics. Two devices are subject to the above procedure. One is a long-channel device of L = 10 um. The CV characteristics, normalized to the C_{gg} of accumulation region, are given in Figure 4.8 for V_{DS} = 0 V and in Figure 4.9 for V_{DS} =3V. These plots agree well with the long-channel expressions from the charge-based capacitance model in Appendix A. Because the parasitic capacitances are small, the total capacitances are essentially equal to the intrinsic device capacitances.

The other simulated device is a short-channel length device of L = 0.3 um and Figure 4.10 and Figure 4.11 show resulting CV characteristics for V_{DS} = 0 V and V_{DS} = 3 V, respectively. Even though source and drain parasitics are intentionally minimized compared to channel length to elim-

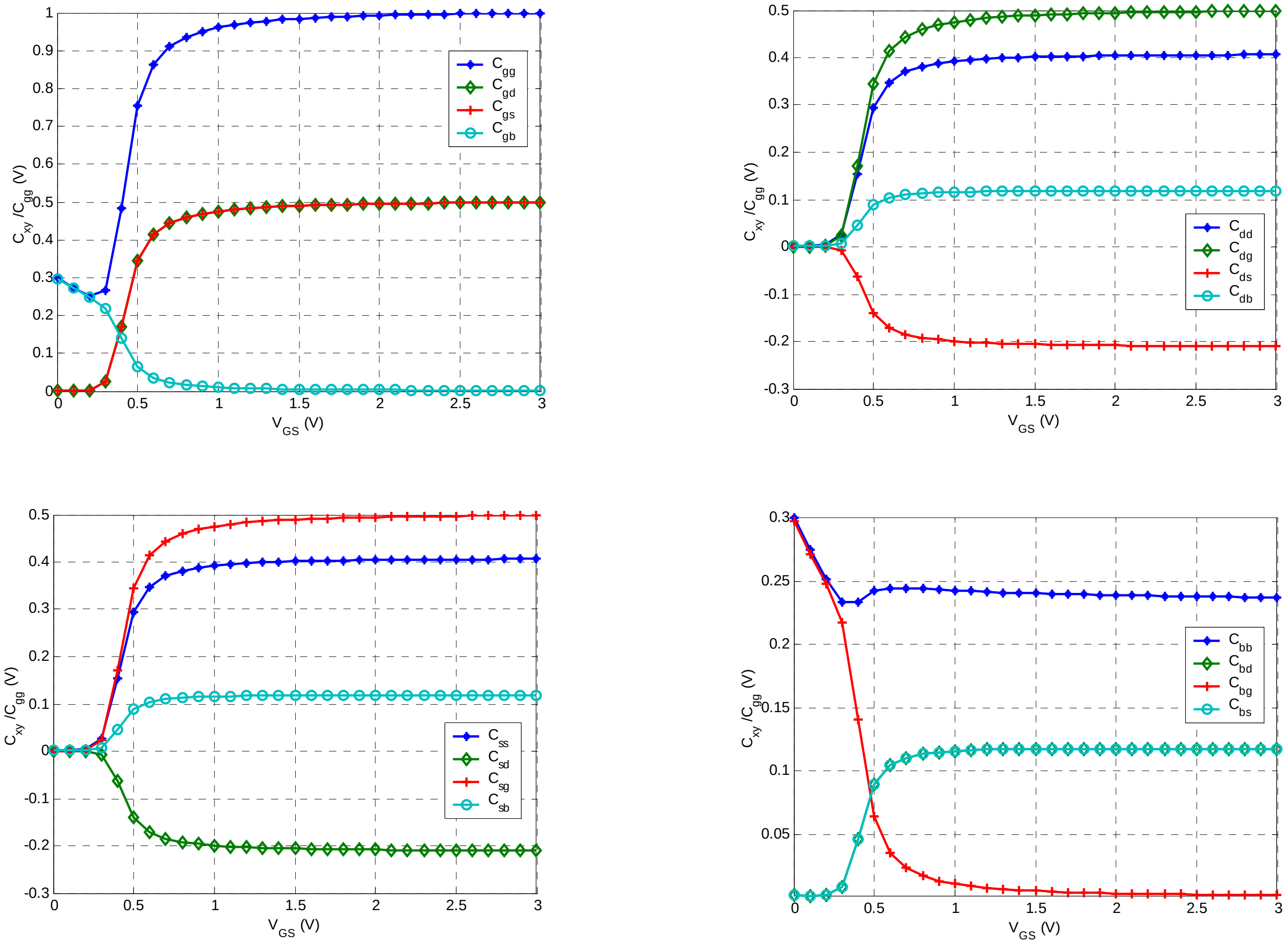


Figure 4.8. Atlas simulated C-V characteristics for L = 10 um, and W = 25 um device at 10 Hz and V_{DS} = 0 V. The capacitances are normalized to the C_{gg} of the accumulation region.

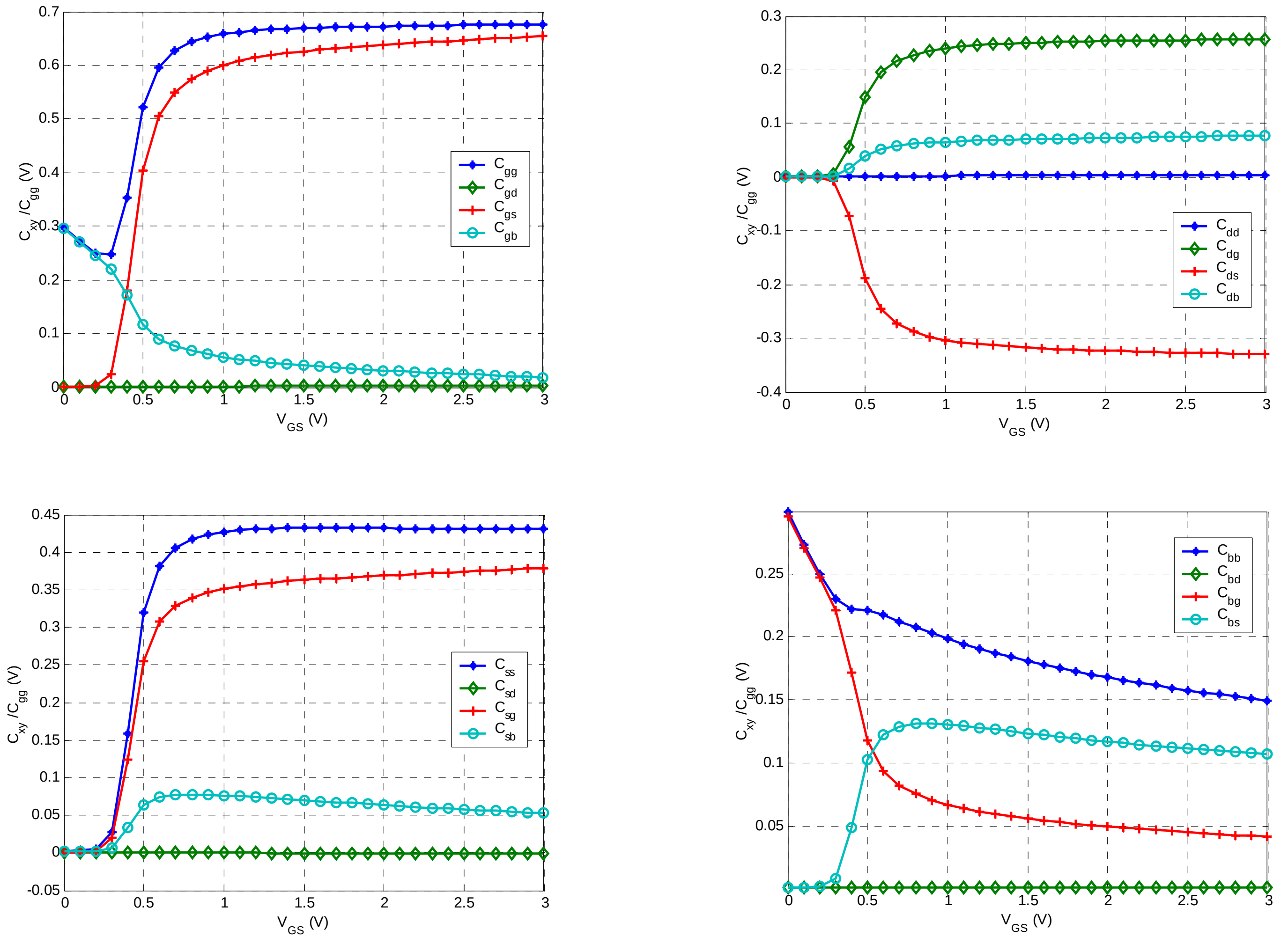


Figure 4.9. Atlas simulated C-V characteristics for L = 10 um, and W = 25 um device at 10 Hz and V_{DS} = 3V. The capacitances are normalized to the C_{gg} of the accumulation region.

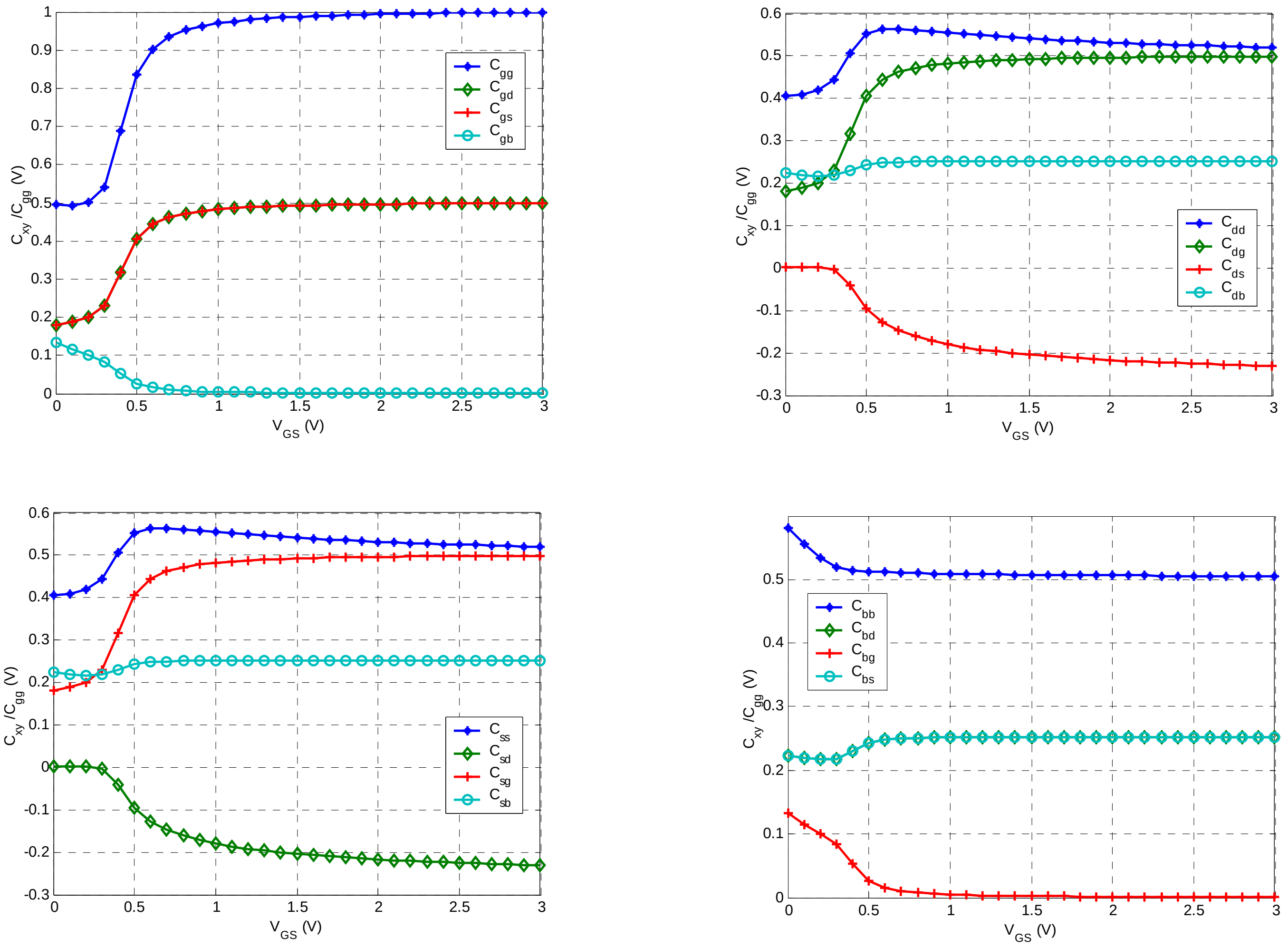


Figure 4.10. Atlas simulated C-V characteristics for L = 0.3 um, and W = 25 um device at 10 Hz and V_{DS} = 0V. The capacitances are normalized to the C_{gg} of the accumulation region.

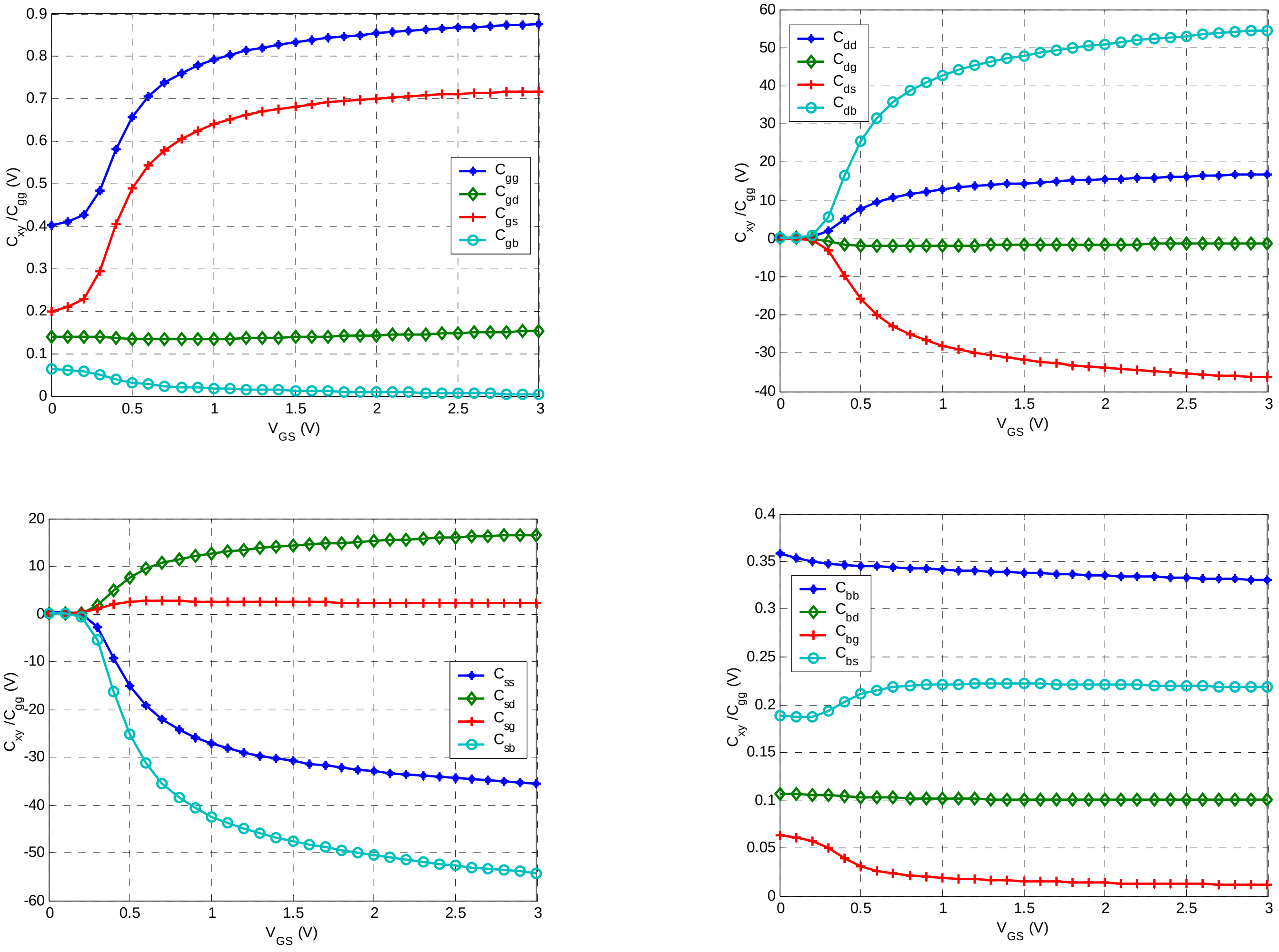


Figure 4.11. Atlas simulated C-V characteristics for L = 0.3 um, and W = 25 um device at 10 Hz and V_{DS} = 3V. The capacitances are normalized to the C_{gg} of the accumulation region.

inate the parasitic effects (junction capacitances), C_{sb} C_{bs} C_{bd} and C_{db} show some amount of parasitic capacitance. Accounting for parasitics, the CV characteristics of the short channel device when $V_{DS} = 0$ basically have the same characteristics as for the long channel device. There are some interesting results shown in Figure 4.11 for devices in saturation. C_{gg}, C_{gd}, C_{gs}, C_{gb}, C_{bb}, C_{bd}, C_{bg}, C_{bs} all show the same normal characteristics as for the long channel device. However C_{dd}, C_{dg}, C_{ds}, C_{db}, C_{ss}, C_{sd}, C_{sg}, and C_{sb} show two dramatically different characteristics. The first noticeable difference is that the magnitude of the parameters are greater than unity, meaning the capacitances become bigger than the maximum gate capacitance by as much as 55 times. The second is the polarity of the parameters. For example, the C_{sd} is negative, close to zero, for the long channel device as described in model in Appendix A, but it is positive and has the normalized magnitude of as high as 16 for short channel device.

It was first thought that the same effect as the NC (negative capacitance) effect due to a similar frequency response was the cause; it turned out that the observed capacitance behavior for short channel device is due to the impact of substrate resistance as explained in following section.

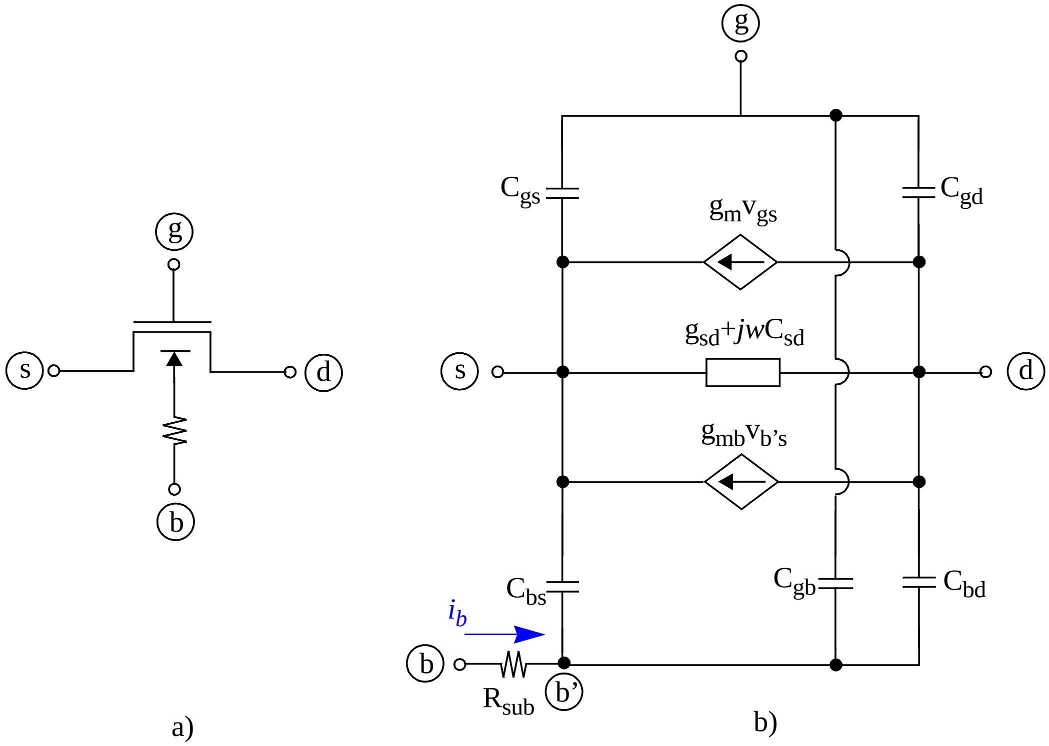


Figure 4.12. a) MOSFET with bulk resistance R_{sub}, impact of junction capacitance is neglected, and b) corresponding small-signal circuit, where b' is an internal node. Note that the small-signal model is the simplified version of quasi-static model in Figure 2.4.

4.5 Impact of Bulk Resistance on MOS Capacitance

In order to calculate the impact of bulk resistance on the (intrinsic) small-signal behavior of a MOSFET, we assume the influence of junction capacitances can be neglected and use the circuit in Figure 4.12. Here, R$_{sub}$ is the substrate resistance, which ideally scales with $1/(W \cdot L)$.

First, we try to calculate the effective drain-source capacitance, C$_{dseff}$, that is seen at the terminals. In this case, we apply a sine wave to the source terminal and see what happens at the drain, bulk and gate are ac-grounded. Using the small-signal in b), we can write for the internal node b' by equating the body current due to v$_s$ to the body current due to v$_{b'}$:

$$i_b = y_{bb}v_{b'} + y_{bs}v_s + y_{bd}v_d + y_{bg}v_g = \frac{1}{R_{sub}}(-v_{b'}) \tag{4.16}$$

since $v_d = v_g = 0$ for y_{dseff} calculation and $y_{bb} = j\omega C_{bb}$, $y_{bg} = -j\omega C_{bg}$, Equation 4.16 becomes:

$$v_{b'} = \frac{j\omega R_{sub}C_{bs}}{1 + j\omega R_{sub}C_{bb}}v_s \tag{4.17}$$

where $C_{bb} = C_{gb} + C_{sb} + C_{db} = C_{bg} + C_{bs} + C_{bd}$. The small-signal voltage on node b' is amplified by the substrate transconductance g$_{mb}$ resulting in an extra term in C$_{dseff}$:

$$C_{dseff} = C_{ds} - \frac{R_{sub}g_{mb}}{1 + \omega^2 R_{sub}^2 C_{bb}^2}C_{bs} \tag{4.18}$$

Next, we can follow the same procedure for the effective drain-bulk capacitance C$_{dbeff}$ that is seen at the terminals. In this case, we find:

$$C_{dbeff} = C_{db} + \frac{R_{sub}g_{mb}}{1 + \omega^2 R_{sub}^2 C_{bb}^2}C_{bb} \tag{4.19}$$

For short-channel devices at low frequencies, the effective drain-bulk capacitance C$_{dbeff}$ may thus become more positive. Again, at higher frequencies this effect disappears. Note that the (angular) corner frequency ($\omega = 1/(R_{sub}C_{bb})$) is the same as for C$_{dseff.}$

Finally, we calculate the effective drain-gate capacitance C$_{dgeff}$ that is seen at the terminals. In this case we find:

$$C_{dgeff} = C_{dg} - \frac{R_{sub} g_{mb}}{1 + \omega^2 R_{sub}^2 C_{bb}^2} C_{bg} \tag{4.20}$$

For short-channel devices at low frequencies, the effective drain-gate capacitance C_{dgeff} may thus become more negative. Again, at higher frequencies this effect disappears. Note that the (angular) corner frequency ($\omega = 1/(R_{sub}C_{bb})$) is the same as for C_{dseff} and C_{dbeff}.

Since $R_{sub} \propto 1/L$, $g_{mb} \propto 1/L$, and $C_{bx} \propto L$, the second term in Equation 4.18 through Equation 4.20 is overall inversely proportional to L. In other words, its absolute value increases with decreasing L. Hence, for short-channel devices at low frequencies, the C_{dseff} and C_{dgeff} may be much more negative than the ideal long-channel value of C_{ds} and C_{dg}. For higher frequencies, i.e., $\omega > 1/(R_{sub}C_{bb})$, this effect disappears and approaches the intrinsic values of C_{ds} and C_{dg} respectively. Note that $R_{sub}C_{bb}$ is independent of L, and as a result the corner frequency is independent of geometry. Figure 4.13 shows the frequency response of various channel length device for C_{ddeff}, C_{dgeff}, C_{dseff}, and C_{dbeff} from device simulation and shows identical frequency response as

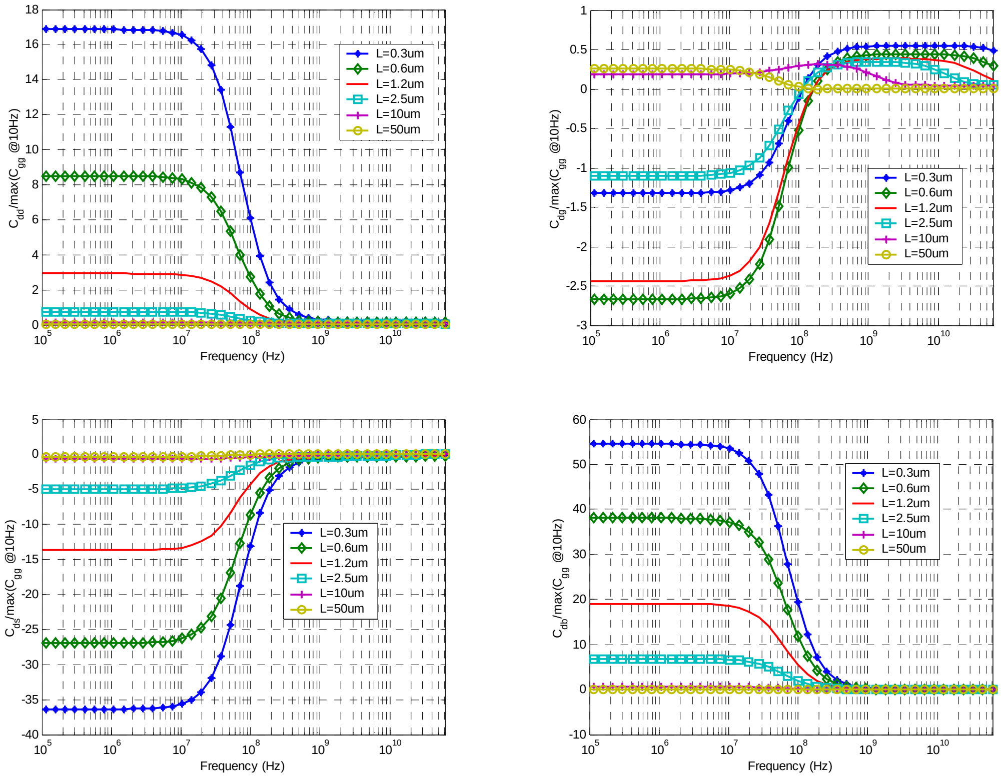


Figure 4.13. When V_{DS} = 3 V and V_{GS} = 3 V, frequency response of C_{dd}, C_{dg}, C_{ds}, and C_{db} for various channel length devices (L = 0.3, 0.6, 1.2, 2.5, 10, and 50 um).

described in Equation 4.18 through Equation 4.20. C_{sseff}, C_{sgeff}, C_{sdeff}, and C_{sbeff} also show similar characteristics and can be found in Figure B.8 in Appendix B.

In the above, we have neglected the impact of drain and source series resistance R_s, which will specifically affect C_{dgeff} at very short channel lengths. A source series resistance will result in an amplification of the C_{sg} (both intrinsic and overlap) via $g_m + g_{mb}$, and it will positively affect C_{dgeff}. In other words, the impact of source series resistance R_s is opposite to the impact of bulk resistance R_{sub}.

5 Modeling of Source to Drain Coupling and Substrate Network

In CMOS technology, as the operation frequency goes up, the substrate parasitic impedance, which exists between drain/source nodes and ground, critically affects the RF performance of the transistor. For example, with common-source amplifier, high substrate resistance lowers the output resistance and transconductance. The well known method to minimize substrate effects is to reduce the substrate resistance by placing substrate contacts around the MOSFET [50][51].

The difficulty in separating bulk characteristics from the intrinsic parasitics results in numerous substrate models that are only accurate within a limited frequency range as shown in Figure 5.1. Two-dimensional simulations are used to fully understand effects of the substrate and its impact on output characteristics.

In addition to the substrate network, source to drain coupling plays an important roll in output characteristics at high frequencies. In this section, it will be shown that the source-to-drain coupling mostly dominates the output characteristics of RF MOSFETs.

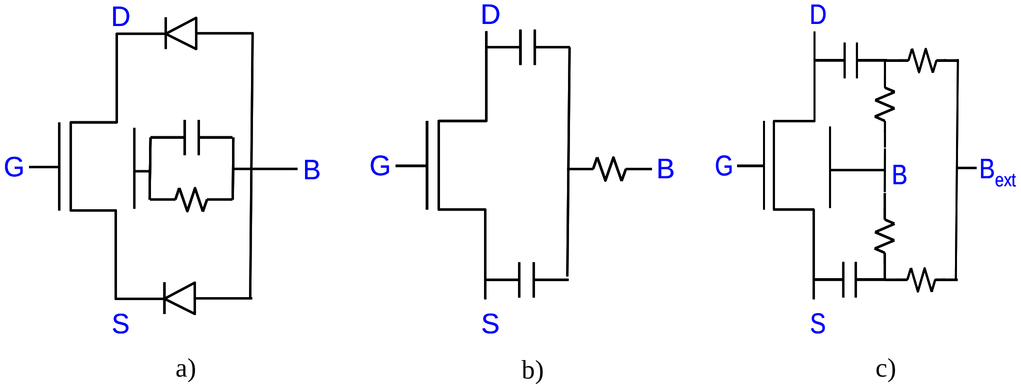


Figure 5.1. Substrate network model of a) [54], b) [57] and, c) [46]

5.1 Substrate Network Modeling for CMOS RF

The extraction of MOSFET parasitics, in particular the bulk related parasitics, is often problematic due to the four-terminal nature of the MOSFET. For measurements of MOSFETs in the common source configuration, bulk characteristics can be difficult to separate from intrinsic parasitics. For example, from measured s-parameters, the converted y_{22} parameter represents the output characteristic of common source configuration. The y_{22} parameters can be divided into the following components:

$$y_{22} = -y_{sd} - y_{bd} - y_{gd} = y_{dd} \tag{5.1}$$

Since y_{gd} is the same as y_{12}, the modeling of output characteristic can be reduced to modeling y_{sd} and y_{bd} as:

$$y_{22} + y_{12} = -y_{sd} - y_{bd} \tag{5.2}$$

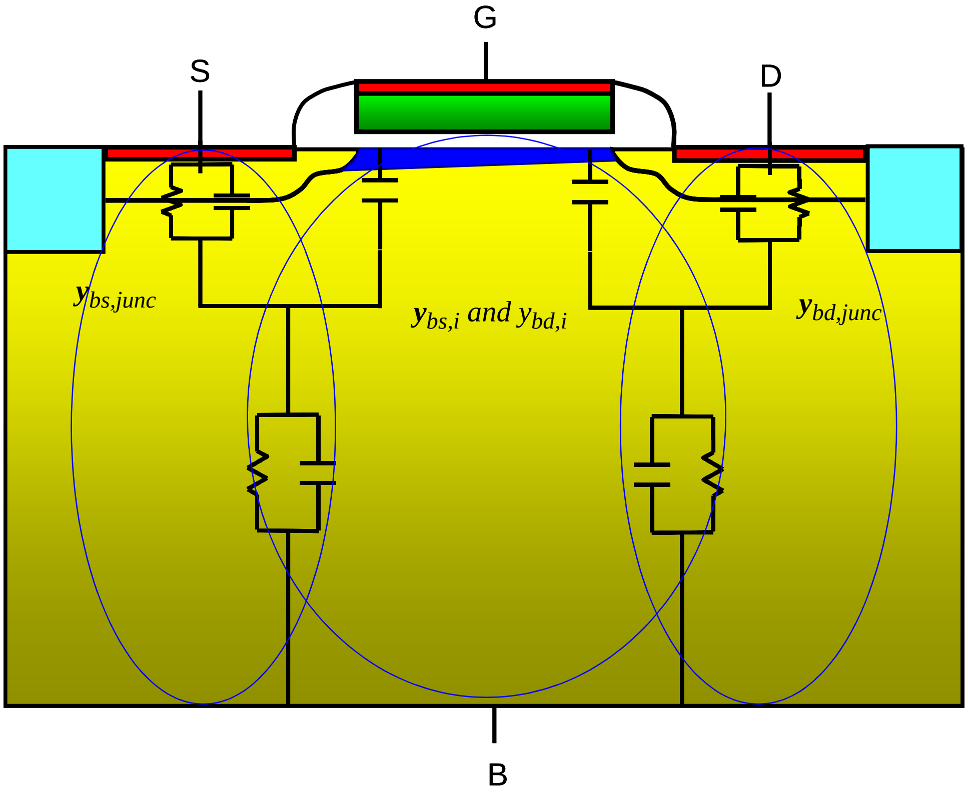


Figure 5.2. Small-signal equivalent circuit of source to substrate and drain to substrate network.

However, it is not trivial to separate y_{sd} and y_{bd} individually. One trick used to separate y_{sd} and y_{bd} involves extraction for $V_{GS} = 0$. Since y_{sd} is minimal due to the absence of channel charge, we have

$$y_{22} + y_{12} \approx -y_{bd} \tag{5.3}$$

However the success of this approach depends on the characteristics of measured transistor since the y_{sd} can be quite comparable to y_{bd} if the device is leaky. Furthermore, even when successful, the extracted y_{bd} represents only the drain junction to substrate admittance as shown in Figure 5.2 marked as $y_{bd,junc}$. As shown in Figure 5.2, y_{bd} is further divided into intrinsic and extrinsic component as follows:

$$y_{bd} = y_{bd,junc} + y_{bd,i} = -g_{bd} - j\omega C_{bd} \tag{5.4}$$

To extract the contribution of $y_{bd,i}$, it is necessary to measure all bias conditions and then de-embed the desired parameter. However, y_{sd} inherently makes it impossible distinguish it from y_{22}. This is one of the main reasons why many of the published reports fail to accurately model both y_{sd} and y_{bd}.

Physical 2D device simulation is quite flexible in extracting the y_{sd} and y_{bd} components individually since y-parameters for all four terminals can be directly simulated without stability problems.

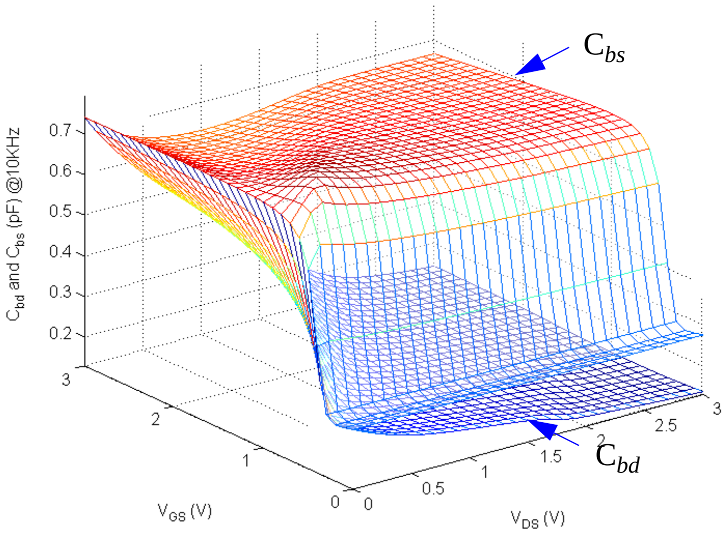


Figure 5.3. 2-D device simulated C_{bs} and C_{bd} for L = 1.2 um device at 10 kHz.

Figure 5.3 shows C_{bs} and C_{bd} obtained from 2D device simulations for L = 1.2 um device extracted at 10 kHz, and V_{DS}/V_{GS} from 0 V to 3 V. It can be seen that the impact of channel to substrate capacitances, $C_{bd,i}$ and $C_{bs,i}$, is quite high for this 1.2 um device since C_{bs} and C_{bd} at $V_{GS} = 0$ is small compared to the values for $V_{GS} > V_{th}$. When $V_{GS} = 0$ V, the bias dependency of the normal junction diode is also shown for C_{bd} (e.g. a gradual decrease of capacitance due to the widening of the depletion layer when the reverse bias, V_{DS}, increases). It is also noticeable that C_{bd_i} and C_{bs_i} exhibit similar charge sharing behavior as for C_{gs} and C_{gd}. The dominance of the intrinsic components, C_{bd_i} and C_{bs_i}, on C_{bs} and C_{bd} mainly depends on the size of the transistor and the area of junction capacitance. In general, junction capacitance is around 40 % of gate capacitance. It should be noted that as we further scale the MOSFET transistor, the junction capacitances, C_{bs_junc} and C_{bd_junc}, tend to dominate over channel to bulk capacitances, C_{bd_i} and C_{bs_i}, because the scaling of junctions mostly depends on contact scaling, which tends to lag behind gate scaling.

Figure 5.4 shows the frequency response of C_{bd} and g_{bd} for various biasing conditions. The frequency response when the MOSFET is off, $V_{DS} = V_{GS} = 0$ V, as in Figure 5.4a, is virtually identical to the frequency response of the diode model shown in Figure 4.5. When the MOSFET is operating in the linear region (Figure 5.4b) C_{bd} and g_{bd} for a L = 50 um device shows NQS effects. The NQS effect occurs when the source/drain to bulk admittance is dominated by intrinsic components, C_{bd_i} and C_{bs_i}. Hence the L = 50 um device experiences the greatest NQS effect compared to smaller channel length devices since the fractional contribution of source/drain junction is relatively small compared to channel lengths used in this experiment, where the junction area is identical for all channel length devices.

Also the NQS effect is dependent on bias conditions in the same way as for C_{gs} and C_{gd} behavior described in Chapter 3.3. In the saturation region, C_{bs}, Figure 5.4d, shows significant NQS effects while C_{bd}, in Figure 5.4c, does not.

However the NQS effect on the substrate network is not likely to occur for most practical RF devices since long channel devices (L > 10 um) are generally not used in RF frequency applications. Hence, the NQS effect on the substrate network for small-signal modeling will be ignored in this work.

The small-signal model of the substrate network in Figure 5.2 can be further simplified as a compact model shown in Figure 5.5. The C_t in Figure 5.5 is a summation of junction capacitance and intrinsic channel to substrate capacitance. The terms g_s, g_d and C_s represent conductance of junction, substrate conductance, and substrate capacitance respectively.

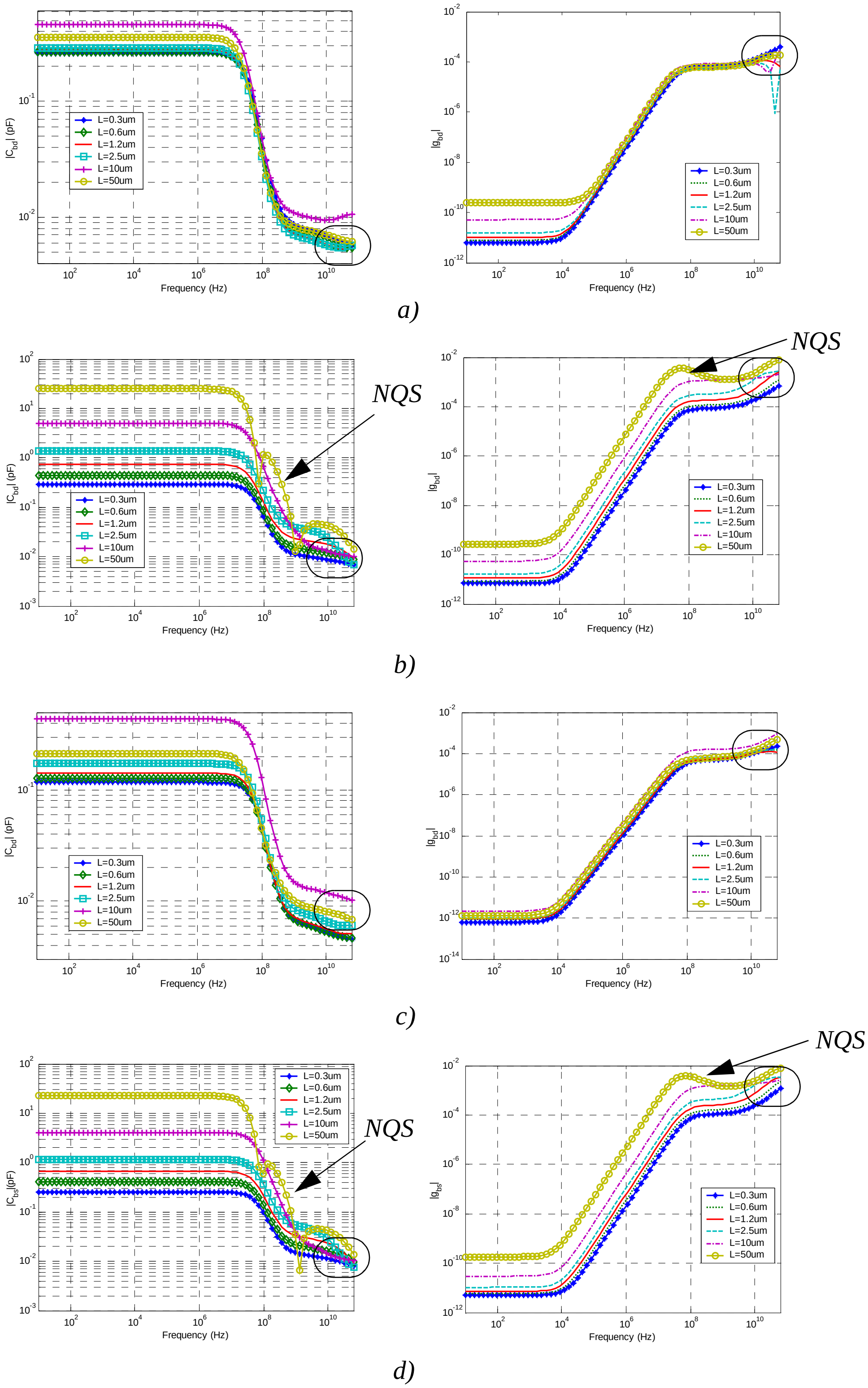


Figure 5.4. Frequency response of C_{bd} and g_{bd} a) when V_{DS} = 0 V and V_{GS} = 0 V, b) when V_{DS} = 0 V and V_{GS} = 3 V, c) when V_{DS} = 3V and V_{GS} = 3 V, d) Frequency response of C_{bs} and g_{bs} when V_{DS} = 3V and V_{GS} = 3 V. Note that L = 50 um device experiences NQS effect at high frequencies (i.e, C_{bd} becomes negative).

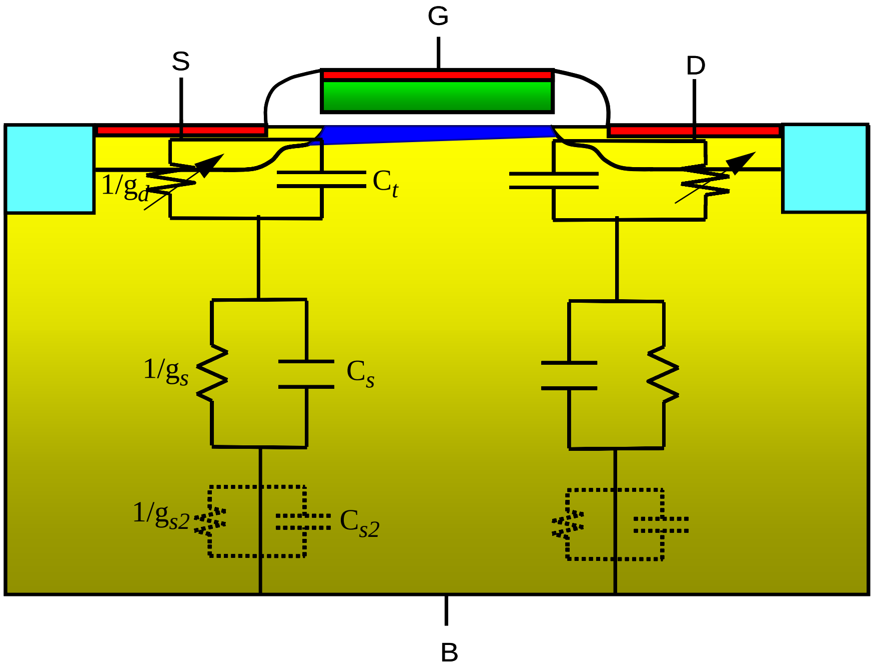


Figure 5.5. Substrate network of MOSFET (y_{bs} and y_{bd}). The dotted parallel RC circuit accounts for second order effects.

The frequency response of the substrate network (y_{bd} and y_{bs}) is modeled following the small-signal approach for the diode as given in Section 3.2. Since we are interested in the reverse biased diode case, Equation 4.7 and Equation 4.8 become:

$$g_{bs}(\omega) = \frac{\omega^2 C_t^2 R_s}{1 + \omega^2 r_s^2 (c_t + c_s)^2} \tag{5.5}$$

$$C_{bs}(\omega) = C_t \left[\frac{1 + \omega^2 C_s (C_s + C_t)}{1 + \omega^2 R_s^2 (C_t + C_s)^2} \right] \tag{5.6}$$

where $R_s = 1/g_s$ (substrate resistance). The term that models the negative capacitance effect in Equation 4.7 and Equation 4.8 is ignored since its effect only appears when the junction is strongly forward biased. The source/drain conductance term, g_d, is also ignored since $g_d \ll g_s$ and only affects the very low frequency regime.

Equations 5.5 and 5.6 accurately represent the frequency response of y_{bs} and y_{bd}. However as frequency goes above 10 GHz (the circled region in Figure 5.4), the characteristics start to disagree with the substrate network model. This is due to the second-order effects resulting from the lossy

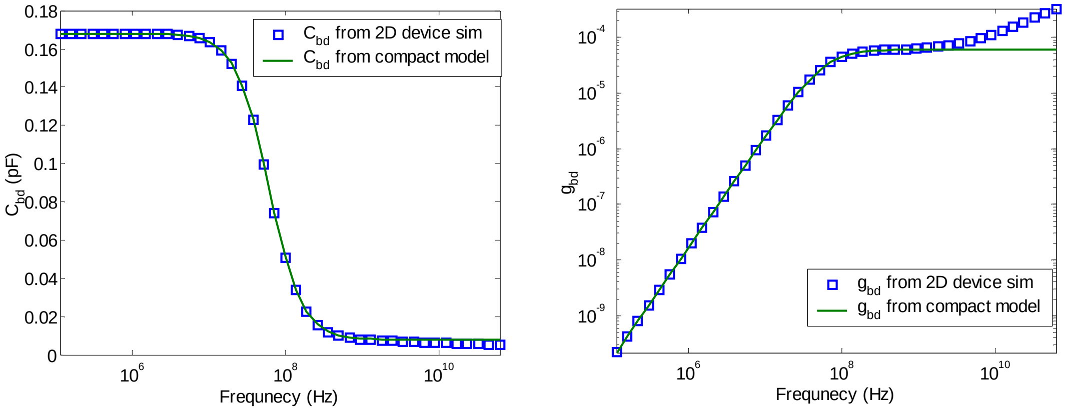


Figure 5.6. Frequency response of C_{bd} and g_{bd} from 2-D device simulation and compact model for L = 0.3 um device at liner region, $V_{DS} = V_{GS} = 1$ V.

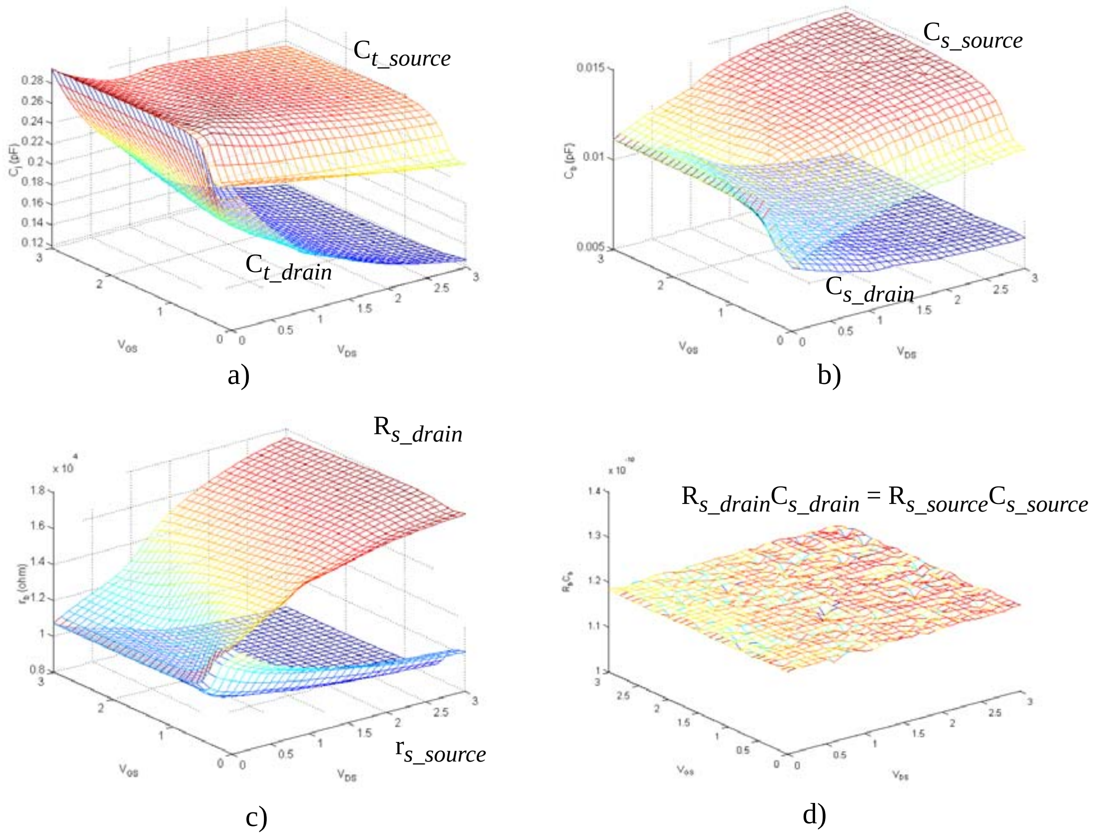
substrate. Additional parallel RC elements (dotted circuit elements in Figure 5.5) are needed to model the second-order effects. The compact model ignores such second order effects since their impact on the small-signal characteristics of the MOSFET are negligible. Figure 5.6 shows the frequency response of C_{bd} and g_{bd} comparing the substrate compact model with 2D device simulations at $V_{DS} = V_{GS} = 1$ V. The compact model precisely matches the simulated frequency response of the substrate up to 10 GHz. As noted, there is an increasing mismatch between the model and 2D device simulations as the frequency increases further due to the second order effects of the substrate.

Figure 5.7 shows the extracted substrate parameters for both drain-side and source-side contributions, and for all biasing conditions in L = 0.3 um device. The extracted drain-side C_t (C_{t_drain}) and source-side C_t (C_{t_source}) are identical to the bias characteristics of low frequency C_{bd} and C_{bs} as shown in Figure 5.3, since from Equation 5.6,

$$C_{bs}(0) = C_t \tag{5.7}$$

The extracted C_{s_source} and C_{s_drain}, Figure 5.7b, shows strong gate and drain bias dependency. It is believed that C_s *is proportional to the effective surface area interfacing with the bulk region electrically*. As more channel area couples to the source side, with increased V_{DS}, C_{s_source} increases while C_{s_drain} decreases. However the R_{s_drain} and R_{b_drain} (Figure 5.7c) shows the opposite bias behavior, which is physically reasonable.

It is very interesting to note that the extracted parameters R_{s_drain}, R_{s_source}, C_{s_drain}, and C_{s_source} show the following conservative behavior.



a)

b)

c)

d)

Figure 5.7. Analytically extracted parameters of substrate network for all biasing region on L = 0.3 um device a) C_t, b) C_s, c) R_s, and d) $R_{s\_drain}C_{s\_drain}$ and $R_{s\_source}C_{s\_source}$.

$$R_{bdrain}C_{bdrain} = R_{bsource}C_{bsource} \tag{5.8}$$

It should be noted that Equation 5.8 is valid when the device is symmetric (i.e. source and drain are symmetric and the bulk contact surrounds the device symmetrically), which is usually the case in RF devices. This relationship is due to the material property of the lossy silicon substrate, dictated by

$$R_{sub}C_{sub} = \frac{\varepsilon_{si}\varepsilon_o}{\sigma_{si}} \tag{5.9}$$

where ε_{si} is the relative permittivity of silicon, ε_o is the permittivity of vacuum and σ_{si} is the average conductivity of silicon substrate. The derivation of this relationship of the lossy silicon substrate is shown in Appendix D. The product of the extracted substrate resistance and the extracted substrate capacitance (Figure 5.7d) shows the same conservative behavior, $\frac{\varepsilon_{si}\varepsilon_o}{\sigma_{si}}$, regardless of biasing conditions. The satisfaction of this relationship is a useful way to verify the extracted substrate parameters are consistent across for various bias conditions.

5.2 Source to Drain Coupling

The coupling effect between source to drain is characterized by y_{sdeff} parameter. The term ‘eff’ is added to distinguish it from intrinsic y_{sd}. The conductance and the capacitance of the y_{sdeff} can be expressed as:

$$y_{sdeff} = -g_{sdeff} - j\omega C_{sdeff} \tag{5.10}$$

The frequency response of the y_{sdeff} is characterized using a similar method as given in Equation 4.16, assuming the substrate resistance network is simplified as in Figure 4.12b. The internal node in b, $v_{b'}$, is expressed as:

$$v_{b'} = \frac{j\omega R_{sub} C_{bd}}{1 + j\omega R_{sub} C_{bb}} v_d \tag{5.11}$$

Since $v_{b'}$ forces additional current in source node, y_{sdeff} is expressed as:

$$y_{sdeff} = y_{sd} - \frac{g_{mb} v_{b's}}{v_d} \tag{5.12}$$

By substituting Equation 5.11 into Equation 5.12, the effective conductance and effective capacitance are:

$$C_{sdeff} = C_{sd} + \frac{R_{sub} g_{mb}}{1 + \omega^2 R_{sub}^2 C_{bb}^2} C_{bd} \tag{5.13}$$

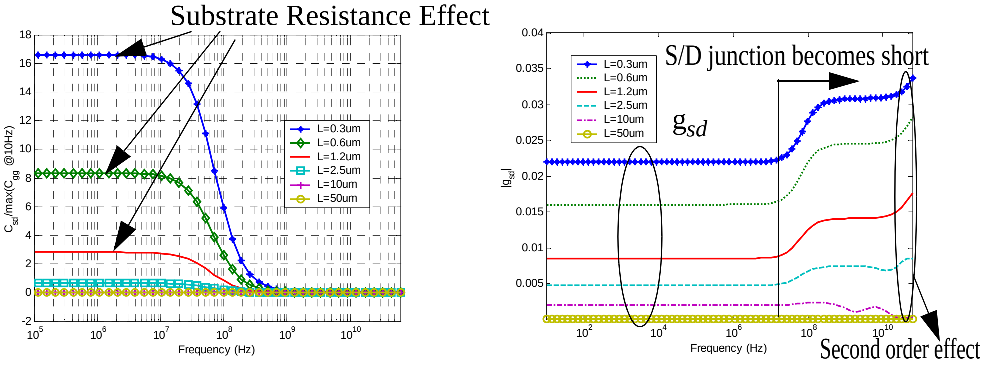


Figure 5.8. The frequency response of y_{sdeff} (C_{sdeff} and g_{sdeff}) when $V_{DS} = 3$ V and $V_{GS} = 3$ V.

$$g_{sdeff} = g_{sd} + \frac{\omega^2 R_{sub}^2 g_{mb}}{1 + \omega^2 R_{sub}^2 C_{bb}^2} C_{bb} C_{bd} \tag{5.14}$$

Both the C_{sdeff} and g_{sdeff} are amplified by g_{mb} due to the existence of the substrate resistance as in the case for C_{dseff}, C_{dbeff}, and C_{dgeff} in Section 4.5. Figure 5.8 shows the frequency response of C_{sdeff} and g_{sdeff} and agrees well with the expressions of Equation 5.13 and Equation 5.14 respectively. At low frequencies, the C_{sdeff} is positive multiple of C_{gg} and, at high frequencies where $\omega > \frac{1}{R_{sub} C_{bb}}$, C_{sdeff} approaches the intrinsic C_{sd}. The g_{sdeff} is the same as g_{sd} at low frequencies and starts to increase at $\omega = \frac{1}{R_{sub} C_{bb}}$. Also Figure 5.9 shows that at low frequency (10 Hz) the bias dependency of C_{sdeff} or C_{dseff} resembles that of g_{mb}, proving that they are in fact amplified by g_{mb}.

When $V_{DS} = 0$, g_{mb} becomes zero and the Equation 5.13 and Equation 5.14 reduces to:

$$C_{sdeff} = C_{sd} \tag{5.15}$$

$$g_{sdeff} = g_{sd} \tag{5.16}$$

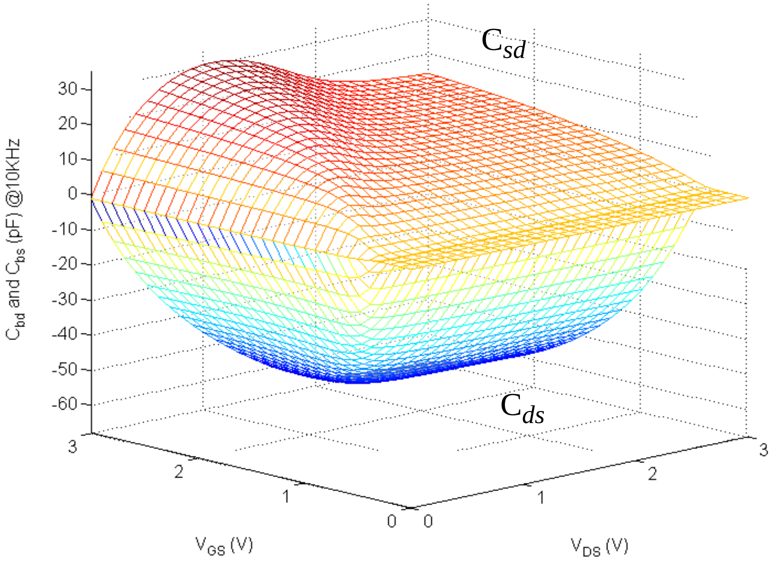


Figure 5.9. C_{sd} and C_{ds} at 10 KHz for L = 1.2 um device. Note that the bias dependency is proportional to g_{mb}.

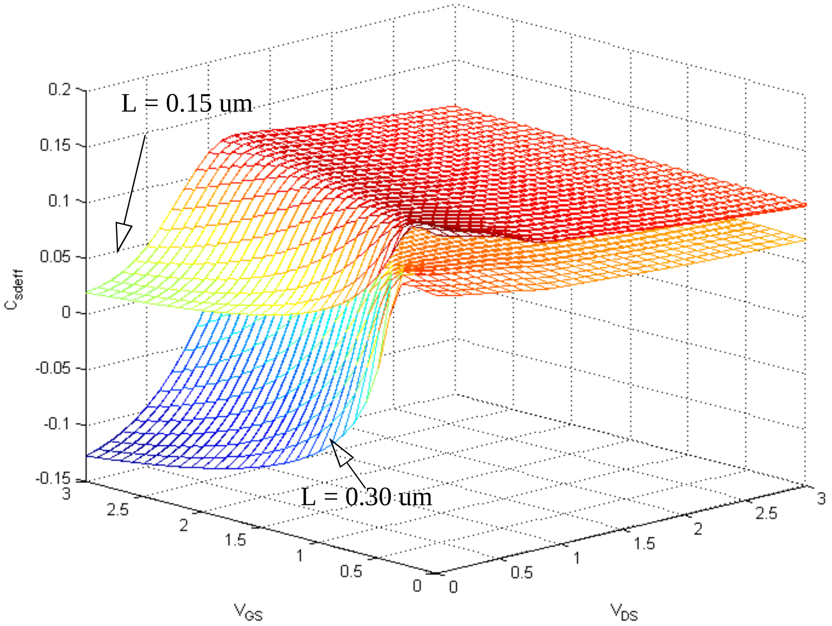


Figure 5.10. C_{sdeff} for L = 0.15 um and L = 0.3 um device at f = 10 GHz where the g_m amplification effect is absent. Note that the C_{sdeff} is positive in all biasing range for L = 0.15 um device due to the positive coupling capacitance.

Note that the intrinsic quantity C_{sd}, excluding the impact of s/d junction, is theoretically negative in non-saturation (in saturation, C_{sd} becomes zero) for long channel devices as in Appendix A. This is in agreement with measurements for long channel devices. The negative value can be viewed intuitively as follows. Raising the drain voltage by an amount dV_d will increase the effective reverse bias at the drain end and will cause the magnitude of the inversion layer charge (Q_I) to decrease. Since Q_I is negative, this means a change $dQ_I > 0$. This positive change in Q_I is shared by positive dQ_S and positive dQ_D. Hence, $C_{sd} = \frac{dQ_S}{dV_D}$ will be negative.

Figure 5.10 shows that the intrinsic term C_{sd}, which is negative for long channel device in the linear region, becomes positive as channel length decreases. It is reported in [26][80] that this is caused by DIBL effects. This work shows that this dependency is mainly a geometrical effect as source and drain become closer as illustrated in Figure 5.11 The C_{sd} is a summation of intrinsic term, C_{sdi}, through the channel and the extrinsic term, C_{sde}, under the channel as:

$$C_{sd} = C_{sdi} + C_{sde} \tag{5.17}$$

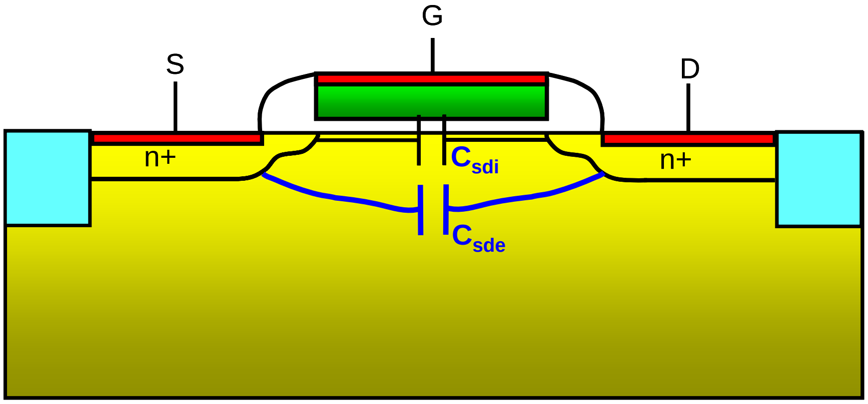


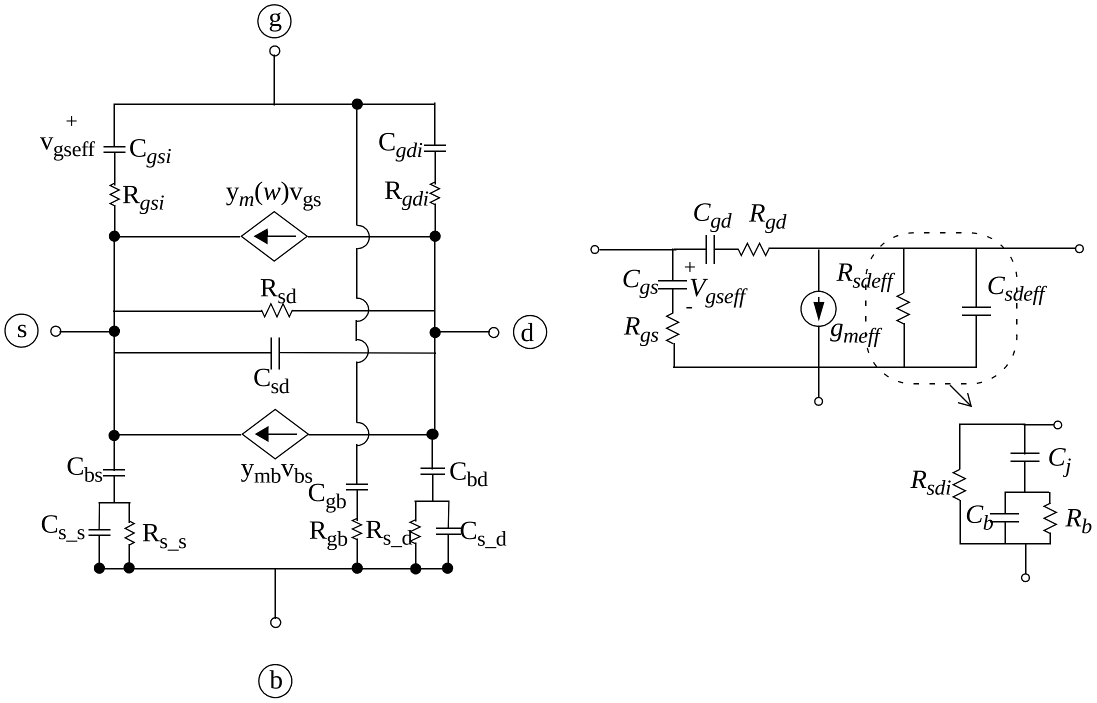
Figure 5.11. Small-signal equivalent circuit of source to drain coupling.

For long channel devices, since C_{sdi} is proportional to L, C_{sdi} dominates and as channel length decreases, the junction capacitance term, C_{sde}, between source and drain becomes comparable or greater than C_{sdi}, resulting in positive C_{sd}.

5.3 Simplified Compact Model of MOSFET in Common Source Configuration

Finally, the general four terminal y-parameter network of MOSFET shown in Figure 2.3 is represented as a circuit model shown in Figure 5.12a.

In the case of a common source configuration, the circuit model in Figure 5.8a is simplified as a 2-port network as shown in Figure 5.12b, where the frequency response of the substrate network and source to drain coupling are effectively modeled by R_{sdi}, C_j, C_b, and R_b. Note that C_{gb} and R_{gb} are lumped into C_{gs} and R_{gs} since they share the same frequency response when they dominate each other. Since source and bulk become effectively shorted out for common-source configuration, the y_{bs} term becomes zero. However the C_{sd}, R_{sd}, y_{bd}, and g_{mb} multiplication through R_{sub} need to be modeled for output characteristics. The impact of these parameters on output characteristics can be effectively modeled using the R_{sdi}, C_j, C_b, R_b, since they share an identical frequency response. This simplified compact model of the MOSFET in common-source configuration as shown in Figure 5.12b is quite useful for de-embedding extrinsic components since there are only a few parameters involved in modeling intrinsic behavior of MOSFET, as discussed in Chapter 8.



a) b)

Figure 5.12. a) general y-parameter network of MOSFET where y_{mx} is ignored. b) simplified compact model of MOSFET in common source configuration.

6 2-D Device Simulation of RF MOSFETS

Instead of extracting a small-signal model from measurements, the complete small-signal model of the intrinsic device is derived from physically-based simulations (e.g., 2-D device simulator using Atlas). This approach has a number of advantages, including the following:

- Possible errors resulting from measurements and extraction of extrinsic component are decoupled;
- It includes NQS effects, resulting in a good description of the electrical performance, even at frequencies beyond f_T;
- Direct comparison between the extracted parameters and simulated parameters is easily achieved.
- The modeling of capacitance is hampered by the fact that many of the MOS device capacitances cannot be easily measured even at low frequency.
- Through two-port s-parameter measurements, only four y-parameters (i.e., y_{gg}, y_{gd}, y_{dg}, and y_{dd}) are determinable. The other y-parameters such as y_{gs}, y_{gb}, y_{bd}, y_{bs}, y_{sd}, and y_{bg} are not identified.

Due to the above reasons, physical 2-D device simulation is employed in order to develop a physically acceptable small-signal model of RF MOSFET behavior.

6.1 2-D Process/Device simulation

Calibration of the process simulator is carefully done using SIMS (Secondary Ion Mass Spectroscopy) to generate a two-dimensional device structure as shown in Figure 6.1. I-V characteristics are also calibrated using mobility parameters in the Lombardi model [98], including semiconductor work function information.

Once the process recipe is calibrated, device structures with different channel lengths (L = 0.15 um, 0.3 um, 0.6 um, 1.2 um, 2.5 um, 10 um, and 50 um) are generated using the process simulator (TSUPREM IV).

In generating the structures with different channel length devices, the following factors are kept the same

- Thickness of gate stack (poly, gate oxide)
- The size of source/drain
- The mesh except channel region
- The vertical doping profile

The structures are assumed to be symmetric from the center of gate. The reason of employing symmetric structures with the same source/drain size for various channel length devices is to differentiate the impact of extrinsic parasitics (i.e source/drain and substrate) from the impact of channel length scaling on small-signal behavior.

The device simulator does not make a distinction between the intrinsic and parasitic parts of the device. To minimize the parasitic impact from the source/drain junctions on transistor characteristics, minimal source/drain size is used.

Also the IV characteristics of the simulated devices were examined to ensure appropriate physical dependency on channel length. For example, for the short channel device, L = 0.3 um, the drive current should have a linear dependency in saturation as V_{GS} increases while the long channel

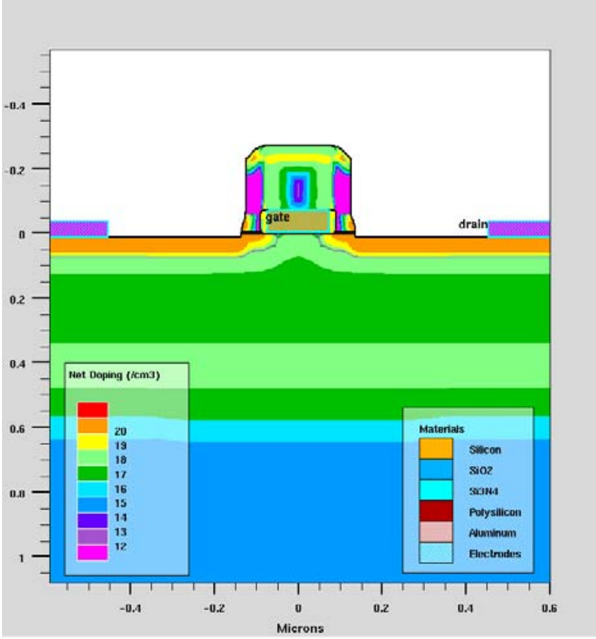


Figure 6.1. Cross section of simulated (calibrated) NMOSFET structure (L = 0.15 um).

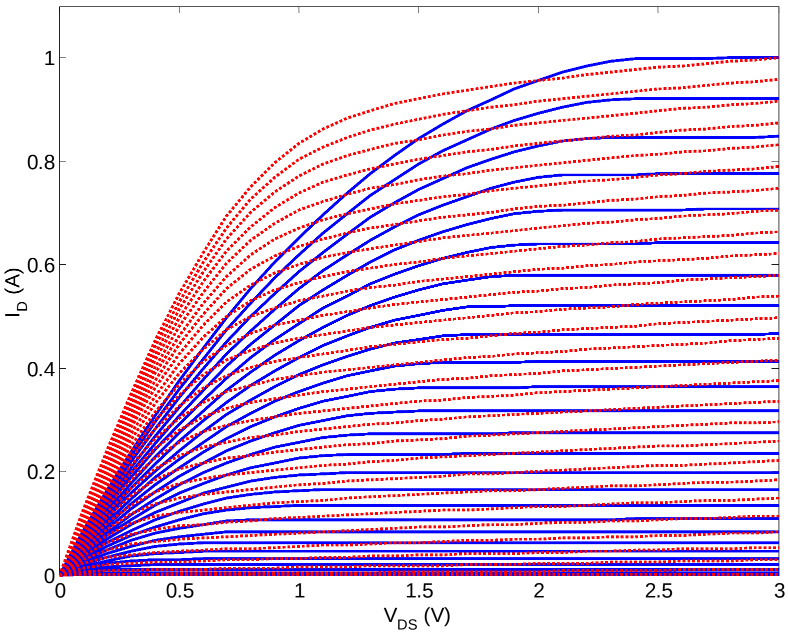


Figure 6.2. Simulated I_D vs. V_{DS} for short channel device (L = 0.3 um device dotted line), and long channel device (L = 50 um solid line). Note that I_D increases quadratically for the long channel device as V_{GS} increases and increases linearly for short channel device. V_{GS} is increasing with a step of 0.1 V and the I_D is normalized by the current at $V_{DS} = V_{GS} = 3$ V.

device should exhibit quadratic increase in drive current as shown in Figure 6.2. This is because for short channel length devices, the saturation current is limited by velocity saturation while for the long channel device, the saturation current is limited by pinch off as [31]:

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{gs} - V_t)^2 \qquad \text{for long channel} \tag{6.1}$$

$$I_D = WC_{ox}(V_{gs} - V_t)v_{sat}\left[1 + \frac{LE_{sat}}{V_{gs} - V_t}\right]^{-1} \qquad \text{for short channel} \tag{6.2}$$

For each DC bias condition, the small signal parameter, $y_{jk,}$ is defined as shown below.

$$-y_{jk} = g_{jk} + j\omega c_{jk} \tag{6.3}$$

To characterize the small-signal properties of the MOSFET, all the 4-terminal network parameters, y_{jk}, are simulated using 2-D device simulations for the bias range of 0 V < V_{GS} < 3 V, and 0 V < V_{DS} < 3 V. For each bias, the frequency is swept from 10 Hz to 64 GHz. The y_{jk} parameters are obtained by applying a small-signal voltage at the k^{th} terminal and detecting current at the j^{th} terminal while all other terminals are AC grounded with following relationship

$$y_{jk} = \frac{i_j}{v_k} \tag{6.4}$$

We shall adopt the convention in which the capacitance c_{xy} (or g_{jk}) is defined as $dxy \times \frac{\partial Q_x}{\partial V_y}$, where dxy is equal to 1 if $x = y$ and -1 if otherwise. The simulated y-parameters are checked to guarantee adherence to following relationships for all bias and across all frequencies:

$$y_{gg} = y_{dg} + y_{sg} + y_{bg} = y_{gd} + y_{gs} + y_{gb} \tag{6.5}$$

$$y_{dd} = y_{gd} + y_{sd} + y_{bd} = y_{dg} + y_{ds} + y_{db} \tag{6.6}$$

$$y_{ss} = y_{gs} + y_{ds} + y_{bs} = y_{sg} + y_{sd} + y_{sb} \tag{6.7}$$

$$y_{bb} = y_{gb} + y_{db} + y_{sb} = y_{bg} + y_{bd} + y_{bs} \tag{6.8}$$

For each of the y_{jk} parameters, the four sets of terminal capacitances and conductances, g_{gg}, g_{gs}, g_{gd}, g_{gb}, g_{dd}, g_{dg}, g_{ds}, g_{db}, g_{ss}, g_{sg}, g_{sd}, g_{sb}, g_{bb}, g_{bg}, g_{bd}, g_{bs}, c_{gg}, c_{gs}, c_{gd}, c_{gb}, c_{dd}, c_{dg}, c_{ds}, c_{db}, c_{ss}, c_{sg}, c_{sd}, c_{sb}, c_{bb}, c_{bg}, c_{bd}, are c_{bs}, are extracted for each frequency. The frequency response of the extracted parameters are plotted for the bias of V_{DS} = 0 V, V_{GS} = 3 V and V_{DS} = V_{GS} = 3 V in Appendix B.

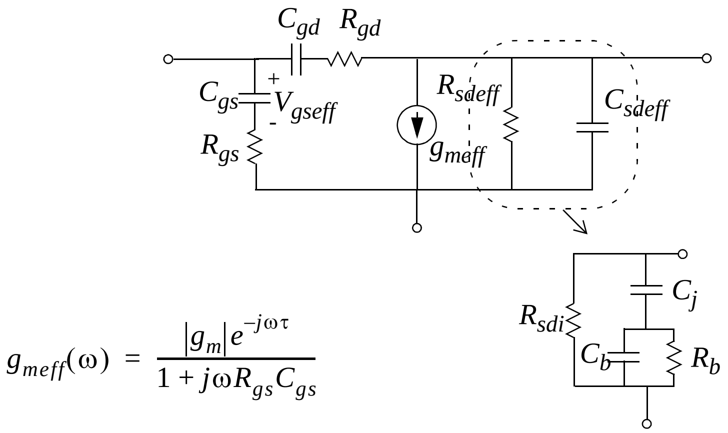
7 Extraction of Intrinsic Parameters

The MOSFET is a four-terminal device and requires three-port network parameters to completely describe the small-signal behavior. However, two-port s-parameter measurements are the only practical method to characterize the device at RF and therefore all four-terminal model parameters should be extracted from two-port s-parameter data.

Extraction of the parameters of the proposed model, shown in Figure 7.1, are necessary in order to model RF behavior of the device. The full set of parameters is extracted based on measured s-parameters. In this section, the deembedding of extrinsic parasitics is excluded, and its discussion deferred until Chapter 8.

7.1 Extraction of y_{gs} and y_{gd}

Given the y_{gs} parameter, extracting the series RC network, C_{gsi} and R_{gsi} shown in Figure 3.3 a), of the gate to source network is fairly straightforward as given by:



$$g_{meff}(\omega) = \frac{|g_m| e^{-j\omega\tau}}{1 + j\omega R_{gs} C_{gs}}$$

Figure 7.1. Common source configuration small-signal model of RF MOSFET. Note that g_{meff} is controlled by V_{gseff}.

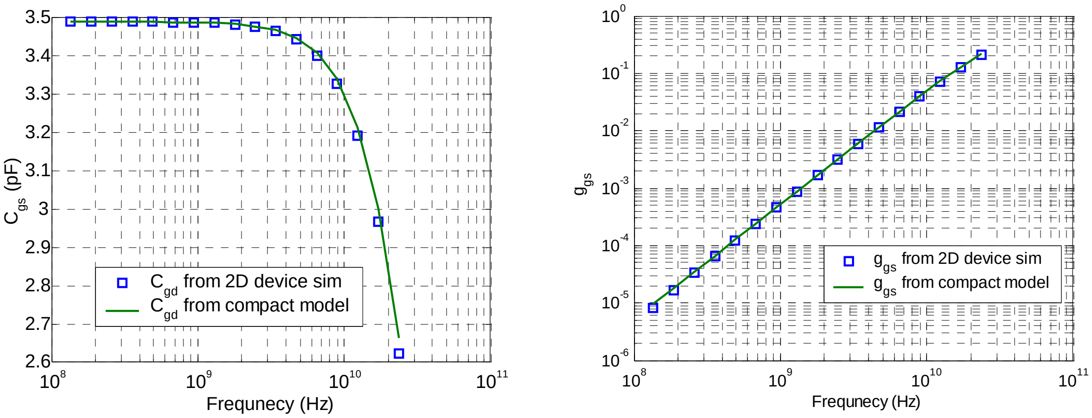


Figure 7.2. Frequency response of C_{gs} and g_{gs} from 2D device simulation and compact model for L = 1.2 um device at $V_{DS} = V_{GS} = 3$ V.

$$C_{gsi} = \frac{Im(Y_{gs})}{\omega}\left(1 + \frac{Re(Y_{gs})^2}{(Im(Y_{gs}))^2}\right) \tag{7.1}$$

$$R_{gsi} = \frac{Re(Y_{gs})}{(Im(Y_{gs}))^2 + (Re(Y_{gs}))^2} \tag{7.2}$$

Similarly for the gate to drain RC network,

$$C_{gdi} = \frac{Im(Y_{gd})}{\omega}\left(1 + \frac{Re(Y_{gd})^2}{(Im(Y_{gd}))^2}\right) \tag{7.3}$$

$$R_{gdi} = \frac{Re(Y_{gd})}{(Im(Y_{gd}))^2 + (Re(Y_{gd}))^2} \tag{7.4}$$

The frequency response of the terms C_{gs} and g_{gs} extracted from both the 2D device simulation and from the compact model using Equation 7.1 and Equation 7.2, are shown in Figure 7.2 with good agreement. Figure 7.3 shows the extracted parameters, C_{gsi}, C_{gdi}, R_{gsi}, and R_{gdi}, for the L = 0.12 um device. The C_{gsi} and C_{gdi} are identical to C_{gs} and C_{gd} at low frequency respectively.

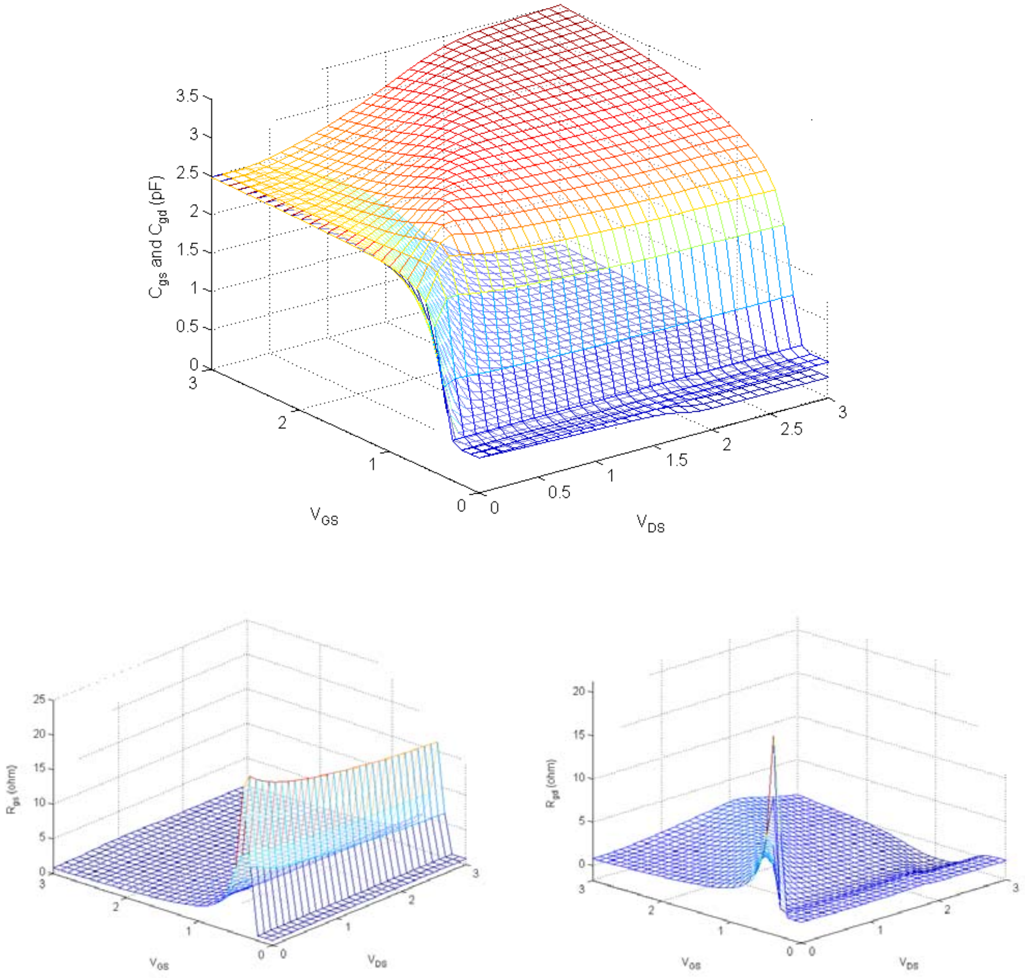


Figure 7.3. Extracted C_{gsi}, C_{gdi}, R_{gsi}, and R_{gdi}. The extraction is performed on L = 1.2 um device for the frequency range from 0.1 GHz to 20 GHz.

7.2 Extraction of y_{sd}

The source to drain coupling network in Figure 7.1 can be written in the form of conductance and capacitance as follows:

$$g_{sd} = \frac{1}{r_{sdi}} + \frac{\omega^2 r_b C_j^2}{1 + \omega^2 r_b^2 (C_b + C_j)^2} \tag{7.5}$$

(7.6)

$$= \frac{1}{r_{sdi}} + \frac{k_1\omega^2}{1 + k_2\omega^2} \tag{7.7}$$

$$C_{sd} = C_j\left[\frac{1 + \omega^2 r_b^2 C_b(C_b + C_j)}{1 + \omega^2 r_b^2 (C_b + C_j)^2}\right] \tag{7.8}$$

$$= C_j\left[\frac{1 + m_1\omega^2}{1 + m_2\omega^2}\right] \tag{7.9}$$

The parameters, k_1, k_2, m_1 and m_2, are used to simplify the equations; they are assumed to be frequency independent. Solving for R_{sdi}, R_b, C_j and C_b given y_{sd}, g_{sd} and C_{sd}, is not a simple matter. Some of the previous work [3][6] uses curve fitting or optimization methods. The curve fitting and optimization tends to generate less accurate results. An analytical method is described in following section.

7.2.1 Calculation of C_b, C_j, R_b and R_{sdi}

Given three data points, (ω_1, P_1), (ω_2, P_2), and, (ω_3, P_3) of y_{sd}, at a fixed bias condition, three unknowns, R_{sdi}, k_1, and k_2 of Equation 7.7, can be solved as follows:

$$k_2 = \frac{n_{12}l_{13} - n_{13}l_{12}}{n_{13}(p_1 - p_2) - n_{12}(p_1 - p_3)} \tag{7.10}$$

$$R_{sd} = \frac{n_{12}}{l_{12} + (p_1 - p_2)k_2} \tag{7.11}$$

$$k_1 = \frac{p_1}{\omega_1^2} + p_1 k_2 - \frac{k_2}{R_{sd}} - \frac{1}{R_{sd}\omega_1^2} \tag{7.12}$$

where P_1, P_2, and P_3 are *real parts* of y_{sd} corresponding to the frequency of ω_1, ω_2, and ω_3 respectively. Also the l and n are defined as,

$$l_{1j} = \frac{p_1}{\omega_1^2} - \frac{p_j}{\omega_j^2}, j = 2, 3 \tag{7.13}$$

$$n_{1j} = \frac{1}{\omega_1^2} - \frac{1}{\omega_j^2}, j = 2, 3 \tag{7.14}$$

Likewise, for the imaginary part of y_{sd}, the solutions of m_1, m_2, and C_j of Equation 7.7 are:

$$m_1 = \frac{z_{12}x_{13} - z_{13}x_{12}}{y_{12}z_{13} - y_{13}z_{12}} \tag{7.15}$$

$$C_j = \frac{z_{12}}{x_{12} + m_1 y_{12}} \tag{7.16}$$

$$m_2 = \frac{C_j}{Q_1 \omega^2_1} + \frac{m_1 C_j}{Q_1} - \frac{1}{\omega^2_1} \tag{7.17}$$

where

$$x_{1j} = \frac{1}{Q_j \omega^2_j} - \frac{1}{Q_1 \omega^2_1}, j = 2, 3 \tag{7.18}$$

$$y_{1j} = \frac{1}{Q_j} - \frac{1}{Q_1}, j = 2, 3 \tag{7.19}$$

$$z_{1j} = \frac{1}{\omega^2_j} - \frac{1}{\omega^2_1}, j = 2, 3 \tag{7.20}$$

where Q_1, Q_2, and Q_3 are *imaginary parts* of $\frac{y_{sd}}{\omega}$ corresponding to the frequency of ω_1, ω_2, and ω_3 respectively.

Finally R_b and C_b can be solved for using the following relationships:

$$R_b = \frac{k_2}{k_1}\left[1 - \frac{m_1}{m_2}\right]^2 \tag{7.21}$$

$$C_b = \frac{m_1 C_j}{m_2 - m_1} \tag{7.22}$$

This method works quite well for the 2-D device simulation case. However, in measured s-parameter data, the extraction might not be robust due to errors created by measurements. In that case, post processing of the extracted parameters for the every three frequency points is needed to enhance the accuracy of extraction.

7.3 Extraction of g_m and τ

Most of the variables can be determined by simple algebraic operations. To separate g_m and τ we have to use following equation:

$$Y_{21} = \frac{g_m\left|e^{-j\omega\tau}\right|}{1 + j\omega C_{gs}R_{gs}} - \frac{R_{gd}C_{gd}^2\omega^2}{D_{gd}} - j\omega\frac{C_{gd}}{D_{gd}} \tag{7.23}$$

This can be rewritten as

$$Y_{21} = \frac{g_m\left|e^{-j\omega\tau}\right|}{1 + j\omega C_{gs}R_{gs}} + Y_{12} \tag{7.24}$$

$$Y_{21} = \frac{g_m(1 - j\omega R_{gs})(cos((\omega\tau) - j sin(\omega\tau)))}{1 + R_{gs}^2 C_{gs}^2 \omega^2} + Y_{12} \tag{7.25}$$

We can separate the real and imaginary parts:

$$Re(Y_{21} - Y_{12}) = \frac{g_m(cos(\omega\tau) - \omega R_{gs}C_{gs}sin(\omega\tau))}{1 + R_{gs}^2 C_{gs}^2 \omega^2} \tag{7.26}$$

$$Im(Y_{21} - Y_{12}) = \frac{g_m(\omega R_{gs}C_{gs}cos(\omega\tau) - sin(\omega\tau))}{1 + R_{gs}^2 C_{gs}^2 \omega^2} \tag{7.27}$$

For simplification of the notation we use

$$R = Re(Y_{21} - Y_{12}) \tag{7.28}$$

$$I = Im(Y_{21} - Y_{12}) \tag{7.29}$$

$$\theta = \omega\tau \tag{7.30}$$

$$b = \omega C_{gs}R_{gs} \tag{7.31}$$

$$a = \frac{g_m}{1 + b^2} \tag{7.32}$$

Then we get

$$R = a(\cos\theta - b\sin\theta) \tag{7.33}$$

$$I = -a(b\cos\theta + \sin\theta) \tag{7.34}$$

Rewriting the above two equations

$$\cos\theta = \frac{R}{a} + b\sin\theta \tag{7.35}$$

$$\sin\theta = \frac{-I - bR}{a(1 + b^2)} \tag{7.36}$$

Now we can solve for a:

$$a = \sqrt{\frac{I^2 + R^2}{I + b^2}} \tag{7.37}$$

Finally by back-substitute the results in order to get we get g_m and τ .

7.4 Two-port y-parameters

In summary, the 2 port y-parameters can be represented as:

$$Y_{11} = \frac{R_{gs}C_{gs}^2\omega^2}{D_{gs}} + \frac{R_{gd}C_{gd}^2\omega^2}{D_{gd}} + j\omega\left(\frac{C_{gs}}{D_{gs}} + \frac{C_{gd}}{D_{gd}}\right) \tag{7.38}$$

$$Y_{12} = -\left(\frac{R_{gd}C_{gd}^2\omega^2}{D_{gd}} + j\omega\frac{C_{gd}}{D_{gd}}\right) \tag{7.39}$$

$$Y_{21} = \left(\frac{g_m\left|e^{-j\omega\tau}\right|}{1 + j\omega C_{gs}R_{gs}} - \frac{R_{gd}C_{gd}^2\omega^2}{D_{gd}} - j\omega\frac{C_{gd}}{D_{gd}}\right) \tag{7.40}$$

$$Y_{22} = \frac{R_{gd}C_{gd}^2\omega^2}{D_{gd}} + \frac{1}{R_{sdeff}} + j\omega\left(C_{sdeff} + \frac{C_{gd}}{D_{gd}}\right) \tag{7.41}$$

where

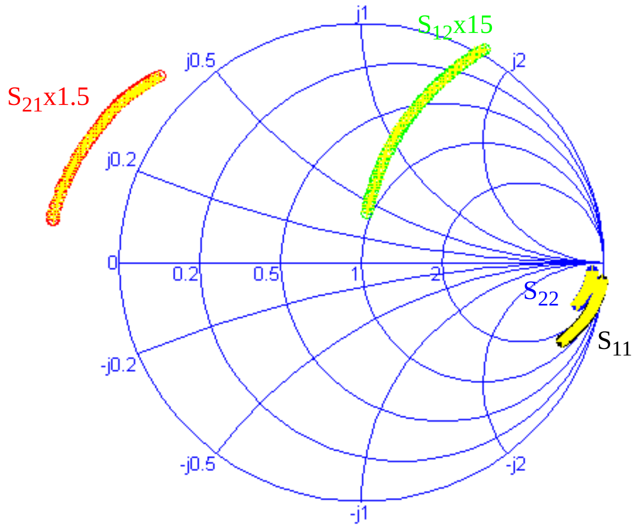


Figure 7.4. Measured s-parameters compared with constructed s-parameters from model (V_{DS} = 1.8 V, V_{GS} = 2.0 V). Model and measurements (yellow) agrees very well (from 0.5 GHz to 23 GHz).

$$D_{gs} = 1 + (\omega C_{gs} R_{gs})^2, D_{gd} = 1 + (\omega C_{gd} R_{gd})^2 \tag{7.42}$$

From the extracted parameters, the re-constructed s-parameters are compared with simulated s-parameters using following error function to validate the extraction process.

$$E_{i,j} = \frac{1}{4} \sum_{i,j=1}^{2} \left(\frac{1}{N} \sum_{n=1}^{N} \frac{|deviceS_{ijn} - extractedS_{ijn}|}{deviceS_{ijn}} \right) \cdot 100 \ \% \tag{7.43}$$

The errors using Equation 7.43 resulted in less than 2 % for all biasing regions, proving the validity of the compact model and extraction method. Figure 7.4 shows that measured s-parameters agree very well with s-parameters from model.

8 Extraction of Extrinsic Parameters

When dealing with small-signal equivalent circuits, the extraction of parameters is of great importance. The first problem is to de-embed the pad parasitics. These parasitics include everything between the calibration plane and the device. There are several ways to do this, and they all have their pros and cons in terms of simplicity, accuracy, and the type of devices that are being characterized.

The problem then is to extract the series impedances, which are the gate, drain, and source resistances and their corresponding wire inductances as visible in Figure 8.1. There are several different strategies to do this extraction. A method originating from the cold FET method used for MESFETs assumes that the intrinsic device is purely capacitive when the applied biases are zero. In this method, the series resistance is independent of bias and values are extracted only at one bias condition [72][75]. Other methods take the intrinsic part into account and extrapolate the curves to extract

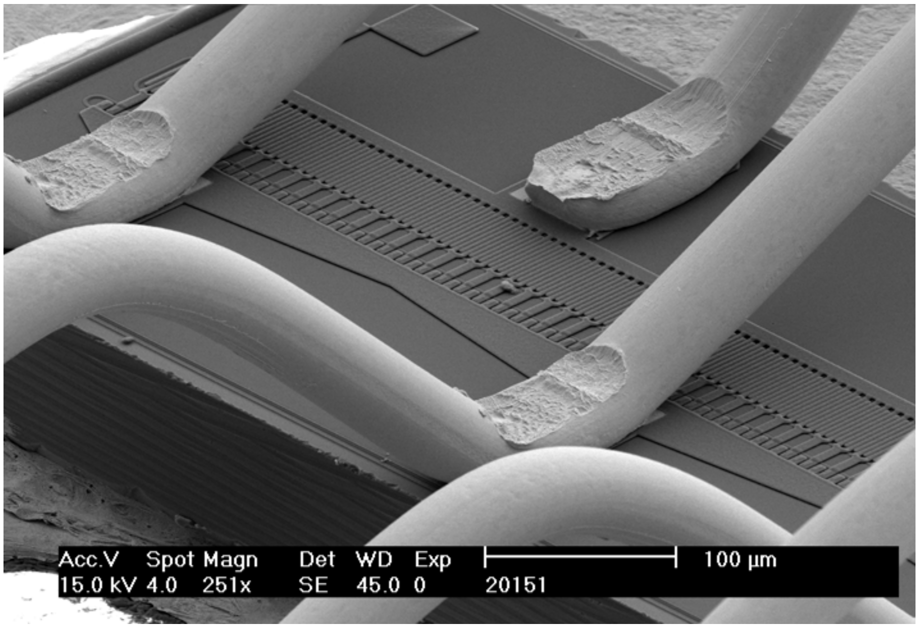


Figure 8.1. RF power device.

the series impedances, which can be done for each bias point [73][77]. This is made possible by approximating the intrinsic part until the expression becomes simple enough. However, errors in the approximation of the intrinsic device results in inaccuracies in extraction of parasitics. In this chapter, a new analytical extraction method for de-embedding the extrinsic parasitics is discussed. Excellent agreement for test cases has been obtained.

8.1 Calibration and Measurement

RF components are often characterized by using a vector network analyzer (VNA), which measures the vector ratio of reflected and transmitted energy components, relative to the energy incident upon the device under test (DUT) as shown in Figure 8.2.

One must define the electrical boundary where the measurement system ends and the DUT begins in the setup. This boundary is often called the “reference plane.” A reference plane can be established by measuring patterns with known electrical characteristics. This process is called calibration: short, open, matched load, and through (SOLT) for on-wafer calibration. There is also more advanced calibration methods -- through-reflect-line (TRL) and line-reflect-match (LRM)-- which provide more accurate calibration over SOLT for on-wafer probing [76][89]. The calibration patterns can be fabricated on the wafer together with the device being characterized or on an off-wafer calibration substrate called the impedance standard substrate (ISS), which has high-precision patterns for calibration. The ISS is usually fabricated on a specific material with low loss and

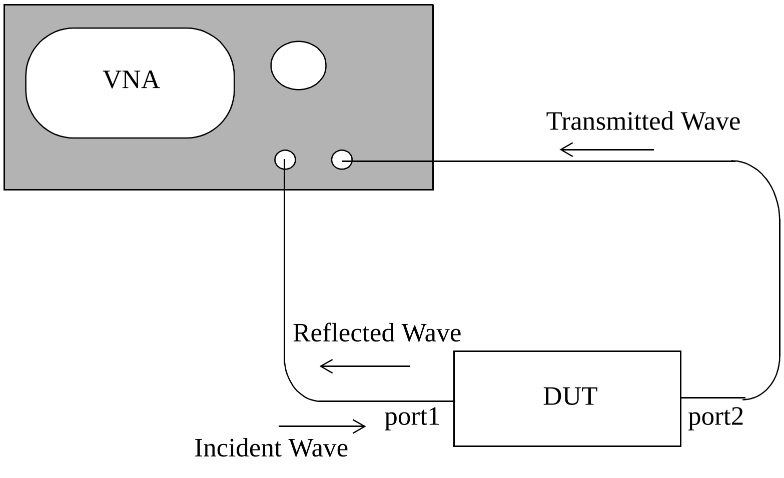
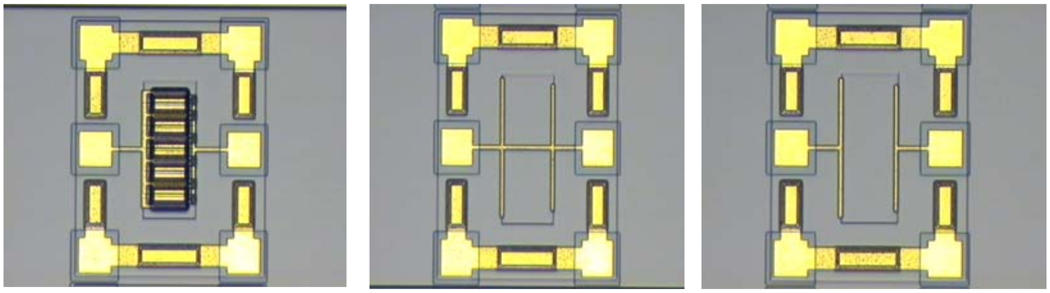


Figure 8.2. Two-port network analyzer measurements.



DUT Short Open

Figure 8.3. Device pattern and dummy patterns for s-parameter measurement and deembedding of pad parasitics.

smooth surface such as ceramic or sapphire. Since calibration is performed using probe tips, the reference plane can in fact be the probe tips. The setup measures the response of whatever is touching the probe tips, which are usually referenced to a standard level of 50 Ω after the calibration procedure.

The primary interest in RF probing for device characterization purposes is to characterize the intrinsic device for the purpose of modeling its behavior at GHz frequencies when embedded in an IC design environment. It is obvious that the intrinsic device in an IC design environment will not have probe pads attached to it except when used as a test structure. Therefore, the probe pad parasitic effects must be de-embedded from the measurement since a measurement on wafer with calibrated probe tips has the intrinsic device characteristics plus pad parasitics. The primary pad parasitics are in parallel with the pad structure. The idea is to be able to easily convert the measured s-parameters into y-parameters for an open set of pads and for the DUT with pads and subtract the y-parameters to de-embed the pad parasitics leaving the DUT characteristics.

The procedure to de-embed parasitics such as pad and interconnect using the short, open structures as shown in Figure 8.3 is generally considered to be accurate. Even after the standard de-embedding procedure, there are still extrinsic parasitics from the device itself (DUT in Figure 8.3), for example: source/drain contact resistance, gate resistance and local interconnect resistance. These resistances can impact the performance of the RF device significantly and need to be modeled carefully. The following sections will discuss the methodology to extract the frequency-independent extrinsic components.

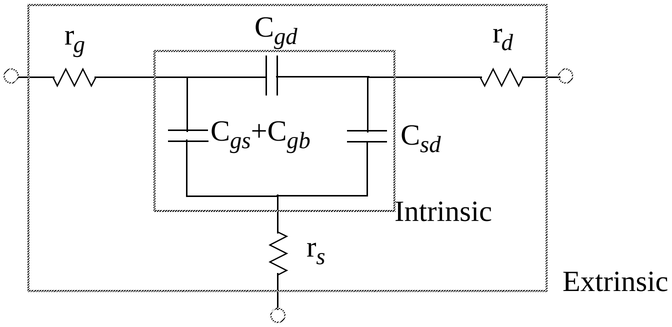


Figure 8.4. Zero bias ($V_{DS} = V_{GS} = 0$) small-signal equivalent circuit.

8.2 Conventional Extraction Method of Extrinsic Parameters

Direct extraction of the small signal model parameters for a silicon MOSFET have previously been hampered by the inability to directly determine the parasitic gate resistance value. The traditional GaAs FET parameter extraction methods utilize either DC measurements to establish all of the extrinsic resistance values or cold FET AC measurements [72]. These techniques cannot be used with the MOSFET because the gate is DC isolated from the remainder of the device.

D. Lovelace [75] proposed a new method for de-embedding parasitic resistance (r_g, r_d, and r_s) at zero bias condition ($V_{DS} = V_{GS} = 0$) assuming the intrinsic device model can be simplified as shown in Figure 8.4 by assuming $g_m = 0$, and $g_{sd} = 0$. Equations for the parasitic resistances of the model, as shown in Figure 8.4, are given by:

$$Re(z_{11}) = r_g + r_s \tag{8.1}$$

$$Re(z_{22}) = r_d + r_s \tag{8.2}$$

$$Re(z_{21}) = Re(z_{12}) = r_s \tag{8.3}$$

z_{11}, z_{22}, z_{21}, and z_{12} correspond to the z-parameters of the 2-port network at the zero-bias condition. To check the validity of the above equations used by Lovelace, intrinsic s-parameters are obtained from device simulation of the intrinsic device structure and then the known extrinsic resistances, r_g, r_s, and r_d, are added to the 2-port network. However, the extracted resistances, r_d, r_s, and r_g, using Lovelace's method result in frequency-dependent characteristic as shown in Figure 8.5.

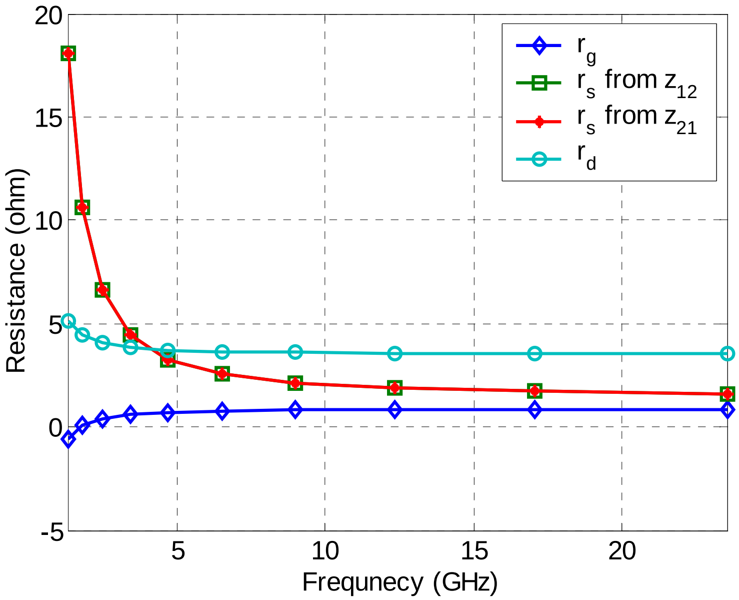


Figure 8.5. Example of the extracted parasitic resistance of the small-signal model (L = 1.2 um) using Lovelace's method. The extracted values are highly frequency dependent at low frequency (< 10 GHz) and the extracted values are not correct at any frequency. The correct resistances are: r_g = 1.00 ohm, r_d = 2.50 ohm, and r_s = 0.50 ohm while the extracted resistances at 23.5 GHz are: r_g = 0.86 ohm, r_d = 3.52 ohm, and r_s = 1.62 ohm.

This is due to the assumption that the intrinsic small-signal model at zero bias is purely capacitive. For example, the g_{sd} parameters can not be assumed to be zero at zero bias since the magnitude of g_{sd} depending on device size, which can be comparable to the capacitive parameters, $j\omega C_{gd}$, $j\omega C_{gs}$, *and* $j\omega C_{sd}$ at low frequencies. This can be overcome by increasing the frequency range for parasitic extraction to make the magnitude of capacitive term, $j\omega C$, dominant. However, as frequency increases, the conductance terms such as g_{gd}, g_{gs}, g_{gb} can no longer be ignored and all the capacitive elements become frequency dependent due to the NQS effect.

8.3 Extraction Method of Extrinsic Parasitics

Consider the generalized two-port network of MOSET as shown in Figure 8.6. The MOSFET is categorized as two networks as shown in Figure 8.6. One is the intrinsic network, denoted as z^i and the other group is the total network which includes extrinsic parasitics, denoted as z^t. The r_g corre-

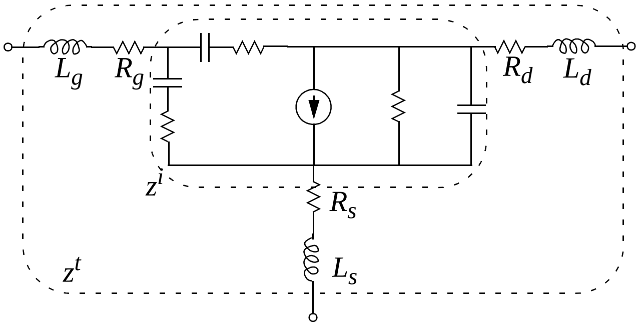


Figure 8.6. MOSFET with a generalized extrinsic component.

sponds to the distributed gate resistance; r_s and r_d are the source and drain resistances respectively. The two-port network of an intrinsic MOSFET can be written in general admittance form as:

$$y^i = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} G_{gg} + j\omega C_{gg} & -G_{gd} - j\omega C_{gd} \\ -G_{dg} - j\omega C_{dg} & G_{dd} + j\omega C_{dd} \end{bmatrix} \tag{8.4}$$

where

$$G_{gg} = G_{gd} + G_{gs} + G_{gb} = G_{dg} + G_{sg} + G_{bg} \tag{8.5}$$

$$G_{dd} = G_{dg} + G_{ds} + G_{db} = G_{gd} + G_{sd} + G_{bd} \tag{8.6}$$

$$G_{ss} = G_{sg} + G_{sd} + G_{sb} = G_{gs} + G_{ds} + G_{bs} \tag{8.7}$$

$$G_{bb} = G_{bg} + G_{bd} + G_{bs} = G_{gb} + G_{db} + G_{sb} \tag{8.8}$$

Note that C_{ij} *and* G_{ij} *are not the same as* C_{ji} *and* G_{ij} respectively. These non-reciprocal effects arise because the channel charge in a MOSFET is controlled by three or more bias voltages.

Assume that the device has a symmetric source and drain structure, which is true for most applications. Then due to the symmetry condition, $C_{gs} = C_{gd}$ and $G_{gs} = G_{gd}$. At $V_{DS} = 0$, $g_m = 0$. If we use the small-signal model for the intrinsic MOSFET developed in Chapter 5, the following relationships can be established:

$$y_{12} = -\frac{r_{gd} C_{gd}^2 \omega^2}{D_{gd}} - j\omega \frac{C_{gd}}{D_{gd}} = -A - j\omega B \tag{8.9}$$

$$y_{11} = \frac{r_{gs}C_{gs}^2\omega^2}{D_{gs}} + j\omega\frac{C_{gs}}{D_{gs}} - y_{12} \approx 2A + j\omega 2B \tag{8.10}$$

where

$$A = \frac{r_{gs}C_{gs}^2\omega^2}{D_{gs}} = \frac{r_{gd}C_{gd}^2\omega^2}{D_{gd}} \tag{8.11}$$

$$B = \frac{C_{gs}}{D_{gs}} = \frac{C_{gd}}{D_{gd}} \tag{8.12}$$

$$D_{gd} = D_{gs} = 1 + (\omega C_{gs} r_{gs})^2 = 1 + (\omega C_{gd} r_{gd})^2 \tag{8.13}$$

The gate-to-bulk terms, C_{gb} and G_{gb}, are ignored, assuming that V_{GS} is greater than V_{th}. As a result, Equation 8.4 becomes:

$$\begin{bmatrix} G_{gg} + j\omega C_{gg} & -G_{gd} - j\omega C_{gd} \\ -G_{dg} - j\omega C_{dg} & G_{dd} + j\omega C_{dd} \end{bmatrix} = \begin{bmatrix} 2A + j\omega 2B & -A - j\omega B \\ -A - j\omega B & g_{seff} + A + j\omega(C_{sdeff} + B) \end{bmatrix} \tag{8.14}$$

Now converting the above y^i parameters into z^i parameters using the parameter conversion table in Appendix C, the following z^i parameters are obtained:

$$\dot{z}^i = \begin{bmatrix} \dfrac{G_{sdeff} + A + j\omega(C_{sdeff} + B)}{D} & \dfrac{A + j\omega B}{D} \\ \dfrac{A + j\omega B}{D} & \dfrac{2A + j\omega 2B}{D} \end{bmatrix} \tag{8.15}$$

Where

$$D = \left| y_{11}^i y_{12}^i - y_{12}^i y_{21}^i \right|$$

$$= (A^2 + 2Ag_{sdeff} - \omega^2 2BC_{sdeff} - \omega^2 B^2) + j\omega(2AB + 2AC_{sdeff} + 2Bg_{sd})$$

$$= \left(\frac{\omega^4 C_{gd}^4 r_{gd}^2}{D_{gd}^2} + \frac{2\omega^2 C_{gd}^2 r_{gd} g_{sdeff}}{D_{gd}} - \frac{2\omega^2 C_{gd} C_{sdeff}}{D_{gd}} - \frac{\omega^2 C_{gd}{}^2}{D_{gd}^2} \right)$$

$$j\omega\left(\frac{2\omega^2 C_{gd}{}^3 r_{rd}}{D_{gd}^2} + \frac{2\omega^2 C_{sdeff} C_{gd}^2 r_{gd}}{D_{gd}} + \frac{2C_{gd} g_{sdeff}}{D_{gd}^2}\right) \tag{8.16}$$

Assuming V$_{GS}$ is at maximum (g$_{sdeff}$ increases), and by choosing a proper frequency range so that $D_{gd} \cong 1$, Equation 8.16 can be further reduced as follows,

$$D \approx \left|\omega^2(2C_{gd}^2 r_{gd} g_{sdeff} - 2C_{gd}C_{sdeff} - C_{gd}^2) + j\omega 2C_{gd} g_{sdeff}\right|$$

$$= \left|\omega^2 M + j\omega N\right| \tag{8.17}$$

subject to the constraints

$$M = 2C_{gd}^2 r_{gd} g_{sdeff} - 2C_{gd}C_{sdeff} - C_{gd}^2 \tag{8.18}$$

$$N = 2C_{gd} g_{sdeff} \tag{8.19}$$

Then the real part of the z^i parameter becomes:

$$Real(z^i) = \begin{bmatrix} \frac{g_{sdeff}M + (C_{sdeff} + B)N}{\omega^2 M^2 + N^2} & \frac{AM + BN}{\omega^2 M^2 + N^2} \\ \frac{AM + BN}{\omega^2 M^2 + N^2} & \frac{2AM + 2BN}{\omega^2 M^2 + N^2} \end{bmatrix} \cong \begin{bmatrix} \frac{g_{sdeff}M + (C_{sdeff} + B)N}{\omega^2 M^2 + N^2} & \frac{BN}{\omega^2 M^2 + N^2} \\ \frac{BN}{\omega^2 M^2 + N^2} & \frac{2BN}{\omega^2 M^2 + N^2} \end{bmatrix} \tag{8.20}$$

The approximation to the right side term in Equation 8.20 results from the assumption that $AM \ll BN$ by choosing a frequency range well below f$_{NQS}$ at the given bias condition. Similarly, the imaginary part of the z^i parameter becomes:

$$Imag(z^i) = \begin{bmatrix} \frac{-\omega g_{sdeff}N}{\omega^4 M^2 + \omega^2 N^2} & \frac{\omega\left(BM - R_{gs}C_{gs}^2 N\right)}{\omega^2 M^2 + N^2} \\ \frac{\omega\left(BM - R_{gs}C_{gs}^2 N\right)}{\omega^2 M^2 + N^2} & \frac{2\omega\left(BM - R_{gs}C_{gs}^2 N\right)}{\omega^2 M^2 + N^2} \end{bmatrix} \tag{8.21}$$

By adding extrinsic parameters to z^i, the total network z^t is:

$$z^t = \begin{bmatrix} z^t_{11} & z^t_{12} \\ z^t_{21} & z^t_{22} \end{bmatrix} = \begin{bmatrix} z^i_{11} + r_g + r_s + j\omega(l_g + l_s) & z^i_{12} + r_s + j\omega l_s \\ z^i_{21} + r_s + j\omega l_s & z^i_{22} + r_d + r_s + j\omega(l_d + l_s) \end{bmatrix} \tag{8.22}$$

Each element in Equation 8.22 can be simplified to have the following format:

$$\begin{aligned} Real(z^t_{ij}) &= r + \frac{C_1}{\omega^2 + B_1} \\ \frac{Imag(z^t_{ij})}{\omega} &= l + \frac{C_2}{\omega^2 + B_2} \end{aligned} \tag{8.23}$$

where B_1, B_2, C_1 and C_2 are frequency-independent constants and r and l are the extrinsic resistance and inductance need for the de-embedding process. By analyzing the frequency response of the two port networks, z^t, desired extrinsic components, r_s, r_d, r_g, l_s, l_d, and l_g, can be extracted.

Assuming r, B, and C are frequency-independent constants, extrinsic resistances can be analytically solved for, given three data points (ω_1, z_1), (ω_2, z_2), and (ω_3, z_3) at a fixed bias. where ω_1, ω_2, and ω_3 are the applied frequencies and z_1, z_2, and z_3 are the real part of z^t parameters. The solution for the extrinsic parameter, r given the three data points is:

$$r = \frac{(z_2 - z_1)(z_1\omega_1^2 - z_3\omega_3^2) + (z_1 - z_3)(z_1\omega_1^2 - z_2\omega_2^2)}{(z_2 - z_1)(\omega_1^2 - \omega_3^2) + (z_3 - z_1)(\omega_2^2 - \omega_1^2)} \quad . \tag{8.24}$$

Similarly, the extrinsic inductances can be analytically solved given three data points (ω_1, z_1), (ω_2, z_2), and (ω_3, z_3) at a fixed bias, where ω_1, ω_2, and ω_3 are the applied frequencies and z_1, z_2, and z_3 are the imaginary part of z^t/ω. The solution for the extrinsic parameter l, given the three data points, is:

$$l = \frac{(z_2 - z_1)(z_1\omega_1^2 - z_3\omega_3^2) + (z_1 - z_3)(z_1\omega_1^2 - z_2\omega_2^2)}{(z_2 - z_1)(\omega_1^2 - \omega_3^2) + (z_3 - z_1)(\omega_2^2 - \omega_1^2)} \quad . \tag{8.25}$$

The extracted extrinsic parameter r_d using Equation 8.24 is shown in Figure 8.7, which results in bias dependent extracted values. In general, extrinsic parasitics from the metal lines, vias, and contacts shows little bias dependency. The bias dependency is due to the fact that Equation 8.24 and Equation 8.25 are derived assuming V_{GS} is maximum and $V_{DS} = 0$. From Figure 8.7, when V_{DS} =

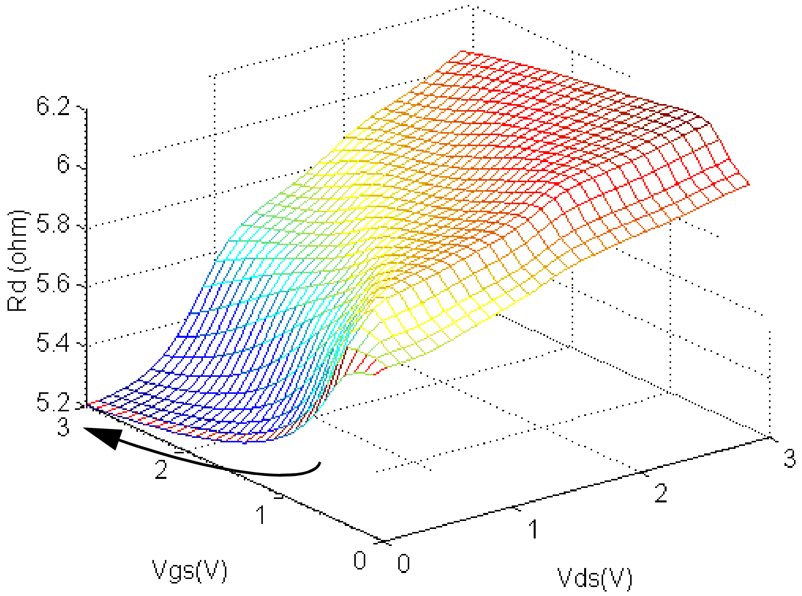


Figure 8.7. Extracted extrinsic parameter, r_d using Equation 8.24. Note that the extracted parameters are bias dependent. The correct r_d should be when V_{GS} = MAX, and $V_{DS} = 0$.

0, as V_{GS} increases the extracted value converges toward the expected limiting case value. Since it is difficult to increase V_{GS} without breaking down the gate oxide, non-linear curve fitting is used to estimate the expected value at infinite V_{GS}. The estimated value is achieved by finding the asymptotic value using a simple linear function:

$$r_{extracted}, l_{extracted} = E_{expected} + \frac{X_1}{V_{gs}^P + X_2} \tag{8.26}$$

X_1, X_2 are fitting parameters and $E_{expected}$ is the desired asymptotic value. P is the power-law term: $P = 0.5$ for the resistance component; $P = 1.7$ for the inductance term. Each give a good estimation of asymptotic values. Figure 8.8 shows all resistances and inductances extracted using this simple non-linear fitting method. It is verified through device simulation that this method is accurate and achieves error less than 2 %.

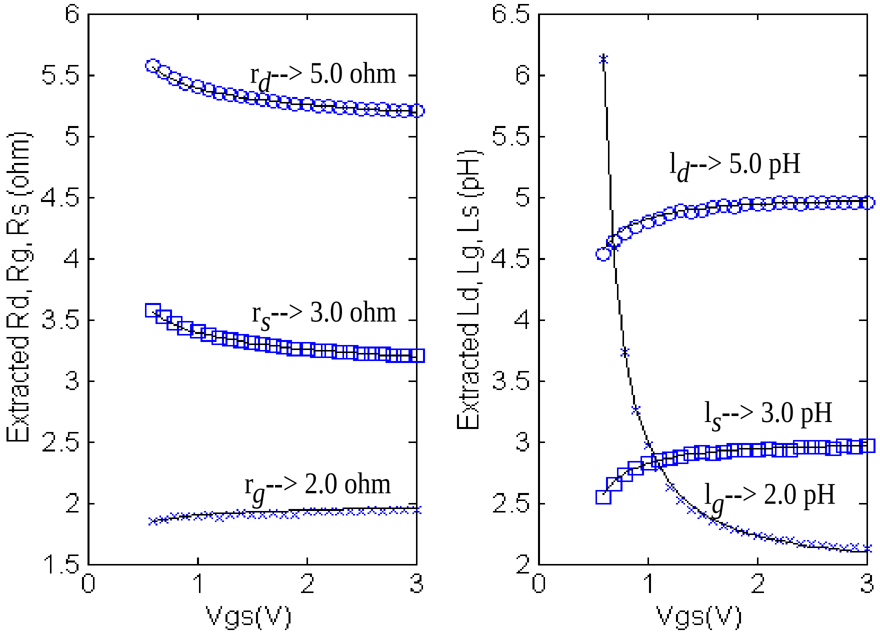


Figure 8.8. Non-linear curve fitting (line) of extracted extrinsic parameters (symbol) at $V_{DS} = 0$ from 0.13 um MOSFET. The $E_{expected}$ for r_d, r_s, and r_g are 5 Ω, 3 Ω, and 2 Ω respectively. The $E_{expected}$ for l_d, l_s, and l_g are 5 pH, 3 pH, and 2 pH respectively.

9 RF LDMOS Characterization and Its Compact Modeling

This Chapter presents characterization using device simulation and analytical modeling of power LDMOS devices. The unique features of the LDMOS such as graded channel and quasi-saturation effects result in a peculiar behavior of capacitance and non-linear LDD resistance. These effects are analyzed and modeled using advanced device simulation. A compact model for the LDMOS is implemented in HSPICE in combination with a BSIM3 MOSFET model.

9.1 Introduction

Radio Frequency (RF) communication systems have created a demand for cost effective, linear, high-gain RF power transistors for application in base station transmitter power amplifiers. Peak power requirements from the transmitter power amplifier can be as high as 120 Watts in single carrier applications and typically these amplifiers are operated from a 24-28 Volt power supply. This power level can be achieved by placing several transistors in parallel, while minimizing the number of power devices in both the final stage and the driver stages, which can improve system reliability and cost. Silicon technology has evolved to meet this need with the development of sub-micron LDMOS device structures that include special features which enhance performance for RF applications.

Optimal design of high-voltage integrated circuits requires physical LDMOS models implemented in a circuit simulator like SPICE. Several physically based models of LDMOS have been developed [91] ~ [93], but a complete physical model is still lacking. This chapter considers a detailed simulation study of the physical operation in terms of quasi-saturation behavior of a LDMOS device using Atlas [101]. From the characterization and analysis, an analytical model is derived in connect with parameterization of a conventional SPICE MOSFET model.

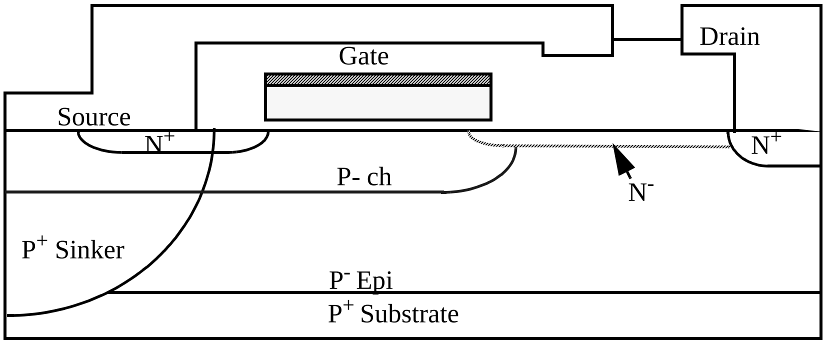


Figure 9.1. Cross section of LDMOS.

9.2 Intrinsic Device Structure

LDMOS devices offer significant performance enhancements for RF applications. Figure 9.1 shows the cross-section of the basic LDMOS structure. A laterally diffused p^+ graded channel implant enhances the RF gain and prevents punch-through at high drain-source voltages. The n^+ source is strapped to a p^+ sinker region by a source contact; the p^+ sinker is diffused to connect to the p^+ substrate, which is itself bounded to the RF ground, thus minimizing common lead inductance and maximizing common source amplifier RF gain. Both resistance and inductance in the source path can contribute to negative feedback and degrade power gain. Drain-source breakdown voltage is controlled by the lightly doped drain extension. R_{ds} (on) is also partially controlled by the doping level in the drain extension while a positive temperature coefficient for R_{ds} (on) contributes to the excellent reliability of this device structure under output mis-matched conditions. The device also includes a metal field shield at the edge of the gate, thus increasing the breakdown voltage and reducing C_{dg}.

9.3 Modeling of Intrinsic Device Using Device Simulation

The device structure for simulation (shown in Figure 9.2) was created using an advanced process simulator where the actual process recipe used for wafer fabrication serves as the input. The device structure is represented as a 2-D discretized grid and the device simulator was then used to simu-

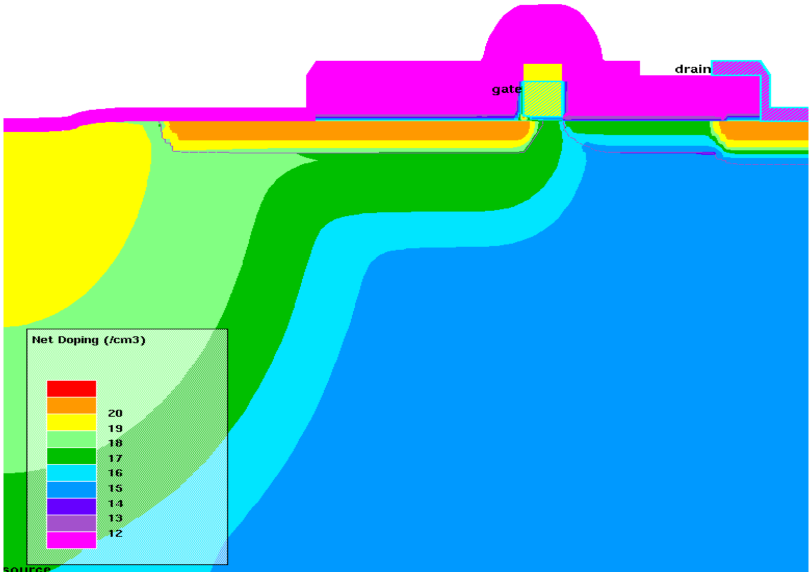


Figure 9.2. Cross section of LDMOS from process simulation.

lated the DC characteristics. Minor changes in the doping profiles were necessary to obtain good agreement between the measured and simulated value of V_{th} (4.3 V).

Modeling of the intrinsic device focuses on selecting a suite of models that represents the physics in the device [99]. For the LDMOS structure the following basic models are required: concentration dependent Shockly-Read-Hall recombination; Auger recombination; and band gap narrowing. The recombination processes model the regions that are heavily doped and the areas that can have a high concentration of carriers (i.e. the channel region.) The band gap narrowing model addresses the energy bands in the heavily doped N^+ source and P^+ substrate.

The mobility models are the single most important parameter set that affect simulation accuracy. The Lombardi (CVT) model is selected because it provides excellent modeling of the inversion layer in MOSFET’s [98]. it is given by

$$\frac{1}{\mu} = \frac{1}{\mu_b} + \frac{1}{\mu_{ac}} + \frac{1}{\mu_{sr}} \tag{9.1}$$

The model contains parameters for degradation due to surface acoustical phonon scattering:

$$\mu_{ac} = \frac{B}{E_\perp} + \frac{\alpha N^\beta}{T_L E_\perp^{1/3}} \tag{9.2}$$

and surface roughness scattering:

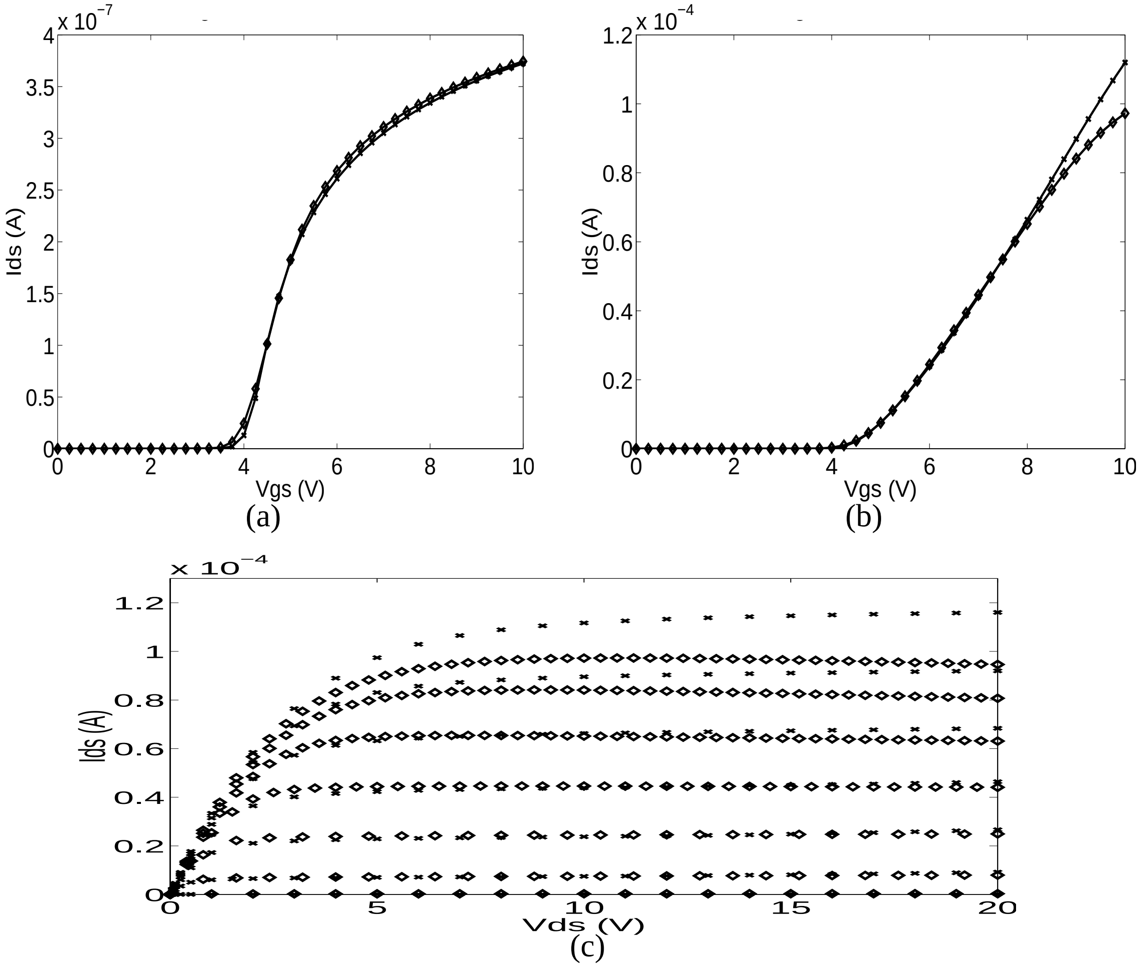


Figure 9.3. Comparison between measurements and device simulation. (a) I_{DS} vs. V_{GS} at V_{DS} = 0.01 V (b) I_{DS} vs. V_{GS} at V_{DS} = 10.0 V. (c) I_{DS} vs. V_{DS} for V_{GS} = 4 - 10 V. Note that at high gate and high drain bias, there is discrepancy between measurement and simulation. This is because self-heating is not modeled in device simulation.

$$\mu_{sr} = \frac{\delta}{E_{\perp}^{2}} \tag{9.3}$$

as well as a bulk mobility value μ_b. Surface phonon scattering and surface roughness scattering are dependent upon the transverse electric field $E_{\perp}$, doping concentration N, lattice temperature T_L, and material parameters (α, β, B, δ). The transverse field component is important because of the high gate biases that occur in RF power applications.

In addition to the transverse fields, the longitude field (i.e. parallel to current flow in the channel $E_{\|}$) leads to a reduction in the mobility of carriers given by

$$\mu = \frac{\mu_0}{\left[1 + \left(\frac{E\|\mu_0}{v_{sat}}\right)^{\beta}\right]^{\frac{1}{\beta}}} \qquad (9.4)$$

The principal component comes from saturation of the carrier velocities (v_{sat}) flowing from the source to drain as well as a material-dependent factor β. The carriers experience high longitude electric fields throughout the channel because of the graded doping profile.

First, the transverse mobility parameters are calibrated at low drain bias throughout the gate bias range as shown in Figure 9.3. Second, longitudal mobility parameters are calibrated at high drain bias as shown in Figure 9.3 (b). Figure 9.3 (c) shows comparison between measurements and device simulation for I_{DS} vs. V_{DS}. The deviation at high gate bias and negative resistance of measured data originates from self heating effects [97].

9.4 Modeling of Quasi-Saturation in LDMOS

High voltage LDMOS transistors exhibit a limitation in the current level that can be attained. This is manifested in the high output conductance and the insensitivity to the increase in the gate voltage at high current levels as shown in Figure 9.4.

It has been shown that this effect is due to carrier velocity saturation induced by the high electric field, and to low impurity concentrations in the drift layer (lightly doped drain region) [91].

To understand the underlying physics in detail, device simulation is performed using a calibrated LDMOS structure. Figure 9.5a (at pre quasi-saturation) and Figure 9.5b (at quasi-saturation) show the distribution of lateral electric fields along the channel and drift region for various

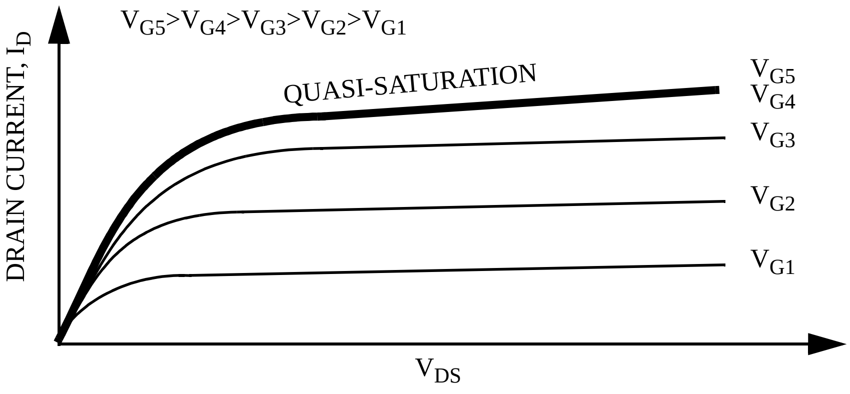
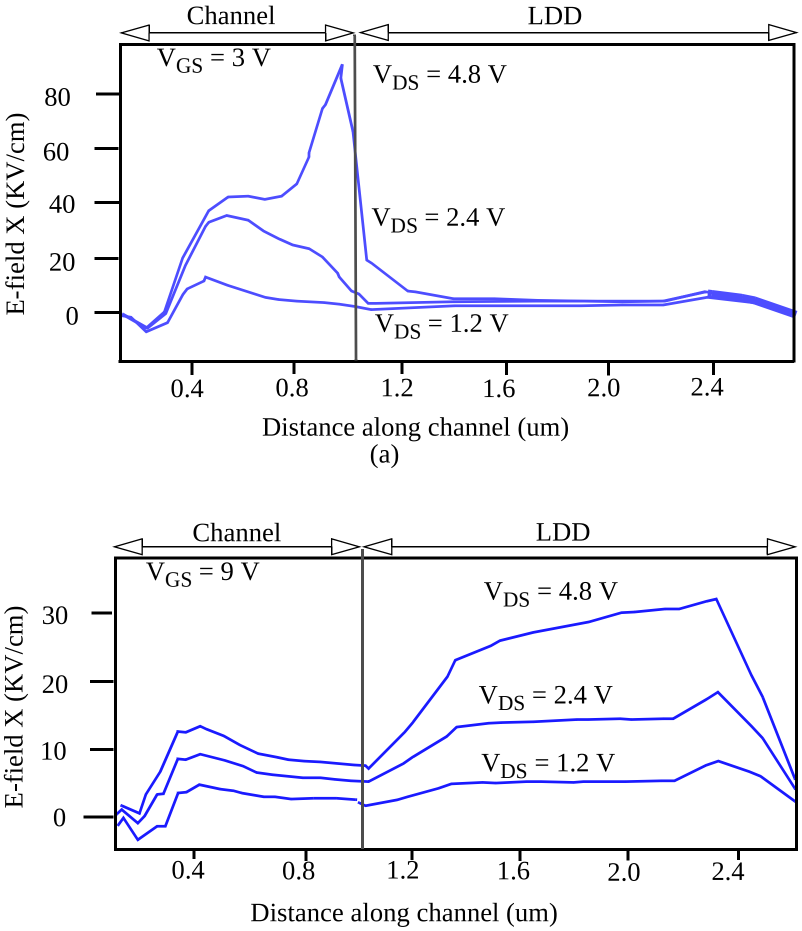


Figure 9.4. Quasi-saturation of LDMOS cross section of LDMOS.



(a)

(b)

Figure 9.5. Electric field along channel and LDD, a) at pre quasi-saturation and b) at quasi-saturation.

drain bias. At pre-quasi-saturation, the electric field peaks inside the channel region and at V_{DS} = 4.5 V, drain current starts to saturate. However as the device moves into quasi-saturation, the electric field peaks inside drift region and the channel current is no longer saturated.

By solving Poisson's equation along the drift region using simulated electron concentrations at quasi-saturation and by solving channel current equation, the non-linear resistive behavior of the drift region is formulated. Let's assume that the LDMOS device is operating in the linear region and the current equation for the channel is given by

$$I_D = \mu \cdot C_{ox}\frac{W}{L_s}\left[(V_{GS}-V_T)\cdot(\Psi_{ch}-V_S)-\frac{1}{2}(\Psi_{ch}-V_S)^2\right] \tag{9.5}$$

Where ψ_{ch} is drain side channel voltage. In the drift region, the current becomes velocity-saturated as given by:

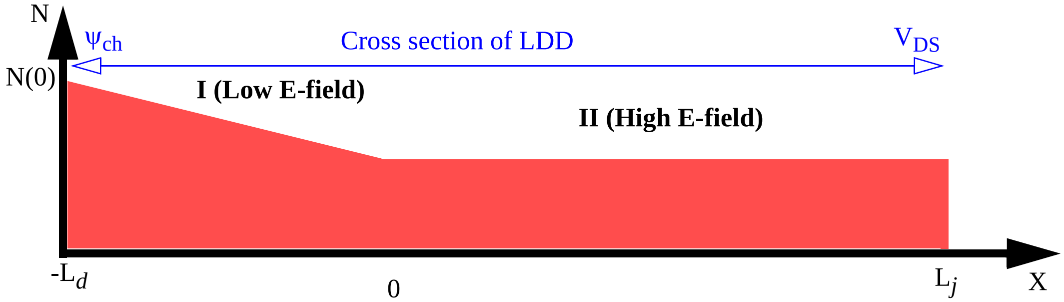


Figure 9.6. Simplified electron concentration along LDD based on device simulation.

$$I_D = N(0)qWl\upsilon_d(0) \tag{9.6}$$

The drift region is divided in two regions as low e-field and high e-field region as shown in Figure 9.6. Poissons equation in Region I (Low electric field) is given by:

$$\Psi(L_d) - \Psi(0) = \frac{q}{2\varepsilon}[N(0) - N_D]L_d^2 + E(0)L_d \tag{9.7}$$

and in Region II (high electric field) is given by:

$$\Psi(0) - \Psi_{ch} = -\frac{q}{2\varepsilon}[N(0) - N_D]L_j^2 + q\frac{k}{6\varepsilon}L_j^3 + E(0)L_j \tag{9.8}$$

By solving Equation 9.5 through Equation 9.8, the drain side channel voltage is expressed as a function of V_{GS} and V_{DS} and is given by:

$$\boxed{\Psi_{ch} = V_{GS} - V_{TS} + \frac{1}{BC} - \sqrt{\left(V_{GS} - V_T + \frac{1}{BC}\right)^2 - \frac{2(V_{DS} + A)}{BC}}} \tag{9.9}$$

where,

$$A = \frac{q}{2\varepsilon}N_D[L_d^2 - L_j^2] + q\frac{k}{3\varepsilon}L_j^3 + q\frac{k}{2\varepsilon}L_j^2L_d + \frac{q}{\varepsilon}N_DL_j(L_d + L_j) \tag{9.10}$$

$$B = \frac{q}{2\varepsilon}(L_d^2 - L_j^2) + \frac{q}{\varepsilon}L_j(L_d + L_j) \tag{9.11}$$

$$C = \frac{\mu C_{ox}}{qlv_sl_s} \tag{9.12}$$

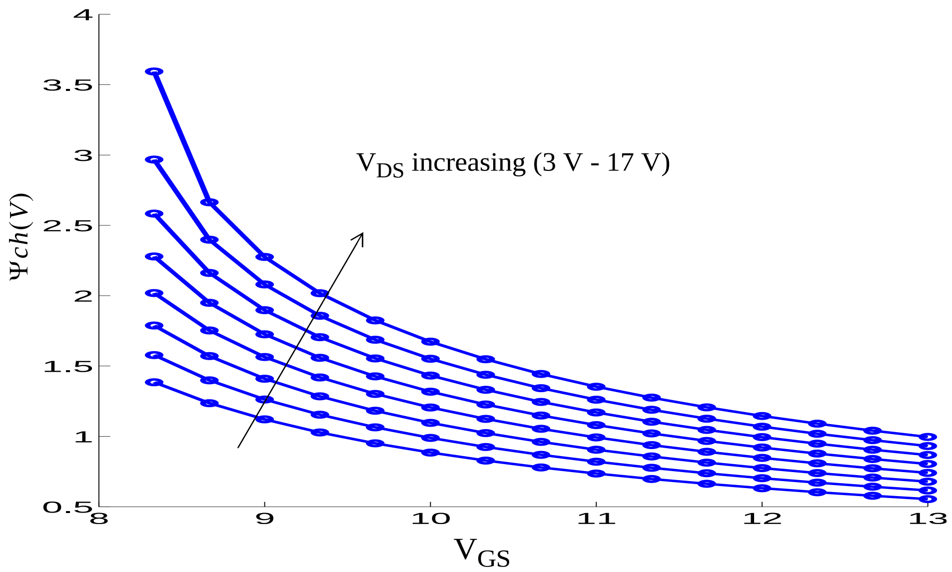


Figure 9.7. Drain side Channel voltage vs. V_{GS} for V_{DS} (3 - 17 V, step = 2 V) using analytical equation given in Equation 9.9.

N_D denotes doping concentrations in the LDD region, and k, L_j, L_d, l, and l_s are geometry parameters of the channel and the LDD regions, respectively. Figure 9.7 shows the behavior of ψ_{ch} in the quasi-saturation region using the Equation 9.9. When the gate bias increases, the drain side channel voltage decreases for the same drain bias, which means that current is limited by velocity saturation in the drift region.

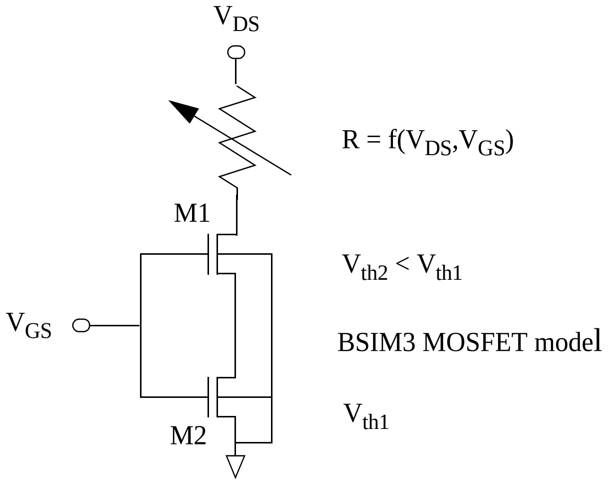


Figure 9.8. Large-signal equivalent circuit of the LDMOS.

9.5 Large-Signal Model

From a comparative study between LDMOS and MOSFET, the channel region is modeled using two MOSFET devices with different channel doping levels to account for the effect of a graded channel; the drift region is modeled using a non-linear resistor as a function of V_{GS} and V_{DS} to account for the quasi-saturation behavior as shown in Figure 9.8.

Using Equation 9.9 and device simulation, an effective resistive value is extracted as shown in Figure 9.9. For increasing gate bias the non-linear behavior of the LDD region increases. At low gate bias, the LDD region shows a small bias dependence but the resistance increases with V_{DS}, due to reduction of the effective conduction area owing to depletion between the bulk and LDD region The largest dynamic resistor (dV/dI) value occurs when drain current becomes insensitive to the gate bias increase.

To model these DC characteristics in SPICE, the low gate and low drain bias regions are first calibrated using measurements since in those regions the non-linear behavior of the LDD region is negligible. After calibration, the non-linear resistor is implemented using a voltage-controlled resis-

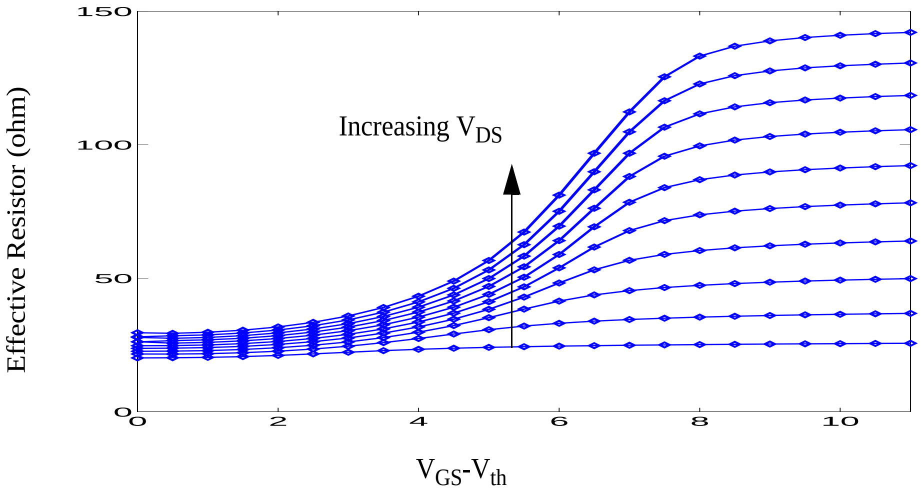


Figure 9.9. V_{GS}-V_{th} vs. effective resistor of LDD for V_{DS} = 2 - 20 V.

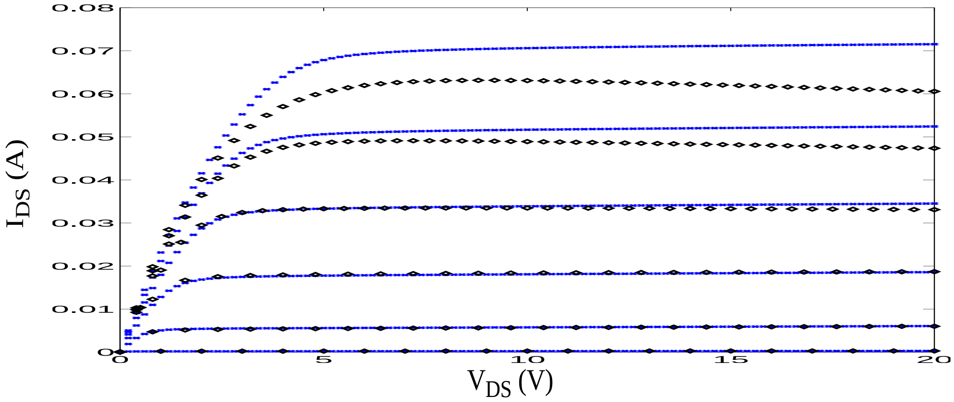


Figure 9.10. Comparison between measurement and SPICE simulatation of I_D vs. V_{DS} for V_{GS} = 4 - 9 V (o: measured, x: simulated).

tor in SPICE. Figure 9.10 shows a comparison between measurements and SPICE BSIM3 simulation results. Again, at high gate bias, measurements are influenced by self-heating effects.

9.6 Small-Signal Model

Figure 9.11 shows the schematic of the equivalent model used to characterize the small-signal behavior of the silicon LDMOSFET. Unlike the MOSFET equivalent model [75], r_d is not constant in the LDMOS. The r_d is not a constant for the LDMOS as evidenced by Figure 9.9. Therefore r_d was taken from device simulation as described in the previous section. Owing to capacitive coupling between gate and channel at high frequency, part of the channel conductance is present as a resistance (r_i) in series with the gate input capacitance. The parasitic resistor model parameters (r_g, r_d and r_s) were extracted through the use of a set of S-parameters of a device biased at V_{GS} = V_{DS}

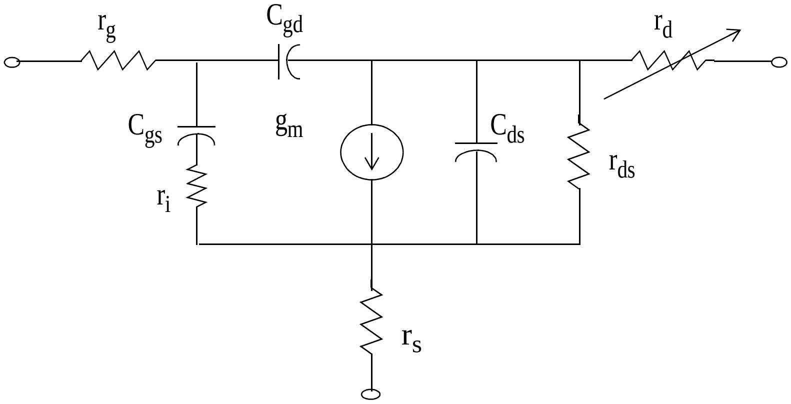


Figure 9.11. Silicon LDMOS small-signal equivalent model.

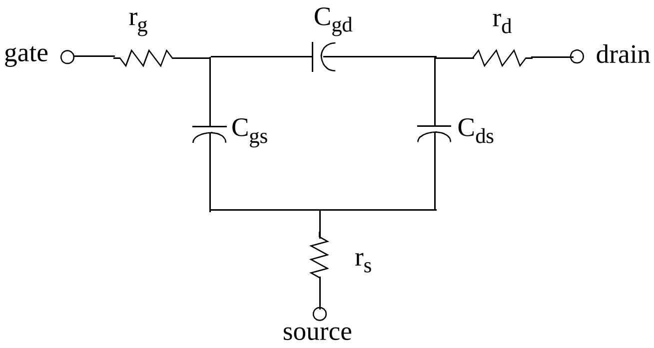


Figure 9.12. Zero bias small-signal equivalent circuit.

= 0 V [75]. This bias condition causes the contribution of the voltage dependent current generator (g_m) used in the model to become zero and maximizes the drain-source capacitance (C_{ds}) and the output resistance (r_{ds}). Channel resistance (r_i) is also ignored due to the absence of channel charge. A schematic of the zero bias equivalent circuit is shown in Figure 9.12. The Figure 9.13 shows the values of r_g, r_s, and r_d extracted by this technique.

With knowledge of the parasitic resistance parameters (r_g, r_d, and r_s), the intrinsic model can be determined. As with the extraction of the parameters r_g, r_s and r_d, the intrinsic parameters should remain constant with frequency, otherwise the model shown in Figure 9.11 does not apply. The intrinsic model z-parameters of the intrinsic model shown in Figure 9.11 are:

$$z_{11}^{i} = z_{11} - (r_g + r_s) \qquad (9.13)$$

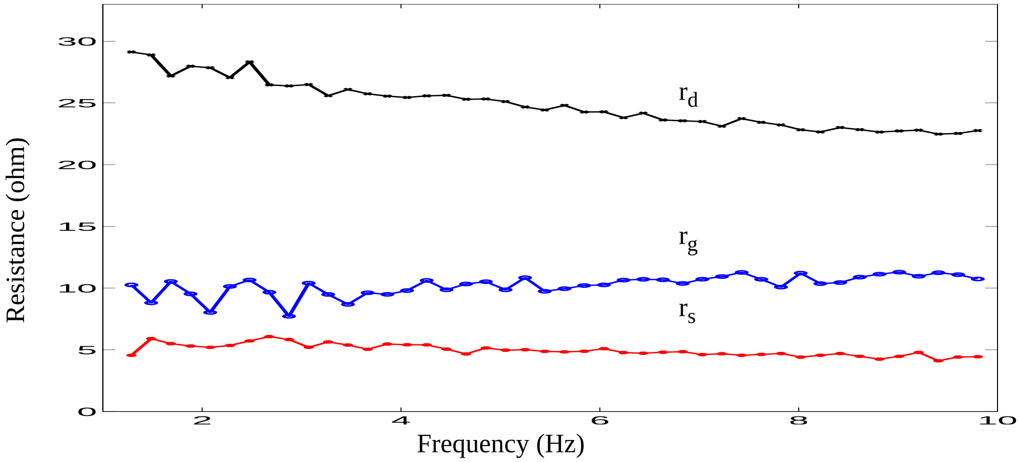


Figure 9.13. Extracted r_g, r_s, and r_d vs. frequency at $V_{DS} = V_{GS} = 0$.

$$z_{22}^{i} = z_{22} - (r_d(V_{GS}, V_{DS}) + r_s) \tag{9.14}$$

$$z_{12}^{i} = z_{12} - r_s \tag{9.15}$$

$$z_{21}^{i} = z_{21} - r_s \tag{9.16}$$

where z is the z-parameter network of the device under bias conditions and z^i is the z-parameter network describing the intrinsic model. Here r_d is expressed as a function of both V_{GS} and V_{DS} as described in Figure 9.9.

From the intrinsic z^i network, y-parameters (y^i) can be generated by a simple conversion. The intrinsic y-parameter network can be expressed as a function of the small-signal model parameters given by:

$$y_{11}^{i} = \frac{r_i C_{gs}^2 \omega^2}{D} + j\omega\left(\frac{C_{gs}}{D} + C_{gd}\right) \tag{9.17}$$

$$y_{12}^{i} = -j\omega C_{gd} \tag{9.18}$$

$$y_{21}^{i} = \frac{g_m e^{-j\omega\tau}}{1 + j\omega r_i C_{gs}} - j\omega C_{gd} \tag{9.19}$$

$$y_{22}^{i} = \frac{1}{r_{ds}} + j\omega(C_{ds} + C_{gd}) \tag{9.20}$$

$$D = 1 + \omega^2 C_{gs}^2 r_i^2 \tag{9.21}$$

Separating Equation 9.17 through Equation 9.20 into their real and imaginary parts, the elements of the small-signal equivalent circuit can be determined analytically as follows:

$$C_{gd} = \frac{-Im(y_{12}^{i})}{\omega} \tag{9.22}$$

$$C_{gs} = \frac{Im(y_{11}^{i}) - \omega C_{gd}}{\omega}\left(1 + \frac{(Re(y_{11}^{i}))^2}{Im(y_{11}^{i}) - \omega C_{gd}{}^{2}}\right) \tag{9.23}$$

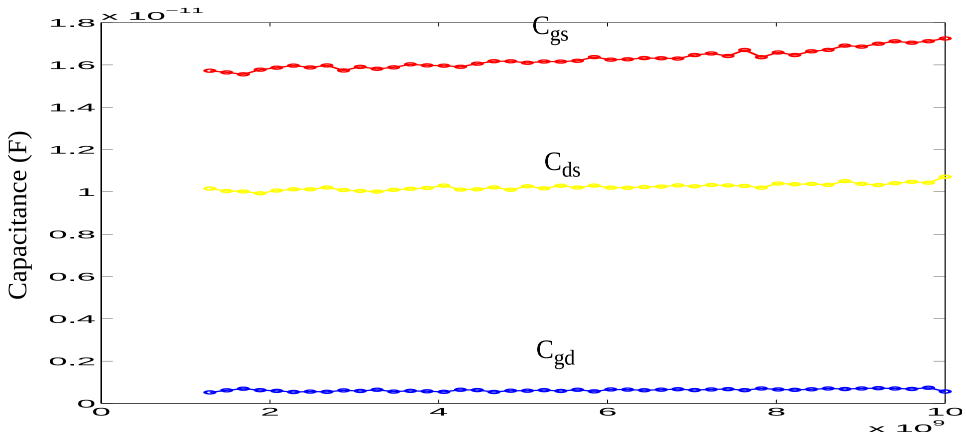


Figure 9.14. Extracted C_{ds}, C_{gs}, and C_{gd} and r_{ds} at V_{DS} = 10 V and V_{GS} = 5 V.

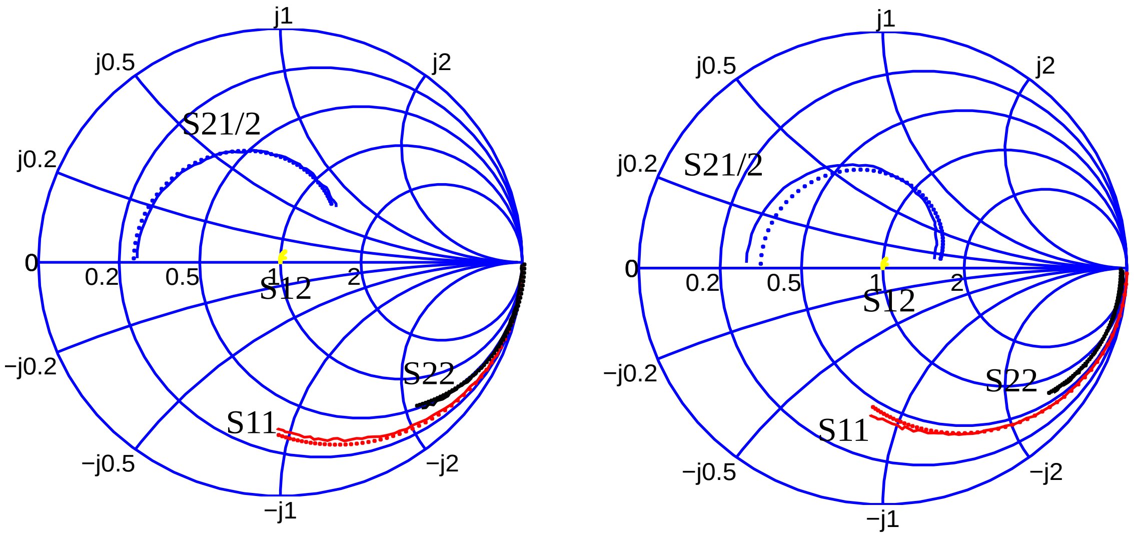
$$r_i = \frac{Re(y^i_{11})}{(Im(y^i_{11}) - \omega C_{gd})^2 + (Re(y^i_{11}))^2} \tag{9.24}$$

$$\tau = \frac{1}{\omega} arcsin\left(\frac{-\omega C_{gd} - Im(y^i_{21}) - \omega C_{gs} r_i Re(y^i_{21})}{g_m}\right) \tag{9.25}$$

$$C_{ds} = \frac{Im(y^i_{22}) - \omega C_{gd}}{\omega} \tag{9.26}$$

$$r_{ds} = \frac{1}{Re(y^i_{22})} \tag{9.27}$$

$$g_m = \sqrt{((Re(y^i_{21}))^2 + (Im(y^i_{21}) + \omega C_{gd})^2)(1 + \omega^2 C^2_{gs} r^2_i)} \tag{9.28}$$



(a)

(b)

Figure 9.15. (a) Measured and modeled s-parameters using extracted model parameters at V_{DS} = 20 V and V_{GS} = 5 V, (b) at V_{DS} = 30 V and V_{GS} = 9 V (solid line: measured, dot: simulated).

As shown in Figure 9.14, extracted capacitances are constant-valued across a broad range of frequencies (1 - 10 GHz). Using the analytical approach, the s-parameter comparison between measurements and simulations are shown in Figure 9.15. Good agreement with measurements throughout the whole operating range is achieved.

10 Conclusions

This chapter summarizes the contribution of this thesis to small-signal modeling of RF devices. Possible future research areas are then discussed in the second section.

10.1 Summary

Modern consumer products require cost competitive technology and RF CMOS has proven to be cost-effective and high volume technology. CMOS is also best suitable to integrate RF with digital circuits making it possible to build a system on a single chip. Due to these advantages, there has been growing interest in modeling of RF CMOS. This work describes small-signal models of MOSFETs in detail.

The first part of this thesis work has considered on y-parameter based modeling of MOSFETs, since modeling of high frequency devices is often done by y-parameter analysis. With frequency operating in the gigahertz range, conventional quasi static models are no longer applicable. Based on a transmission line analogy, the non-quasi static effect is explained and modeled. The NQS frequency (f_{NQS}) is defined as the frequency when NQS effects start to occur. Bias dependency of the NQS frequency is examined for critical modeling parameters (i.e., C_{gg}, C_{gs}, and C_{gd}); the strong bias dependency of the parameters is due to the charge sharing between source and drain, and mobility. At high frequencies, the existence of substrate network cannot be ignored. The substrate network is modeled as parallel R_{sub} and C_{sub}, and the product ($R_{sub}C_{sub}$) shows conservative behavior (i.e., dielectric relaxation time constant of Si). The existence of substrate resistance impacts terminal admittances, even at low frequencies, and this fact suggests that the QS model needs to include substrate components in order to achieve accurate terminal characteristics. In addition, the negative capacitance (NC) effect of a diode is discussed and the corresponding compact model is developed. The negative capacitance effect of a diode occurs at forward bias and the capacitance becomes positive (i.e., geometric capacitance) at high frequencies. Instead of analyzing a small-signal model from measurement data alone, two dimensional simulation is employed in order to develop a physically acceptable small-signal model of RF MOSFETs.

When dealing with small-signal equivalent circuits, the extraction of parameters is of great importance. The second part of this thesis is on extraction of parameters including extrinsic parasitics. Accurate extraction of parasitics is critical in RF circuit simulation and accurate modeling of intrinsic device. Characterization of RF MOSFETs is often done using two-port s-parameter measurements, where the source and bulk are tied together. A compact model of MOSFETs for the common source configuration is developed to identify two-port characteristics and the model is used to effectively de-embed extrinsic parasitics with good accuracy. The extraction of gate resistance is particularly important. The de-embedding methodology is capable of isolating gate resistance (e.g. poly resistance and gate contact resistance) from the channel resistance (i.e., component of gate induced noise), which is crucial in accurate noise modeling of MOSFETs.

Finally, Chapter 9 presents characterization using device simulation and analytical modeling of a LDMOS device, which is one of most widely used device in RF power amplifier application. The unique features of the LDMOS such as graded channel and quasi-saturation effects results in nonlinear LDD resistance. These effects are analyzed and modeled.

10.2 Recommendations for Future Work

CMOS modeling remains one of the most active research areas due to its performance impact on future's high frequency ICs. Device performance at high frequencies needs to be fully understood and modeled correctly. The intent of this thesis is to better understand the physics and characteristics of RF CMOS. However, there are various challenging issues that await exploration in future research. In a more general way, the first and foremost is the development of fast simulator capable of electromagnetics, circuits, and device simulation with easy of use. This unified simulator should be able to deal with the design environment that most modeling/design communities confront in real life and by doing so, more advances in RF applications will be promoted.

Traditionally, the gate oxide of a MOSFET has been considered as a perfect barrier for carriers allowing no current flow between the gate and silicon. As CMOS technology scales to smaller dimensions, the gate leakage current (i.e., Fowler-Nordheim tunneling current and direct tunneling current) is no longer ignored. The impact on RF performance due to the gate leakage needs to be understood for 90 nm technology and beyond.

In a given technology, the control over process variation is not perfect, leading to variations of device performance. At the DC level, variations on device performance are well characterized and implemented into model. However, the impact of RF performance due to the process variations is not much studied and understood. Characterizing the performance variation is quite important for today’s mass production environment for consumer ICs.

APPENDIX A

CAPACITANCES AND CHARGES FOR ALL BIAS CONDITIONS

The following expressions are charge and capacitances of the intrinsic transistor, not including the parasitic capacitances. These expressions are derived with the 40/60 partition scheme [30], which is the physical scheme once the quasi-static approximation is made.

For the inversion region ($V_{GS} > V_T$):

$$C_{gg} = WLC_{ox}\left[\frac{2}{3} \times \frac{\alpha^2 + 4\alpha + 1}{(1+\alpha)^2} + \frac{\delta}{3(1+\delta)} \times \left(\frac{1-\alpha}{1+\alpha}\right)^2\right] \tag{A.1}$$

$$C_{gd} = WLC_{ox}\left[\frac{2}{3} \times \frac{\alpha^2 + 2\alpha}{(1+\alpha)^2}\right] \tag{A.2}$$

$$C_{gd} = WLC_{ox}\left[\frac{2}{3} \times \frac{\alpha^2 + 2\alpha}{(1+\alpha)^2}\right] \tag{A.3}$$

$$C_{gs} = WLC_{ox}\left[\frac{2}{3} \times \frac{2\alpha + 1}{(1+\alpha)^2}\right] \tag{A.4}$$

$$C_{gb} = WLC_{ox}\left[\frac{\delta}{3(1+\delta)} \times \left(\frac{1-\alpha}{1+\alpha}\right)^2\right] \tag{A.5}$$

$$C_{dg} = WLC_{ox}\left[\frac{2}{15} \times \frac{3\alpha^2 + 11\alpha^2 + 14\alpha + 2}{(1+\alpha)^3}\right] \tag{A.6}$$

$$C_{dd} = WLC_{ox}\left[\frac{2(1+\delta)}{15} \times \frac{3\alpha^3 + 9\alpha^2 + 8\alpha}{(1+\alpha)^3}\right] \tag{A.7}$$

$$C_{ds} = -WLC_{ox}\left[\frac{4(1+\delta)}{15} \times \frac{\alpha^2 + 3\alpha + 1}{(1+\alpha)^3}\right] \tag{A.8}$$

$$C_{db} = \delta \times C_{dg} \tag{A.9}$$

$$C_{sg} = WLC_{ox}\left[\frac{2}{15} \times \frac{2\alpha^2 + 14\alpha^2 + 11\alpha + 3}{(1+\alpha)^3}\right] \tag{A.10}$$

$$C_{sd} = -WLC_{ox}\left[\frac{4(1+\delta)}{15} \times \frac{\alpha^3 + 3\alpha^2 + \alpha}{(1+\alpha)^3}\right] \tag{A.11}$$

$$C_{ss} = WLC_{ox}\left[\frac{2(1+\delta)}{15} \times \frac{8\alpha^2 + 9\alpha + 3}{(1+\alpha)^3}\right] \tag{A.12}$$

$$C_{sb} = \delta \times C_{sg} \tag{A.13}$$

$$C_{bg} = C_{gb} \tag{A.14}$$

$$C_{bd} = \delta \times C_{gd} \tag{A.15}$$

$$C_{bs} = \delta \times C_{gs} \tag{A.16}$$

$$C_{bb} = WLC_{ox}\left[\frac{2\delta}{3} \times \frac{\alpha^2 + 4\alpha + 1}{(1+\alpha)^2} + \frac{\delta}{3(1+\delta)} \times \left(\frac{1-\alpha}{1+\alpha}\right)^2\right] \tag{A.17}$$

The saturation index (α) is given by

$$\alpha = \begin{bmatrix} 1 - \dfrac{v_{DS}}{v_{DS,\,sat}} & for & v_{DS} < v_{DS,\,sat} \\ 0 & for & v_{DS} \ge v_{DS,\,sat} \end{bmatrix} \tag{A.18}$$

where

$$v_{DS,\,sat} = \frac{v_{GS} - V_T}{1+\delta} \tag{A.19}$$

The bulk-charge factor is given by

$$\delta = -\frac{dV_T}{dV_{BS}} \tag{A.20}$$

In the depletion region ($V_{GS} < V_T$ but $V_{GB} > V_{FB}$):

$$C_{gg} = C_{gb} = C_{bb} = C_{bg} = WLC_{ox}\left[\frac{\gamma}{2\sqrt{\frac{\gamma^2}{4} + V_{GB} - V_{FB}}}\right] \tag{A.21}$$

$$\begin{aligned} C_{gs} &= C_{gd} = C_{dg} = C_{dd} = C_{ds} = C_{db} = C_{sg} \\ &= C_{sd} = C_{ss} = C_{sb} = C_{bd} = C_{bs} = 0 \end{aligned} \tag{A.22}$$

where γ is the body-effect coefficient.

In the accumulation region ($V_{GB} < V_{FB}$):

$$C_{gg} = C_{gb} = C_{bb} = C_{bg} = WLC_{ox} \tag{A.23}$$

$$\begin{aligned} C_{gs} &= C_{gd} = C_{dg} = C_{dd} = C_{ds} = C_{db} = C_{sg} \\ &= C_{sd} = C_{ss} = C_{sb} = C_{bd} = C_{bs} = 0 \end{aligned} \tag{A.24}$$

APPENDIX B

All the simulated y-parameters of MOSFET are plotted in terms of conductance and capacitance for reference.

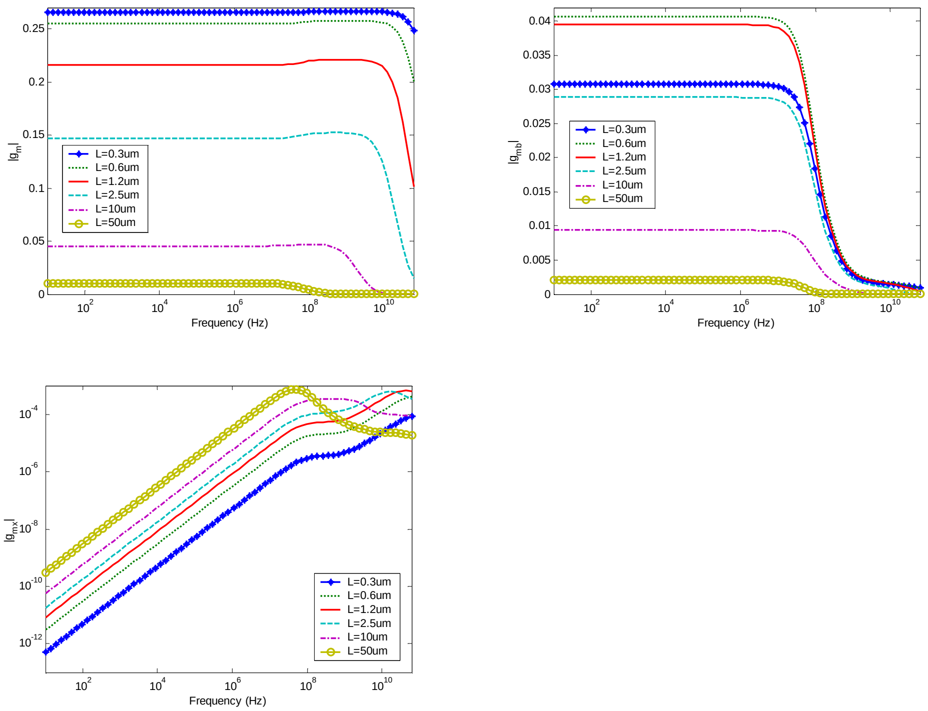


Figure B.1. Frequency response of g_m, g_{mb}, and g_{mx} for various channel length devices (L = 0.3, 0.6, 1.2, 2.5, 10, 50 um) for V_{DS} = 0 V and V_{GS} = 3 V.

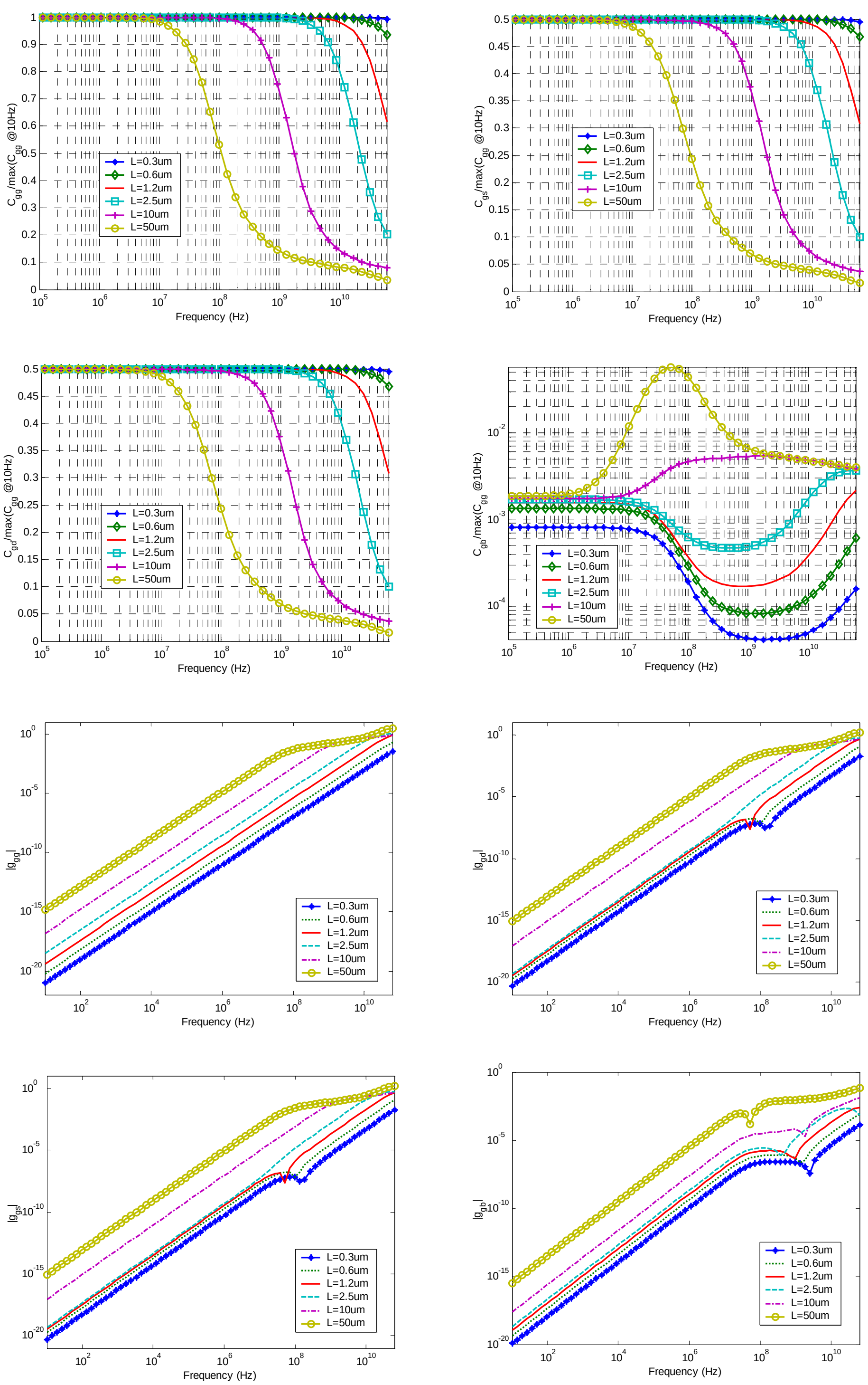


Figure B.2. Frequency response of C_{gg}, C_{gs}, C_{gd}, C_{gb}, g_{gg}, g_{gd}, g_{gs}, and g_{gb} for various channel length devices (L = 0.3, 0.6, 1.2, 2.5, 10, and 50 um) for V_{DS} = 0 V and V_{GS} = 3 V.

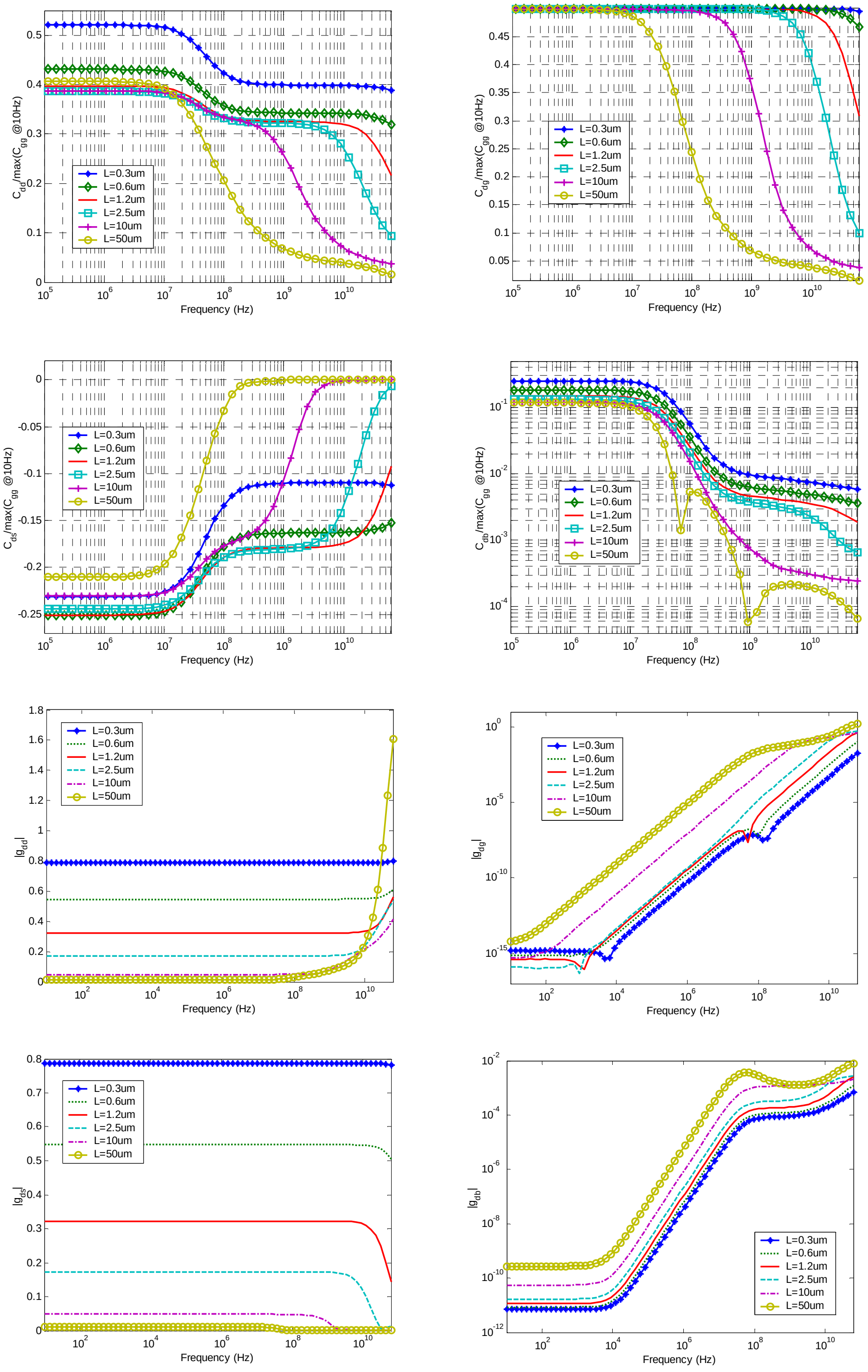


Figure B.3. Frequency response of C_{dd}, C_{dg}, C_{ds}, C_{db}, g_{dd}, g_{ds}, g_{dg}, and g_{db} for various channel length devices (L = 0.3, 0.6, 1.2, 2.5, 10, and 50 um) for V_{DS} = 0 V and V_{GS} = 3 V.

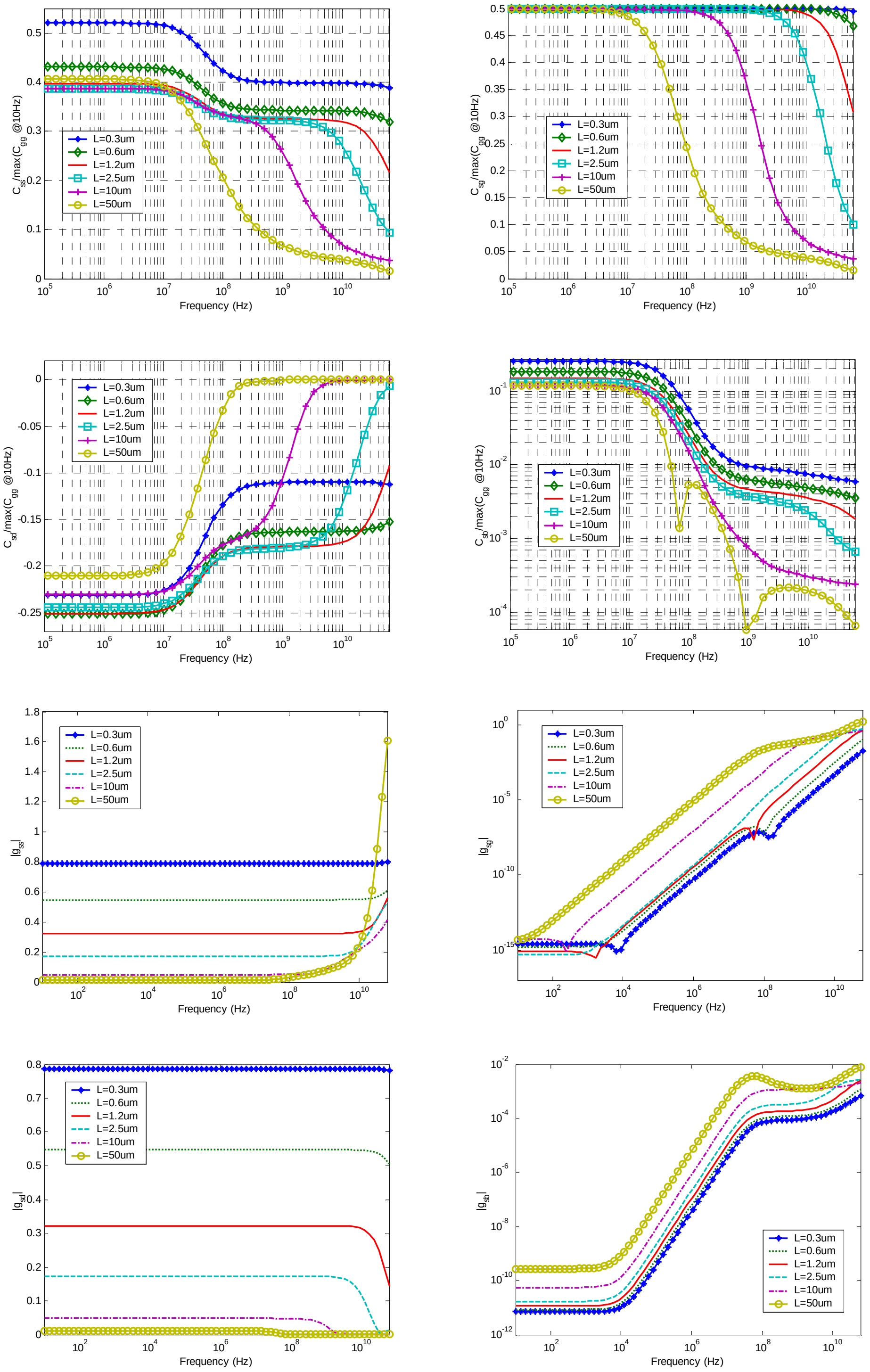


Figure B.4. Frequency response of C_{ss}, C_{sg}, C_{sd}, C_{sb}, g_{ss}, g_{sg}, g_{sd}, and g_{sb} for various channel length devices (L = 0.3, 0.6, 1.2, 2.5, 10, and 50 um) for V_{DS} = 0 V and V_{GS} = 3 V.

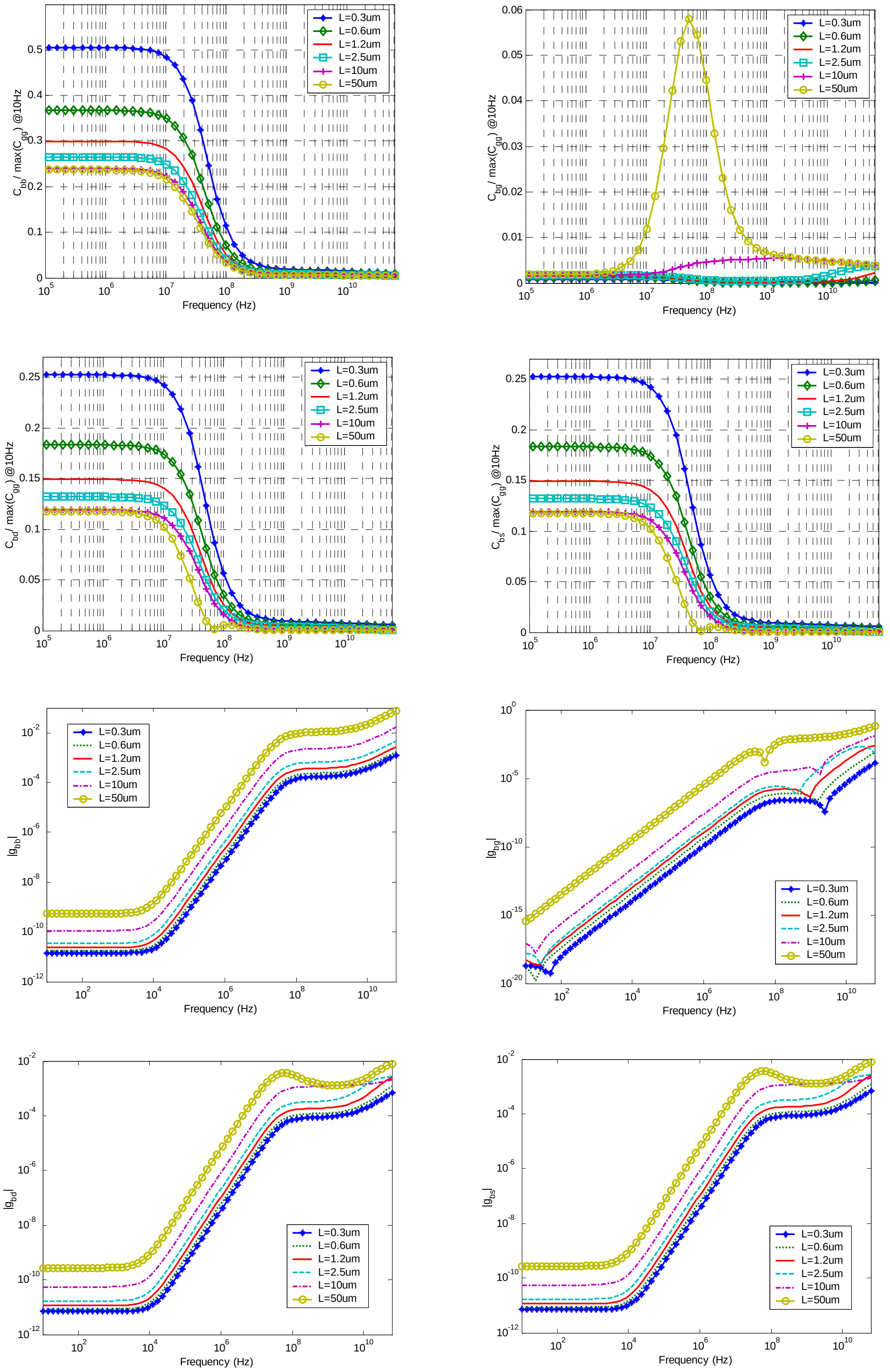


Figure B.5. Frequency response of C_{bb}, C_{bg}, C_{bd}, C_{bs}, g_{bb}, g_{bg}, g_{bd}, and g_{bs} for various channel length devices (L = 0.3, 0.6, 1.2, 2.5, 10, and 50 um) for V_{DS} = 0 V and V_{GS} = 3 V.

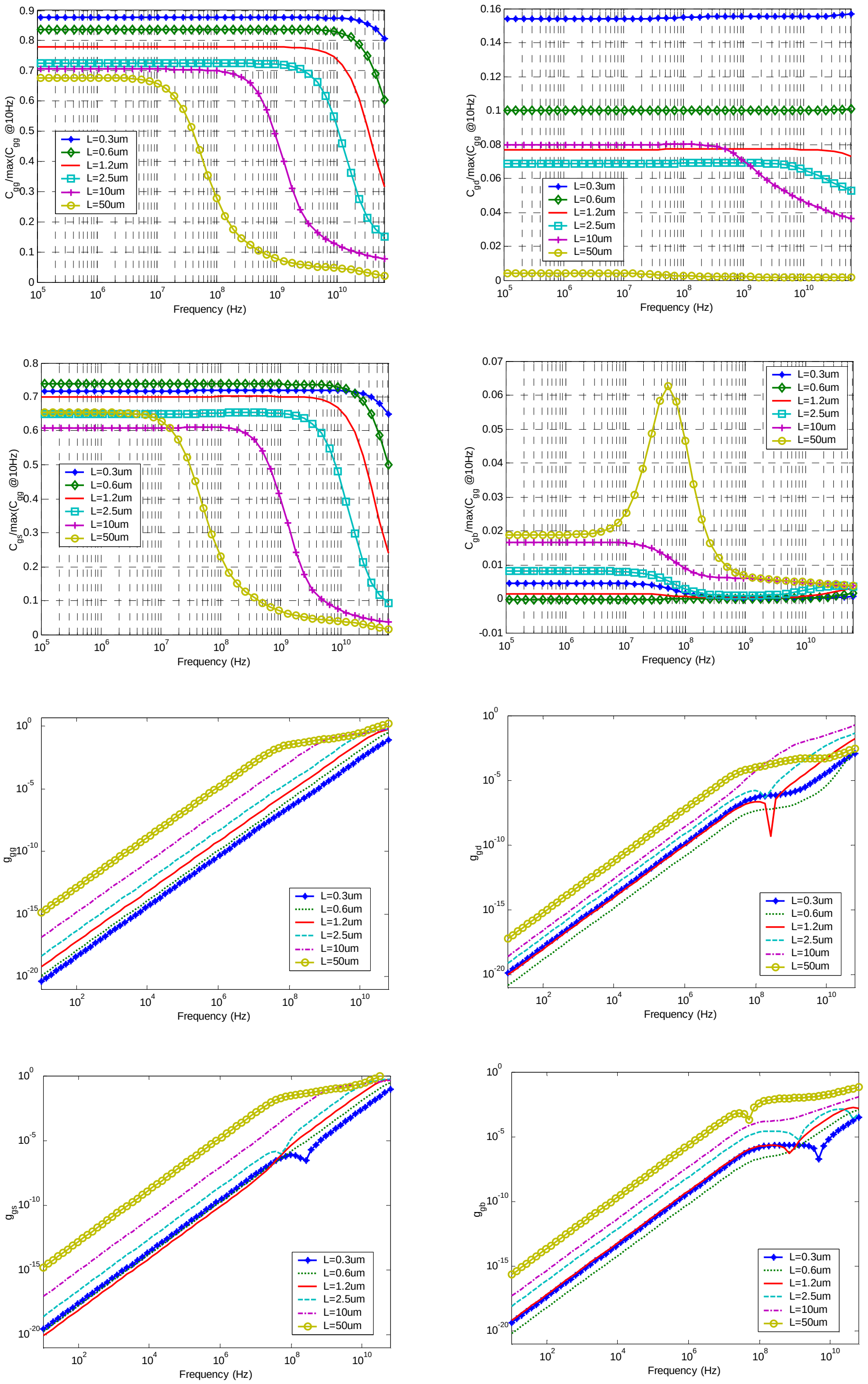


Figure B.6. Frequency response of C_{gg}, C_{gs}, C_{gd}, C_{gb}, g_{gg}, g_{gd}, g_{gs}, and g_{gb} for various channel length devices (L = 0.3, 0.6, 1.2, 2.5, 10, and 50 um) for V_{DS} = 3V and V_{GS} = 3 V.

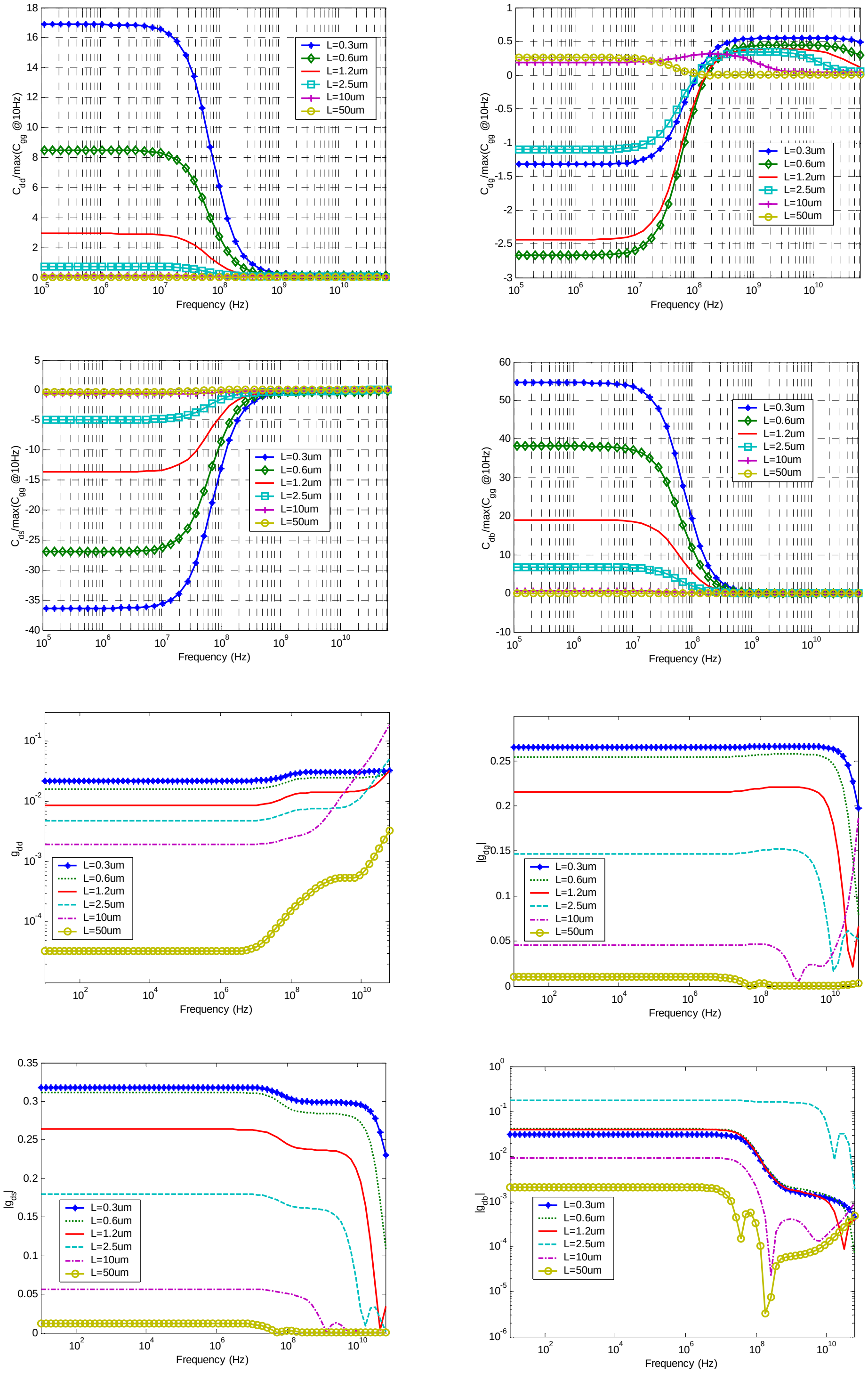


Figure B.7. Frequency response of C_{dd}, C_{dg}, C_{ds}, C_{db}, g_{dd}, g_{ds}, g_{dg}, and g_{db} for various channel length devices (L = 0.3, 0.6, 1.2, 2.5, 10, and 50 um) for V_{DS} = 3 V and V_{GS} = 3 V.

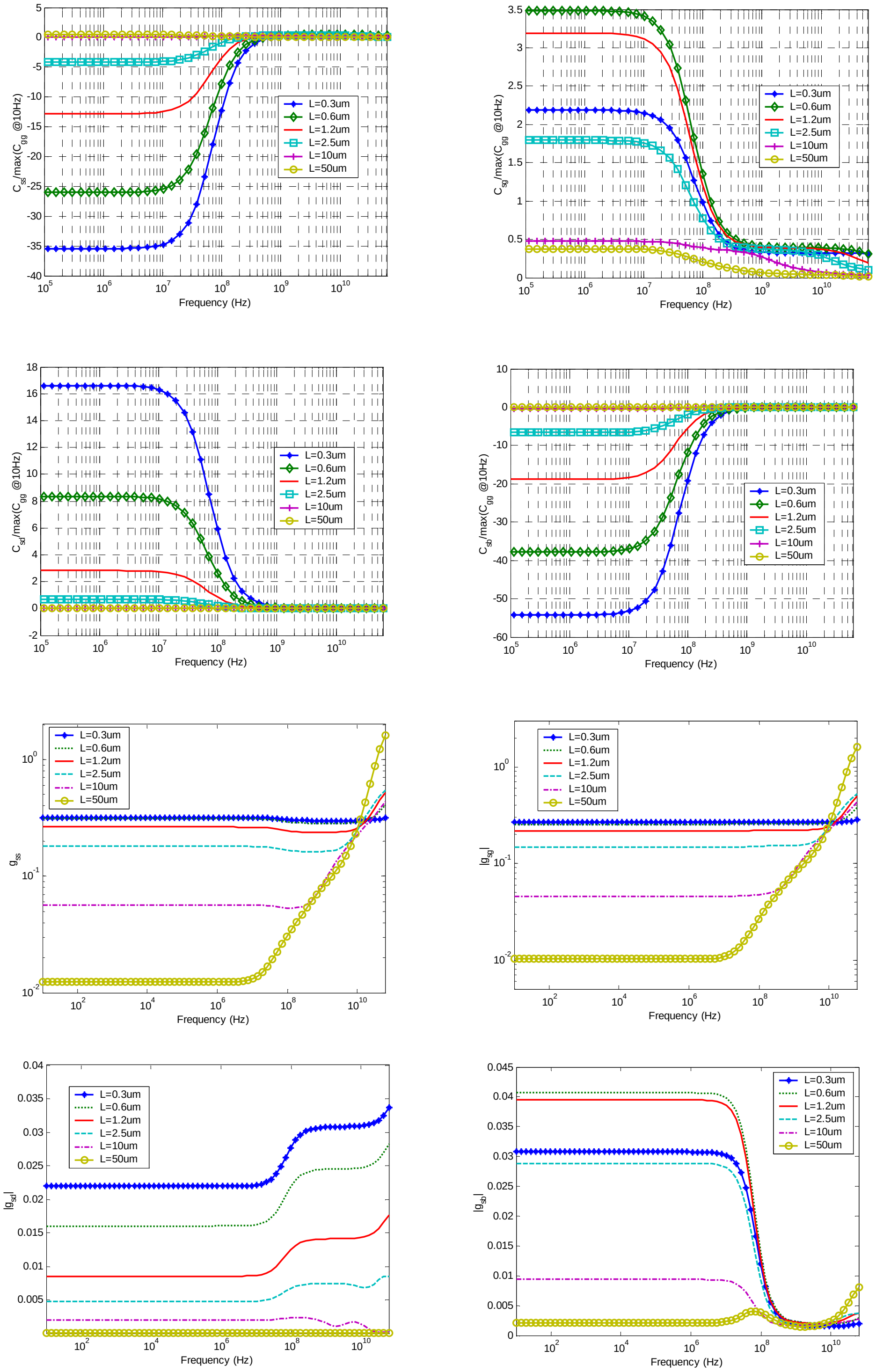


Figure B.8. Frequency response of C_{ss}, C_{sg}, C_{sd}, C_{sb}, g_{ss}, g_{sg}, g_{sd}, and g_{sb} for various channel length devices (L = 0.3, 0.6, 1.2, 2.5, 10, and 50 um) for V_{DS} = 3 V and V_{GS} = 3 V.

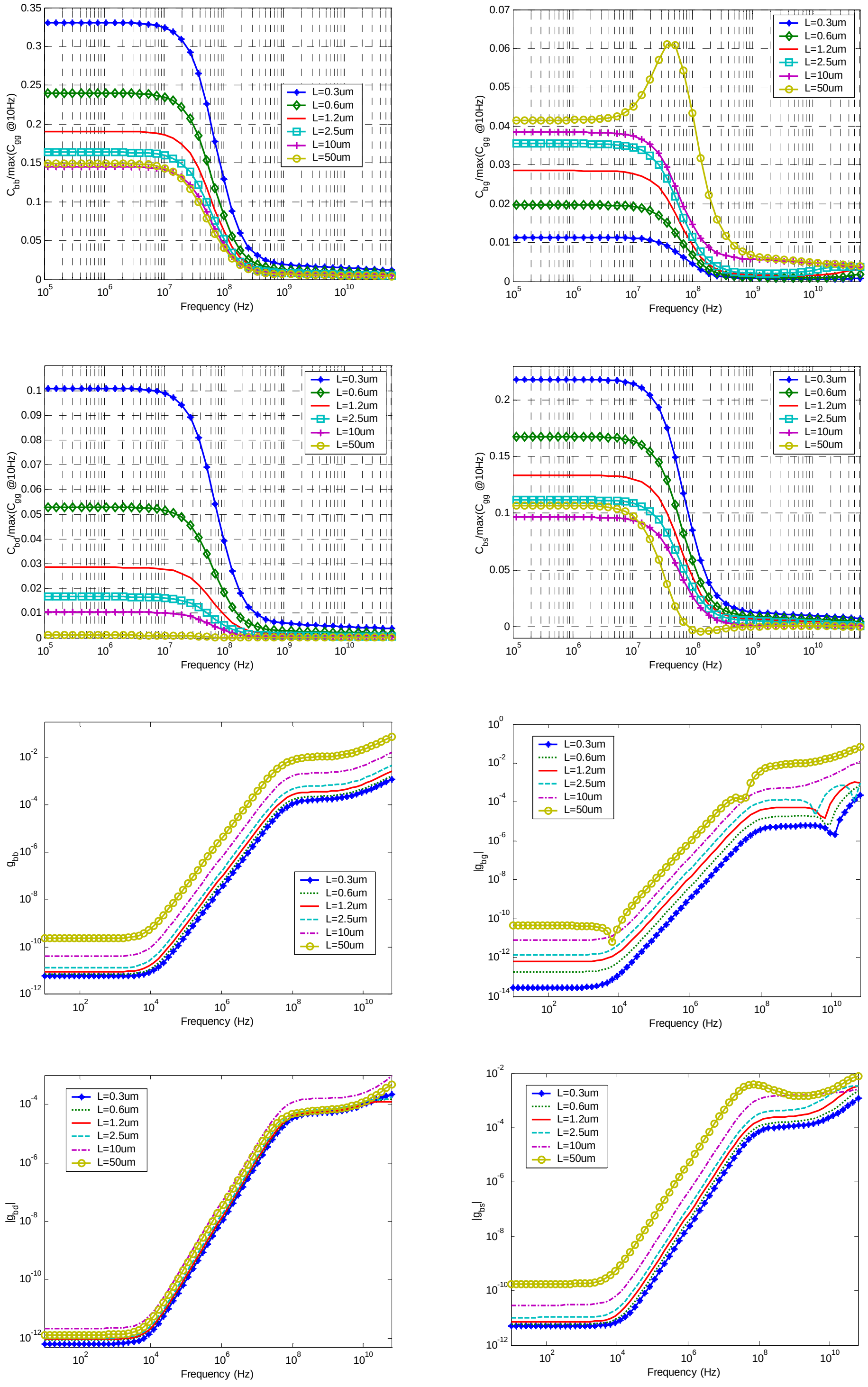


Figure B.9. Frequency response of C_{bb}, C_{bg}, C_{bd}, C_{bs}, g_{bb}, g_{bg}, g_{bd}, and g_{bs} for various channel length devices (L = 0.3, 0.6, 1.2, 2.5, 10, and 50 um) for V_{DS} = 3V and V_{GS} = 3 V.

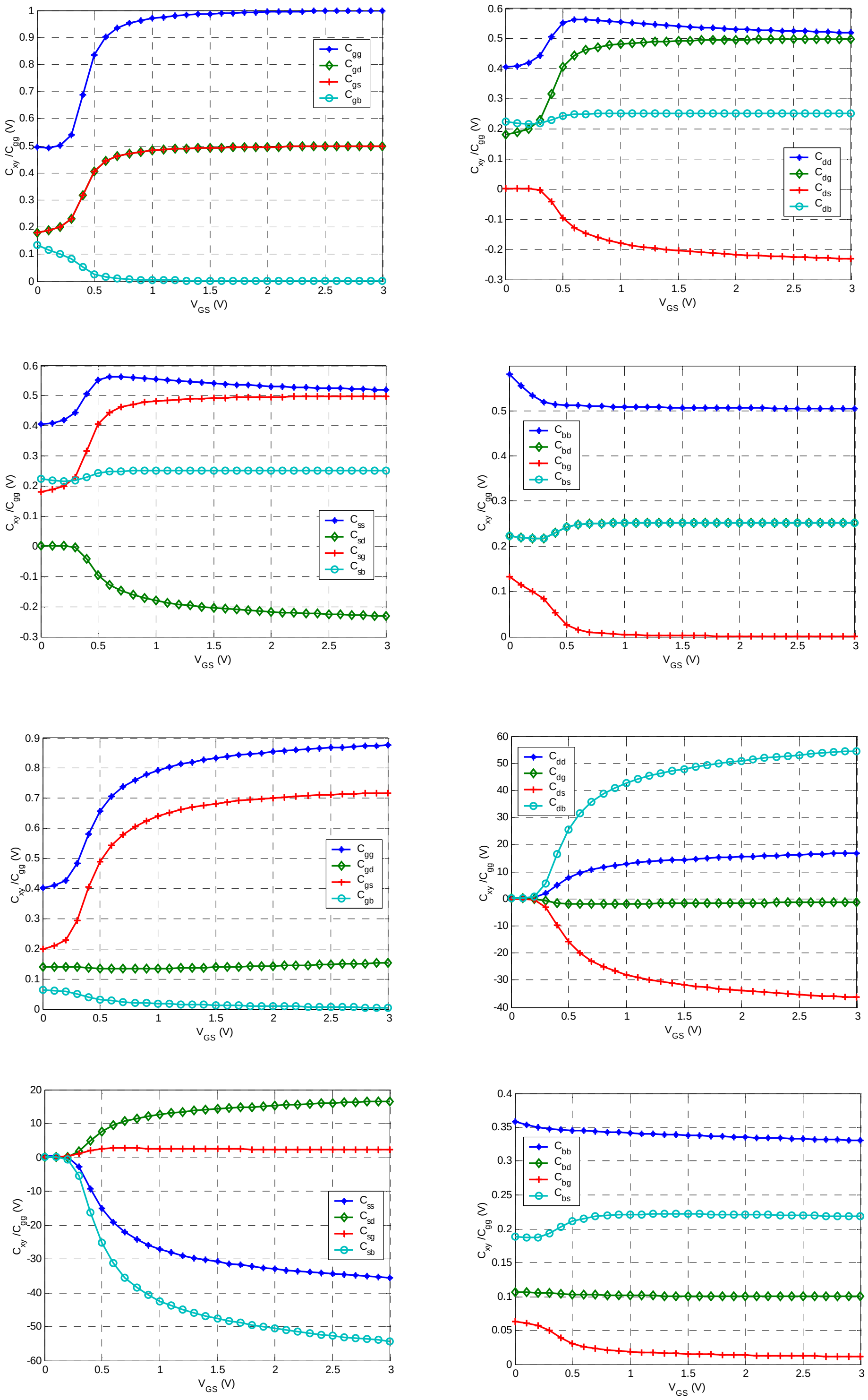


Figure B.10. CV characteristics for L = 0.3 um with V_{DS} = 0 V (top 4) and V_{DS} = 3 V (Bottom 4).

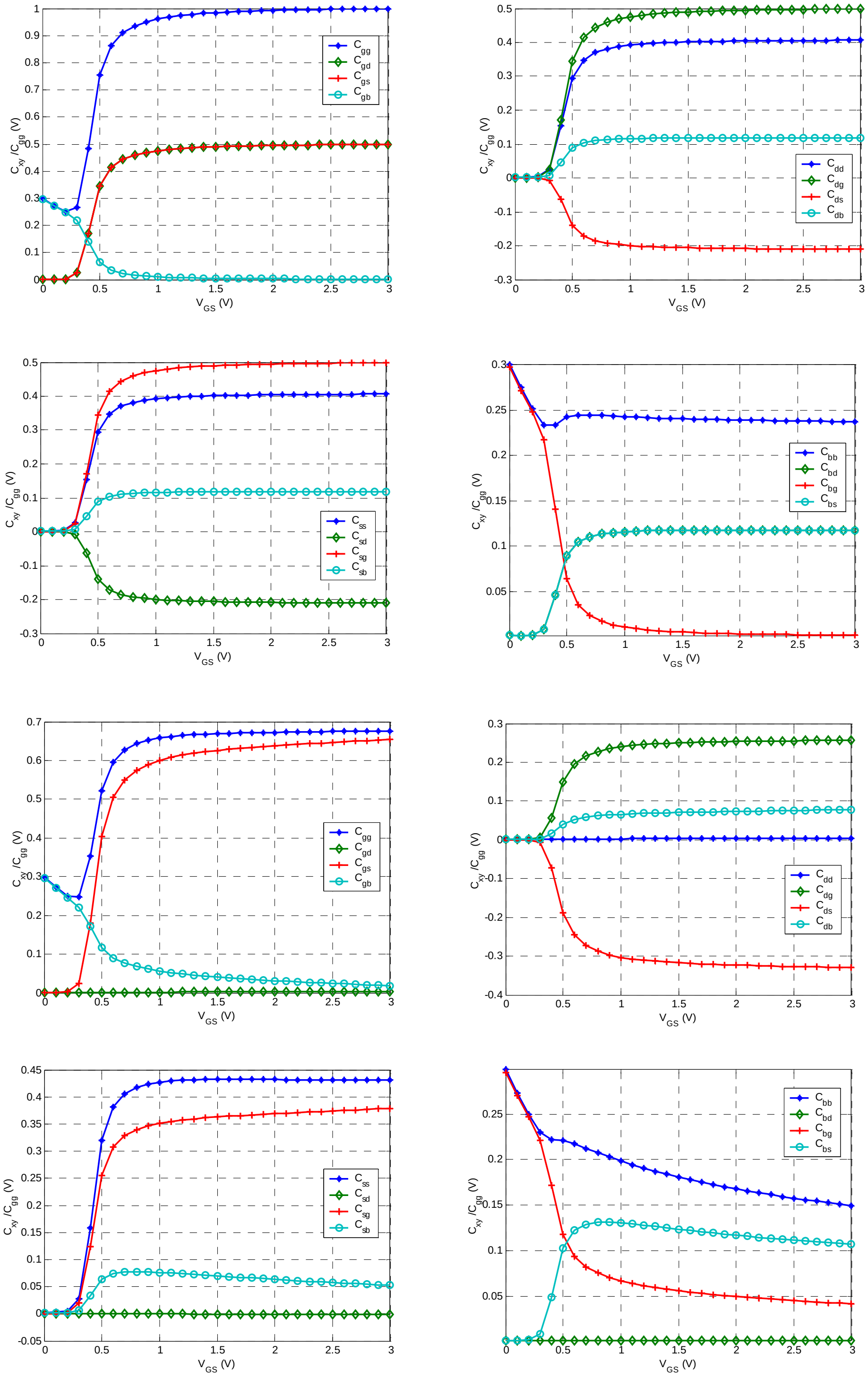


Figure B.11. CV characteristics for L = 50 um with V_{DS} = 0 V (top 4) and V_{DS} = 3 V (Bottom 4).

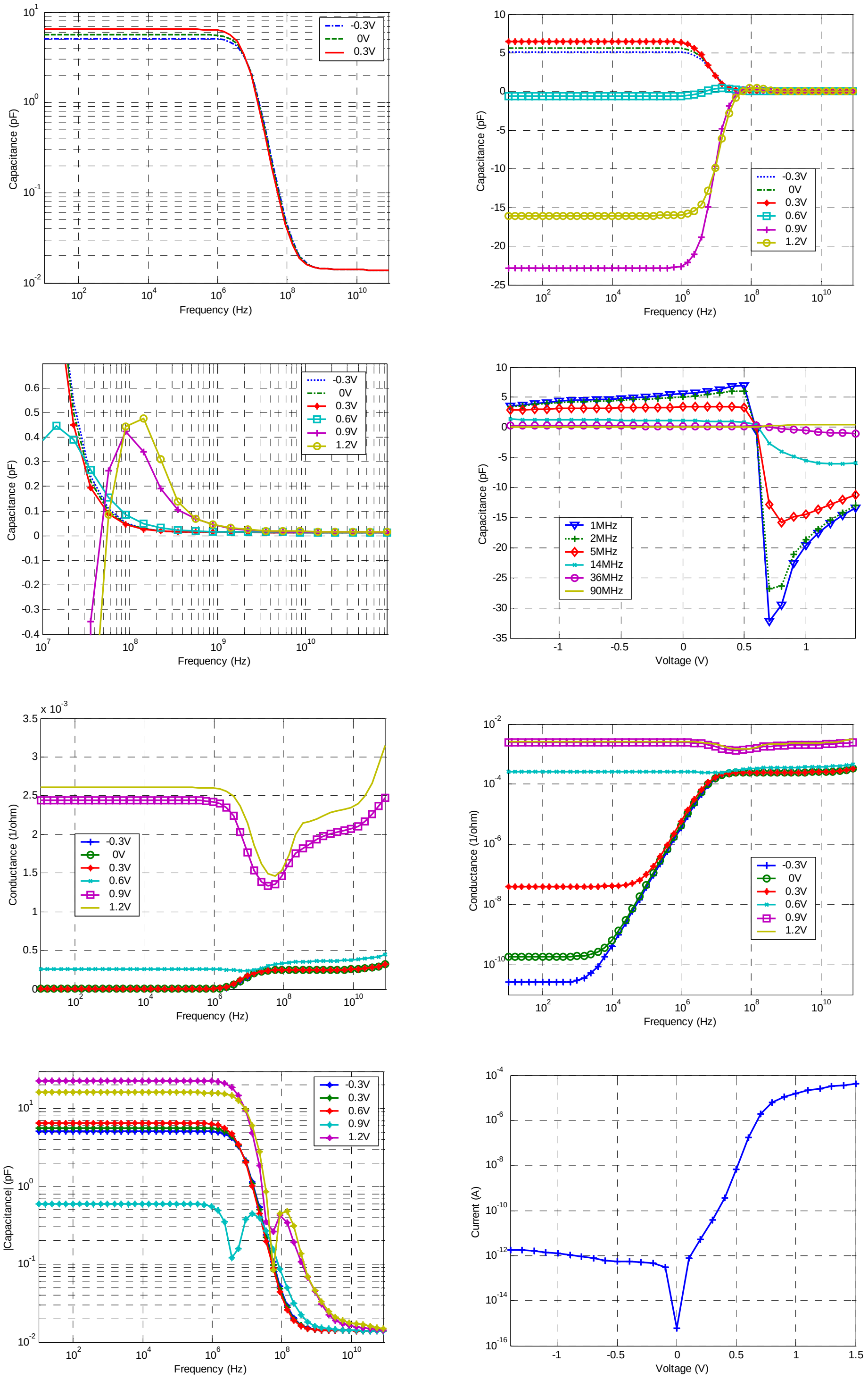


Figure B.12. N+ Pwell diode characteristics.

APPENDIX C

Table 10-1. 2 port parameter conversion table [102].

	s	z	y	h
s	$\begin{matrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{matrix}$	$s_{11} = \frac{(z_{11}-1)(z_{22}+1)-z_{12}z_{21}}{\Delta_1}$ $s_{12} = \frac{2z_{12}}{\Delta_1}$ $s_{21} = \frac{2z_{21}}{\Delta_1}$ $s_{22} = \frac{(z_{11}+1)(z_{22}-1)-z_{12}z_{21}}{\Delta_1}$	$s_{11} = \frac{(1-y_{11})(1+y_{22})+y_{12}y_{21}}{\Delta_2}$ $s_{12} = \frac{-2y_{12}}{\Delta_2}$ $s_{21} = \frac{2y_{21}}{\Delta_2}$ $s_{22} = \frac{(1+y_{11})(1-y_{22})-y_{12}y_{21}}{\Delta_2}$	$s_{11} = \frac{(h_{11}-1)(h_{22}+1)-h_{12}h_{21}}{\Delta_3}$ $s_{12} = \frac{2h_{12}}{\Delta_3}$ $s_{21} = \frac{-2h_{21}}{\Delta_3}$ $s_{22} = \frac{(1+h_{11})(1-h_{22})+h_{12}h_{21}}{\Delta_3}$
z	$z_{11} = \frac{(1+s_{11})(1-s_{22})-s_{12}s_{21}}{\Delta_4}$ $z_{12} = \frac{2s_{12}}{\Delta_4}$ $z_{21} = \frac{2s_{21}}{\Delta_4}$ $z_{22} = \frac{(1-s_{11})(1+s_{22})+s_{12}s_{21}}{\Delta_4}$	$\begin{matrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{matrix}$	$\begin{matrix} \frac{y_{22}}{\lvert y\rvert} & \frac{-y_{12}}{\lvert y\rvert} \\ \frac{-y_{21}}{\lvert y\rvert} & \frac{y_{11}}{\lvert y\rvert} \end{matrix}$	$\begin{matrix} \frac{\lvert h\rvert}{h_{22}} & \frac{h_{12}}{h_{22}} \\ \frac{-h_{21}}{h_{22}} & \frac{1}{h_{22}} \end{matrix}$
y	$y_{11} = \frac{(1-s_{11})(1+s_{22})-s_{12}s_{21}}{\Delta_5}$ $y_{12} = \frac{-2s_{12}}{\Delta_5}$ $y_{21} = \frac{-2s_{21}}{\Delta_5}$ $y_{22} = \frac{(1+s_{11})(1-s_{22})+s_{12}s_{21}}{\Delta_5}$	$\begin{matrix} \frac{z_{22}}{\lvert z\rvert} & \frac{-z_{12}}{\lvert z\rvert} \\ \frac{-z_{21}}{\lvert z\rvert} & \frac{z_{11}}{\lvert z\rvert} \end{matrix}$	$\begin{matrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{matrix}$	$\begin{matrix} \frac{1}{h_{11}} & \frac{-h_{12}}{h_{11}} \\ \frac{h_{21}}{h_{11}} & \frac{\lvert h\rvert}{h_{11}} \end{matrix}$
h	$h_{11} = \frac{(1+s_{11})(1+s_{22})-s_{12}s_{21}}{\Delta_6}$ $h_{12} = \frac{2s_{12}}{\Delta_6}$ $h_{21} = \frac{-2s_{21}}{\Delta_6}$ $h_{22} = \frac{(1-s_{11})(1-s_{22})-s_{12}s_{21}}{\Delta_6}$	$\begin{matrix} \frac{\lvert z\rvert}{z_{22}} & \frac{z_{12}}{z_{22}} \\ \frac{-z_{21}}{z_{22}} & \frac{1}{z_{22}} \end{matrix}$	$\begin{matrix} \frac{1}{y_{11}} & \frac{-y_{12}}{y_{11}} \\ \frac{y_{21}}{y_{11}} & \frac{\lvert y\rvert}{y_{11}} \end{matrix}$	$\begin{matrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{matrix}$

where $\Delta_1 = (1+z_{11})(1+z_{22})-z_{12}z_{21}$
$\Delta_2 = (1+y_{11})(1+y_{22})-y_{12}y_{21}$
$\Delta_3 = (1+h_{11})(1+h_{22})-h_{12}h_{21}$
$\Delta_4 = (1-s_{11})(1-s_{22})-s_{12}s_{21}$
$\Delta_5 = (1+s_{11})(1+s_{22})-s_{12}s_{21}$
$\Delta_6 = (1-s_{11})(1+s_{22})+s_{12}s_{21}$

and $|z| = z_{11}z_{22}-z_{12}z_{21}$
$|y| = y_{11}y_{22}-y_{12}y_{21}$
$|h| = h_{11}h_{22}-h_{12}h_{21}$

APPENDIX D

THE PROPERTIES OF LOSSY SILICON SUBSTRATE

The lossy properties of the silicon material can be examined by analyzing the frequency response as

$$Y_{substrate} = \frac{1}{R} + j\omega C \tag{D.1}$$

R and C represents resistance and capacitance of the silicon material.

Let's assume that the silicon substrate has a symmetric rectangular shape as in Figure D.1 with area, A, and distance, t, between top and bottom electrode. Also it is assumed that no fringing field exists. By applying a small signal and measuring the frequency response at elctrode_top, the $Y_{substrate}$ can be measured For this configuration, since

$$C = \frac{Q}{V} \tag{D.2}$$

and from Gauss's law,

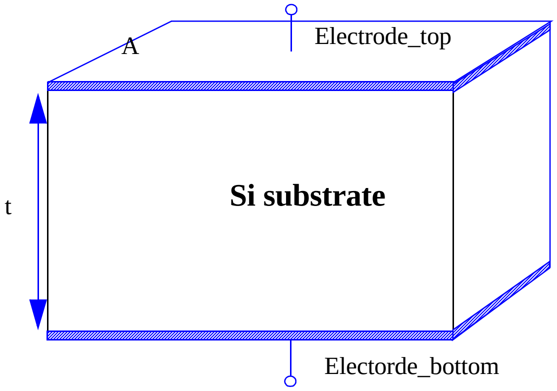


Figure D.1. Si substrate contacted by 2 electrodes.

$$V = \int_0^t E \cdot dl = \frac{Q}{\varepsilon_{si}\varepsilon_o} \qquad (D.3)$$

So

$$C = \frac{\varepsilon_{si}\varepsilon_o}{t}A \qquad (D.4)$$

Now for the resistance of the substrate,

$$R = \frac{V}{I} \qquad (D.5)$$

and

$$I = \int J \cdot dA = \sigma E \cdot A \qquad (D.6)$$

Thus

$$R = \frac{t}{\sigma A} \qquad (D.7)$$

So the product of RC becomes

$$\boxed{RC = \frac{\varepsilon_{si}\varepsilon_o}{\sigma}} \qquad (D.8)$$

The RC product of the substrate is independent of geometry, t and A, and constant for a given material properties $\varepsilon_{si}\varepsilon_o$. The RC product is also known as a *dielectric relaxation time constant*.

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