MEASUREMENT, SUPPRESSION, AND PREDICTION OF DIGITAL SWITCHING NOISE COUPLING IN MIXED-SIGNAL SYSTEM-ON-CHIP APPLICATIONS

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DOCTOR OF PHILOSOPHY

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Abstract

In system-on-chip (SoC) applications the digital switching noise propagates through the substrate and power distribution networks to analog circuits, degrading their performance. To overcome these interactions, measurement, suppression, and prediction of noise coupling are essential. Measurements can help to monitor and analyze the noise coupling distribution within the chip, suppression techniques reduce the effect of noise coupling on analog circuits, and prediction allows the identification of potential noise coupling issues before fabrication. This research work focuses on all three aspects, by developing new and improved measurement techniques for substrate and power supply noise, by proposing novel suppression methods based on active noise cancellation, and by creating a modeling technique for early prediction of noise coupling in architectural stages of the design.

The measurement work first identifies the importance to measure both substrate and power supply noise, and not to affect the propagation or inject additional noise in the substrate. A set of requirements is developed based on these aspects and on the particularities of performing measurements in large and complex mixed-signal SoCs. Driven by these requirements, a measurement technique is proposed based on small and compact sensors that can easily be placed within high-density layout regions. Their outputs are multiplexed and routed to an on-chip digitizing waveform recorder.

The sensors contain only PMOS transistors in a topology designed to minimally affect the noise propagation, and not to inject additional noise. The on-chip digitizing reduces the bandwidth limitation and signal contamination due to off-chip routing, and eliminates additional analog output pins. Based on the experimental evaluation on a 0.13-µm CMOS test chip, bandwidth from DC to 1.6 GHz, linearity better than 1.5% for substrate, and 6 % for power supply sensors have been achieved. Power supply rejection of 64 dB has been achieved in substrate probing. The substrate noise coupling into power supply probing was below detectable limits. Experimentally reconstructed waveforms with 20 ps time resolution allowed the measurement of amplitude, rise-time, and overshoot of transition edges.

The suppression work first discusses previous reported methods of reducing noise generation, propagation, and reception by analog circuits. It is noticed that while these methods reduce the noise coupling effect they don't completely solve the problem. For example, noise still exists inside guard rings, having magnitudes varying across the region. To reduce even more the noise coupling effects, this research work proposes three active cancellation structures that can be used in addition to conventional guard ring methods. The first technique addresses the common-source NMOS amplifier stage, and senses the substrate noise through a source-follower PMOS transistor, which generates a noise cancellation current. The second technique is a derivation of the first one for active loads made of a current source and a diode-connected transistor. The third technique addresses the NMOS in common-source with degeneration configuration, and uses a negative feedback loop to cancel out the substrate noise effect. The proposed substrate noise cancellation structures have been evaluated in a 0.13 µm CMOS test chip. The active loads have been implemented in the delay cells of a ring oscillator. Coupling reduction for the NMOS in common-source amplifier structure of 8.8 times has been achieved at 10 MHz sinusoidal substrate noise, decreasing for higher frequencies to 5.6 times at 1 GHz. Coupling reduction for NMOS common source with degeneration of 56 times has been achieved at 10 MHz, decreasing to 10 times a 100 MHz, and to 1.5 times at 1 GHz. Ring oscillator sideband suppression of 25 dB has been achieved at 1 MHz sinusoidal

substrate noise, decreasing for higher frequencies to 4 dB at 600 MHz. The ring oscillator frequency deviation has been reduced from 1% to 0.05% at 50 mV variation of substrate potential, and from 5.5% to 0.8% at 250 mV.

The suppression work first discusses the noise coupling modeling and prediction in SoCs, and the coverage of various stages of the design process. It is then noticed the correlation between modeling accuracy and the stage of design where the methods can be applied. Also, it is emphasized that the most accurate methods use the complete layout which is available only late in the design process, and the problems found at this stage often require major rework that significantly impacts cost and schedule. Driven by the desire to predict the noise coupling problems early in the design process, this work proposes a novel hybrid lumped-distributed model of the chip substrate and power distribution integrated in a macro-model of the chip, package, and PCB. The model has a two-dimensional and a simplified one-dimensional version. Transient simulations and correlation with experimental measured data have been performed on the one-dimensional model. Correlation of overshoot, two types of ringing, and amplitudes has been achieved between the measured and simulated waveforms. Correlation of frequency domain simulations between the one and two-dimensional models has also been achieved. Despite the fact that the accuracy is lower than with the techniques using physical layout, or schematics and behavior models, this approach can be used to predict major noise coupling issues during the architectural stage of the design.

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topic, and for supporting and allowing me to perform my Ph.D. research in the company's labs and allowing me to implement my experiments on Teradyne's test chips. Special thanks also to the test chips project managers Alan Hussey and ST Chen, and my functional group managers during these years: Roger Bartley, Ron Gyurcsik, Marc Hutner, and Farrokh Aghaeepour.

Last but certainly not least, I would like to thank my wife Mihaela, for her love, support, encouragement and understanding along my Ph.D. study, and my kids Helen and Michael for their encouragement and understanding throughout these years. I dedicate this dissertation to my family and to the memory of my parents.

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Chapter 1

Background of Digital Switching Noise Coupling in Mixed-Signal Systems-on-Chip

1.1 Introduction

The semiconductor industry has significantly advanced in the past decades mainly driven by computing technology, the Internet, communication networks, and portable consumer electronics. Market demands requiring increased functionality and lower costs have pushed the technology scaling to sub-micron, deep sub-micron, and nano-scale dimensions. The number of devices per chip, and the system performance has improved exponentially over the last three decades, similarly to Moore's prediction in 1975 [1]. The International Technology Roadmap for Semiconductors (ITRS) predicts shrinking of transistor physical length gate to 25 nm in 2009, 20 nm in 2011, and close to 10 nm in 2015 [2]. Technology scaling has generated the trend to integrate more and more functionality towards the goal of implementing complete systems on a single chip, concept referred as System-On-Chip (SoC). SoCs eliminate the connection between multiple chips used in previous architectures, thus reducing the number of output buffers, and the cost of packaging and fabrication. Besides the advantages of integrating complete systems in a single chip, SoCs encounter tremendous challenges.

These challenges are generated primarily by the high density of circuits, and include coupling interaction between blocks and interconnects, increased power supply and substrate noise, thermal cooling, and limitations of design and verification tools. Because SoCs implement sensitive analog circuits on the same die with high-speed digital processing circuits, the switching noise produced by the digital circuits propagates through substrate and power distribution to the analog circuits, degrading their performance. This problem is aggravated with technology scaling because larger number of transistors and more functions are implemented in the digital core resulting in more noise injected into substrate and power distribution circuits. Device scaling increases the substrate doping concentration to reduce the transistors threshold voltage. As a consequence, the substrate conductivity increases and provides a lower resistivity path for noise coupling. The device scaling reduces the headroom and voltage swings in the analog circuits, thus making them more sensitive to the coupled noise. As transistor sizes are predicted to shrink to smaller and smaller dimensions, the noise coupling challenges in SoCs are projected to worsen. To overcome these challenges, the development of coupling suppression techniques and circuits that are less sensitive to noise is essential to progress in SoC implementation.

1.2 Noise Coupling Mechanism

The digital switching noise coupling mechanism has three components: generation, propagation, and injection into the analog circuits. Figure 1.1 illustrates the noise coupling mechanisms on an example consisting of a digital inverter and an NMOS

transistor physically located on the same die. The inverter generates noise, which propagates and couples into the NMOS transistor.

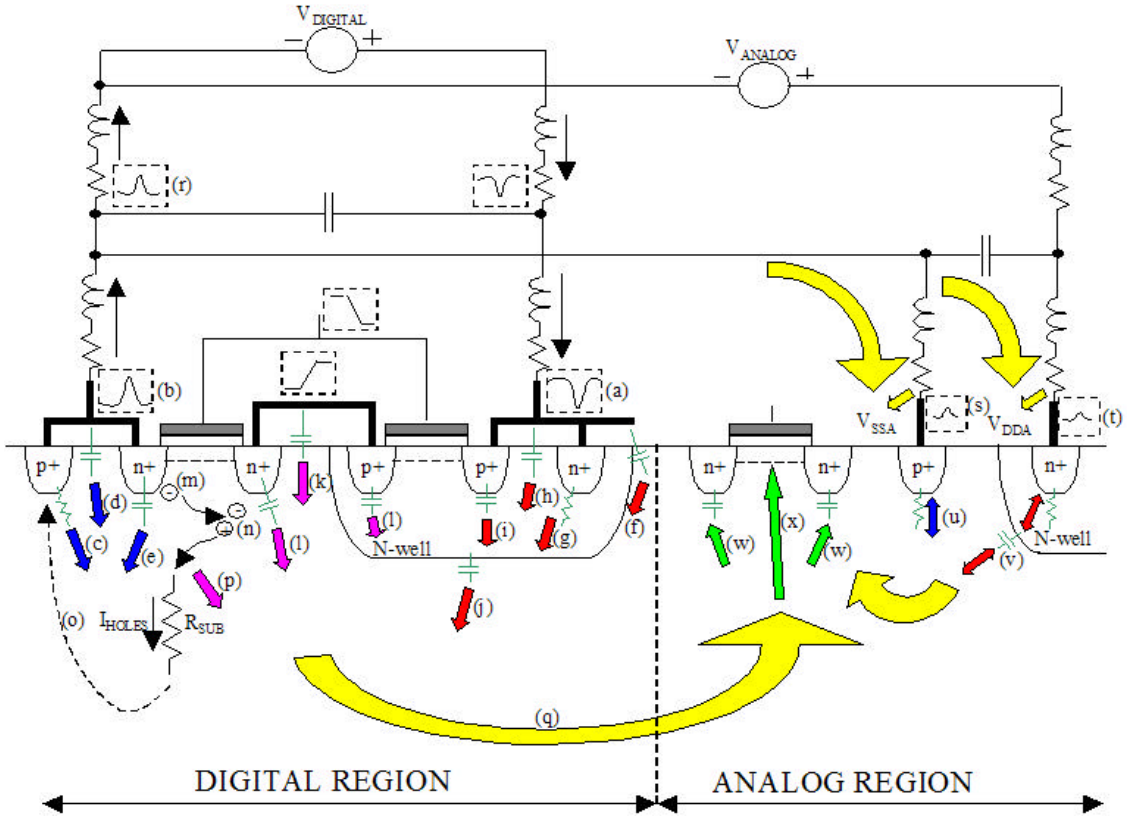


Figure 1.1: Illustration of the noise coupling mechanism on an example consisting of a digital inverter and an NMOS transistor located on the same die

1.2.1 Noise Generation

Simultaneous switching of multiple digital gates produces large transient current spikes, which flow through the chip, package, and PCB power distribution network. The power distribution path includes on-chip metal wires and pins, bond wires, package wires and pins, and PCB interconnects to the assumed clean supplies. The

dominant inductive and resistive impedances of this path produce transient voltage drops due to the switching current spikes. The voltage drops on the V_{DD} path can be expressed by the equation:

$$V_{DD\_DROP} = R_{VDD} \cdot I_{DD} + L_{VDD} \cdot \left(\frac{dI_{DD}}{dt} \right) \quad (1.1)$$

and on the V_{SS} path by the equation:

$$V_{SS\_DROP} = R_{VSS} \cdot I_{SS} + L_{VSS} \cdot \left(\frac{dI_{SS}}{dt} \right) \quad (1.2)$$

where R_{VDD} and R_{VSS} represent the resistance, and L_{VDD} and L_{VSS} the inductance of the power and ground networks. For typical R and L values, a transient step increase of the I_{DD} current generates a negative voltage spike on the on-chip V_{DD} node, and a transient step increase of the I_{SS} current generates a positive voltage spike on the on-chip V_{SS} node. These spikes are illustrated in Figure 1.1 by waveforms (a) and respectively (b). The magnitudes of the spikes are larger for larger devices and faster current transients. Also, when multiple gates switch simultaneously, the individual switching currents combine and increase significantly the magnitude of spikes. Technology scaling reduces the size of transistors but increases their number. As a result of scaling the total switched current may be larger or may remain the same.

However, the switching transients *dI/dt* become significantly faster. Consequently, the generation of digital switching noise is expected to increase with technology scaling.

The voltage noise on the on-chip V_{SS} couples into the substrate through the resistance of substrate contacts, and through the capacitance of metal wires and reversed biased diffusion junctions. The coupling through substrate contacts, which is dominant at low frequencies and, due to the RC filtering effect, can be neglected at high frequencies, is illustrated by (c) in Figure 1.1. The coupling through wires capacitance is illustrated by (d), and through reversed biased junctions by (e).

Also referring to Figure 1.1, the voltage spikes on the on-chip V_{DD} couples directly into substrate through the wire capacitance (f). A secondary path consists of coupling into N-wells through the resistance of N-well contacts (g), capacitance of metal wires (h), and capacitance of reverse biased junctions (i), and from here into substrate through the N-well capacitance (j).

Besides the voltage spikes on V_{DD} and V_{SS}, the transient voltages on the outputs of digital cells couples into substrate through the capacitance of metal wires (k) and reversed biased junctions (l).

As technology scaling has reduced transistor sizes, the impact-ionization effect has become more significant, although it is mitigated by voltage scaling. Referring to Figure 1.1, the channel carriers (m) are accelerated by the high electric field near the drain, and gain enough energy to generate electron-hole pairs (n) by scattering with the crystal lattice. The electrons are swept into the drain, but the holes flow through the substrate and are collected by the p+ substrate contacts connected to V_{SS}, causing the current I_{HOLES} in Figure 1.1. This current produces *IR* drops on the substrate

resistance R_{SUB}, which appear as dynamic voltage variations in the substrate. This mechanism is illustrated by (o) and (p) in Figure 1.1.

1.2.2 Noise Propagation

The sum of all digital switching noise components described in the previous section couples into the analog region through the substrate resistance. This mechanism is shown by (q) in Figure 1.1.

Besides coupling into the on-chip V_{DD} and V_{SS}, the digital switching current couples also into the analog power distribution network through the package parasitic capacitance and through the shared ground path. While separate power supplies are used for the analog and digital circuits, the ground return current typically shares a common path either on the package and PCB, or only on the PCB. The digital switching current produces voltage drop on this shared impedance, illustrated by waveform (r) in Figure 1.1. This voltage variation couples into the on-chip analog ground, V_{SSA}, and analog supply V_{DDA}. Because of the topology differences in the two coupling paths, the noise on V_{SSA} and V_{DDA} are not the same. Their difference is seen as power supply noise by the analog circuits. Noise on V_{SSA} couples into the substrate through the substrate contact's resistance, and noise on V_{DDA} couples into the substrate through the N-well vertical resistance and junction capacitance. Also, noise may couple on the same paths from substrate into the on-chip ground and power grid. These two mechanisms are illustrated by (u) and (v) in Figure 1.1.

1.2.3 Noise Injection into Analog Circuits

Substrate noise interacts with the NMOS transistors primarily through source and drain junction capacitances and through the body-effect. These two mechanisms are illustrated by (w) and (x) in Figure 1.1. The capacitance of the reversed biased junctions acts as a direct coupling path between substrate and the drains and sources of transistors. The body-effect is manifest as threshold voltage modulation by the substrate noise. To illustrate this effect the square-law IV characteristic of an NMOS transistor is

$$I_D = m \cdot C_{OX} \cdot \left(\frac{W}{L}\right) \cdot (V_{GS} - V_T)^2 \qquad (1.3)$$

where I_D is the drain current, μ the mobility, C_{OX} the gate oxide capacitance, V_{GS} the gate to source voltage, and V_T the threshold voltage. The threshold voltage depends on the potential difference between source and substrate bulk, V_{SB}, following the relation

$$V_T = V_{T0} + g \cdot \left(\sqrt{|2 \cdot f_F| + V_{SB}} - \sqrt{|2 \cdot f_F|}\right) \qquad (1.4)$$

Substrate noise is reflected in V_{SB} voltage variations, which further affect V_T and I_D.

The noise coupled into transistors affects the performance of analog circuit blocks. Reports of digital switching noise coupling effects on A/D converters have been

reported in [3], D/A converters in [4], PLLs in [5], VCOs in [6]-[7], and LNAs in [8]. With technology scaling the digital switching noise coupling increases. Therefore, significant effort has been invested in recent years to reduce the effect of digital switching noise on analog circuits. This effort has focused on measurements, modeling, and finding means of its suppression. Measurement is needed for understanding of noise coupling mechanisms, validation of modeling techniques, and evaluation of reduction techniques. Modeling is needed to simulate and predict the noise coupling effects before fabrication. Suppression techniques reduce the effect of noise coupling, and improve performance. The research work presented in this dissertation creates a new and improved noise measurement technique, develops novel noise coupling cancellation techniques, and expands the coverage of prediction methods in architectural stages of the design process.

1.3 Organization

The first chapter presented a background of digital switching noise coupling in mixed-signal SoCs. The rest of the dissertation is organized as follows.

Chapter 2 addresses the noise coupling measurement in mixed-signal SoCs. The importance to measure both substrate and power supply noise is illustrated, while not altering the noise propagation or inject additional noise into the substrate. Also, the complexity of SoCs requires small and compact sensors that can easily be implemented in dense layout regions. Because of the high complexity of SoCs, multiplexing and on-chip measurement processing is desirable. Driven by these

requirements, a technique using compact substrate and power supply sensors and an on-chip digitizing waveform recorder is presented. The performance of an implementation on a 0.13 µm CMOS test chip is evaluated.

Chapter 3 addresses the noise coupling suppression. It is emphasized that propagation reduction by guard ring isolation does not completely eliminate the coupling, and substrate noise exists and varies with physical location inside guard rings. Driven by this result, three proposed substrate noise cancellation circuit structures are presented. Experimental implementation on a 0.13 µm test chip, and the performance evaluation are presented.

Chapter 4 proposes a noise coupling prediction technique focused on the architectural stage of the design process. Previous published modeling techniques are discussed, emphasizing the correlation between accuracy and the stages of design process where they are used. The most accurate techniques require the complete physical layout, which becomes available late in the design process. However, major noise coupling issues found at this stage of the design often require a large amount of rework, which can significantly impact the cost and schedule. Driven by the desire to predict the noise coupling at early stages in the design process, this technique proposes a novel hybrid lumped-distributed model of the substrate, integrated in a macro-model of the overall power distribution on package and PCB.

Chapter 5 draws conclusions and suggests future work in substrate and power supply noise coupling research.

Chapter 2

Measurement of Substrate and Power Supply Noise

2.1 Introduction

In system-on-chip (SoC) applications analog circuits are placed on the same die with high-speed digital processing circuits. The fast switching transients produced by the digital circuits propagate through substrate and power distribution to the analog circuits, degrading their performance. In recent years research has focused on the measurement, modeling, and reduction of noise coupling through substrate [9]-[17], and through substrate and power supply [5], [18]-[20]. Reported measurement techniques implement noise sensors connected to either on-chip, or off-chip instrumentation. Effort has been made for sensors not to affect noise propagation or inject additional noise, and to preserve the signal integrity on the interconnect path to the measurement instrument. Single-ended analog sensors have been reported either based on using p+ substrate contacts [9], or NMOS transistors that sense the substrate noise through the body effect [10]-[11]. Their outputs were routed off-chip to external instruments. While, these sensors can provide accurate measurements for simple test chips, in complex Very Large Scale Integration (VLSI) circuits, the crosstalk and ground bounce due to package parasitics may couple into the single-ended wires altering the results. To reduce these effects, on-chip sampling sensors have been developed [12]-[15]. The digital encoding method implemented by these sensors reduces the measurement contamination due to coupling into the output lines. However, careful attention needs to be given to the layout since additional noise can be injected in the substrate from associated switching circuits, and the supporting clock distribution networks. [16]-[17] present differential amplifier-based analog

sensors, having the inputs capacitively coupled to the substrate and to a reference voltage. The differential path between sensor and measuring instrument reduces the crosstalk and ground bounce coupling, and the analog architecture eliminates the injection of additional noise from switching circuits. However, bandwidth is limited at low frequencies by the input series capacitors, and cannot extend down to low frequencies and zero Hertz (DC). The low frequency substrate noise components resulting from digital switching cannot be neglected [21], and are reported to produce phase noise spurs at the output of LC-tank Voltage Controlled Oscillators [22]-[24]. [25] reports increased cycle jitter of ring oscillators due to low frequency substrate noise, and [26]-[27] investigate the DC and transient substrate coupling effect on latchup. For these applications it is desirable to measure the substrate noise at low frequencies and at DC. Also, the sensors in [12]-[14] and [16]-[17] use both PMOS and NMOS transistors. A common layout practice in PMOS-NMOS designs is to add substrate contacts to reduce noise-coupling effects [28]-[29], and to prevent latch-up [30]-[31]. When used in sensors, these contacts produce additional shunting to ground, altering the substrate noise propagation.

This chapter is organized as follows. Section 2.2 presents a set of requirements for making accurate measurements of substrate and power supply noise. These requirements have been developed based on published measurement techniques and mechanisms of noise generation, propagation, and coupling. A comparison of existing techniques and motivation of the proposed sensors are also presented. Section 2.3 presents the architecture and functionality of the proposed sensors, and the on-chip waveform sampler. Section 2.4 presents the test chips architectures, Section 2.5 the experimental validation of the proposed measurement technique, and Section 2.6 application examples of noise coupling measurements on the test chips. Conclusions are given in Section 2.7.

2.2 Requirements for Making Accurate Measurements and Motivation of the Proposed Technique

The following requirements for making accurate measurements have been developed based on the study of published measurement techniques, and mechanisms of noise generation, propagation, and coupling into sensitive circuits.

1. The sensors and measurement circuits should not affect the noise propagation or inject additional noise into the substrate, or power grid. Since the focus is on studying the noise coupling, if the sensors and measurement circuits change the noise propagation in the region, the results of the study will be corrupted. Typical ways to affect the noise propagation are shunting the substrate to ground through substrate contacts, and injecting additional noise into substrate or power supply from switching circuits.

2. The signal integrity of the sensor output needs to be preserved on the interconnect path to the on-chip or off-chip measurement instruments. Especially in complex SoC chips, noise from the surrounding circuits can couple into the interconnect wires, corrupting the measurement results. Using differential signals cancels out as common mode this coupling. Differential buffers and multiplexers reduce additional noise coupling from power supply, ground, and substrate.

3. The measured bandwidth needs to be high enough to measure the high frequency components of the coupled noise, and also to extend down to zero Hertz to be able to capture the very low frequency components. The high frequency range is usually limited by the technology and by the load capacitance. The low frequency range down to DC is typically limited by series capacitors in the signal path.

4. The sensors need to be small and compact to be easily implemented in complex VLSI circuits.

5. Since the sensitive circuits are affected simultaneously by power supply, ground, and substrate noise, it is desirable to measure all of these components.

6. Since typically the noise measurements are done in various locations across the test chip, it is desirable to be able to multiplex the outputs of the sensors, and thus minimize the number of output pins. The number of available output pins is usually an important constraint in complex SoCs.

Table 2.1 compares previously published measurement techniques, presented in the introduction section, and the proposed technique, which will be presented and analyzed in the rest of this chapter.

Table 2.1: Summary of substrate and power supply measurement techniques

Reported Measurement Techniques / Requirements	[9]	[10]	[11]	[12]	[13]	[14]	[15]	[16]	[17]	Proposed Sensors
Sensors do not affect noise propagation	x	x	x					x	x	x
Sensors do not inject additional noise	x	x	x					x	x	x
Signal is not contaminated from crosstalk or power and ground noise				x		x	x	x	x	x
Bandwidth is enough high to capture switching noise	x	x	x	x	x	x	x	x	x	x
Bandwidth expands down to DC	x	x	x		x					x
Sensors can measure both substrate and power supply noise				x	x		x			x
Sensors are small, compact, and easy to implement in VLSI chips.	x	x	x	x	x		x	x	x	x
Sensors can be multiplexed on-chip		x	x	x	x		x	x	x	x

It can be noticed that each type of sensor satisfies part of the requirements, but none of them satisfies all requirements. Thus, most of the sensors can be used only in specific

applications where the not satisfied requirements do not impact the accuracy of the measurement. However, in mixed-signal SoC applications in order to make accurate measurements and not interfere with the noise generation and propagation, the sensors need to satisfy all the requirements. Hence, it is desirable to develop new substrate and power supply sensors that address all the above-mentioned requirements. The proposed technique, which is compared with the previous reported sensors in the last column of Table 2.1, uses a PMOS-based differential substrate sensor, DC coupled to the substrate. The DC input coupling allows the bandwidth to be extended down to zero Hertz, the differential architecture reduces the signal contamination from crosstalk and ground bounce, and the PMOS-based structure reduces the shunting through substrate contacts. N-well contacts also provide shunting to AC ground, but this effect is smaller because of the intervening junction capacitance. A separate PMOS-based differential sensor is used to measure the power supply noise. Both sensors are physically implemented in the same N-well, creating a small compact structure easy to be embedded within high-density SoC designs. The outputs are routed to either an external instrument or to an on-chip waveform sampler. In both cases the signal is routed through differential circuits to reduce the parasitic coupling from the rest of circuitry on the chip. The interface to the external instrument is done through a buffer amplifier, which provides 50 O output impedance. This is necessary to avoid transmission line reflections when connecting the external instrument through 50 O characteristic impedance cables. The on-chip waveform sampler converts the analog signal into digital data. The digital data are much less sensitive to crosstalk and ground bounce, and can be routed off-chip without significant signal contamination. On-chip samplers using differential latched comparator controlled by three-phase clocks have been reported in [12], and using single ended chopper-type comparators controlled by four-phase clocks in [13]. Both measure the input noise by comparing it to a single ended type reference voltage. The proposed sampler is controlled by a one-phase differential clock, and measures the differential noise input by comparing it to a differential reference voltage. Using one-phase clocking reduces the complexity of clock distribution circuits, and thus eliminates as much as possible

the additional noise injected by these circuits. Using a differential reference voltage reduces the contamination from crosstalk and ground bounce coupling. To avoid noise injection into substrate and power supply, the waveform sampler needs to be placed far from sensors, and isolated using a guard ring.

2.3. Description of the Proposed Substrate and Power Supply Measurement Technique

The proposed noise measurement technique uses substrate and power supply sensors having their outputs multiplexed and routed to either an internal waveform sampler or to an external instrument. This section describes the architecture and functionality of the sensors and waveform sampler.

2.3.1 Substrate Sensor

The substrate sensor, shown in Figure 2.1, has differential structure and contains only PMOS transistors.

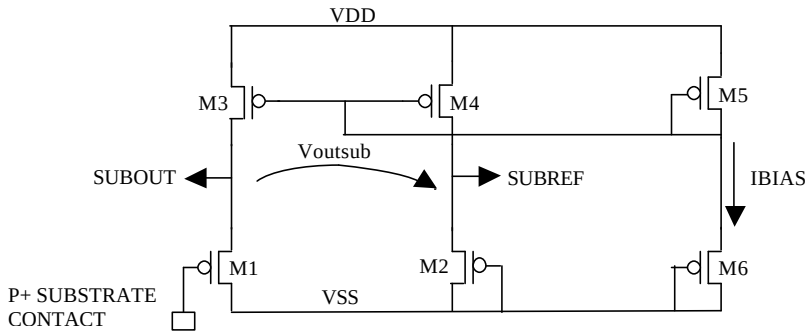


Figure 2.1: Schematic of the substrate sensor and local bias circuit.

The substrate sensor consists of two branches made of same size transistors *M1*, *M3*, and *M2*, *M4*, and a bias generator made of *M5* and *M6*. The inputs are the gates of *M1* and *M2*, one connected to a p+ substrate contact, and the other to ground. Since there are no series decoupling capacitors, the bandwidth extends down to DC. The outputs are taken from the sources of *M1* and *M2*. Assuming from a DC perspective that the substrate potential at one of the inputs is close to the local ground at the other input, the gates of *M1* and *M2* are both at the ground potential, and the output voltages are equal. The output common mode voltage depends on the size of *M1* and *M2*, and the bias current generated by *M5* and *M6*, which mirrors into *M3-M1* and *M4-M2* branches. A simplified calculation of the common mode voltage is given by:

$$Voutsub\_cm = \sqrt{\frac{2Ibias}{mCox\frac{W}{L}}} + |Vth| \qquad (2.1)$$

where Ibias is the generated bias current in the *M5-M6* branch, μ is the hole mobility, *Cox* is the oxide capacitance, *W* and *L* are the width and length of *M1* and *M2*, and *Vth* is the threshold voltage. The voltage gain has been calculated using the small signal model, shown in Figure 2.2.

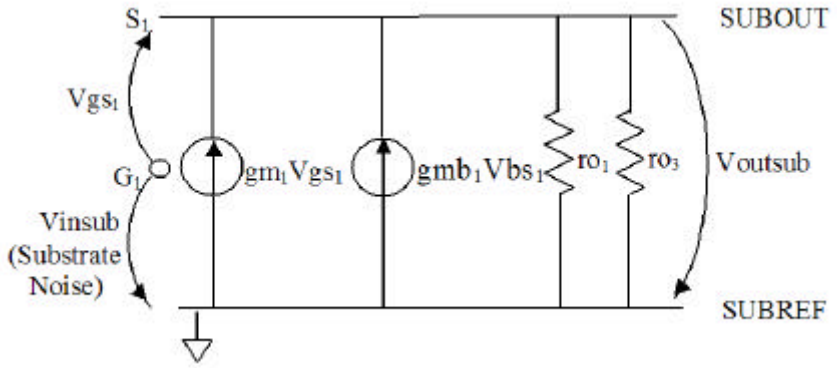


Figure 2.2: Small signal model of the substrate sensor

From an AC perspective the *SUBREF* node does not vary with the substrate, thus in terms of the voltage gain calculation it can be assumed to be a virtual ground.

$$Voutsub = Vinsub \frac{gm1(ro1 // ro3)}{1 + (gm1 + gmb1)(ro1 // ro3)} \tag{2.2}$$

Since both *M1* and *M3* operate in saturation,

$$(gm1 + gmb1)(ro1 // ro3) >> 1 \tag{2.3}$$

thus the voltage gain can be approximated with

$$\frac{Voutsub}{Vinsub} = \frac{gm1}{gm1 + gmb1} \tag{2.4}$$

which is close to unity. The rejection of power supply noise is achieved by using a symmetrical architecture. The noise on the power supply produces variations of the current through the *M5* and *M6* transistors, current that mirrors into *M3*-*M1*, and *M4*-*M2* branches. Since these branches are identical, the current variation couples only as common mode at the two outputs. Thus, the power supply noise coupled into the differential output is reduced. Multiple sensors can be multiplexed to study the variation of noise across the chip. Since the unity voltage gain does not significantly depend on the bias currents, the mismatch between the bias generator transistors among multiple sensors have little effect on their voltage gain. Thus, using local bias generators when implementing multiple sensors does not significantly affect the performance, but eliminates additional bias distribution wires, and the potential contamination from extra noise coupling on these wires

2.3.2 Power Supply Sensor

The power supply sensor, shown in Figure 2.3, consists of *M7-M8* and *M9-M10* branches, biased at equal currents.

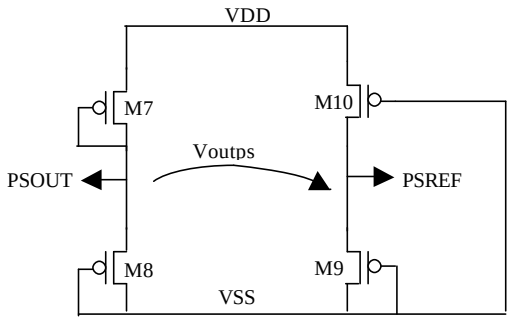


Figure 2.3: Schematic of the power supply sensor

M7, *M8*, and *M9*, identical size in diode-connected configuration, operate in saturation, and *M10*, having *Vgs10-Vds10 = Vgs9 > Vth*, in triode region. *M10* is sized from the condition to have equal bias currents through the two branches. Since *M8* and *M9* are identical, equal bias currents result in equal voltages at *PSOUT* and *PSREF* outputs. The size of *M10* has been calculated using the quadratic equations for the drain current in triode and saturation regions, and approximating PSOUT and PSREF voltages equal to *0.5Vdd*. The result is shown in Equation 2.5, where *W* and *L* are the width and lengths of the transistors, *Vdd* is the power supply voltage, *Vth* is the threshold voltage.

$$\left(\frac{W}{L}\right)_{10} = \left(\frac{W}{L}\right)_{7} \frac{\left(\frac{1}{2}Vdd + Vth_{7}\right)^{2}}{Vdd\,(Vdd + Vth_{10}) - \frac{1}{4}Vdd^{2}} \qquad (2.5)$$

The transfer function has been calculated using the simplified small signal model of the sensor in Figure 2.4, and is shown in Equation 2.6.

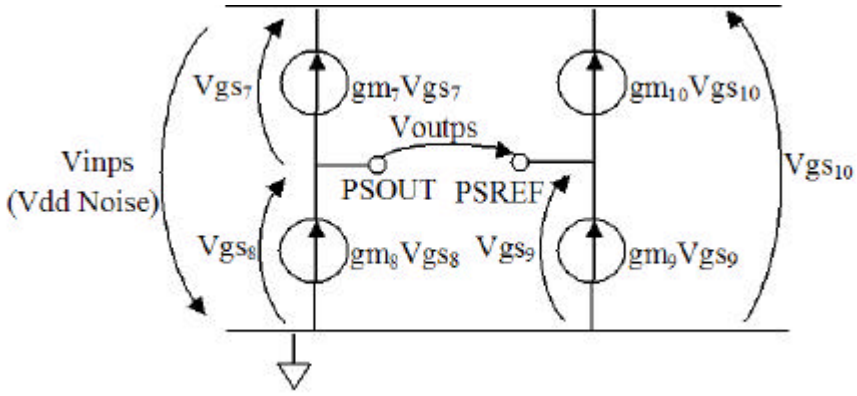


Figure 2.4: Small signal model of the power supply sensor

$$Voutps = Vinps\left(\frac{gm7}{gm7+gm8} - \frac{gm10}{gm9}\right) \tag{2.6}$$

In the current implementation the diode-connected transistors, *M7*, *M8*, and *M9*, have *W*=1.2 µm, and *L*=130 nm, and *M10* *W*=850 nm and *L*=770 nm, resulting in *gm7*= *gm8*=*gm9*=5*gm10*. Inserting this condition in (2.6), the differential output of the sensor *Voutps*=0.3*Vinps*. Thus the differential output measures the power supply noise with a gain lower than unity. For equal sizes *M7*, *M8*, and *M9*, and equal bias currents, the common mode output voltage can be approximated as *Voutps_cm*= *0.5Vdd*. The layout requires special attention from the perspective of common-mode suppression, which is effectively addressed using symmetric placement, transistor matching, and balanced bus differential interconnects.

2.3.3 Waveform Sampler

The on-chip waveform sampler converts the analog measurement into digital data by successive comparisons with an external programmable reference voltage. The digital data are much less sensitive to crosstalk and ground bounce, and can be routed off-chip without significant signal contamination. Repeated measurements create a sequence of samples from which the analog waveform is reconstructed. This method can be used only if the injected noise is a periodic signal, which can be achieved by running periodic patterns in the digital core of the SoC. Figure 2.5 shows the block diagram of the waveform sampler.

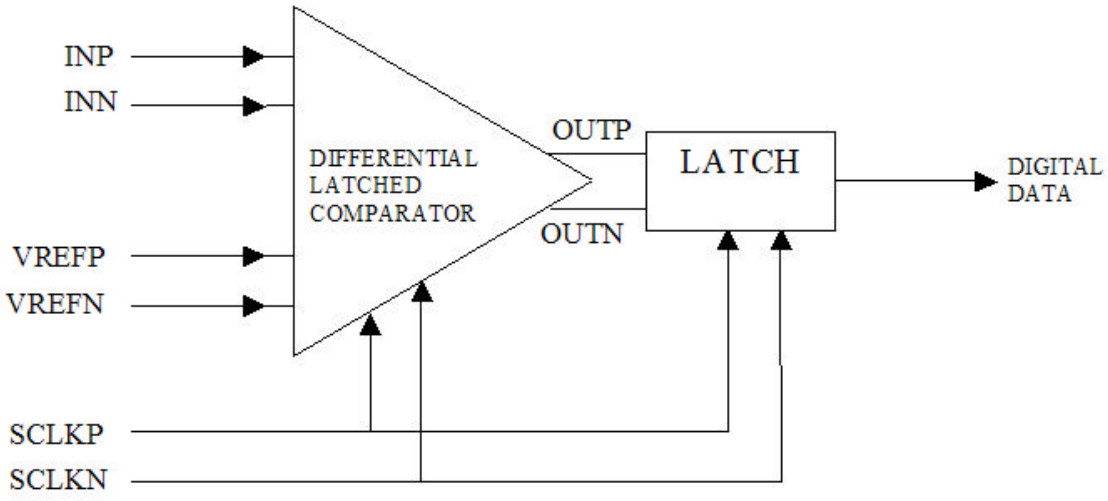


Figure 2.5: Block diagram of the waveform sampler

The differential input, *INP-INN*, and the differential reference signal, *VREFP-VREFN*, are connected to a latched comparator. The output of the latched comparator is connected to a second latch circuit, the two latches forming a flip-flop circuit. To reduce the noise injected by the clock distribution circuits, both latches use differential clocks. In addition, special attention needs to be given regarding layout to avoid the coupling of the clock into comparator. The programmable reference voltage, provided externally, is a differential signal, this way reducing the contamination from ground bounce and crosstalk coupling. Figure 2.6 shows the schematic and timing diagram of the waveform sampler.

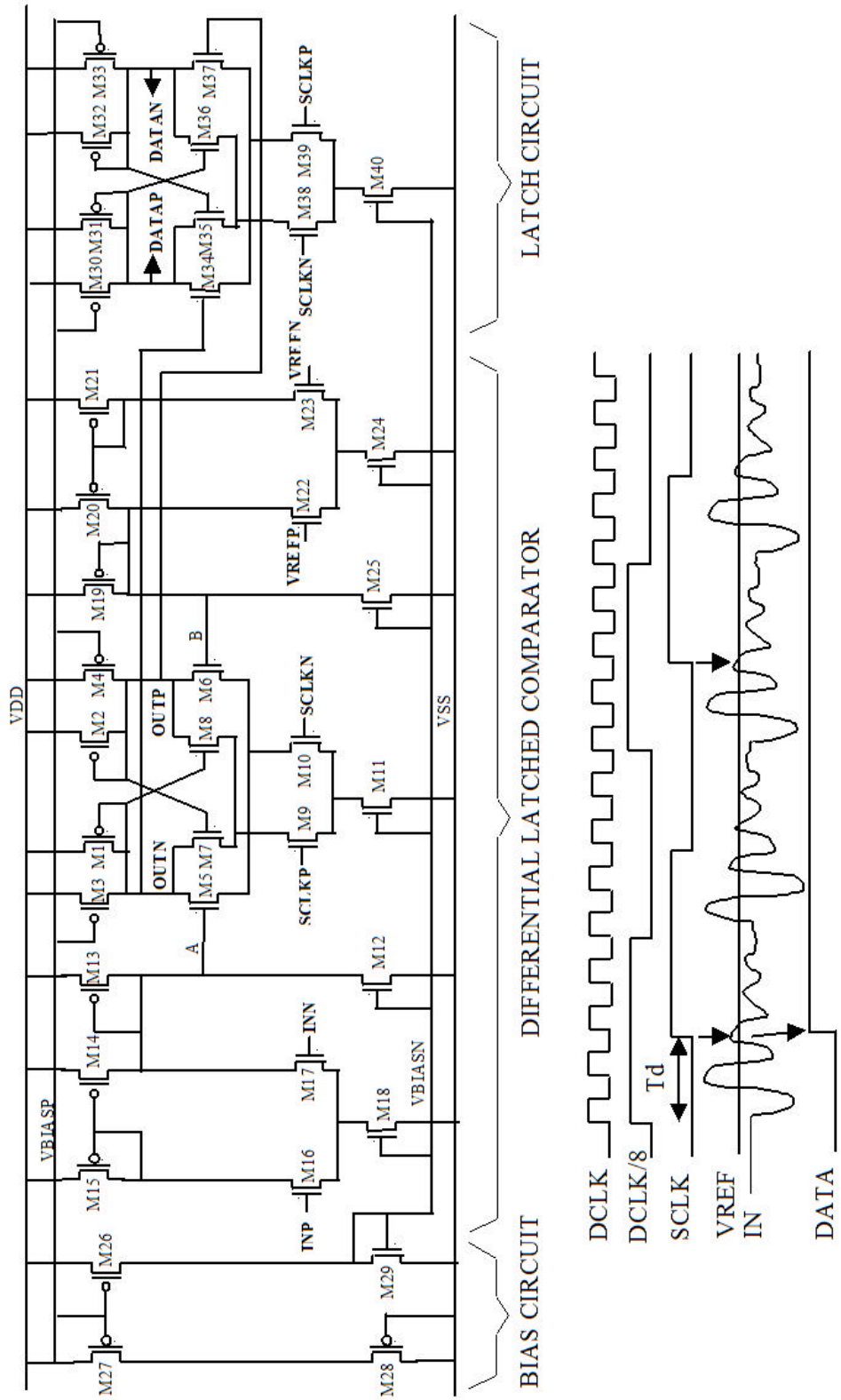


Figure 2.6: Schematic and timing diagram of the waveform sampler

When the clock is low, the comparator operates in transparent mode, and the output equals:

$$Vout = OUTP - OUTN = Av \cdot [(INP - INN) - (VREFP - VREFN)] \qquad (2.7)$$

where *Av* is the comparator gain. In this implementation a low gain of about 5 provides enough amplification to be able to latch the outputs. The gain can be estimated using the simplified equation,

$$Av = \frac{gm17 \cdot gm5}{gm13 \cdot gm1} \qquad (2.8)$$

where the output resistances of the transistors have been neglected. When the clock is high the comparator latch mode is activated; the output is set to either the positive or negative differential rail corresponding to the positive or negative *Vout* at the time of the clock rising edge. The second latch holds the output data during clock low, when the comparator operates in transparent mode. Referring to the timing diagram in Figure 2.6, the analog input *IN* is compared with *VREF*, and the result latched on the rising edge of the sampling clock *SCLK*. *SCLK* is a divided version of the digital core clock *DCLK*, shown here as *1/8*, and has programmable delay *Td*. This way *SCLK* is synchronized with the switching noise generated by the digital core. For a fixed *Td* the *IN* level is sampled by successive comparisons sweeping *VREF*. Repeated samples sweeping *Td* create a time-voltage table from which the input waveform can be reconstructed.

2.4 Test Chips

2.4.1 Introduction

The evaluation experiments of the proposed measurement technique have been implemented on three test chips built in 0.13-µm CMOS flip-chip technology on a lightly doped substrate. The test chips have been mounted on BGA ceramic packages, and placed on a test board for characterization. The first test chip was a new design, and the following ones were redesigns of the first one. The size, package, and infrastructure circuits are the same for all test chips. This has allowed the same characterization fixture to be used for all test chips. Besides the noise coupling experiments, the test chips included high-speed timing generators and data recovery circuits, which were not part of this research work, and thus are not covered in this dissertation. The noise coupling experiments have been focused on substrate and power supply noise measurement, noise coupling suppression, and noise coupling prediction. The first test chip consisted in experiments focused on validation of the substrate and power supply sensors, and the waveform sampler. The second test chip fixed a clock coupling problem into the waveform sampler, and implemented more noise propagation experiments. The third test chip focused on noise coupling suppression experiments. Coupling prediction has been developed based on experiments implemented in all three test chips.

2.4.2 Test Chip 1

2.4.2.1 Block Diagram

Figure 2.7 shows the block diagram of the substrate and power supply noise measurement circuit as it was implemented in the first test chip. The experiment includes sixteen pairs of sensors, each pair made of one substrate and one power supply sensor. The outputs of these sensors are multiplexed and sent to both an on-chip waveform sampler, and an external oscilloscope. The connection to the external oscilloscope has been done through an amplifier and a source follower differential output stage. The noise is injected into substrate and power supply by digital noise emulators (DNE), and by p+ substrate contacts. Both DNE and p+ noise injector substrate contacts are driven from an external signal generator. Besides the sensors, direct probing of the power supply, ground, and substrate has been also implemented. The direct probing of the substrate has been done through p+ substrate contacts, and the direct probing of power and ground through sense wires routed off-chip. The architecture and functionality of the sensors and waveform sampler have been presented in a previous section. The architecture and functionality of the multiplexers, buffers, output stage, and DNEs are based on typical differential stages, and will be described in the following section.

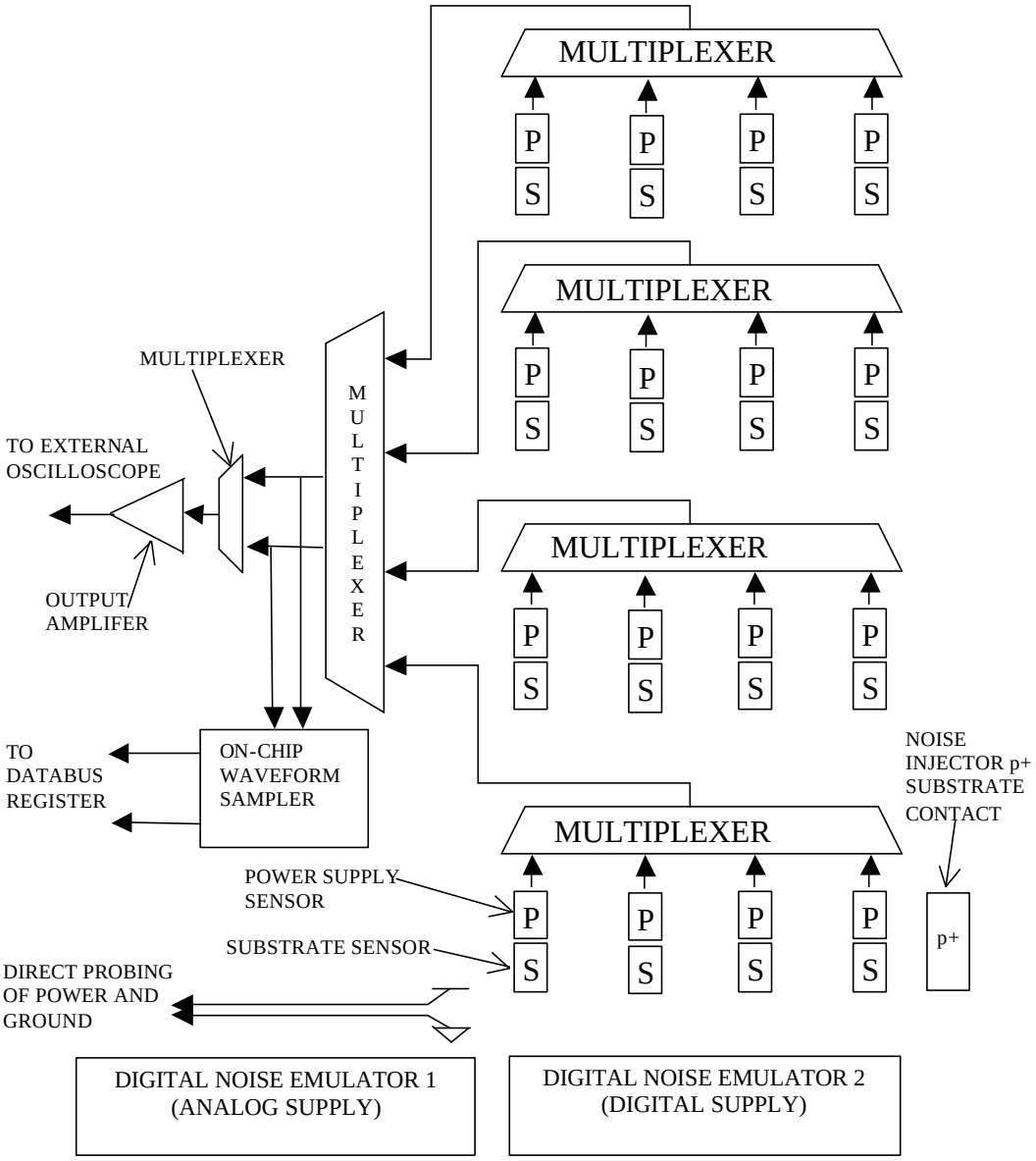


Figure 2.7: Block diagram of the substrate and power supply noise measurement circuit implemented in Test Chip 1

2.4.2.2 Support Circuits

Support circuits are needed to connect the outputs of multiple sensors to the measurement instruments. Differential stages have been used on the signal path to reduce the contamination from crosstalk and ground bounce. The differential stages

operate at constant current, thus minimizing the noise injection into supply and ground.

2.4.2.2.1 Differential Multiplexer

The multiplexer has a conventional differential stage structure, and achieves switching by turning on/off the bias currents of the input stages. The schematic is shown in Figure 2.8

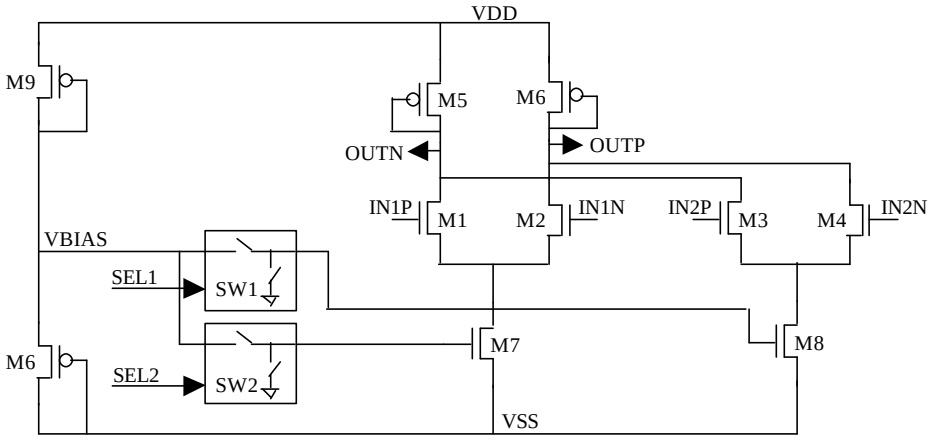


Figure 2.8: Schematic of the differential multiplexer implemented in Test Chip 1

The select inputs, *SEL1* and *SEL2*, control the switches *SW1* and *SW2*, which connect the bias voltage, *VBIAS*, to either *M7* or *M8*. The differential input stage receiving the bias voltage becomes active, while the other stage remains inactive. The *M8-M9* branch generates the bias voltage locally. An issue with this approach is the dependence of the differential pair bias current on the *M6* threshold voltage. Redesigning the bias branch to use NMOS transistors can reduce this dependence. Also, the gate to drain capacitance of the differential pair transistors may provide a feed-through path at high frequency for the unselected input.

2.4.2.2.2 Differential Buffer

Figure 2.9 shows the schematic of the buffer. Similar to the multiplexer, the buffer has a conventional differential pair structure, and a local bias generator made of transistors *M6* and *M7*.

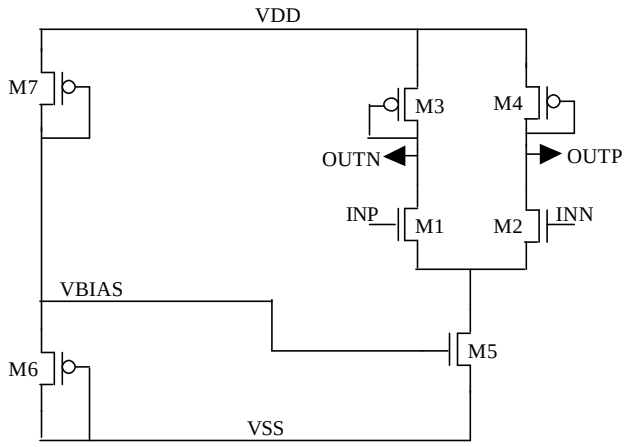


Figure 2.9: Schematic of the differential buffer implemented in Test Chip 1

2.4.2.2.3 Output Amplifier

The output stage consists of two source follower NMOS transistors, sized to provide 50 O output impedance. The 50 O output impedance is needed to minimize transmission line reflections on the coaxial cables connecting to the oscilloscope.

2.4.2.2.4 Digital Noise Emulators

The digital noise emulator (DNE) consists of a chain of four stages of inverters increasing in size linearly. Driven by an external signal, the DNE generates digital switching noise which couples into substrate and power supply. The DNE also contains an NMOS transistor connected between power supply and ground. Driven by an external signal this transistor shorts the power and ground with a current of about

60 mA. Because of the non-zero impedance of the power and ground grids, the shorting current generates variations of the local power supply voltage. This voltage variation emulates noise on the power supply.

2.4.2.3 Physical Layout

The noise coupling experiments have been implemented in an IBM 0.13µm CMOS test chip, which also included other experiments not related with this research. The chip dimensions are 4800 µm by 4200 µm, and the noise coupling experiment dimensions are 250 µm by 240 µm. Figure 2.10(a) shows the die photo of the test chip with the experiment region highlighted, and Figure 2.10(b) shows the physical layout of the test chip.

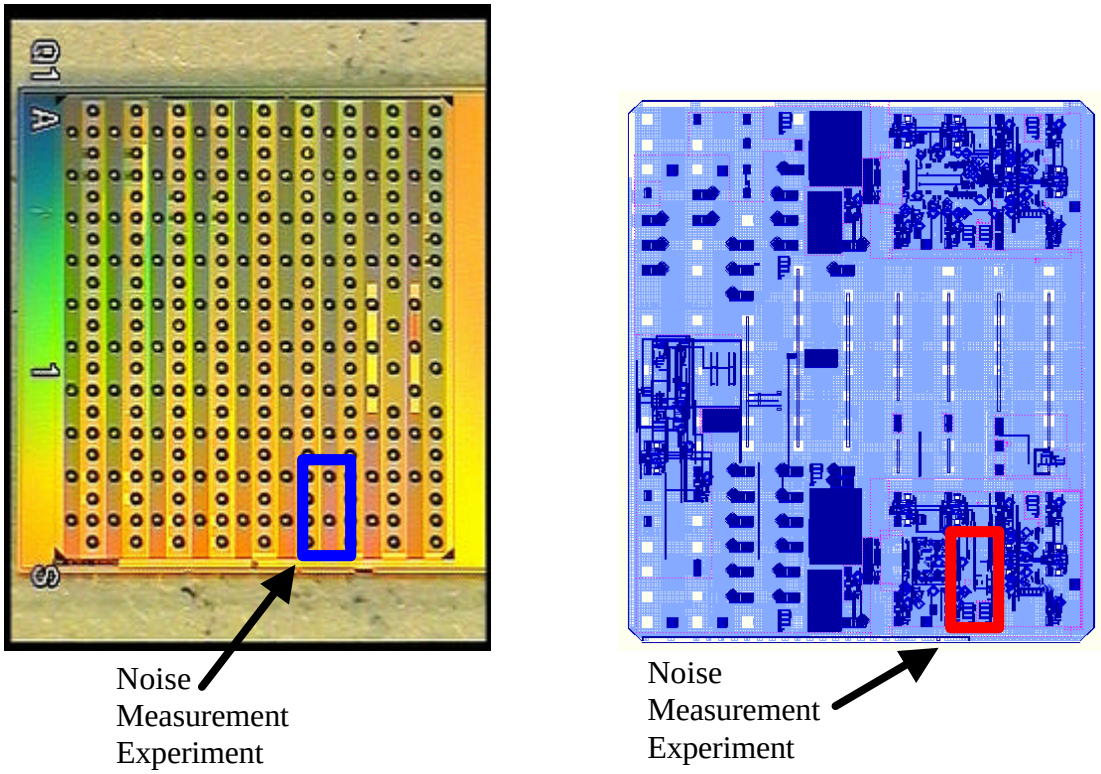


Figure 2.10: (a) Microphotograph of Test Chip 1, and (b) physical layout

The physical structures are covered by seven layers of metal, and are not visible in the die photo even with magnification. Figure 2.11 shows the physical layout of the experiments.

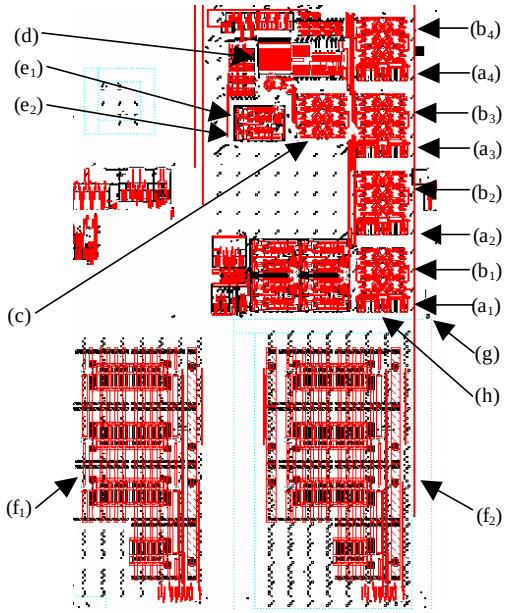


Figure 2.11: Physical layout of the substrate and power supply noise measurement experiment implemented in Test Chip 1.

The experiment implements four groups of sensors (a_1)-(a_4), each group containing four substrate and four power supply sensors. The four groups are connected to multiplexer blocks (b_1)-(b_4). The output signals of these multiplexers are connected to another multiplexer (c) which selects the signal for the output buffer (d). The same signals are connected to the waveform samplers (e_1) and (e_2). The noise injection is provided by two blocks, (f_1) and (f_2), each block containing seven DNEs. Substrate noise is also injected through the p+ substrate contact (g). The p+ substrate contact has been sized to have a 50 Ω input resistance, thus providing a matched termination when driven using 50 Ω characteristic impedance cables. Direct probing of ground and power supply (h) are placed near group 1 of sensors. Additional direct probing sensors and DNEs are placed in other locations of the test chip, outside of this experiment. Details about these sensors and DNEs will be presented in the noise coupling prediction chapter.

2.4.3 Test Chip 2

Figure 2.12 shows the block diagram of the experiments implemented in Test Chip 2. The architecture is similar to Test Chip 1, by multiplexing the sensors signals and routing the output to an internal waveform sampler and an external oscilloscope.

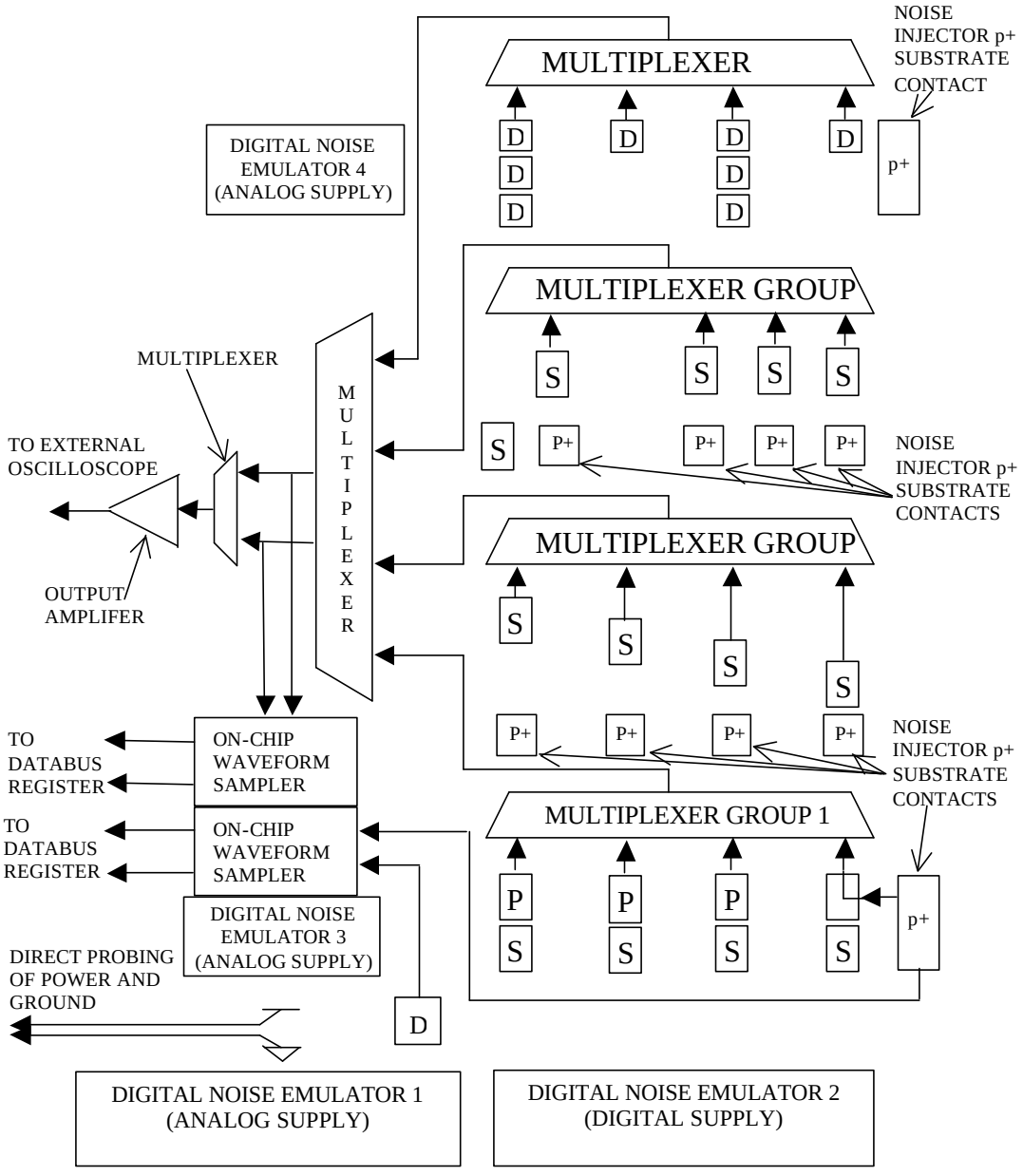


Figure 2.12: Block diagram of the experiments implemented in Test Chip 2

The differences from Test Chip 1 consist of new substrate noise propagation experiments implemented in the four groups of sensors, two additional DNEs placed close to group 1 and 4 of sensors, a redesigned waveform sampler that fixes a clock coupling issue, reversed multiplexers and buffers made only of PMOS transistors, and a study of noise coupling effects on imbalanced differential amplifier stages. An imbalanced amplifier consists of two cascaded differential stages, each having one of the differential pair transistors physically placed inside a guard ring. Substrate noise is attenuated inside the guard ring, thus coupling more into one transistor of the differential pair than into the other. Figure 2.13 shows the physical layout of the experiments implemented in Test Chip 2.

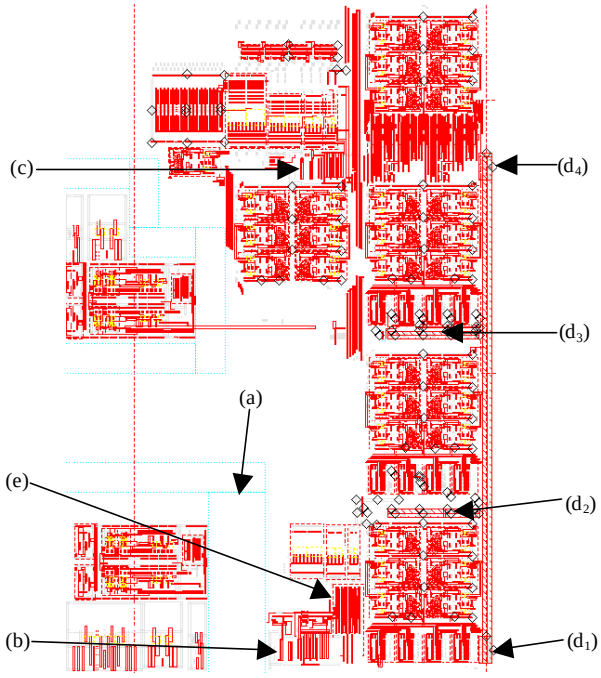


Figure 2.13: Physical layout of the substrate and power supply noise measurement experiment implemented in Test Chip 2.

The multiplexers, buffers and output stage are placed identical as in Test Chip 1. The waveform samplers are isolated using high resistive substrate guard rings also named

MOAT (a). The new DNEs, (b) and (c), are placed close to sensor groups 1 and 4. P+ noise injection substrate contacts are placed in locations (d_1), (d_2), (d_3), and (d_4). Each group of sensors implements different substrate noise propagation experiments. A detailed description of each experiment will be presented in the results section. The imbalanced amplifiers experiment has been implemented in group 4 of sensors, and one imbalanced amplifier (e) has been placed near DNE3 (b). The output of this amplifier has been routed directly to a waveform sampler.

2.4.4 Test Chip 3

Figure 2.14 shows the block diagram of the experiments implemented in Test Chip 3. The architecture is similar to Test Chips 1 and 2, by multiplexing the outputs of four sensor groups, and routing the outputs to an on-chip waveform sampler and to an off-chip measurement instrument.

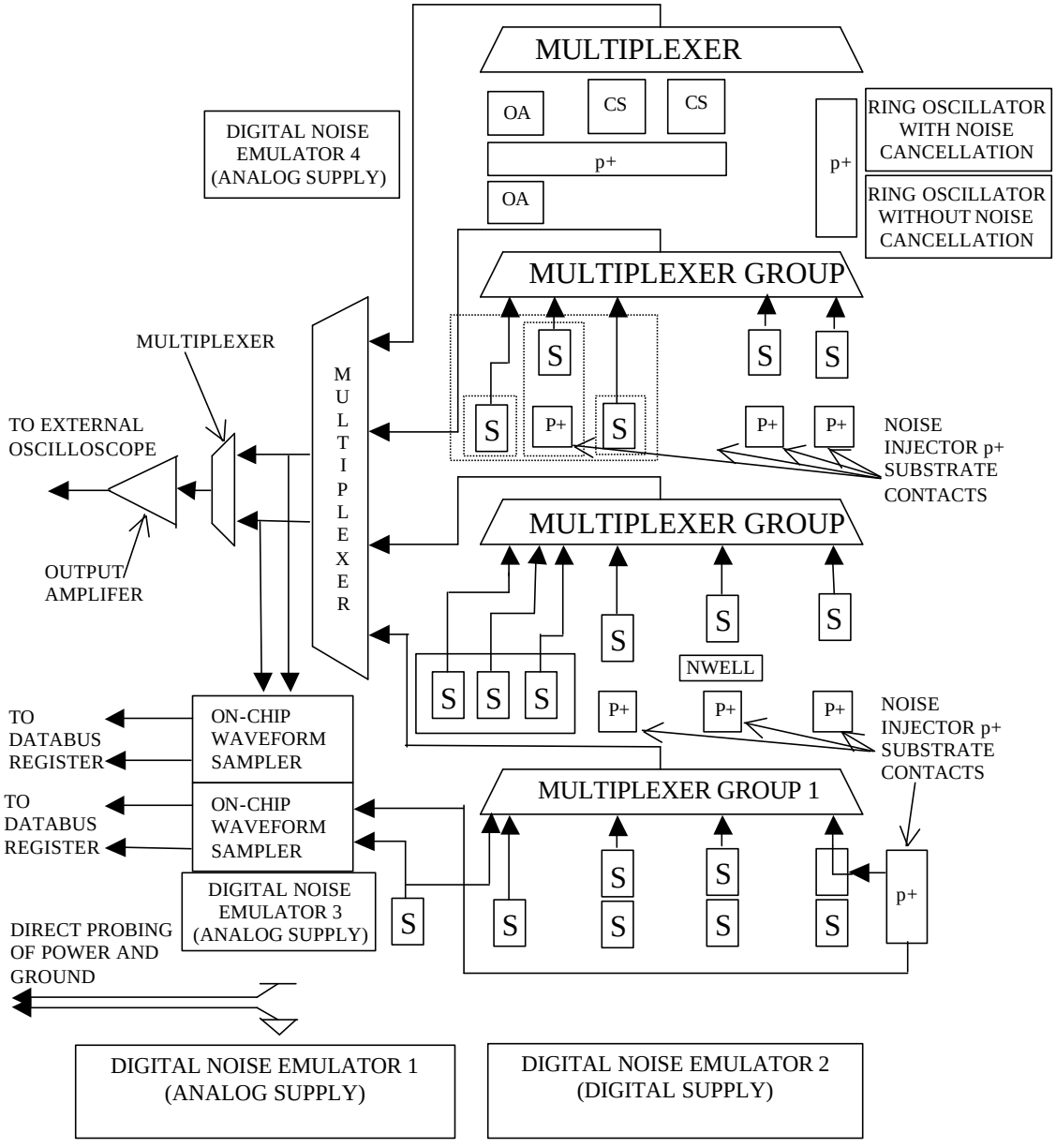


Figure 2.14: Block diagram of the experiments implemented in Test Chip 3.

Figure 2.15 shows the physical layout of the experiments implemented in Test Chip 3. The new experiments focus on noise suppression through guard rings (a) and active noise cancellation structures (b). One active noise cancellation circuit has been implemented in the delay cells of a ring oscillator (c). For comparison, a ring oscillator without noise cancellation has also been implemented (d).

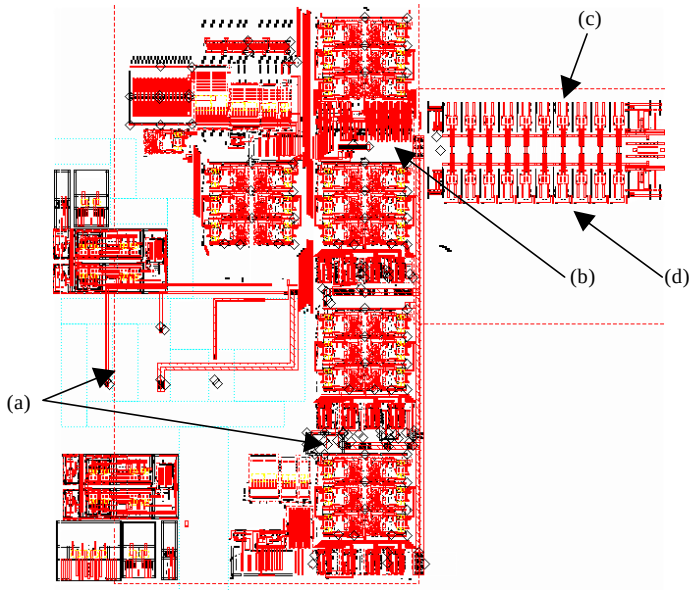


Figure 2.15: Physical layout of the substrate and power supply noise measurement experiment implemented in Test Chip 3.

The new guard ring experiments are using sensors in groups 2 and 3, and the active compensation techniques are using sensors in group 4. The two ring oscillators have the outputs connected to the multiplexer of group 3 and routed to the external oscilloscope. Details about the noise suppression experiments will be presented in the noise suppression chapter.

2.5 Experimental Results

2.5.1 Test Bench and Measurement Setup

Figure 2.16 shows the block diagram of the test bench characterization setup. The test chip has been placed on a test board in a temperature-controlled socket, and powered from an external power supply. An HP8133A pulse generator provides the clock signal for the waveform sampler, and a DAC board inside the computer provides the programmable voltage reference for the latched comparator. The computer also controls the registers inside the test chip through a parallel interface. Two 50 O input channels of the Tektronix TDS8200 oscilloscope probe the differential analog outputs. The HP8133A pulse generator also drives the DNEs or inject noise into the substrate through the p+ contacts. For some of the experiments an HP8665A signal generator, or an HFS9003 stimulus system have been used instead of the HP8133A pulse generator.

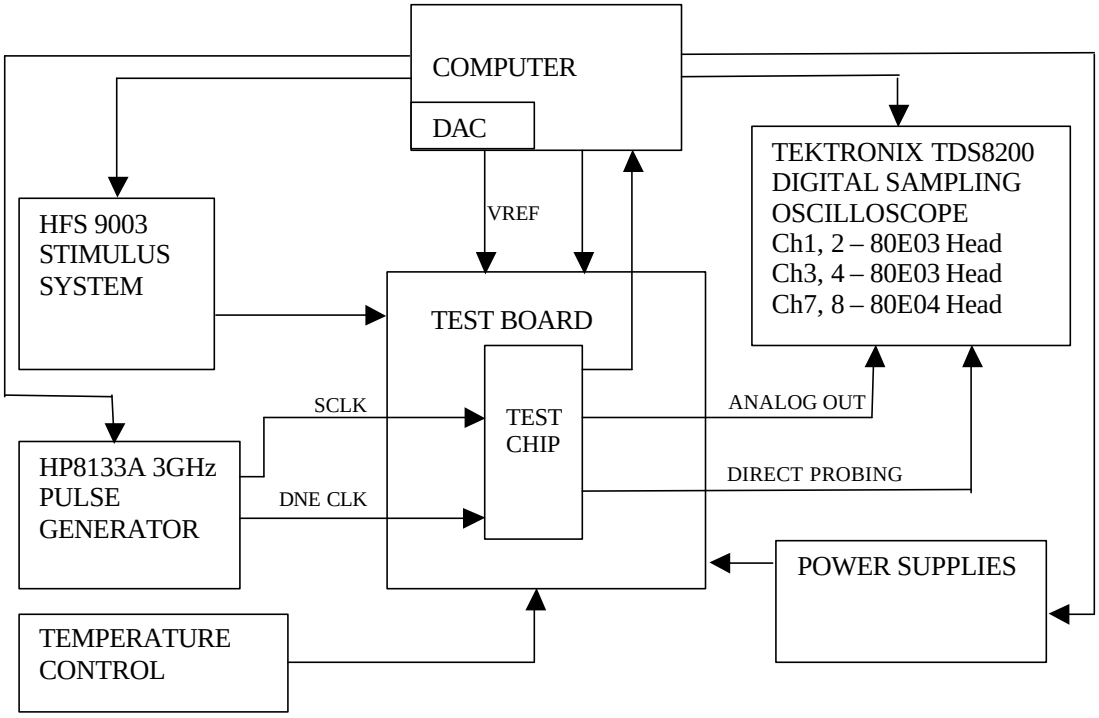


Figure 2.16: Block diagram of the test bench characterization setup.

Figure 2.17 shows a picture of the characterization bench. The test chip is placed in a thermally controlled socket part of the test board shown in the middle of the picture. The HFS9003, power supplies, and a multimeter are placed on the shelf. The rest of instruments are on the main table. The computer is not shown in this picture.

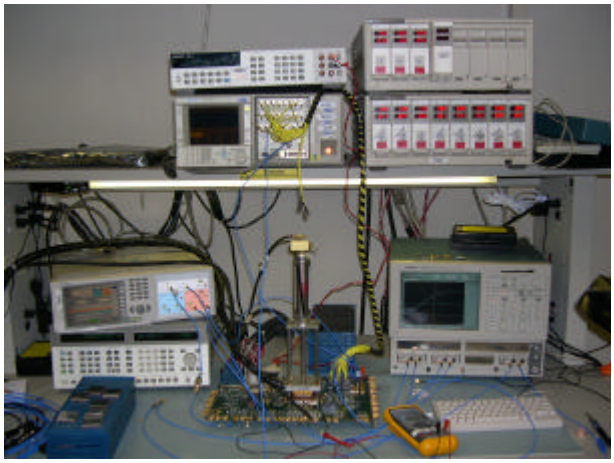


Figure 2.17: Photograph of the test bench characterization setup.

The test chip has been controlled from the computer using a Visual Basic program. Figure 2.18 shows the Visual Basic control panel.

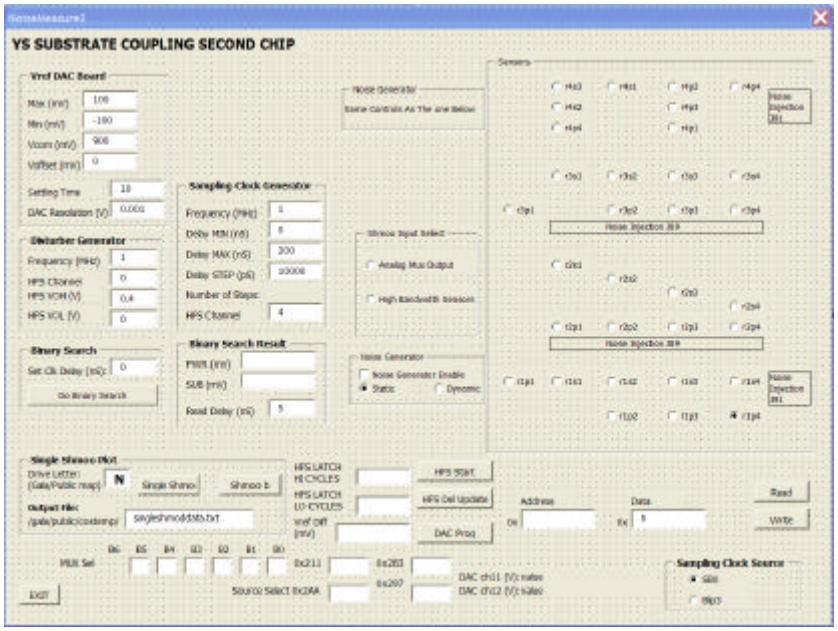


Figure 2.18: Visual Basic panel for controlling the noise measurement experiment.

This panel controls the registers, analog multiplexers and waveform sampler circuits.

2.5.2 Measurement Methods

The measurements have been performed at the board level with an oscilloscope and internally with the on-chip waveform sampler. In the external measurements, the sensors outputs have been routed differentially to two inputs of the oscilloscope through multiplexers, buffers, and the source follower output stage. Thus, the measured values include the parasitic effects of all these stages of the signal path. Using source termination at the test chip output stage, and load termination at the oscilloscope, has reduced the transmission line reflections. The differential measurement has been achieved by subtracting the waveform of one channel from the other. The subtraction function is embedded in the TDS8200 oscilloscope, thus the displayed waveform represented the difference between the two input channels. Because of the double transmission line termination, the signal seen by the oscilloscope equals one half of the signal driving the source follower buffer. The measured output impedance of the source follower stage equals 38 O and not 50 O, thus the actual attenuation factor is 0.6 not 0.5. All the measurements have been adjusted by this attenuation factor. The bandwidth of the off-chip measurement path has been limited to 450 MHz mainly because of the source follower output stage. As it will be shown later, the bandwidth of the on-chip waveform sampler expands to 3 Ghz. Because of the bandwidth limitation, the external oscilloscope has been used mainly for troubleshooting purpose, and in some low frequency high resolution measurements. Figure 2.19 shows an example of the sampled waveform measured by substrate sensor 4 of group 1 in Test Chip 2, obtained with 25 mV square pulse noise injected into the p+ contact.

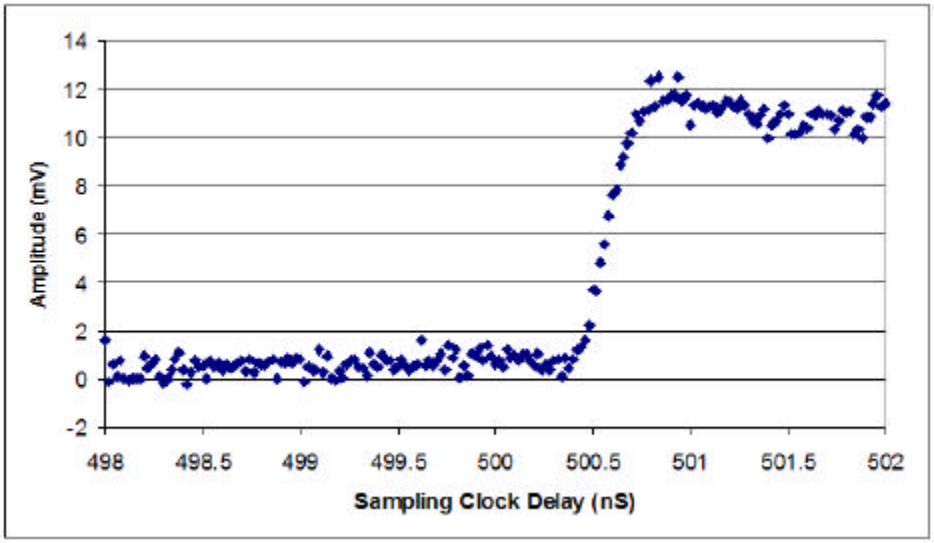


Figure 2.19: Example of waveform at substrate sensor 4, obtained with 25 mV square pulse noise injected into the p+ contact.

It can be noticed that the waveform has an amplitude of 10mV, a rise time of 200 ps, and an overshoot of about 8%. About 1 mV peak-to-peak noise is seen on the high and low levels. This plot shows that the main components of a transient waveform can be measured with the on-chip sampler.

2.5.3 Characterization of Substrate and Power Supply Sensors

This section presents the characterization of the substrate and power supply sensors, which covers the evaluation of voltage gain, linearity, frequency response, and sensitivity to measurement corruption from crosstalk and ground bounce.

2.5.3.1 Evaluation of Sensors Voltage Gain

The gains of the substrate and power supply sensors have been measured using the setup shown in Figure 2.20.

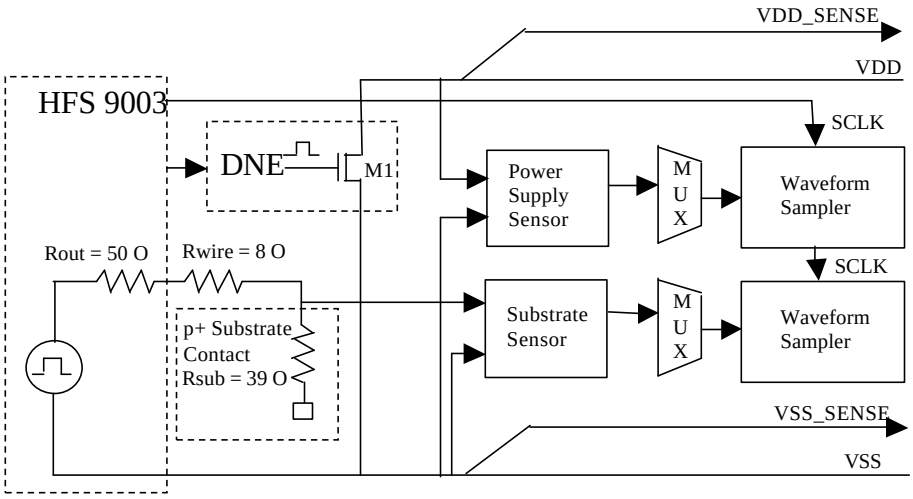


Figure 2.20: Block diagram of the sensors gain measurement setup.

Substrate and power supply sensors are connected through multiplexers to two waveform samplers. The substrate sensor has been modified by removing its own p+ substrate contact, and connecting the corresponding input to the p+ substrate contact used for noise injection. Thus the amplitude at the substrate sensor input can be determined by a resistor divider scaling, as shown in the block diagram. The power supply sensor probes the local power grid. To measure the input into the power supply sensor a sense wire for power, *VDD_SENSE*, and a sense wire for ground, *VSS_SENSE*, have been routed to the external oscilloscope.

The gain of the substrate sensor has been measured by injecting a 200 mV square wave signal into the p+ substrate contact using the HFS9003 stimulus system. Due to the resistor divider effect of the HFS9003 output impedance, *Rout* = 50 O, on-chip wire resistance, *Rwire*=8 O, and p+ substrate contact impedance, *Rsub* = 39 O, the amplitude at the sensor input equals *Vin* = 80.4 mV. The measured amplitude using the waveform sampler was *Vout* = 74 mV. From these measurements, the combined gain of substrate sensor, signal path, and on-chip sampler can be calculated as *Gsub*= *Vout*/*Vin* = 0.92.

The gain of the power supply sensor has been measured by injecting a square wave voltage pulse into the local power supply grid. This has been achieved by shorting the

power and ground grids through the NMOS transistor *M1*. The amplitude of the injected signal was *Vin* = 4.8 mV, measured with an external oscilloscope between the power supply and ground sense lines. The measured amplitude using the waveform sampler was *Vout* = 1.25 mV. An average of 100 points has been used in the measurement of *Vout* to reduce the error due to the random noise of the sampling comparator. Thus, the combined gain of power supply sensor, signal path, and on-chip sampler can be calculated as *Gpwr* = *Vout*/*Vin* = 0.26.

2.5.3.2 Evaluation of Sensor Linearity

The sensor's linearity has been evaluated using the on-chip waveform sampler. A square wave pulse of 100 MHz and variable amplitude has been injected in the p+ substrate contact in Test Chip 1. The measurements have been done on sensor 4 of group 1, located 25 µm apart from the p+ noise injector contact. The linearity error is shown in Figure 2.21.

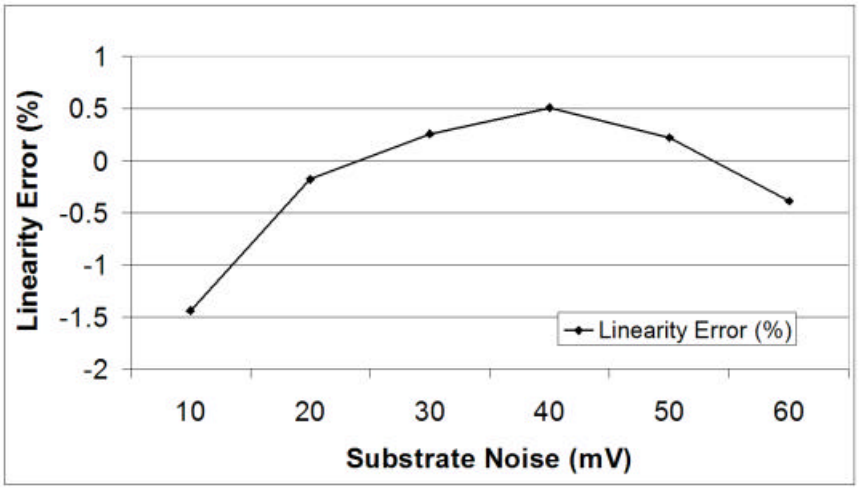


Figure 2.21: Linearity error of substrate sensor 4 with 100 MHz square pulse injected into the p+ contact.

Linearity better than 1.5% has been measured for substrate noise amplitudes between 10 mV and 60 mV. The linearity of the power supply sensor has been measured by injecting a square wave noise signal into the power supply grid using DNE1 and measuring the waveform of sensor 4 in group 1, located 200 µm form the DNE. Figure 2.22 shows between +/- 6% linearity error for injected noise amplitudes between 1 mV and 5 mV.

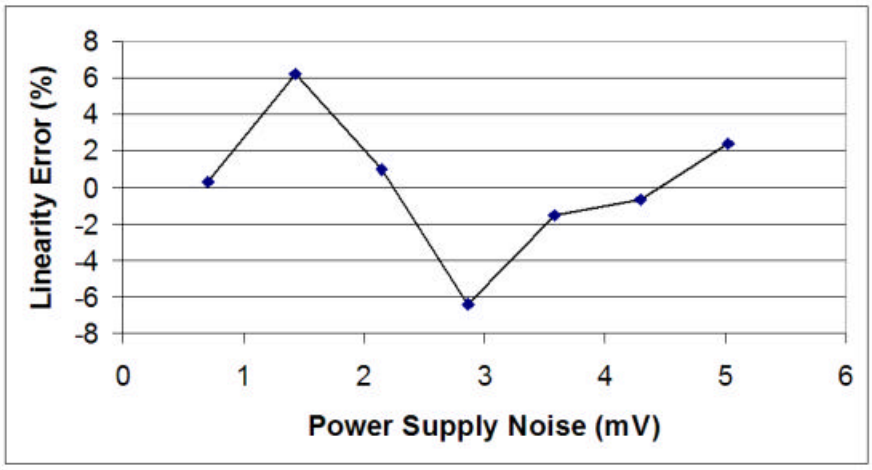


Figure 2.22: Linearity error for the power supply sensor 4 with injected noise amplitude between 1 mV and 5 mV.

2.5.3.3 Sensitivity to Power Supply and Substrate Noise

The substrate sensor and signal path needs to be insensitive to noise on power supply to avoid measurement corruption. Similarly, the power supply sensor and signal path needs to be insensitive to substrate noise. Power supply rejection of 64 dB has been measured for the substrate sensor, including buffers, multiplexers, and sampler, by injecting 10 mV 40 MHz noise pulses into the power supply grid. An average of 100 points have been used to measure the high and low levels. The substrate noise coupling into the power supply probing circuit was below the detectable limit for 60 mV 100 MHz - 1.6 GHz noise pulse injected through the p+ contact.

2.5.3.4 Frequency Response

To measure the frequency response of the substrate sensor, the HP8665A signal generator injects a sinusoidal signal into the p+ substrate contact placed near group 1 of sensors in Test Chip 1. The amplitude of sensor 4 is measured using the on-chip sampler. For the frequency response of the power supply sensor, the HP8133A signal generator activates the NMOS shorting transistor of DNE3, injecting a variable frequency pulse noise into the power grid. The amplitude of the power supply sensor 2 of group 1 is measured using the on-chip sampler. Figure 2.23 shows the frequency response of the substrate and power supply probing circuits.

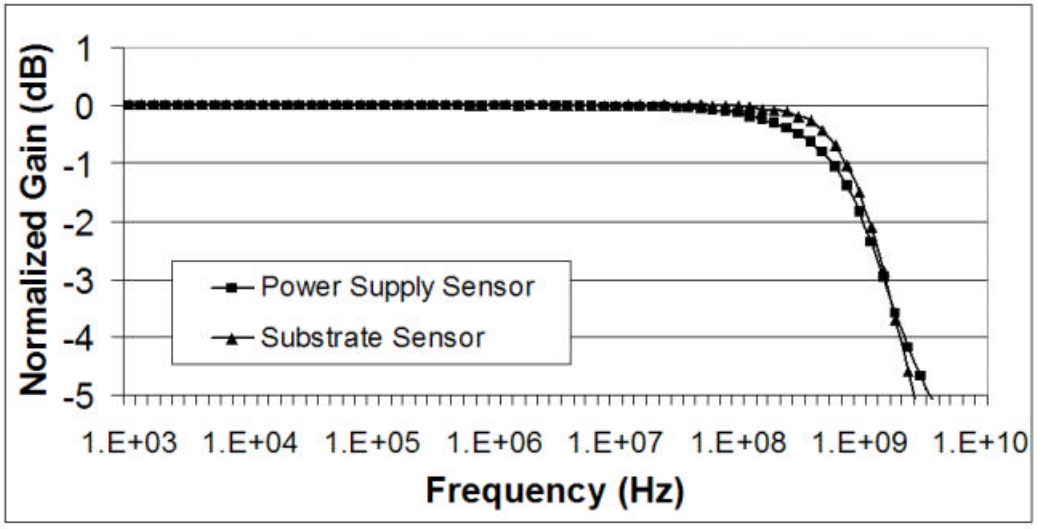


Figure 2.23: Frequency response of the substrate and power supply probing circuits.

It can be noticed that the –3dB point occurs in both cases at about 1.6 GHz, and there is no attenuation at low frequencies like it was in the capacitive coupled sensors [16]-[17].

2.5.4 Characterization of the Waveform Sampler

2.5.4.1 Introduction

The measurement setup used to characterize the waveform sampler is identical to the one used to measure the substrate sensor gain and previously presented in Figure 2.20. The dual channel HP8133A pulse generator provides both the input signal and the sampling clock. The input signal is injected into the p+ substrate contact, and the metal connection to this substrate contact is routed to a substrate sensor. The substrate sensor has been modified by removing its own p+ substrate contact, thus functioning like an amplifier stage. This way the impedance of the p+ substrate contact acts as transmission line termination for the input signal path from the pulse generator. The programmable differential reference voltage needed by the waveform sampler has been provided by a National Instruments DAC board located inside the computer. The clock delay is swept with a programmable time step over a selectable period of time. For each timing position of the clock edge, a binary search is performed to find the value of the input signal. This value is equal to the programmed reference voltage corresponding to the binary search result. The binary search results are stored in a text file, thus creating a time-voltage table consisting of the sample values and time when the samples were taken. This table is then imported in a spreadsheet and plotted in a graph format. The waveform obtained through this method is also named shmoo plot.

2.5.4.2 Input Range and Linearity

The linearity has been measured by injecting noise into the p+ substrate contact and measuring the signal at the metal connection to this p+ contact, as described in the previous section. Figure 2.24 shows the linearity plot superimposed on a best fit linear trend line of the points corresponding to 0-200mV input signal. Higher input signals affect significantly the linearity making the circuit unusable. Figure 2.25 shows the linearity error as the difference between the linearity plot and the linear trend line.

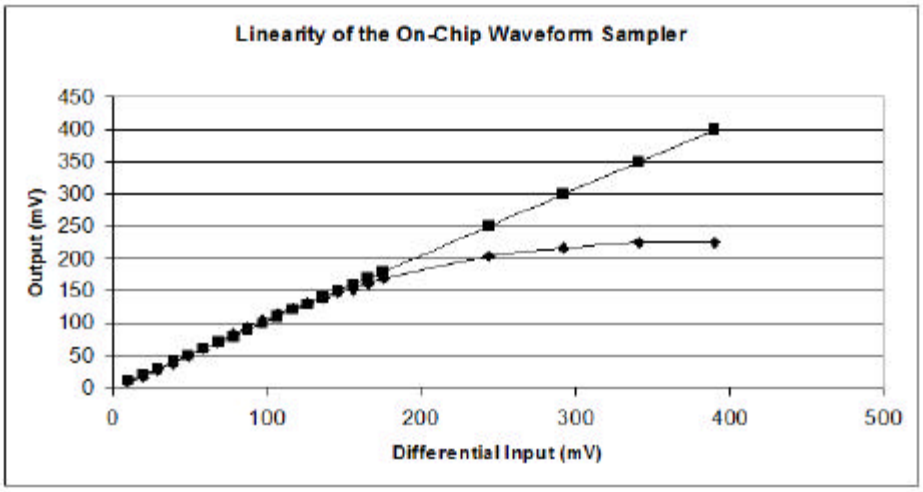


Figure 2.24: Linearity plot of the on-chip waveform sampler superimposed on the best fit linear trend line.

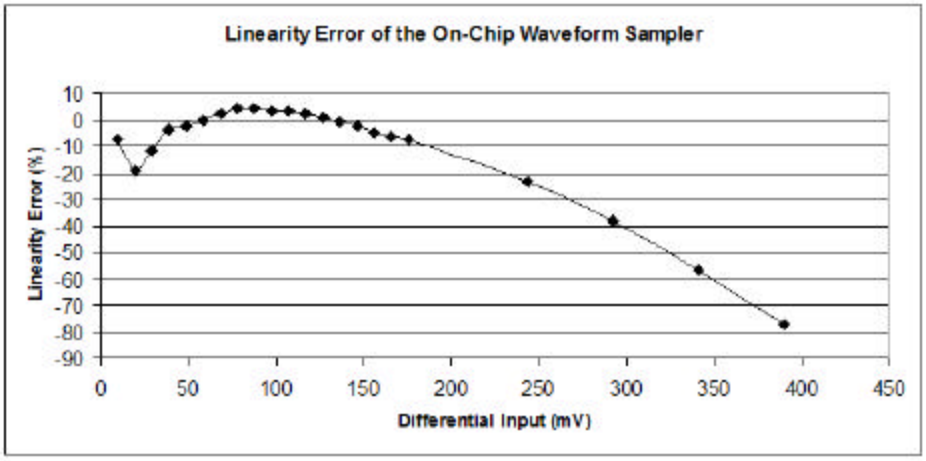


Figure 2.25: Linearity error of the on-chip waveform sampler for inputs between 0 mV and 400 mV.

It can be noticed that the linearity degrades for input signals larger than 200 mV. However, the 200 mV range covers the typical range of expected noise values inside the chip.

2.5.4.3 Bandwidth Evaluation

The bandwidth of the on-chip waveform sampler has been estimated from the rise-time of a transient step response based on the method presented in [66]. The 10-90% rise time of a square wave rising edge is measured and converting into an equivalent -3db bandwidth using the formula

$$F_{3dB} = \frac{K}{t_R} \tag{2.9}$$

where t_R is the 10-90% rise time, K = 0.338 for Gaussian transition edges, or K = 0.350 for exponential transition edges [66]. As input signal has been selected the signal generated by the imbalanced differential stage amplifier connected directly to one waveform sampler, in Test Chip 2. Figure 2.26 shows the rising edge of the sampled waveform with square wave noise injected by DNE 2.

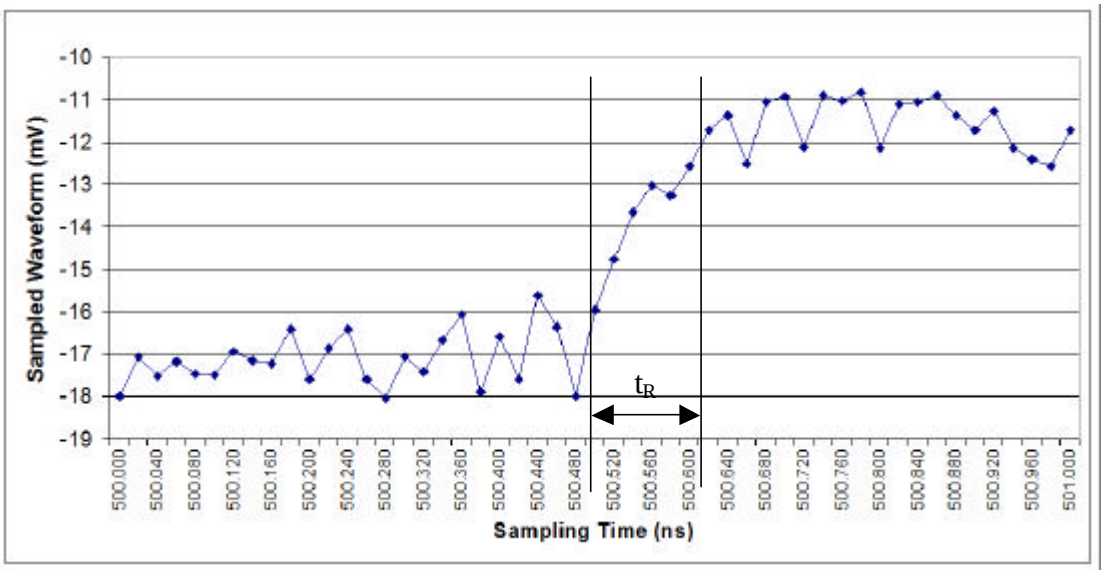


Figure 2.26: Rising edge of the sampled waveform with square pulse noise injected by DNE 2.

The 10% crossing point occurs at 500.495 ns, and the 90% crossing point at 500.610 ns. The rise time is the difference between these two values, equal to 115 ps. Since

the actual input signal is not accessible, it has been assumed ideally equal to zero, thus the 115 ps represents the rise time degradation of the waveform sampler. This assumption will make the calculated bandwidth lower than it is in reality. Since this rising edge looks more exponential than Gaussian, the value $K = 0.350$ has been used in Equation (2.9). The resulting -3dB bandwidth equals $F_{3dB} = 0.350/115\text{ps} = 3.043$ GHz. In reality the bandwidth is higher due to the non-zero rise time of the input signal. For a guessed 50 ps rise time, value equal to the pulse generator rise time, the calculated bandwidth would be 3.38 GHz.

2.6 Application Examples of Substrate and Power Supply Noise Coupling Measurements

2.6.1 DNE Generated Substrate and Power Supply Noise

This experiment has been implemented in group 1 of sensors of Test Chip 2. Figure 2.27 shows the physical layout of sensors and DNE3.

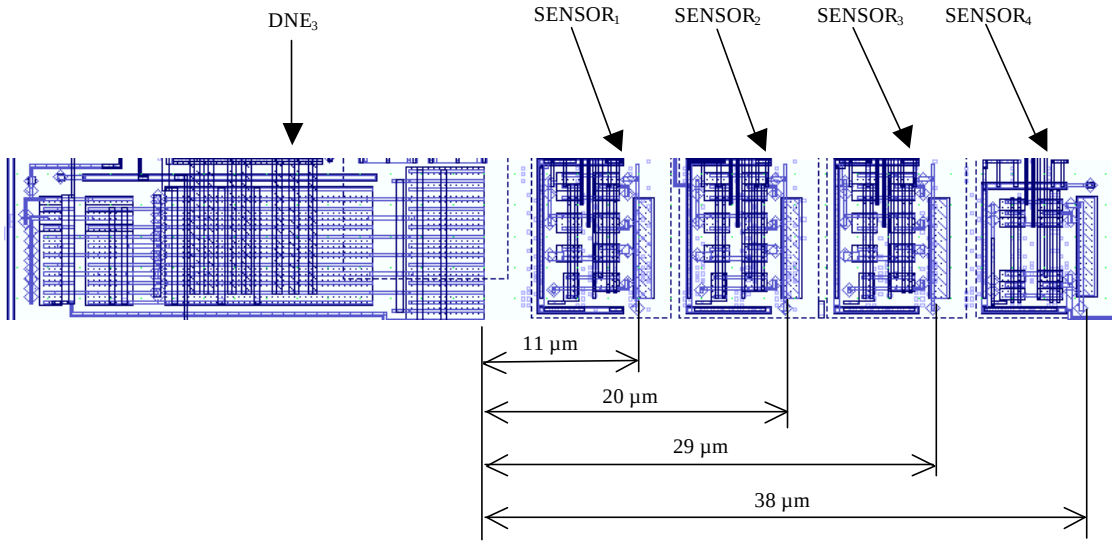


Figure 2.27: Physical layout of DNE3 and sensors in group 1 of Test Chip 2.

The DNE operates at 5.5 MHz, and the sampling step has been set to 200 ps. Figure 2.28 shows the transient waveforms measured by the substrate and power supply sensors 1, which are placed at 11 µm distance from the DNE.

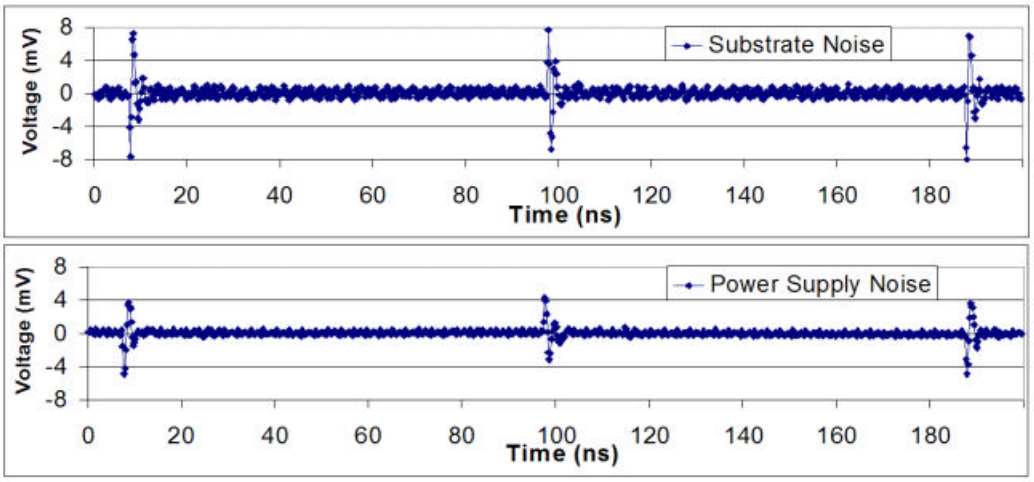


Figure 2.28: Transient waveforms of substrate and power supply measured by sensor 1 of group 1, with digital switching noise injected by DNE 3.

Similar substrate noise waveforms but with smaller peak amplitudes are measured by sensors 2, 3, and 4, placed respectively at 20 µm, 29 µm, and 38 µm, from the DNE. This attenuation of amplitude for increased distance, shown in Figure 2.29, is expected from the perspective of a mesh type model of the substrate [10].

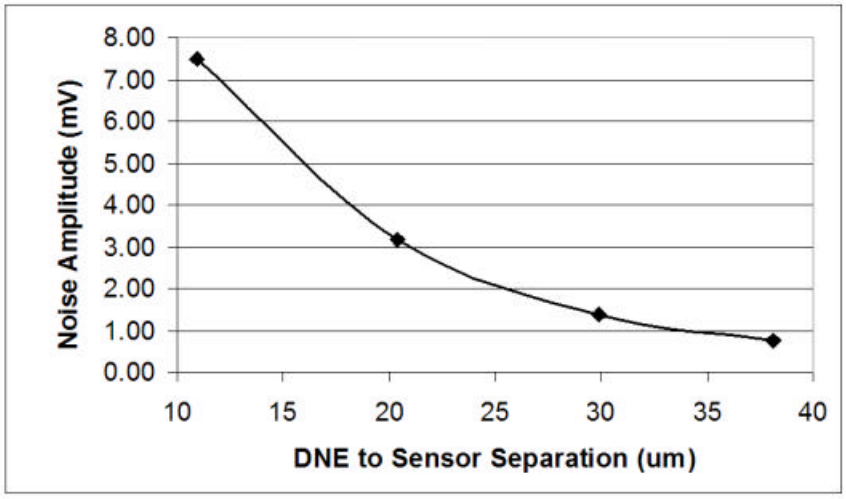


Figure 2.29: Substrate noise attenuation with increased separation between DNE and sensors.

The power supply noise does not change significantly at sensors 2-3 because of the low power grid impedance. These results indicate that the sensors and the on-chip sampler can be used to perform waveform measurements of substrate and power supply noise, and the differential structure is essential in reducing the contamination from ground bounce and coupling on interconnect wires.

2.6.2 Substrate Noise Propagation for Short Distances in p-type Substrate

This experiment has been implemented in sensor group 2 of Test Chip 2, and consists of four sensors placed at 0.8 µm, 3 µm, 6 µm, and 10 µm distance from four p+ noise injector substrate contacts. Figure 2.30 shows the physical layout of this experiment.

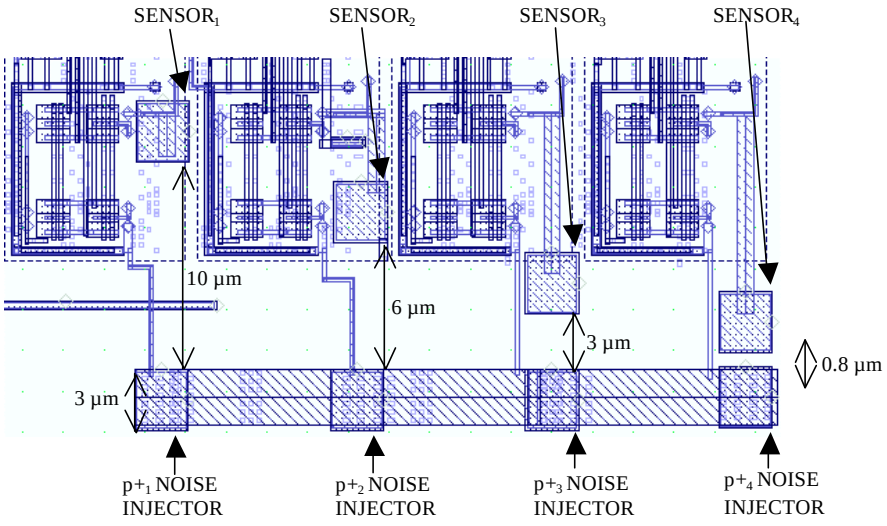


Figure 2.30 Physical layout of the substrate noise propagation experiment for short distances, in p-type substrate.

The HP8133A generator injects a pulsed square wave noise in the substrate through the p+ noise injector contacts. Figure 2.31 shows the amplitude at each sensor, measured with the external oscilloscope.

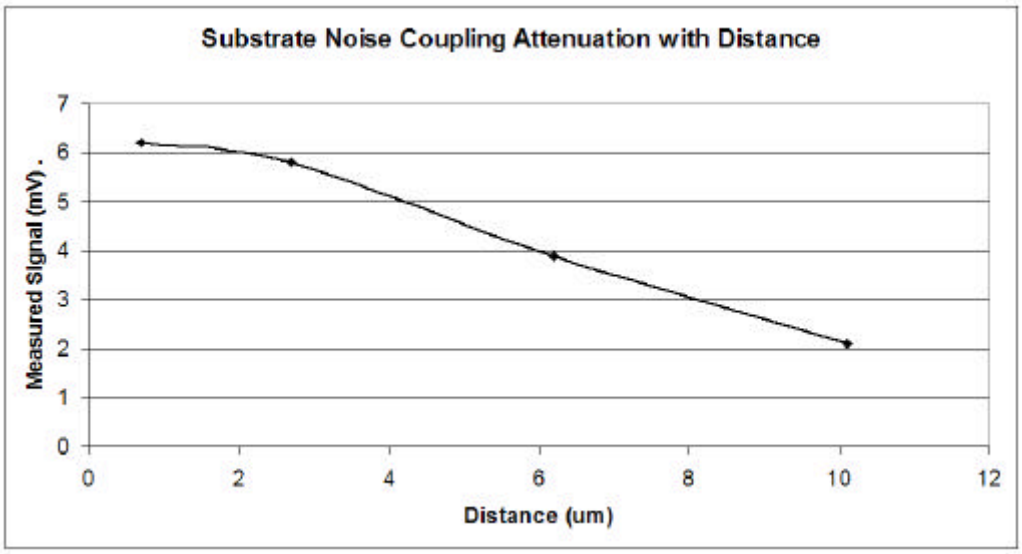


Figure 2.31: Signal amplitude at each sense point, measured with the external oscilloscope.

The coupling dependence on distance looks linear between about 2.4 µm and 10 µm. However, as it can be noticed in the physical layout, each sensor measures not only the noise generated by the corresponding p+ substrate contact, but also the noise generated by the rest of p+ substrate contacts. Because of this, the measured values are higher than if the sensors were measuring only the noise generated by their corresponding p+ substrate contact. To adjust the measured values the following two simplifying assumptions have been made. First, the additional noise coming from the immediate left and right p+ substrate contacts dominates, and the noise coming from the other p+ substrate contacts is neglected. Second, based on the physical layout, the distances between sensors and the left and/or right p+ substrate contacts are assumed all the same, and equal to about 10 µm. Based on the second assumption, sensor 1 measures the noise propagating from two p+ substrate contacts, $p+_1$ and $p+_2$, both located 10 µm distance. Since the measured value equals 2 mV, 1 mV is the contribution from $p+_1$ contact, and 1 mV is the additional noise coupling from p^+_2 contact located in the right side. Based on this result, sensors 2 and 3 measure an additional 2 mV of noise from the left and right p+ contacts, and sensor 4 an additional 1 mV from the left p+ contact. Figure 2.32 shows the adjusted

measurement values obtained by subtracting the additional noise from the previous measurements.

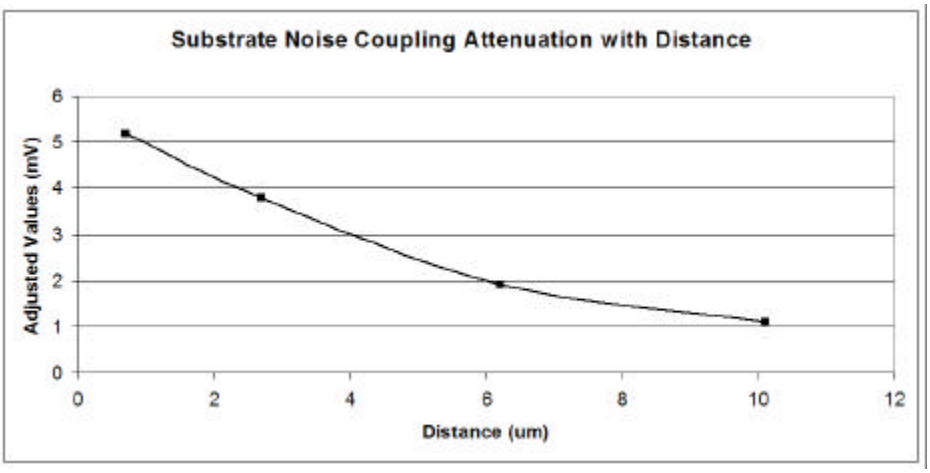


Figure 2.32: Adjusted measurement values obtained by subtracting the additional noise from the previous measurements

2.6.3 Substrate Noise Propagation for Long Distances in p-type Substrate

This experiment evaluates the substrate noise propagation for sensors placed at long distance from the p+ noise injector contact. Figure 2.33 shows the physical layout.

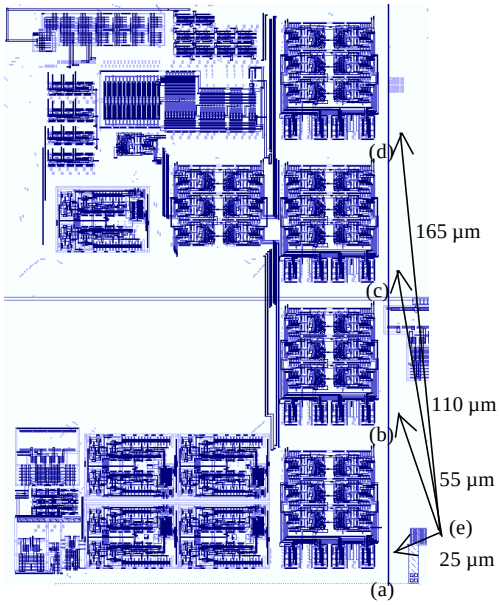


Figure 2.33: Physical layout of the experiment, showing the location of sensors and noise injection p+ substrate contact, as implemented in Test Chip 1.

Four sensors, (a), (b), (c), and (d) are placed at 25 µm, 55 µm, 110 µm, and 165 µm from the p+ substrate contact (e). A pulsed square wave signal is injected into the substrate through the p+ substrate contact, and the output of each sensor is measured with the external oscilloscope. Figure 2.34 shows the amplitude of the measured substrate noise function of distance.

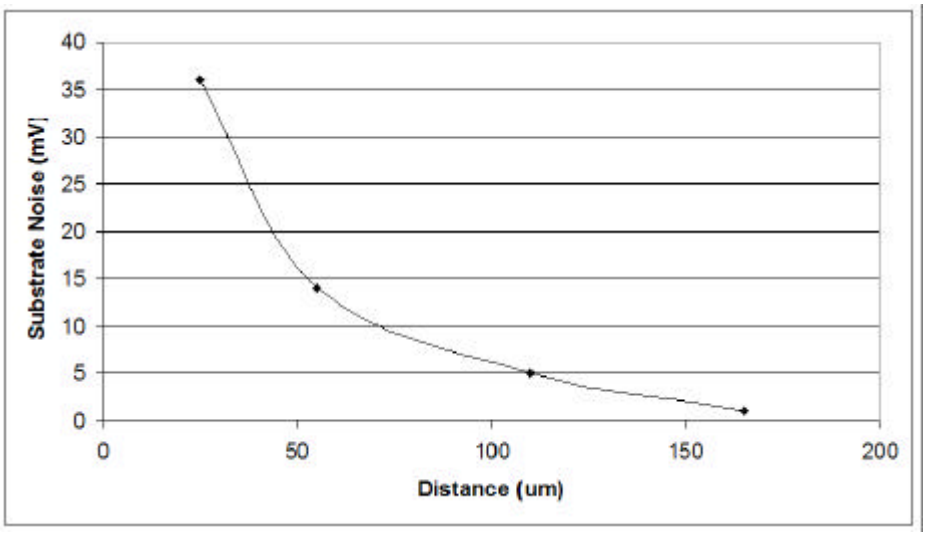


Figure 2.34: Measurement results of substrate noise propagation for long distances in p-type substrate

2.6.4 Effect of NWELL Regions on Noise Coupling through Substrate

This experiment evaluates the effect of NWELL regions on the substrate noise propagation. Figure 2.35 shows the physical layout of the sensors placement, as implemented in sensors group 2 of Test Chip 3.

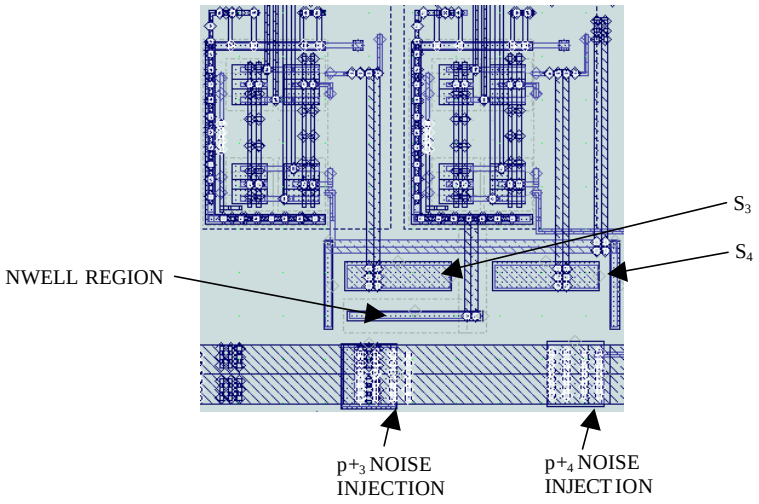


Figure 2.35: Physical layout of the experiment that evaluates the effect of an NWELL region on the substrate noise propagation.

Substrate contacts $p+_3$ and $p+_4$ inject noise into substrate, and sensors S_3 and S_4 measure the coupled noise. An NWELL region has been placed between $p+_3$ and S_3. Figure 2.36 shows the measured substrate noise function of frequency for both sensors.

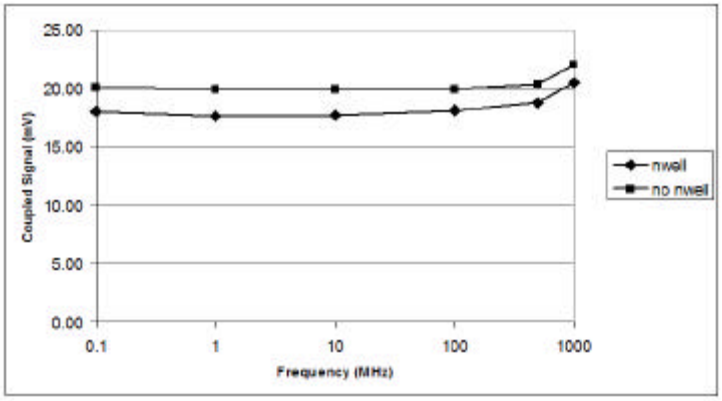


Figure 2.36: Substrate noise coupling function of frequency for direct propagation through the substrate and for propagation through the NWELL region.

It can be noticed that the NWELL region attenuates the noise coupling by about 10% for all frequencies up to 100 MHz, and this attenuation decreases at 500 MHz and 1 GHz.

To study the propagation of substrate noise in a region containing mostly NWELL diffusions, Test Chip 3 has implemented five substrate sensors placed at 2 µm, 11 µm, 20 µm, 29 µm, and 38 µm from a p+ noise injection substrate contact. Figure 2.37 shows the physical layout of the sensors and noise injector.

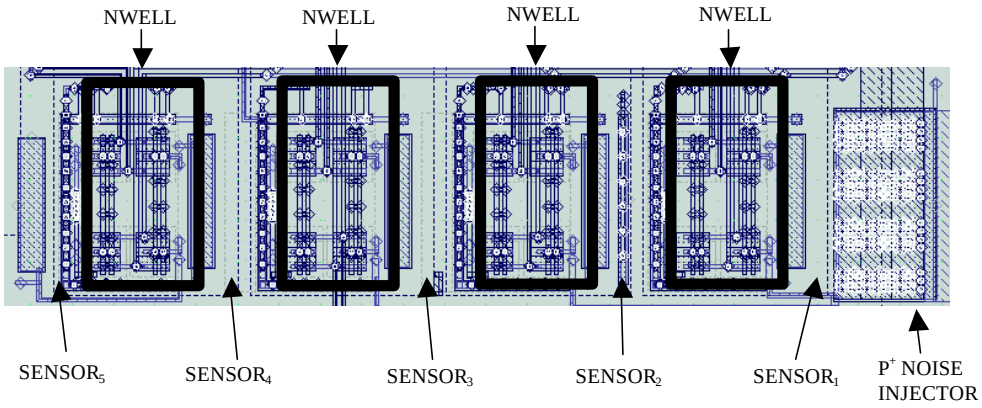


Figure 2.37: Physical layout of the substrate noise propagation through mixed NWELL and p-type substrate regions.

The propagation space between the sensors consists of NWELL regions, which contain the differential sensor circuitry. Thus, the substrate noise propagates through about 1/3 substrate and 2/3 NWELL. A square pulse signal has been injected into the p+ substrate contact, and the sensors outputs have been measured with an external oscilloscope. Figure 2.38 shows the measurement values of all five sensors function of the distance from the noise injector.

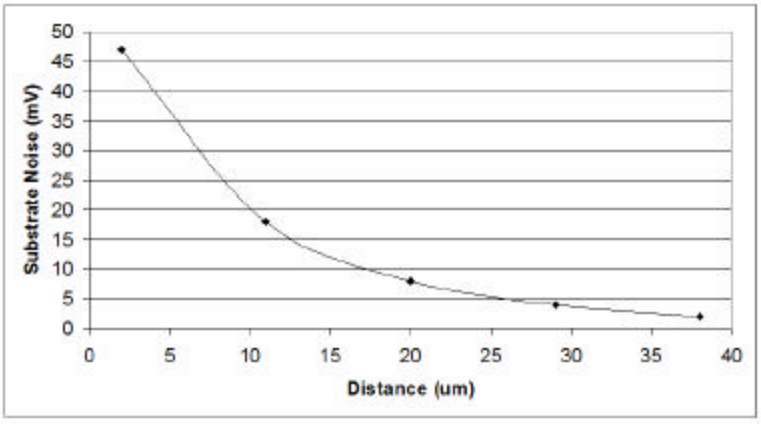


Figure 2.38: Substrate noise propagation in mixed NWELL and p-type substrate.

2.6.5 Effect of Grounded Substrate Contacts on Noise Coupling through the Substrate

The effect of grounded substrate contacts has been evaluated by placing substrate contacts between noise generators and sensors. Figure 2.39 shows the physical layout of the experiment as implemented in sensors group 3 of Test Chip 2.

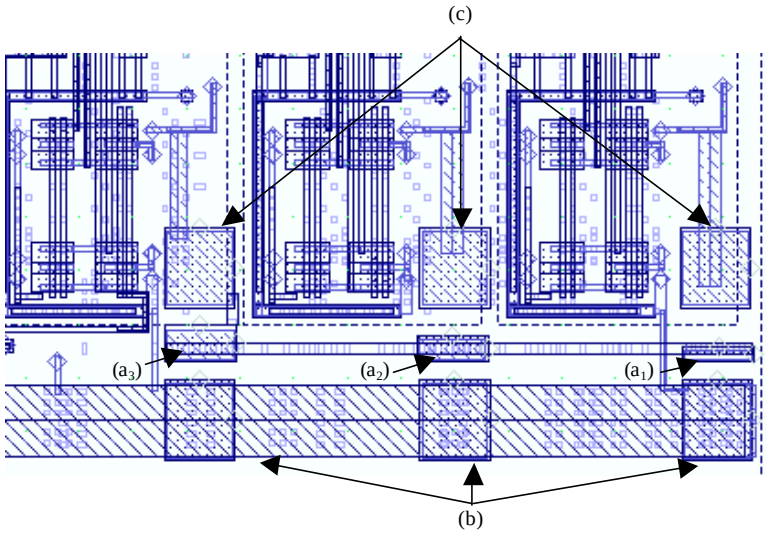


Figure 2.39: Physical layout of the coupling attenuation with grounded substrate contacts.

Three grounded substrate contacts, (a_1), (a_2), and (a_3), of widths 0.44 µm, 0.88 µm, and 1.32 µm, have been placed between the noise injection p+ contacts (b) and sensors (c). Sensor 3 of group 2 in the same test chip, which has no substrate contact and has the same spacing from the noise injector, has been used as reference. Figure 2.40 shows the coupling attenuation dependence on the width of the grounded substrate contact.

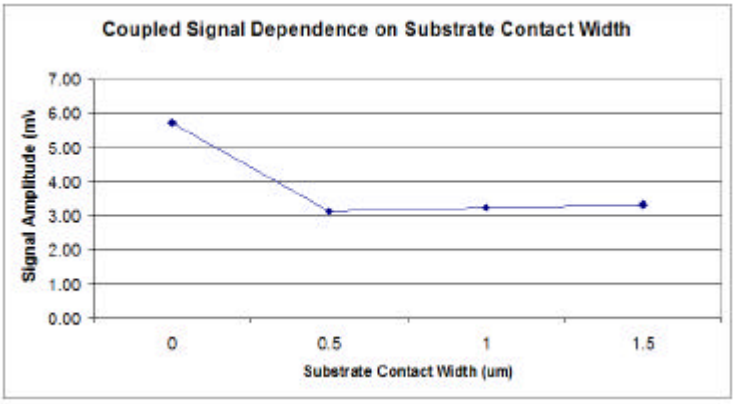


Figure 2.40: Coupling attenuation dependence on grounded substrate contact width, referenced to sensor 3 of group 2.

It can be noticed that the grounded substrate contacts reduced the noise coupling by a factor of two, and the width of the grounded substrate contact has little effect on this attenuation.

2.6.6 Effect of NMOS Transistors and Capacitors on Noise Coupling through the Substrate

Figure 2.41 shows the physical layout consisting of an NMOS transistor (a) and a capacitor (b) placed between one noise injection substrate contact (c) and two sensors (d). This experiment has been implemented in sensors group 3 of Test Chip 2. Sensor 3 of group 2 in the same test chip, which has the same spacing to the noise injector contact, has been used as reference.

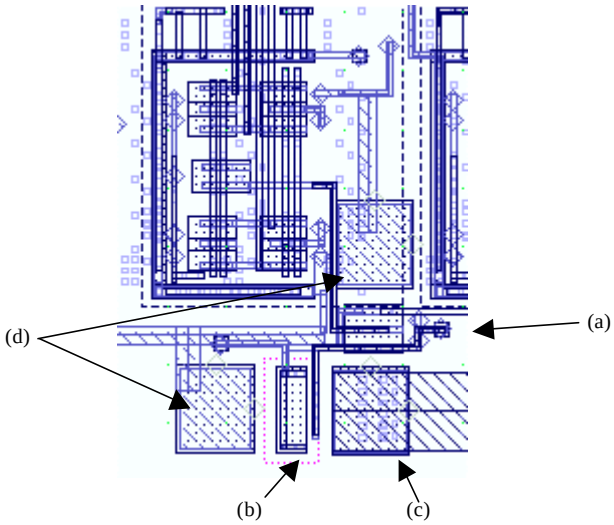


Figure 2.41: Physical layout of the experiment evaluating the NMOS transistors and capacitors effect on substrate noise coupling.

The bias voltages on the capacitor, and on the NMOS gate have been programmed from the external DAC board part of the test bench fixture. This way the transistor has been adjusted to operate in accumulation, triode, or saturation regions. The measurement results did not show any variation in substrate coupling when the transistor went through all these operation regions. Similarly the coupling did not change when the voltage on the capacitor was swept from ground to the power supply levels. However, both sensors measured lower signals compared to case of free space coupling. The capacitor experiment measured 3.6 mV, and the NMOS experiment 4.8 mV, lower values compared to 5.8 mV measured by the reference sensor. These values needed to be adjusted for the additional noise generated by the other p+ noise injection contacts, following the same procedure described in Section 2.6.2. Based on the physical layout placement of sensors it has been assumed that only the sensor measuring the propagation path through the NMOS transistor is affected by additional coupling from the right side. Thus, the measured value needs to be adjusted by subtracting 1mV contribution from the right side. The sensor measuring the effect of the capacitor is not affected because there are no other p+ noise injection contacts placed on the left side. The measurement of the reference sensor has already been adjusted in Section 2.6.2 from 5.8 mV to 3.8 mV. The adjusted results can be

summarized as: reference sensor 3.8 mV, propagation through NMOS 3.8 mV, propagation through capacitor 3.6 mV. It can be concluded that the NMOS has little effect on noise coupling through the substrate, and the capacitor reduces the coupling by 5%.

2.6.7 Coupling Suppression using a Guard Ring

This experiment evaluates the coupling suppression inside a guard ring made of a continuous substrate contact shunted to the chip ground. Figure 2.42 shows the physical layout of the experiment, as implemented in group 2 of Test Chip 3. Three sense points (a), (b), and (c) have been placed inside the guard ring (d), and have been connected to three substrate sensors. A p+ noise injector substrate contact (e) has been placed outside the guard ring. For a reference measurement, a forth sensor (f) has been placed outside the guard ring at the same spacing from the noise injector as sensor (a) inside the ring.

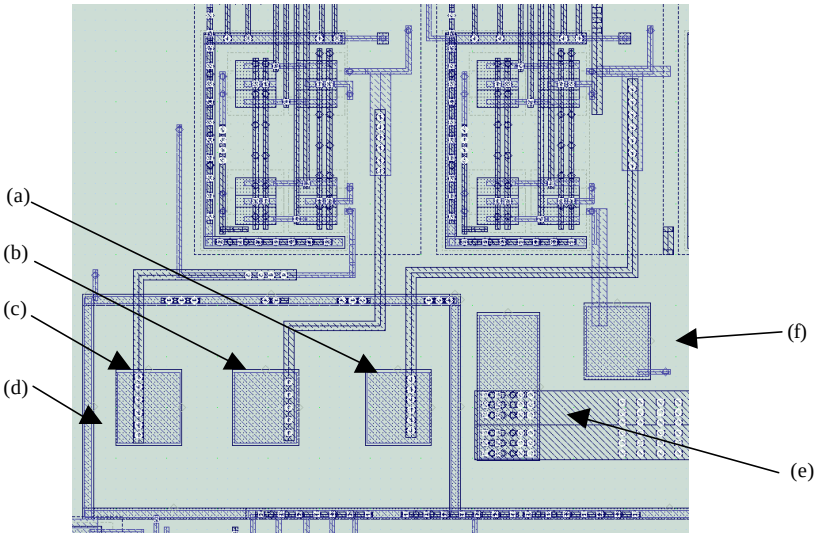


Figure 2.42: Physical layout of the guard ring suppression experiment.

A square wave signal has been injected into the p+ contact, and the substrate noise at each sensor has been measured with the external oscilloscope. Figure 2.43 shows the measurement results.

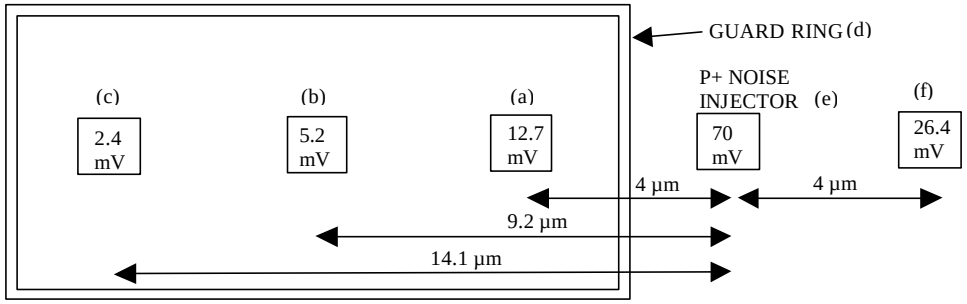


Figure 2.43: Signal amplitude at the sensors inside and outside the guard ring.

By comparing the amplitudes at sensors (a) and (f), it can be noticed that the guard ring attenuates the substrate noise coupling by about 50%. Also, the noise coupling varies inside the ring decreasing with the distance from source.

2.6.8 Coupling Suppression using High Resistive Moat

This experiment evaluates the substrate noise coupling suppression by a high resistive guard ring, also named MOAT. The MOAT region provides higher sheet resistance compared to the rest of the p-type lightly doped substrate. Figure 2.44 shows the physical layout of the experiment, as implemented in sensors group 3 of Test Chip 3.

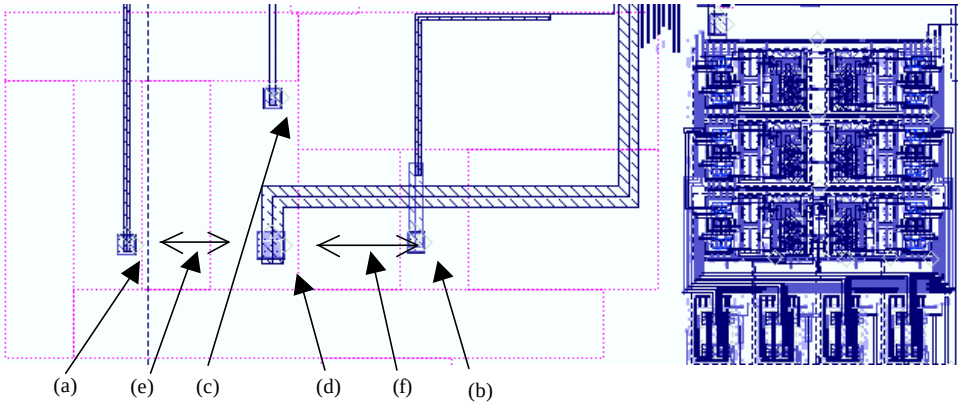


Figure 2.44: Physical layout of the coupling suppression experiment using a high resistive moat.

Three sensors (a), (b), and (c), have been placed at equal distances from a p+ noise injector substrate contact (d). Two of the sensors, (a) and (b) are placed inside isolation rings made of 10 µm (e) and respectively 15 µm (f) wide moats. No isolation has been implemented between sensor (c) and the noise injector. A sinusoidal signal has been injected into the p+ substrate contact, and the coupled signals at each sensor have been measured with the external oscilloscope. Figure 2.45 shows the substrate noise coupling dependence on moat width for signal frequencies between 100 kHz and 1 GHz.

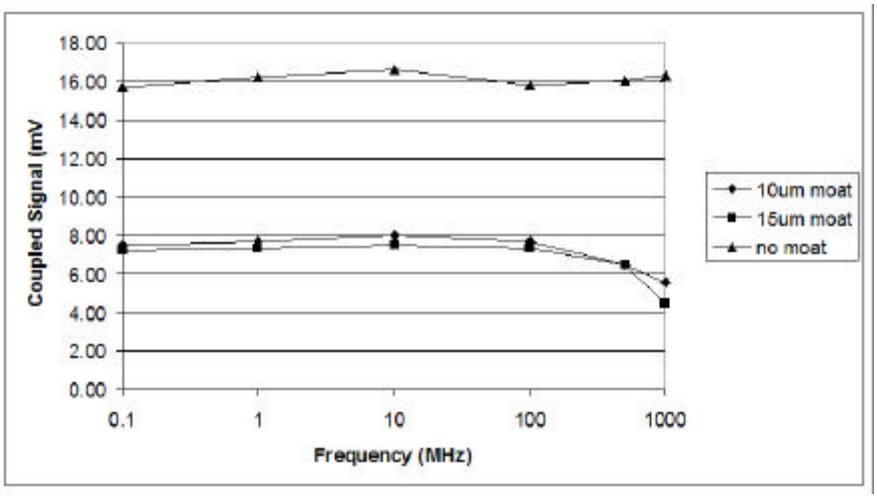
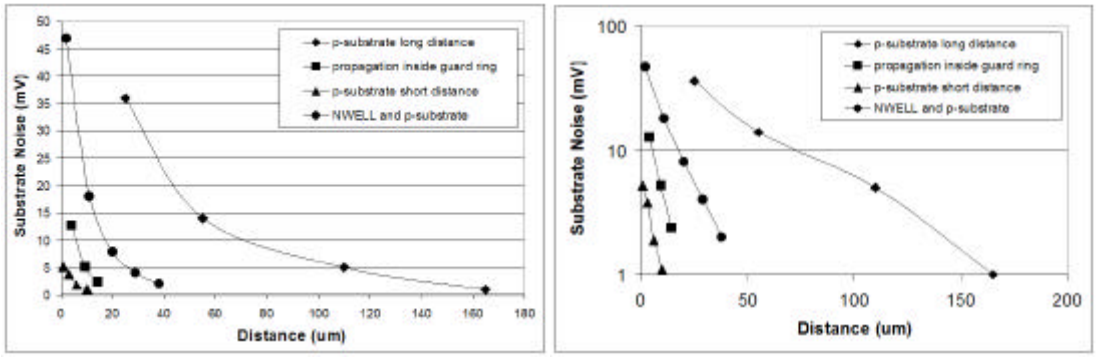


Figure 2.45: Substrate noise coupling dependence on moat width for signal frequencies between 100 kHz and 1 GHz.

Because of the bandwidth limitation of the measurement path to the external oscilloscope, the injected noise amplitude has been increased at higher frequencies to measure the same value at sensor (c). The results show that the moat ring reduces the coupling by about 55 % for frequencies lower than 100 MHz, and the reduction increases at higher frequencies to 70 % at 1 GHz.

2.6.9 Summary of Noise Propagation Measurements

Figure 2.46 (a) shows the summary results of the substrate noise attenuation with distance experiments described in the previous sections. As expected, the measurements of substrate noise propagation show that the noise is attenuated with distance, and with high resistive or shunting guard rings. Inside the shunting guard rings, the substrate noise propagation continues to decay with distance at the same rate as outside.



(a) (b)

Figure 2.46: Summary of substrate noise attenuation with distance experiments.

Figure 2.46 (b) shows the same curves but using a logarithmic scale on the Y-axes. It can be noticed that the curves plotted using the logarithmic scale look like straight lines. The straight-line representation on a logarithmic scale suggests that the substrate noise attenuation can be approximated by exponential decay functions. With this approximation the slope in the logarithmic plot equals the exponential decay coefficient. Thus, it can be noticed that the long-distance propagation has a smaller slope than the short-distance propagation, which means that the noise coupling drops rapidly with distance near the noise injector contact. This result can be explained by the far-field versus near-field effect [9]. In the long-distance experiment the contacts are placed remotely enough to be considered as lumped contact points, but in the short-distance experiment we see the geometry-dependent effects since the separation

between the sensor and noise injector is of the same order of magnitude as the size of the contacts themselves. It can also be noticed that the substrate noise attenuation inside the guard ring follows an exponential decay having the same slope as the near-field substrate noise attenuation outside the guard ring. The propagation through 2/3 NWELL and 1/3 p-substrate has a slope in between the near-field and far-field lines.

Interestingly, both the shunting guard ring and high resistive moat each attenuate the propagation by about 50%. Even the grounded substrate contacts in the near-field propagation attenuate the propagation by 50%. This coincidence can be explained by the geometry of the structures implemented in the test chip. Figure 2.47 shows a simplified cross section of the lightly doped substrate, which implements shunting and high resistive guard rings.

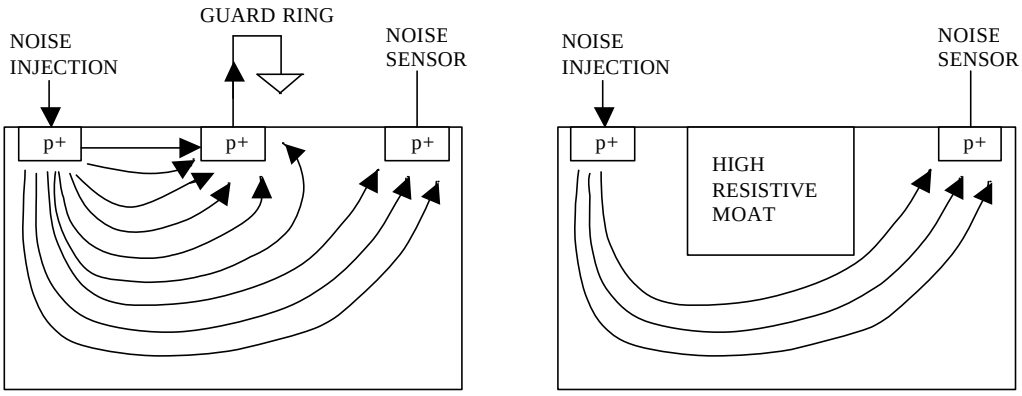


Figure 2.47: Simplified cross section of shunting and a high resistive guard rings implemented in lightly doped substrate.

Due to the conductivity of the substrate, part of the injected noise current in the digital region flows through the substrate into the grounded substrate contacts and diffusion capacitances of the analog region. For simplification, the grounded substrate contacts and the diffusion capacitances are not shown in Figure 2.47, only a p+ sensor is illustrated. Current does not typically flow into the p+ sensor, unless this sensor is connected to a 50 ohms input of an oscilloscope. The shunting ground ring captures part of the injected current, mostly contributions close to the surface, and routes them

to ground. The rest of the current still propagates and reaches the analog region. The high resistive moat blocks the injected current because of the isolator characteristics of the moat implant. However, part of the injected current flows under the moat and reaches the analog region. Measurements show that in both cases the noise propagation is reduced by about 50%, and this reduction does not vary significantly with the width of the guard ring or moat.

2.7 Conclusion

This chapter has presented substrate and power supply sensors, and a waveform sampler for measuring noise coupling in mixed signal SoCs. The sensors have been designed to minimally affect the noise coupling, and not to inject additional noise in the substrate or power supply. Resistive coupling allows the measurement of very low frequency and DC components. Both sensors allow continuous-time wide-bandwidth measurements up to 1.6 GHz. The substrate sensor achieved a power supply rejection of 64 dB. The substrate noise coupling into the power supply sensor was below the detectable limit. Noise waveforms generated by a built-in digital noise emulator, or externally injected into substrate, have been measured with the on-chip signal sampler and with an external oscilloscope. The on-chip measurement reduces the bandwidth limitation and signal contamination due to off-chip routing, and eliminates additional analog output pins. This is an essential advantage of the proposed measurement technique, especially for implementations involving complex VLSI chips.

Chapter 3

Substrate Noise Cancellation Techniques

3.1 Introduction

In mixed-signal integrated circuits the switching noise produced by the digital circuits propagates through substrate to the analog circuits, potentially degrading their performance. In recent years research has focused on reducing the impact of digitally generated substrate noise on sensitive analog circuits. Techniques of increasing the immunity to substrate noise by common mode cancellation in differential structures have been reported in [32]. Since substrate noise couples into MOS transistors through junction capacitances and the body-effect [11], in differential circuits this coupling appears as common-mode signals at the outputs. Methods of suppressing the generation of digital noise by shaping the supply current have been reported in [33]. Coupling reduction by shunting the substrate to the chip ground through substrate contacts has been shown in [29]. Isolation using passive guard rings has been presented in [34]-[35], and using active guard rings in [36]-[39]. Guard rings reduce but do not completely eliminate substrate noise, which still exists inside the isolated region. Namely, the noise is higher in the middle and lower close to the edges of the isolation region [9]. The presence and variation of substrate noise inside guard ring has also been measured in this work and has been presented in Section 2.6.7. Thus, it is desirable to develop substrate noise cancellation techniques that can be implemented along with the sensitive MOS circuits of mixed signal SoCs. This work proposes three substrate noise cancellation techniques for NMOS transistors used in common-source configurations. The techniques can be applied to differential or single ended

circuits, and in conjunction with other noise suppression methods. Common-source PMOS transistors in n-type substrate are not covered by this work, but they can be compensated in a similar way. The proposed techniques address the common-source NMOS transistors used in amplifiers and active loads. The active loads have been implemented in the delay stages of a ring oscillator. Experimental NMOS common-source amplifiers and ring oscillator active loads, with and without substrate noise cancellation, have been implemented in a test chip built in 0.13um CMOS technology on a p-type lightly doped substrate. This chapter is organized as follows: Section 3.2 describes the noise cancellation technique for NMOS transistors in common-source amplifiers, Section 3.3 covers the technique for NMOS transistors in active load structures, and Section 3.4 presents a negative feedback noise cancellation technique for common-source NMOS with source degeneration. Conclusions are given in Section 3.5.

3.2 Substrate Noise Cancellation for Common-Source NMOS Amplifier

3.2.1 Architecture and Functionality

The proposed technique cancels out the drain current variation of the common-source NMOS transistor generated by substrate noise coupling through the body-effect. This cancellation is obtained by adding an equal magnitude and opposite sign current produced by a compensation structure connected in parallel with the NMOS transistor. The schematic diagram of the noise cancellation technique is shown in Figure 3.1(a), and the equivalent small-signal model in Figure 3.1(b).

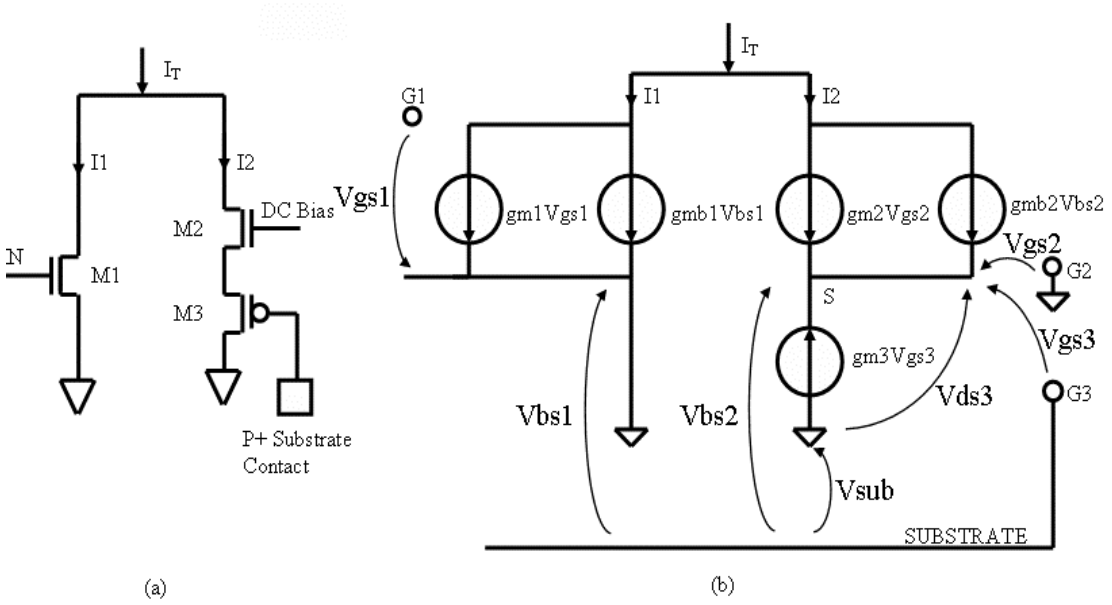


Figure 3.1: Schematic diagram of the noise cancellation technique (a), and the equivalent small-signal model (b).

The common-source NMOS transistor *M1* is placed in parallel with a compensation branch made of a common-gate, *M2*, and a source-follower, *M3*. The DC bias voltage has to be generated by a circuit insensitive to substrate noise. An example of bias generator made only with PMOS transistors is presented in the test chip implementation section. The total current I_T represents the sum of *M1* current, I_1, and *M2-M3* current, I_2. When I_1 varies due to substrate noise, I_2 has to vary with equal magnitude and opposite sign, keeping their sum I_T constant. To quantitatively analyze this, we refer to the small-signal model in Figure 3.1(b). I_1 and I_2 can be expressed as:

$$I_1 = gm_1 Vgs_1 + gmb_1 Vbs_1 \tag{3.1}$$

$$I_2 = gm_2 Vgs_2 + gmb_2 Vbs_2 \tag{3.2}$$

Also from the small-signal model it can be noticed that $I_2 = -gm_3 Vgs_3$, $Vbs_1 = Vsub$, $Vgs_2 = -Vs$, and $Vgs_3 = Vbs_2 = Vsub - Vs$, where *Vsub* is the substrate voltage, *Vbs* is the bulk to source voltage, *Vgs* is the gate to source voltage, and *Vs* is the voltage at

node *S* of *M2-M3* branch. Inserting these conditions in (3.1) and (3.2), I_1 and I_2 can be expressed as:

$$I_1 = gm_1 Vgs_1 + gmb_1 Vsub \tag{3.3}$$

$$I_2 = -\left(\frac{gm_2 gm_3}{gm_2 + gm_3 + gmb_2} \right) Vsub \tag{3.4}$$

It can be noticed in (3.3) that I_1 has a component dependent on the gate voltage, Vgs_1, and a component dependent on the substrate voltage, *Vsub*. The *Vsub* component represents the current variation due to substrate noise, and it can be canceled out if I_2 has the same magnitude and opposite sign. By adding I_1 and I_2, the total current I_T is equal to:

$$I_T = I_1 + I_2 = gm_1 Vgs_1 + \left(gmb_1 - \frac{gm_2 gm_3}{gm_2 + gm_3 + gmb_2} \right) Vsub \tag{3.5}$$

In equation (3.5) the *Vsub* term will vanish if

$$gmb_1 = \frac{gm_2 gm_3}{gm_2 + gm_3 + gmb_2} \tag{3.6}$$

Since *gm* and *gmb* factors can be calculated based on transistor sizes, bias currents, and technology parameters using conventional formulae [42], this condition can be achieved in the design process by properly sizing the transistors. If condition (3.6) is met, the total current I_T is equal to:

$$I_T = gm_1 Vgs_1 \tag{3.7}$$

Equation (3.7) shows that the *M1* compensated-structure operates as a common-source amplifier configuration and does not depend on the substrate voltage. The output resistance can be approximated to $ro = ro_1 // ro_2$, where ro_1 and ro_2 are the output resistances of transistors *M1* and *M2*. The output resistance *ro* has a value lower than ro_1, the output resistance without noise cancellation. However, since both *M1* and *M2* operate in saturation, the combined output resistance is still sufficiently high for typical applications. A disadvantage of this approach is the increased thermal noise due to the addition of the *M2-M3* compensation branch, thus depending on the application, a tradeoff between thermal and digital switching noise needs to be made. Because this noise cancellation technique requires all transistors to operate in saturation, special attention must be given when designing low voltage circuits, or circuits using large number of stacked transistors. Also, the p+ substrate contact needs to be placed close to *M1* in the physical layout to minimize the effects of substrate noise variation across the chip.

3.2.2 Test Chip Implementation

The effectiveness of the noise cancellation technique for common-source NMOS amplifiers has been evaluated by simulations, and by experimental measurements of a test chip fabricated in 0.13µm CMOS technology on a p-type lightly doped substrate. The schematic diagram of the experimental circuit, implemented in sensors group 4 of Test Chip 3 is shown in Figure 3.2.

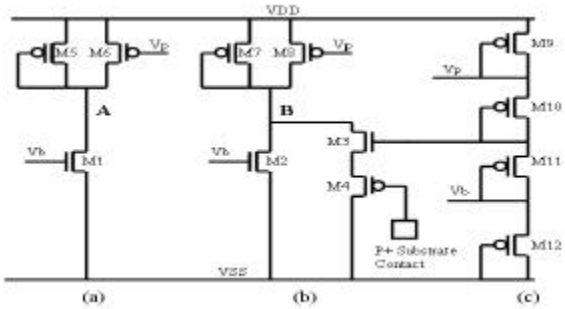


Figure 3.2: Schematic of the noise cancellation for common-source NMOS amplifiers.

A common-source NMOS transistor, *M1*, has the drain connected to a conventional active load circuit, of the type presented in [41], made of two PMOS transistors, *M5* and *M6*. The voltages *Vb* and *Vp* are provided from the *M9-M12* bias generator branch. The load and the biasing circuits are made only using PMOS transistors, which are physically placed in the NWELL. Because the NWELL reverse biased junction capacitance attenuates the substrate noise coupling into the PMOS transistors, it is assumed that the substrate noise couples only into the NMOS transistor *M1*. This coupling produces variations of the drain current, which are measured by probing the voltage at node *A* with an external oscilloscope. A second common-source NMOS transistor of identical size, *M2*, connected to the same type of active load, *M7-M8*, has implemented the proposed noise cancellation circuit made of *M3-M4*. The DC bias is provides also from *M9-M12* bias generator branch. Substrate noise coupling into the structure with noise cancellation is measured similarly by probing the voltage at node *B*. The physical layout of this experiment is shown in Figure 3.3.

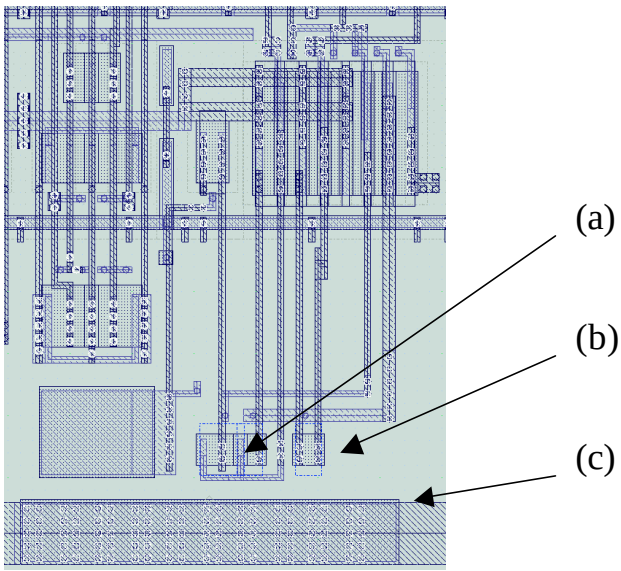


Figure 3.3: Physical layout of the noise cancellation technique for common-source NMOS amplifiers, showing the noise cancellation structure (a), the uncompensated transistor (b), and the noise injector p+ substrate contact (c).

3.2.3 Simulation Results

Hspice transient simulations have been performed to validate the concept before the test chip fabrication. The results are shown in Figure 3.4.

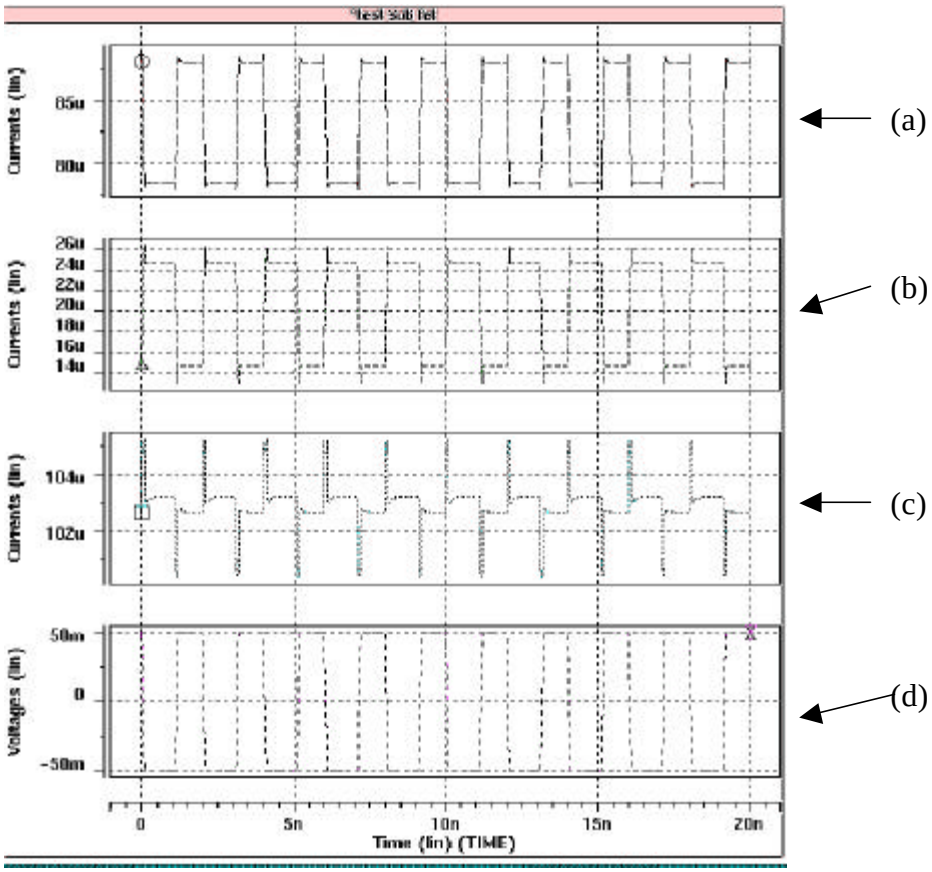


Figure 3.4: Hspice transient simulation results of the substrate noise cancellation technique for common-source NMOS amplifier stage.

Waveform (a) represents the *M1* drain current variation due to 100 mV peak-to-peak square pulse noise injected in the substrate, shown by waveform (d). Waveform (b) shows the current through the *M2-M3* compensation branch, which is in opposite phase with the *M1* drain current. Waveform (c) shows the total current I_T, which is the sum of the currents through *M1* transistor and *M2-M3* compensation branch. The substrate noise coupling into the total current has been reduced from 9uA to about

1uA. The spikes on this waveform are about +/- 2uA, and they show that the noise cancellation is limited at high frequencies. A performance analysis of this technique is presented in the experimental results section.

3.2.4 Experimental Results

The transient response of the common-source NMOS amplifier structures with and without noise cancellation have been evaluated by injecting 50 mV amplitude sinusoidal signals at 10 MHz and 1 GHz into the p+ substrate contact. The experimental and Hspice simulated waveforms at 10 MHz are shown in Figure 3.5, and at 1 GHz in Figure 3.6.

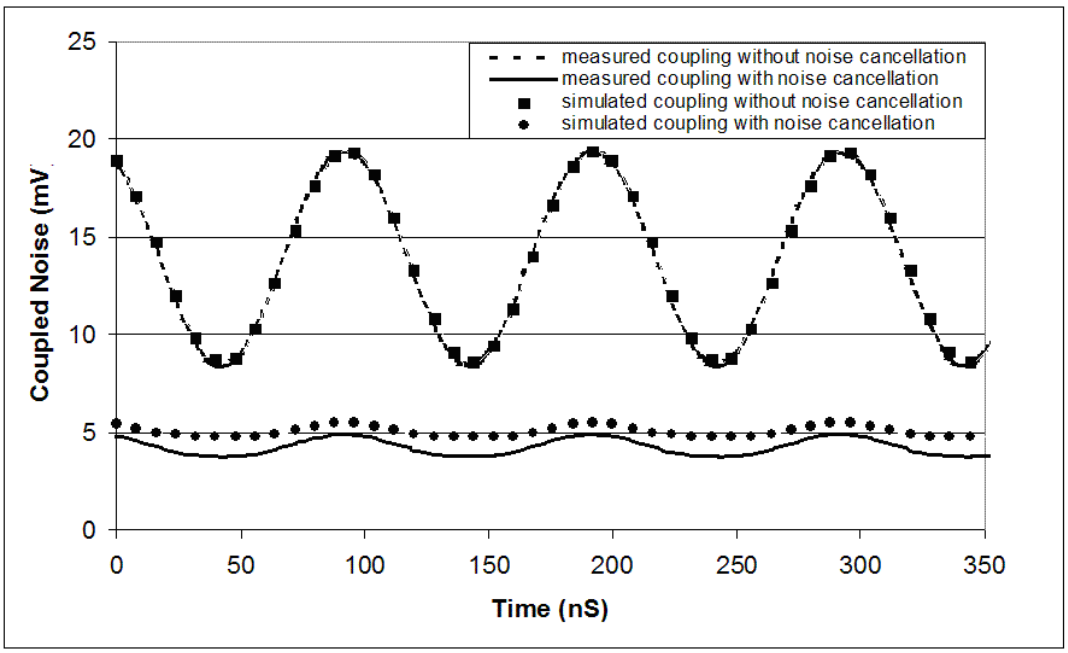


Figure 3.5: Transient response of the common-source NMOS amplifier structures with and without noise cancellation for 50 mV and 10MHz sinusoidal substrate noise.

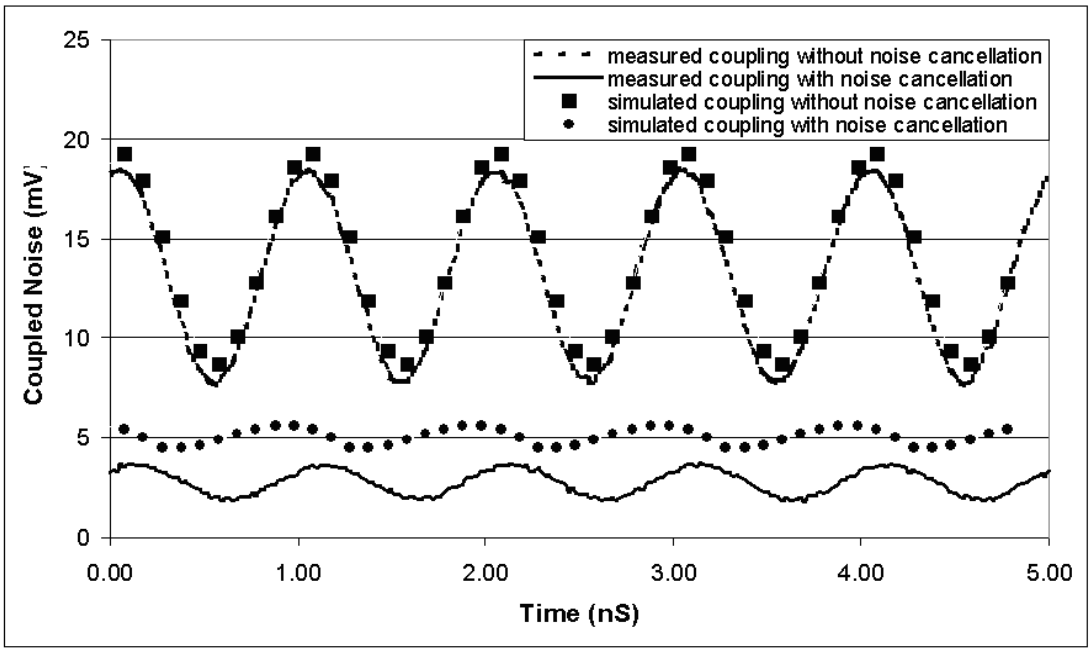


Figure 3.6: Transient response of the common-source NMOS amplifier structures with and without noise cancellation for 50 mV and 1 GHz sinusoidal substrate noise.

The different DC offsets of the measured waveforms are mainly due to the mismatch between the currents through the compensated and uncompensated circuits. The DC offsets of the simulated waveforms have been intentionally added to allow the waveforms representation on the same graph with the measured data. Reduction of substrate noise coupling of 8.8 times has been achieved at 10 MHz, and 5.6 times at 1 GHz. The measured amplitudes for the structures with substrate noise cancellation are 20% larger than simulations at 10 MHz, and 25% at 1 GHz. Figure 3.7 shows the frequency dependence of substrate noise coupling suppression.

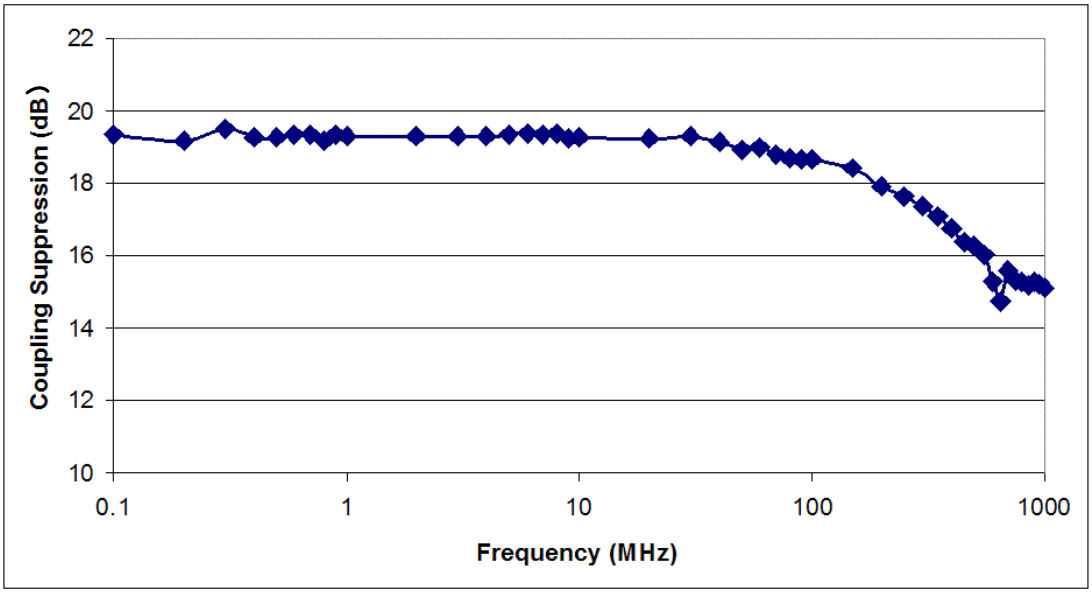


Figure 3.7: Frequency dependence of substrate noise coupling suppression for NMOS transistor in common-source amplifier configuration

Substrate noise suppression of about 19.2 dB is achieved for frequencies lower than 40MHz, and the suppression gradually decreases to 15 dB at 1 GHz.

3.3 Substrate Noise Cancellation for NMOS Transistors in Active Load Structures

3.3.1 Architecture and Functionality

A derivative of the proposed substrate noise cancellation technique for common-source amplifiers can be applied to typical active load circuits made of a diode-connected transistor in parallel with a current-source MOS transistor, and illustrated using PMOS devices in [13]. The same structure can be implemented using NMOS transistors, as shown in Figure 3.8(a), where *M1* is configured as current source, and *M2* as diode-connected.

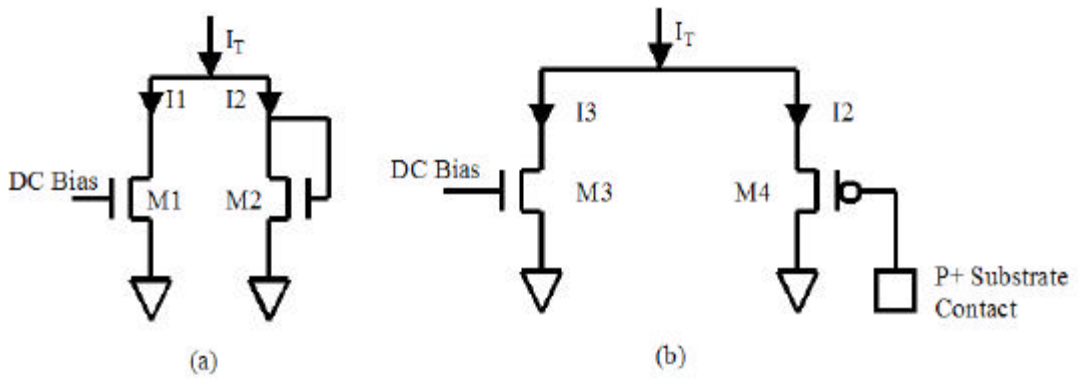


Figure 3.8: Conventional active load circuits (a) and proposed active load with substrate noise cancellation (b).

The proposed compensation technique, shown in Figure 3.8(b), replaces the diode-connected NMOS transistor with a source-follower PMOS having the gate connected to substrate through a p+ contact. The output impedance of *M4* stage equals *1/gm4*, which is the same as if *M4* was configured as diode-connected by having the gate connected to ground. Since *M3* is configured as current-source and *M4* has the same impedance as in diode-connected configuration, the functionality of the proposed structure is similar to the conventional active load in Figure 3.8(a). The noise cancellation technique uses the gate of *M4* to sense the noise in the substrate and to produce variation of I_2 current. This variation needs to have equal magnitude and opposite sign with the substrate noise generated drain current variation in *M3*. If this condition is met, *M3* and *M4* current variations cancel each other, and the active load impedance does not vary with substrate noise. To quantitatively describe this technique, the impedance of the active load small signal model is derived using a test voltage *Vx* applied to the output node *Z*, as shown in Figure 3.9.

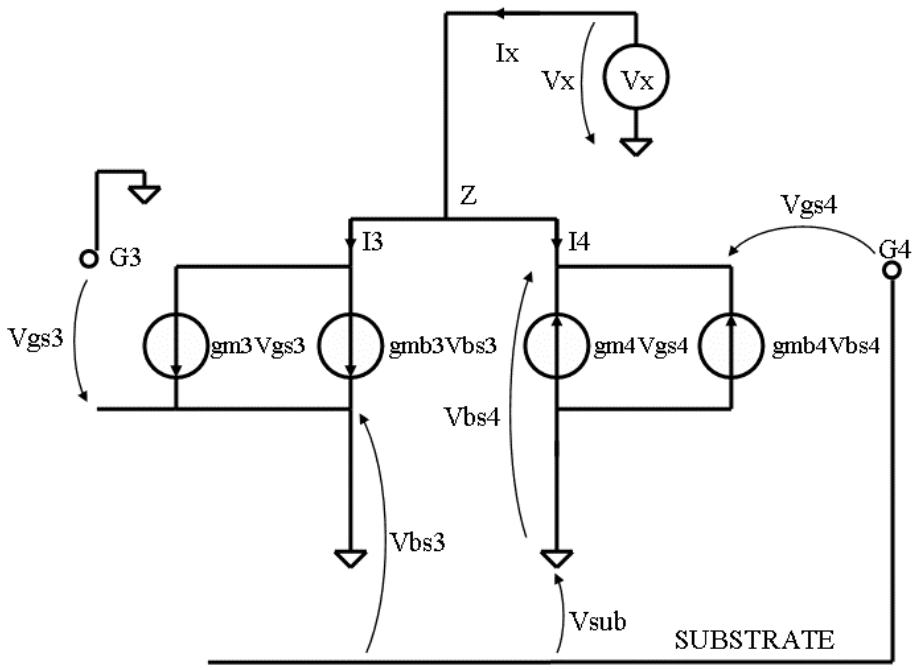


Figure 3.9: Small signal model of the proposed active load with substrate noise cancellation.

The current *Ix* flowing into the active load can be expressed as:

$$Ix = gmb_3 Vbs_3 - gm_4 Vgs_4 - gmb_4 Vbs_4 \quad (3.8)$$

From the small-signal model it can be noticed that $Vbs_3 = Vsub$, $Vbs_4 = -Vx$, and $Vgs_4 = (Vsub - Vx)$. Inserting these conditions in (3.8), *Ix* can be written as

$$Ix = Vx(gm_4 + gmb_4) + Vsub(gmb_3 - gm_4) \quad (3.9)$$

It can be noticed that if $gmb_3 = gm_4$ the term containing *Vsub* vanishes, and the current *Ix* does not depend on *Vsub* anymore. Since the gm_4 and gmb_3 factors can be calculated based on transistor sizes, bias currents, and technology parameters [42], the condition $gmb_3 = gm_4$ can be achieved in the design process by properly sizing *M3* and *M4* transistors. If this condition is met, the impedance of the active load becomes:

$$Z_{LOAD} = \frac{Vx}{Ix} = \frac{1}{gm_4 + gmb_4} \tag{3.10}$$

Equation (3.10) shows that the impedance of the proposed active load structure is independent of substrate noise. A disadvantage of this solution, non-ratiometric NMOS and PMOS structure, makes the noise cancellation dependent on process corners and temperature variations.

3.3.2 Test Chip Implementation

Active loads with and without substrate noise cancellation have been implemented in the differential amplifier delay cells of two ring oscillators, having the schematics shown in Figure 3.10 (a) and (b).

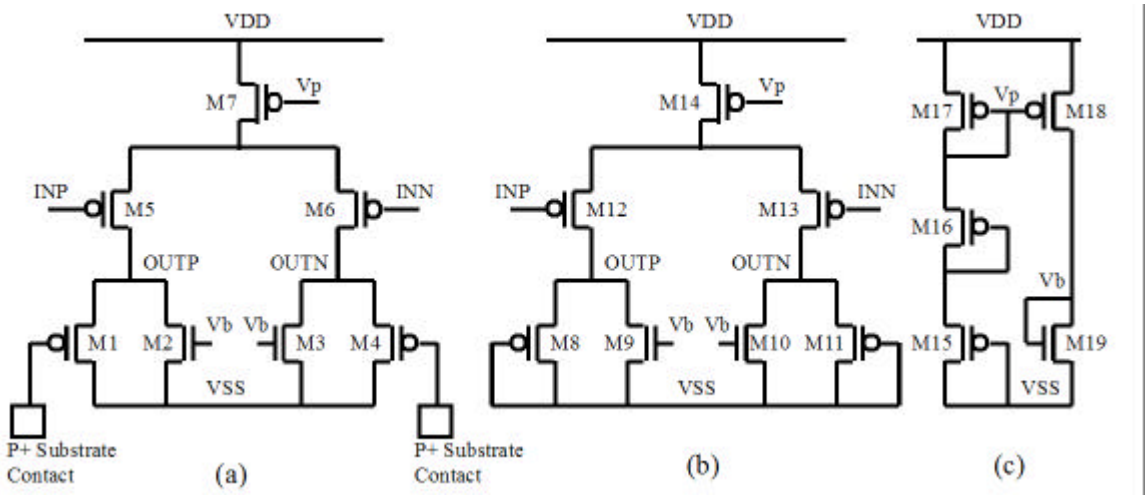


Figure 3.10: Implementation of the substrate noise cancellation experiment for NMOS in active load as part of a differential amplifier delay cell of a ring oscillator; (a) Delay cell with substrate noise cancellation. (b) Delay cell without substrate noise cancellation; (c) Bias generator.

The differential amplifier (a) uses active loads with substrate noise cancellation *M1-M4*, and the differential amplifier (b) uses active loads without noise cancellation *M8-M11*. Each ring oscillator contains ten delay cells. A single bias generator branch

made of PMOS transistors *M15-M17* provides the voltages Vp for all delay cells. Since only PMOS transistors are used, it can be assumed that substrate noise does not couple into Vp. A copy of the current through the *M15-M17* branch is mirrored by M19 into all current source NMOS transistors used in active loads. Ideally the substrate noise should couple as common mode in this multiple branch current mirror. However, because of the spatial variation of substrate noise magnitude across the layout region [9], the substrate noise coupling produces variations of the currents in the active loads. These variations affect the timing performances of the two ring oscillators, which are evaluated using an external spectrum analyzer. Figure 3.11 shows the physical layout of the experiments consisting of two ring oscillators, one with substrate noise cancellation (a), and one without (b).

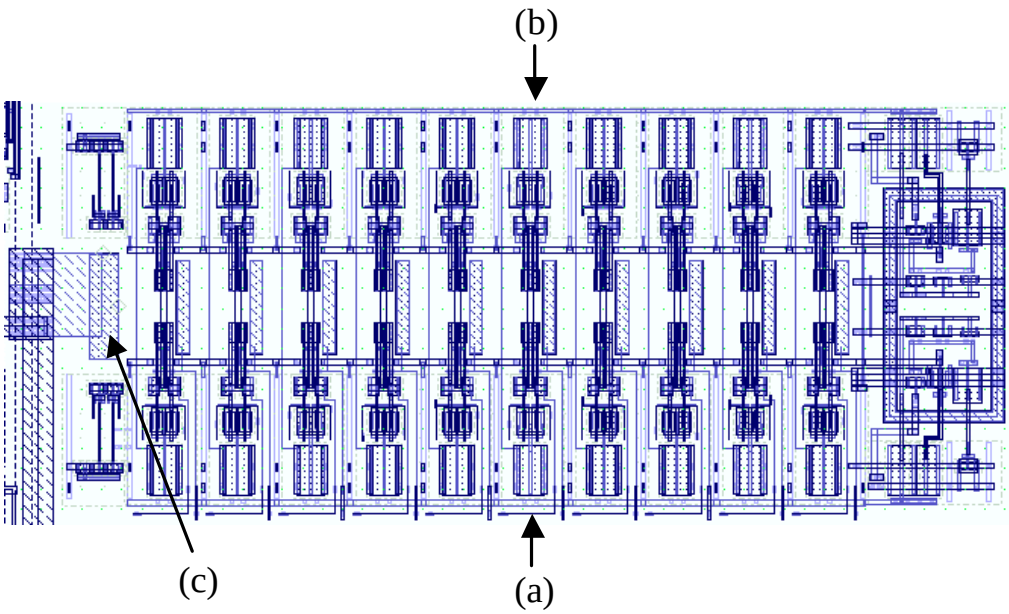


Figure 3.11: Physical layout of the ring oscillators with and without noise cancellation.

The noise signal is provided by an external signal generator and injected into the substrate through a p+ substrate contact (c). This substrate contact has been sized to have 50 Ω input resistance, thus providing matched termination when driven using a 50 Ω characteristic impedance cable.

3.3.3 Simulation Results

Hspice transient simulations have been performed to validate the concept before the test chip fabrication. Figure 3.12 shows the simulation results of the two ring oscillation frequency deviation for a 40 mV change in the substrate potential.

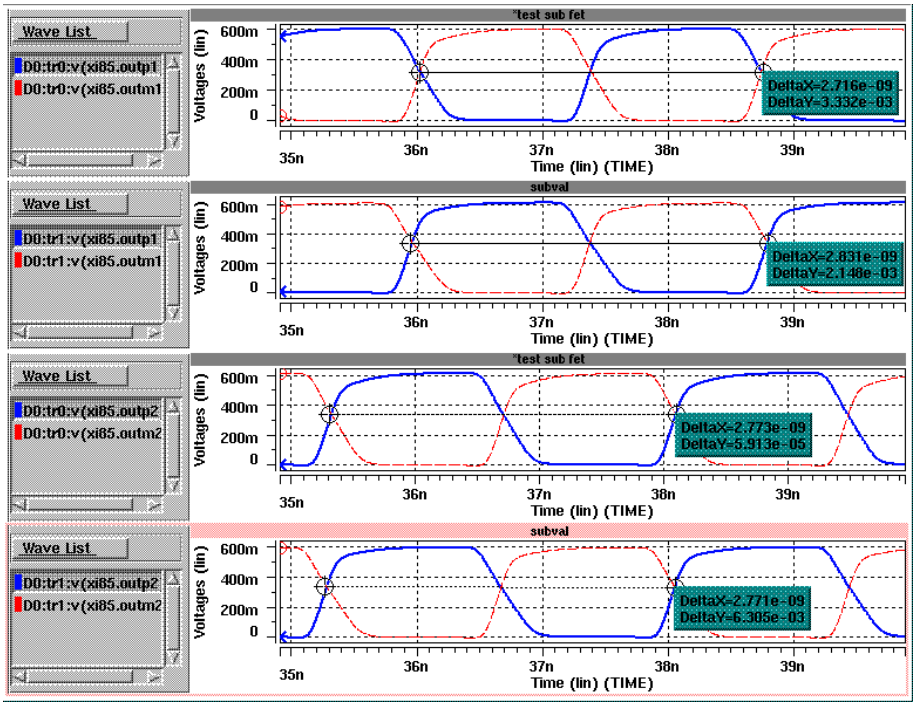


Figure 3.12: Simulations results of the ring oscillator frequency deviation with and without substrate noise cancellation

Panel (a) shows the output waveform of the ring oscillator without noise cancellation for 0 V substrate potential, and panel (b) shows the same waveform for 40 mV substrate potential. The difference in signal periods is 115ps, or 4.2% of the period. Panel (c) shows the output waveform of the ring oscillator with noise cancellation for 0 V substrate potential, and panel (d) shows the same waveform for 40 mV substrate potential. The difference in the periods in this case is 2ps, equivalent to 0.07% of the period. Thus, the substrate noise cancellation technique reduced the noise coupling by a factor of 60, from 4.2% to 0.07%. A performance comparison between the two ring oscillators is presented in the experimental results section.

3.3.4 Experimental Results

The outputs of the two ring oscillators have been connected to a spectrum analyzer, and a sinusoidal noise, having 50 mV amplitude and 5 MHz frequency, has been injected into the substrate. Figure 3.13 shows the measured spectrum of the ring oscillator without noise cancellation.

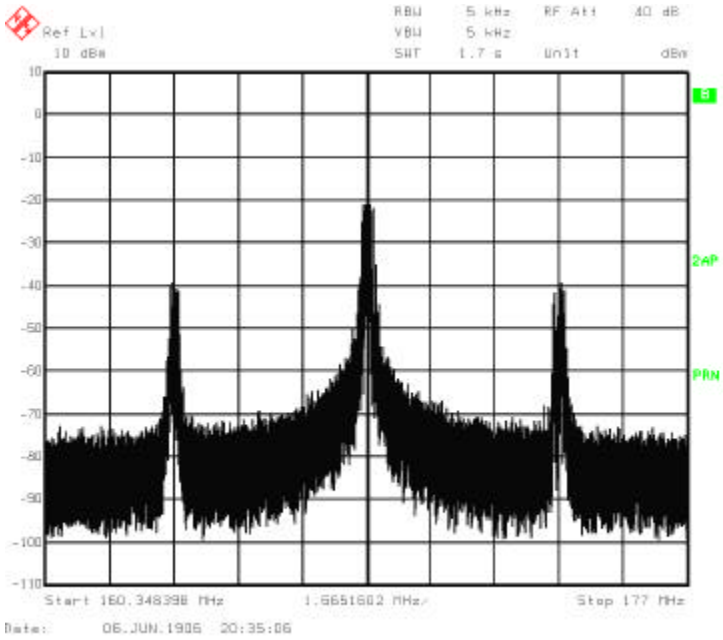


Figure 3.13: Spectrum of the ring oscillator without noise cancellation for an injected substrate noise sinusoidal signal of 50 mV amplitude and 5 MHz frequency.

The injected noise produces sidebands of -40 dBm amplitude at 5 MHz frequency offset. This effect is expected from the perspective of applying the frequency modulation concept to the coupling effect caused by substrate noise [40]. Figure 3.14 shows the spectrum of the ring oscillator using active loads with noise cancellation.

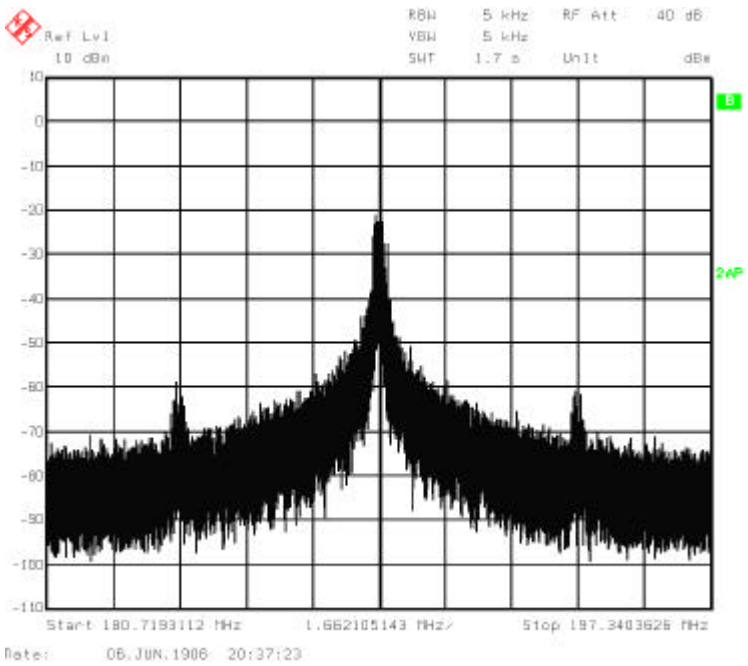


Figure 3.14: Spectrum of the ring oscillator with noise cancellation for an injected substrate noise sinusoidal signal of 50 mV amplitude and 5 MHz frequency.

By comparing the spectrum of the two ring oscillators it can be noticed that the substrate noise cancellation technique reduces the height of the sidebands by 22 dB. Figure 3.15 shows the frequency dependence of the sideband suppression.

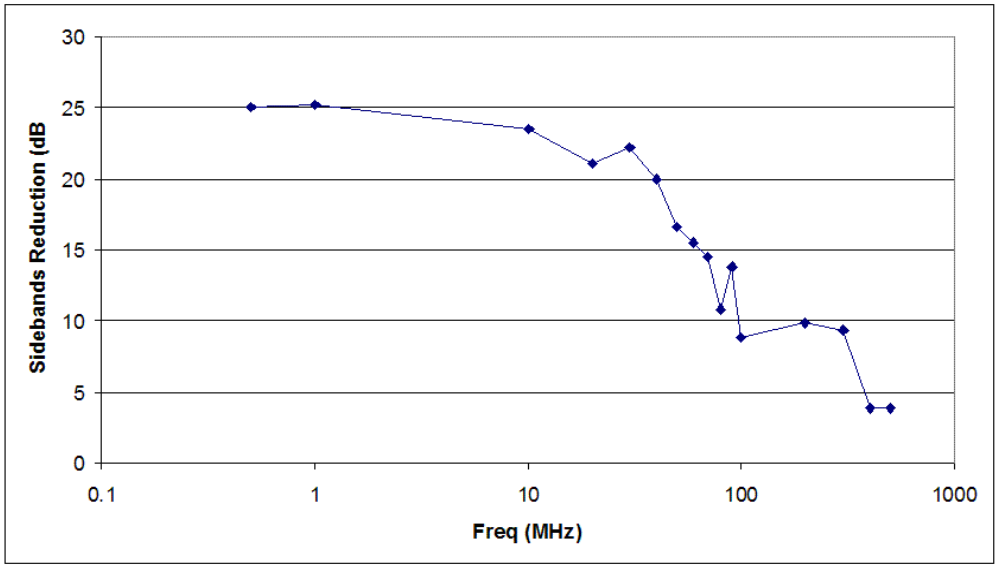


Figure 3.15: Frequency dependence of the sideband suppression.

This measurement shows that the substrate noise suppression decreases from 25 dB at 1 MHz to 4 dB at 600 MHz. Figure 3.16 shows the dependence of the oscillation frequency on the substrate potential, with DC signal injected into the p+ substrate contact.

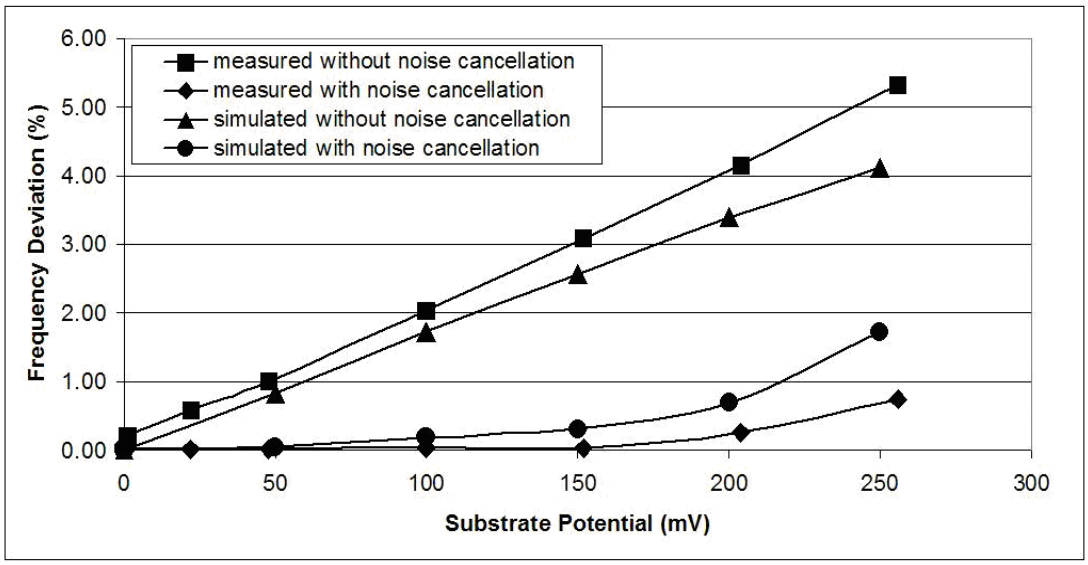


Figure 3.16: Ring oscillators frequency deviation dependence on the substrate potential.

The frequency deviation of the ring oscillator without noise cancellation increases with substrate potential from 1% at 50 mV to 5.5% at 250 mV. The substrate noise cancellation reduces this deviation to 0.02% at 50 mV and 0.8% at 250 mV. Correlation between measurements and Hspice simulations of 95% has been achieved for the ring oscillator with noise cancellation at 50 mV. The correlation decreases for higher substrate potentials to 40% at 250 mV. Correlation of about 80% has been achieved for the ring oscillator without substrate noise cancellation for substrate potentials between 50 mV and 250 mV.

3.4 Substrate Noise Cancellation Using Negative Feedback Circuits

3.4.1 Architecture

Substrate noise cancellation techniques using negative feedback implemented in active guard rings has been reported in [36]-[39]. The proposed method has been derived from these negative feedback active guard rings, by injecting the cancellation noise into electrical circuits, instead of the substrate. It should be noticed that only the effect of substrate noise on circuits is canceled out, not the substrate noise itself. The proposed method can be used in conjunction with other conventional substrate noise suppression techniques. In the case of NMOS transistors used in common-source with source degeneration configuration, a second NMOS transistor operating in the triode region can be used for the degeneration resistor. This way the noise cancellation signal is injected by modulating the *ON* resistance of this NMOS transistor. Figure 3.17 shows a simplified functional diagram of the negative feedback substrate noise cancellation of NMOS transistors in common-source with source degeneration configurations.

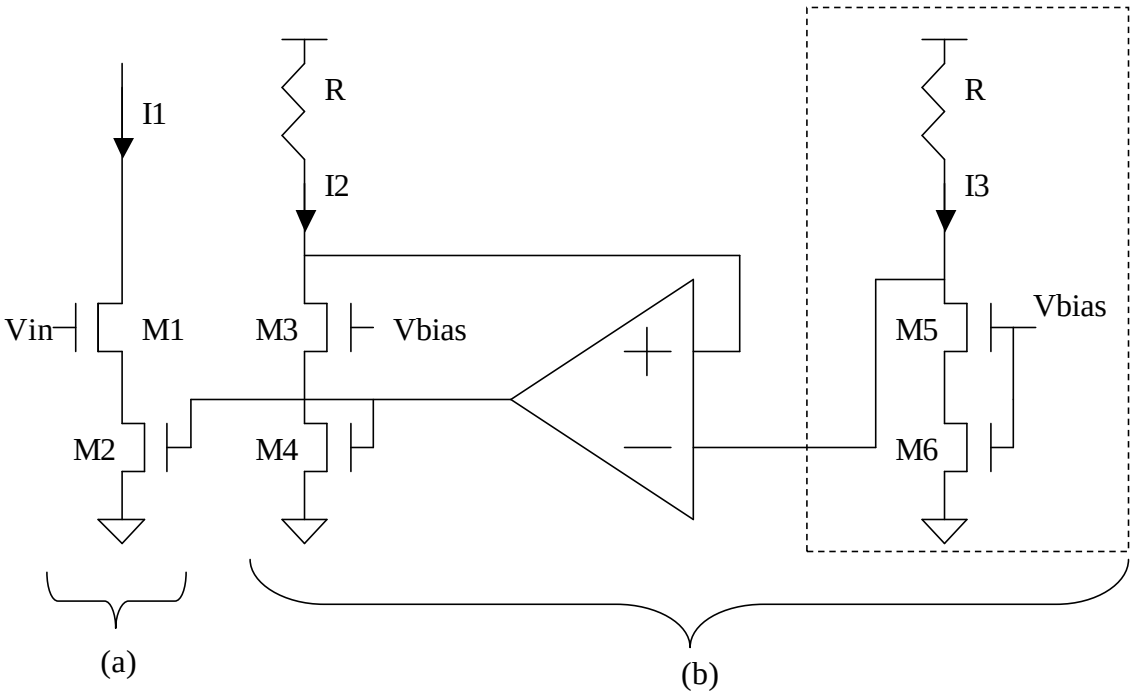


Figure 3.17: Simplified functional diagram of the negative feedback substrate noise cancellation in common-source with source degeneration NMOS transistors; (a) shows the compensated branch, and (b) shows the noise cancellation negative feedback loop.

The compensated transistor, *M1*, is connected in a common source with source degeneration configuration. The degeneration resistor is implemented using transistor *M2*, which operates in the triode region. Substrate noise couples into *M1* and *M2* producing variations of their drain current, I_1. Since I_1 depends on the value of the degeneration resistor, the noise cancellation technique compensate for this current variation by adjusting the value of the degeneration resistor. This value is adjusted by changing the voltage on the gate of M2 transistor. To quantitatively describe this process the transconductance of the *M1-M2* common source with source degeneration structure is expressed by the equation:

$$Gm_1 = \frac{gm_1}{(1 + gm_1 Rs)} \tag{3.11}$$

where gm_1 is the transconductance of *M1*, and *Rs* is the *"ON"* resistance of *M2*. Rs depends on the gate voltage of *M2* by the equation:

$$Rs = \frac{1}{m_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})} \tag{3.12}$$

where μ_n is the mobility, C_{ox} the oxide capacitance, *W* the width of the transistor, *L* the length of the transistor, V_{GS} the gate voltage, and V_{TH} the threshold voltage. Substrate noise couples into both *M1* and *M2* transistors primarily by modulating their threshold voltages. This coupling generates variations of gm_1 in equation (3.11), and V_{TH} in equation (3.12). By adjusting the V_{GS} voltage in equation (3.12), the *Rs* value can cancel out the gm_1 variation, and the overall transconductance Gm_1 can be kept insensitive to substrate noise. The control of V_{GS} is achieved by a negative feedback loop, having the simplified schematic shown in Figure 3.17. An identical branch consisting of transistors *M3* and *M4*, is placed in the immediate vicinity and is biased so that the bias currents $I_1 = I_2$. Since *M1*-*M2* and *M3*-*M4* branches are placed in the physical layout close to each other, and are biased with equal currents, it is assumed that the substrate noise couples identically in both of them. A reference branch, *M5*-*M6* built identically with *M1*-*M2* and *M3*-*M4*, is placed in a "noiseless" location. In this implementation the noiseless location is placed far from the noise source and inside a guard ring, as shown in Figure 3.18. It is assumed that the substrate noise coupling into *M5*-*M6* branch is very small and can be neglected. A disadvantage of placing the reference branch far from the compensated circuit is the transistors mismatch, which may affect the DC values of *I2* and *I1*. The substrate noise coupling into the *M1*-*M2* current will couple in the same manner into the *M3*-*M4* current, but not into the *M5*-*M6* branch. Since the *M3*-*M4* and *M5*-*M6* branches are biased using equal currents and have identical load resistors, the substrate noise coupling translates into voltage variations between the drains of M3 and M5 transistors. An operational amplifier senses this voltage variation and controls the *"ON"* resistance of *M4* in a negative feedback loop, so that the drains of *M3* and *M5* are kept at the same voltage.

This way the substrate noise coupling into the *M3-M4* current branch has been canceled by controlling the value of the degeneration resistor. The output of the operational amplifier also controls the gate voltage of *M2*, and thus the degeneration resistor of the *M1-M2* branch. Since the *M1-M2* and *M3-M4* branches are identical and biased at equal currents, the substrate noise cancellation obtained for the *M3-M4* current applies also to the *M1-M2* current. This way *M1* is configured as a common source amplifier with source degeneration, and the coupled substrate noise is canceled out by the negative feedback loop.

3.4.2 Test Chip Implementation

This noise cancellation using negative feedback experiment has been implemented in sensors group 4 of Test Chip 3. The outputs have been routed to an external oscilloscope through multiplexers, buffers, and the output stage. Figure 3.18 shows the physical layout of this experiment.

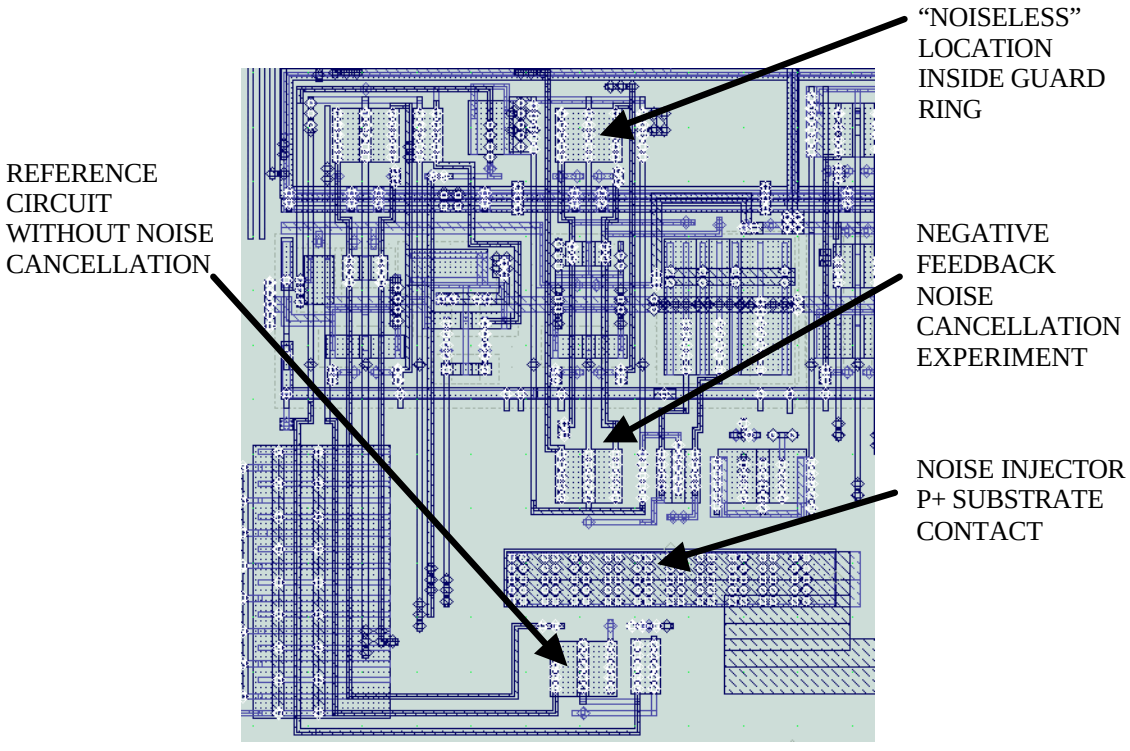


Figure 3.18: Physical layout of the negative feedback noise cancellation experiment

Two structures have been implemented, one with substrate noise cancellation using negative feedback, and another one without noise cancellation for reference measurements. The operational amplifier is made of a typical differential stage with current mirror load [43].

3.4.3 Simulation Results

Hspice transient simulations have been performed to validate the concept before the test chip fabrication. Figure 3.19 shows the simulation results of the two structures, with and without noise cancellation.

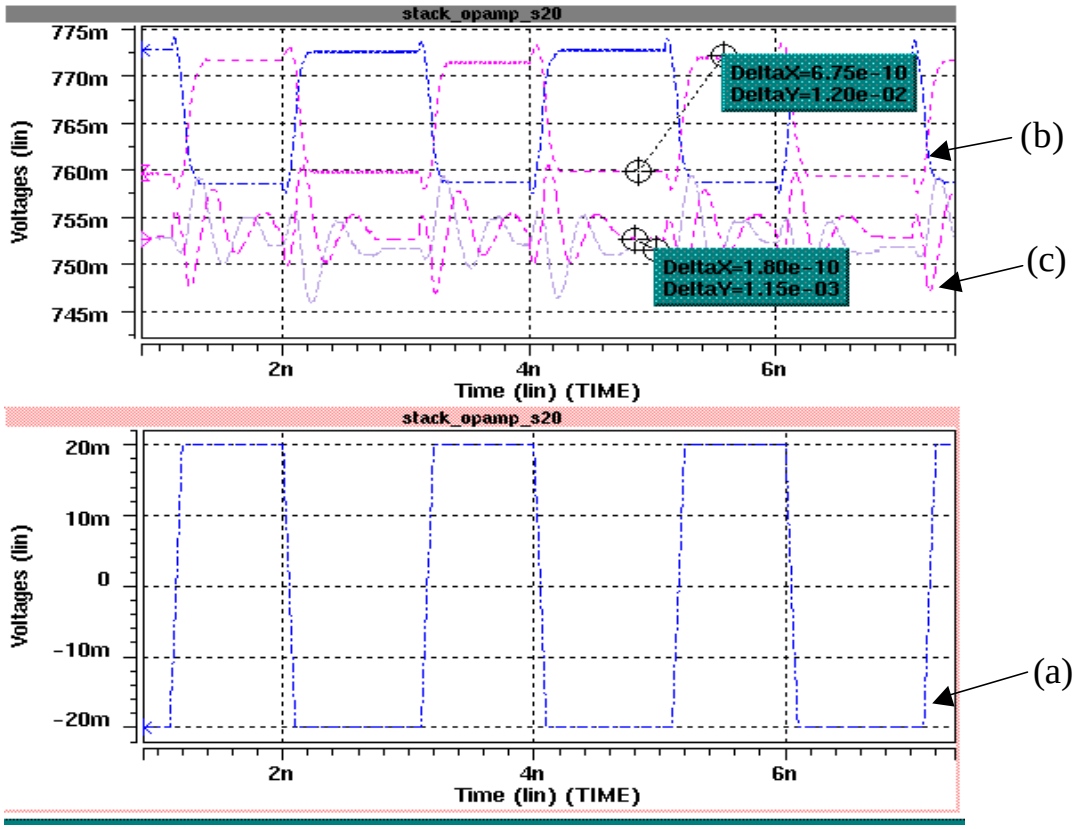


Figure 3.19: Hspice simulation results of the negative feedback noise cancellation technique for common source NMOS transistors with source degeneration.

Waveform (a) shows the square wave substrate noise signal having an amplitude of 40 mV peak-to-peak, and frequency of 500MHz. Waveform (b) shows the differential substrate noise coupled into the transistor without substrate noise cancellation, and waveform (c) shows the substrate noise coupled into the transistor with noise cancellation. It can be noticed that coupling reduction of about 12 times has been achieved with this technique. However, because of the frequency response limitations of the negative feedback loop, the compensation does not work well at high frequencies. This limitation generates glitches and ringing in the transient simulation of fast rise and fall times edges, as shown in Figure 3.19.

3.4.4 Experimental Results

The outputs of the two structures, with and without noise cancellation, have been routed to the external oscilloscope. Noise has been injected into the substrate through the p+ noise injector substrate contact. Figure 3.20 shows the transient response of the NMOS transistor with noise cancellation, compared with the reference NMOS transistor without noise cancellation, for a square wave substrate noise of 50 mV amplitude and 100 MHz frequency.

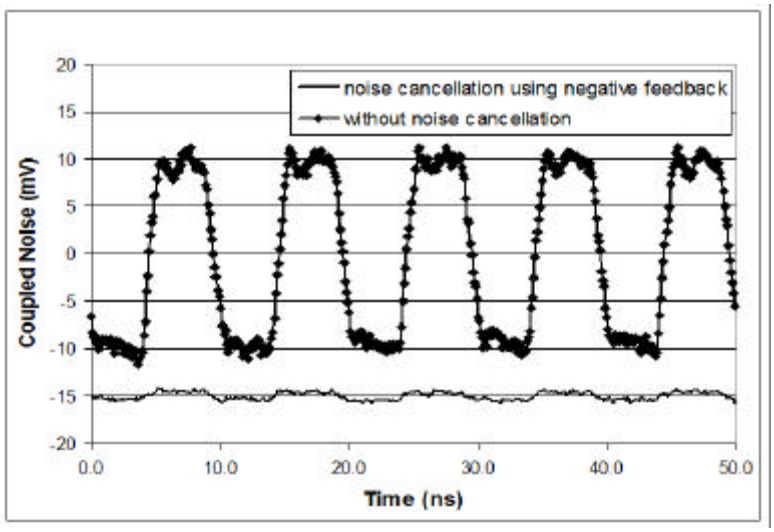


Figure 3.20: Transient response of NMOS transistors with and without negative feedback noise cancellation.

It can be noticed that the substrate noise cancellation technique reduces the coupled noise amplitude from 20 mV to about 2 mV. The DC offset is mainly due to the difference between the bias currents through the compensated and non-compensated circuits. Figure 3.21 shows the frequency dependence of the negative feedback noise suppression, for a sinusoidal signal injected into the substrate.

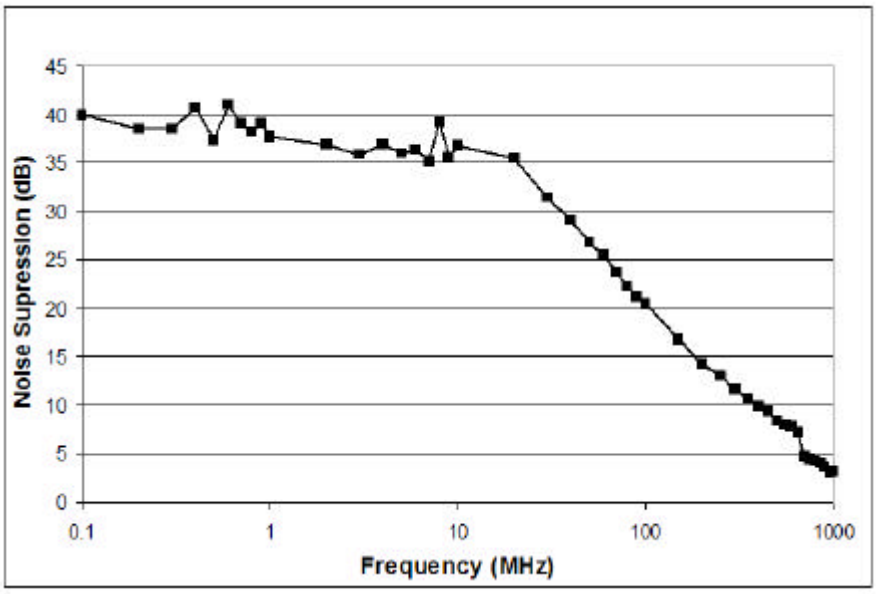


Figure 3.21: Frequency dependence of the negative feedback noise suppression, for a sinusoidal signal injected into the substrate.

Between 35 dB and 40 dB suppression is achieved at frequencies lower than 20 MHz, and the suppression decreases for higher frequencies. This decrease with frequency is primarily caused by the performance limitation of the operational amplifier, and has been expected from the glitches and ringing seen on the transient Hspice simulations. Based on this frequency response, decaying glitches are expected in the transient waveform with noise cancellation in Figure 3.20, but the measurements do not show them. The full understanding of why the transient waveform does not show decaying glitches is not known yet, but a possible explanation can be based on the process of doing the measurements. Each point in the transient waveform with noise cancellation is the result of averaging 1000 binary search results in the waveform sampling

process. This averaging was needed to reduce the effect of random noise when measuring a very low amplitude signal, in this case having the same order of magnitude as the random noise. A disadvantage of averaging is the potential roll off of sharp edges due to the timing jitter of the measured signal and latching clock. This roll off may translate into bandwidth reduction, which in this case may be the cause of not capturing the decaying glitches. The jitter of the noise injector and latching clock cannot be measured separately in the current implementation, and, a future redesign of the experiment is needed for this.

3.5 Conclusions

This chapter has presented three active compensation techniques for reducing the substrate noise coupling effect in common-source NMOS configurations. The first technique uses a source-follower PMOS transistor to sense the substrate potential and generate a noise cancellation current. Typical implementation of this technique places the substrate sensing PMOS transistor in a separate noise cancellation branch connected in parallel with the NMOS transistor. The second technique is a derivation of the first technique for active loads made of a current-source and diode-connected transistors. In this case the noise cancellation PMOS replaces the diode-connected transistor used by the active load. The third technique implements a negative feedback loop which cancels out the drain current variations due to substrate noise of a common-source NMOS transistor with source degeneration, by controlling the value of the degeneration resistor. The first two noise cancellation structures are small and easy to implement in typical designs. The third technique is more complex, and it requires significant area in the physical layout, but it achieves more suppression especially at low frequencies. All these three noise cancellation structures can be used in conjunction with conventional guard ring substrate noise suppression techniques.

Chapter 4

Prediction of Substrate and Power Supply Noise Coupling in Early Stages of the Design Process

4.1 Introduction

In mixed signal Systems-on-Chip (SoC) the noise generated by the digital cores couples into the analog circuits degrading their performance. The effect of noise coupling is often noticed after fabrication during characterization. Because of this, a large effort has been made recently to develop modeling techniques that predict the noise coupling before fabrication. Typical techniques use the circuit description and the technology information as inputs, and generate outputs in the form of either substrate noise voltage or substrate noise coupling netlist. Both output types can be further incorporated in simulations of the sensitive analog circuits. These simulations are beneficial to designers who can modify or redesign the affected circuits before fabrication. Typically, the accuracy of the prediction depends on the level of details in the circuit description, which is imprecise in the early architectural stage of the design, and gradually increases in complexity as the project advances through the design process. The modeling techniques based on physical layout are more accurate than the ones using schematic, behavioral model, or architectural definition. On the other side, especially for complex mixed signal SoC, once the entire layout has been completed it is often too late to make major changes to the design. Thus, it is desirable to identify potential noise coupling problems early in the design process, when changes have minimum impact on cost and schedule. Previous reports of noise coupling modeling techniques focus on various stages of the design process, from architectural definition to physical layout. Table 4.1 shows a comparison of different techniques, based on model type, inputs, outputs, and accuracy.

Table 4.1: Comparison of previous reported substrate and power distribution modeling techniques, and comparison with the proposed prediction method.

REFERENCED MODELING TECHNIQUES / PROPERTIES	[44]	[46]	[48]	[49]	[18]	[52]	[54]	[57]	[59]	[60]	[63]	[64]	[65]	PROPOSED TECHNIQUE
MODEL TYPE														
LUMPED DIGITAL	X	X	X	X	X	X						X	X	X
DISTRIBUTED DIGITAL									X	X	X			
LUMPED ANALOG	X	X										X	X	
DISTRIBUTED ANALOG							X	X	X	X	X			X
MODELS PACKAGE/PCB	X	X		X	X				X	X	X	X	X	X
MODEL INPUT														
ARCHITECTURAL SPECIFICATIONS	X												X	X
BEHAVIOR MODEL		X			X									
DIGITAL CORE NETLIST			X	X		X			X			X		
DIGITAL CORE LAYOUT							X	X	X	X	X			
ANALOG CORE NETLIST									X					
ANALOG CORE LAYOUT							X	X	X	X	X			
MODEL OUTPUT														
LUMPED SUBSTRATE VOLTAGE	X	X	X	X	X	X						X	X	
TWO-DIMENSIONAL SUBSTRATE VOLTAGE							X							X
ANALOG CORE SUBSTRATE NETLIST								X	X	X	X			
ESTIMATED ACCURACY	L	H	H	M	M	H	H	H	H	H	H	M	L	L

The accuracy has been estimated based only on the input type, so that the techniques extracting layout parameters have high accuracy, the ones based on schematic or behavioral models medium accuracy, and the ones based on the architectural

specifications low accuracy. The modeling techniques [44], [46], and [59]-[65] include the effects of power distribution parasitics on package and board. The substrate noise coupling through power and ground lines is considered dominant in [11]-[12]. The high accuracy techniques in [54], [57], [59], [60], and [63] extract the circuit description from the physical layout, and thus, are more suitable for design verification. Their outputs are either two-dimensional maps of substrate noise voltage [54], or substrate netlists [57], [59], [60], and [63]. Complexity reduction techniques have been implemented to simplify the netlists and make possible the simulation of the entire chip. While these techniques are very accurate, they can be used only after the physical layout has been defined. Since problems found at this stage of the design may require major rework that would impact the cost and schedule, it is desirable to be able to identify potential noise coupling problems earlier in the process. Prediction of noise coupling in the pre-layout stage has been reported in [48]-[49], [52], and [64]. These techniques take inputs from schematics, and generate either a lumped [48]-[49], [52], or a distributed two-dimensional, [64], noise voltage of the substrate. Noise coupling prediction based on behavior models has been reported in [46] and [18]. These techniques create macro-models that represent the substrate as a single lumped node. The noise voltage at this node is generated based on the digital switching activity extracted from the behavior models. While the pre-layout techniques address the noise coupling prediction at the schematic and behavioral model stages, some decisions that affect noise coupling are often taken during architectural stages of the design process. Such decisions include technology type, partitioning of the digital and analog regions, space allocation for noise suppression guard rings, placement of power and ground pins, and package requirements. Because the schematic or HDL code is not available at this stage, the prediction is typically done only based on the architectural specifications, the data from previous designs, and the technology information available in the design manual. Noise coupling prediction in the architectural stage of the design has been reported in [44] and [65]. The technique in [44] uses the limits for supply bounces and rough power/ground supply network specifications to estimate the digital switching activity. The noise injection is assumed

only through n-well capacitance and substrate contact resistance. Since these parameters are layout dependent and not available at this stage, the prediction method uses an average density of n-wells and substrate contacts. The technique in [65] uses the power dissipation specification available from system-level power estimation, and creates a macro-model of the entire system in terms of small-signal linear equivalent circuits. Both [44] and [65] estimate the noise voltage at the substrate as a lumped node. While the lumped noise voltage provides an estimate of the overall substrate noise, a two-dimensional distribution would be more beneficial for analyzing the power/ground pins placement, the layout floor plan of sensitive blocks, and the effect of noise suppression guard rings.

The proposed modeling technique overcomes this issue by generating a two-dimensional map of the substrate noise in the analog region of the chip, still based only on information available in the architectural stage of the design process. For comparison purposes, this technique is shown in the last column of Table 4.1. Furthermore, to reduce complexity for chips having the analog region symmetrically placed on one side of the chip, an alternative one-dimensional mesh model of the analog substrate has been developed. This chapter is organized as follows. Section 4.2 presents the motivation and requirements of the proposed noise coupling prediction technique, Section 4.3 a description of simplifying assumptions made by this technique, Section 4.4 the modeling methodology, Section 4.5 the model construction, and Section 4.6 the experimental results. Conclusions are given in Section 4.7.

4.2 Motivation and Requirements of the Proposed Noise Coupling Prediction Technique

In a typical mixed-signal SoC design the digital core is developed simultaneously with the analog circuits. Early stages of the design focus on architecture definition, technology and package selection, power and die size estimation, area partition

between digital and analog cores, and power and ground pin assignments. Analog designers focus on feasibility studies of critical circuits using simulations to evaluate performance. Important decisions can be made based on these simulations regarding circuits topologies, technology options, block level floor-planning, pins assignment, package definition, area partition, and implementation of guard rings for noise coupling suppression. These decisions are often hard to change later as the chip advances in the design process, and changes affect significantly the cost and schedule. The library models used in analog simulations include substrate terminals, which can be used to inject noise and evaluate how it affects the circuit performance. It is then desirable to estimate the expected substrate and power supply noise in order to simulate critical analog circuits. The estimation of noise coupling at different stages of design has been the target of numerous published modeling techniques and commercial tools. However, most of them require the layout to be complete, or at least the schematics or behavior models, which are not available in the early stages of design. Techniques using only the information available in early stages of the design have been reported in [44] and [65], which estimate the noise coupling as a voltage at a lumped substrate noise node. While this can be useful in some simulations, it does not represent the real case in which the noise coupling varies across the analog region. Thus, they cannot evaluate the efficiency of coupling suppression techniques using guard rings, common mode noise cancellation floor planning and power and ground pins assignment. Because of this, it is desired to develop a technique that estimates the substrate and power noise at each location in the analog region based only on information available in early stages of the design process. This technique needs to take the information available in the design specifications of the digital core and power distribution, technology manual, package datasheet or specifications, and data from previous designs, and to estimate the substrate and power supply noise at each location of the analog region. The estimation accuracy is lower compared to that provided by the layout, schematic, or behavior models extraction tools, but good enough to identify major noise coupling issues in early stages of the project.

4.3 Modeling Assumptions

The following simplifying assumptions have been made to overcome the limited or unavailable information in early stages of the design process. These assumptions are based on results of previously published papers.

1. Only lightly doped substrates will be considered, since they are preferred for mixed signal SoC [11].

2. The dominant noise is generated in the digital cores and couples into the analog circuits. The noise generated in the analog circuits can be neglected [44].

3. The mechanism of substrate noise coupling through the power and ground distribution is considered dominant compared to other mechanisms [11]-[12]. The noise couples into substrate through the substrate and well contacts connected to the on chip power and ground grids [65].

4. The high density of grounded substrate contacts in the digital cores shunt the substrate to the digital ground, allowing the digital section of the substrate to be modeled as a single lumped node [45]. The substrate noise can be assumed to be generated only from the *dI/dt* transients on the ground and power lines [45].

These simplification assumptions lower the accuracy of the model, but make possible the estimation of substrate and power supply noise in the early stages of the design.

4.4 Methodology

4.4.1 Lumped-Distributed Hybrid Model of Substrate and Power Distribution

The proposed technique creates a lumped-distributed hybrid model of the chip substrate and power distribution. The technique models the digital region by lumped elements, and the analog region by a two-dimensional *RC* mesh. The lumping of digital region is based on assumption 4, and the work published in [45]. The two-dimensional mesh makes possible the estimation of noise coupling at each location in the analog region. The power distribution on package, PCB, and interconnects is modeled using lumped elements. Figure 4.1 shows a simplified block diagram of the proposed model.

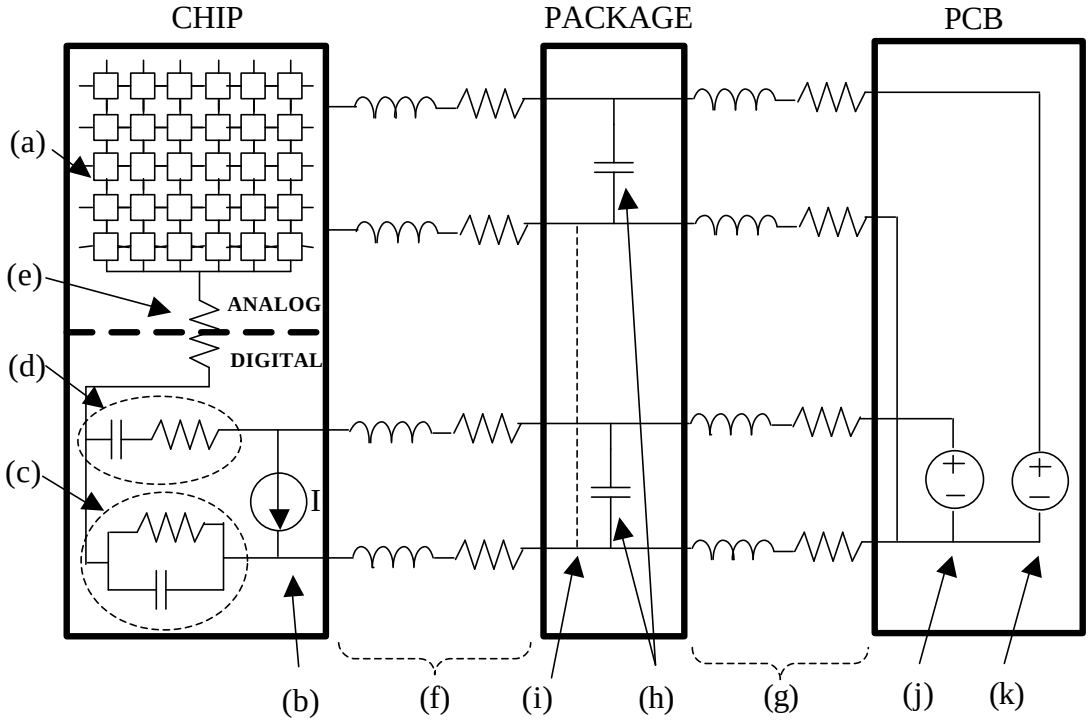


Figure 4.1: Simplified block diagram illustrating the chip, package, PCB, and interconnect models used by the proposed noise prediction technique.

The chip model includes the analog region substrate and power distribution two-dimensional mesh (a), the digital switching current model made of a current source

(b), the coupling through the total substrate contact resistance and n-diffusion capacitance modeled by a parallel *RC* network (c), the coupling through the total n-well depletion capacitance modeled by a series *RC* network (d), and the coupling between the digital and analog substrate regions modeled by a lumped resistor (e). This resistor connects to the analog mesh cells adjacent to the digital substrate. In this case one side of the mesh is shown connected to the resistor, but depending on the physical placement of the analog core, the resistor may connect to two, three, or all four sides of the mesh. The chip to package and package to PCB interface pins are modeled by series inductor and resistor networks (f) and (g). The package decoupling capacitors, if implemented, are modeled by the capacitors (h). For better accuracy, full models including parasitic inductance and resistance can be used for the package decoupling capacitors. When the package ground is shared between analog and digital circuits, the model is adjusted by connecting a shorting wire (i). The PCB analog and digital supplies are modeled by the voltage supplies (j) and (k). For better accuracy, the PCB parasitic inductance and resistance, and the decoupling capacitors, can be included in the model.

4.4.2 Estimation of the Digital Core Switching Noise

Digital switching noise is generated by the current source (b), and represents the estimation of the worst case switching current in the digital core. Once generated, the digital switching noise propagates through the substrate and power distribution into the mesh model of the analog core. One difficult task in early stages of the design is to estimate the digital switching noise. Previously published papers present multiple methodologies for estimating the switching activity in a digital circuit. In [44] it is proposed the use of supply bounces limits and rough power-ground network characterization, available early in the design process. In [65] the switching activity is represented by a computed *rms* current, and all the analysis is done in terms of a "small signal" linear equivalent model. This technique does not model the transient characteristics of the circuit, but it predicts an *rms* equivalent noise in the substrate.

Other methodologies extract the switching activity from the Verilog code and use Spice simulations of the digital library macro-models to estimate the switching current. The proposed technique models the digital switching noise in frequency domain simulations by a sinusoidal current source using the power spectrum density estimate method presented in [44], and in transient simulations by a pulsed current source having the amplitude and rise/fall times estimated from the dynamic power of the digital core, clock frequency, and rise and fall times of the digital cells, information typically available early in the design process. This estimation is based on a number of simplification assumptions illustrated in Figure 4.2.

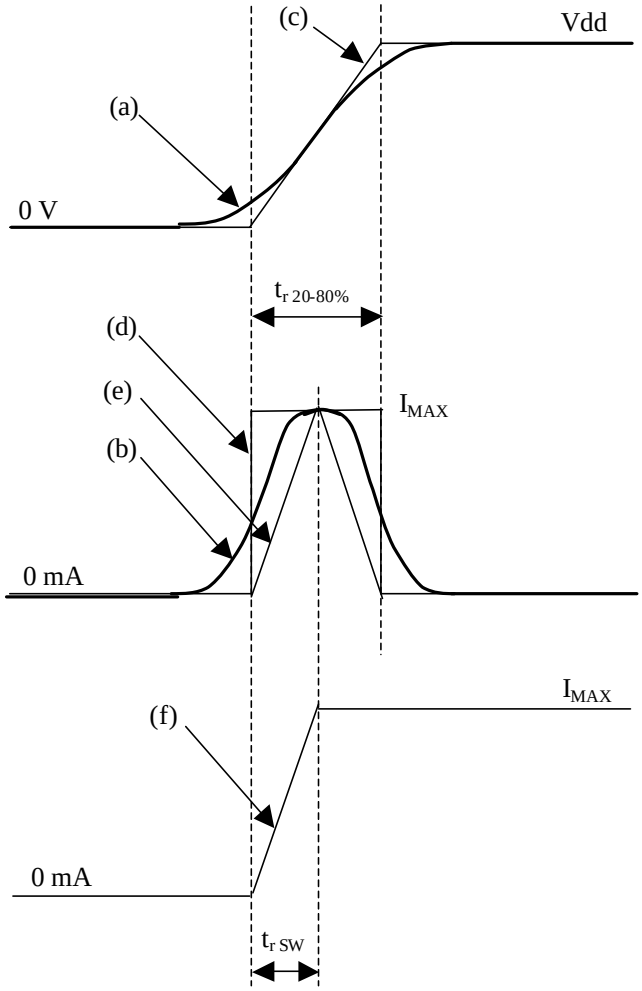


Figure 4.2: Illustration of the simplifying assumptions made to derive the rise time and amplitude of the pulsed current source modeling the digital switching noise.

Waveform (a) represents the voltage variation of the switched capacitance during a rising edge transition, and waveform (b) the corresponding charging current. This current also flows through the on-chip and off-chip power distribution network, and, because of the non-zero impedance of interconnects, it produces voltage variations on the power and ground. The chip circuits see these voltage variations as digital switching noise. Because of the parasitic inductance of the power distribution network, the digital switching noise depends mainly on the derivative of the charging current, *dI/dt*. The worst case switching noise occurs at the maximum value of *dI/dt*, which corresponds to the maximum slope on waveform (b). Since the proposed technique models the worst case switching noise transients, it uses a current source that generates a pulsed square wave having the amplitude and rise/fall slopes equal respectively to the maximum amplitude and maximum dI/dt of the charging current. To estimate these parameters, first the total switched capacitance is derived. The dynamic power, is expressed by equation (4.1):

$$P = a \cdot C \cdot Vdd^2 \cdot f \tag{4.1}$$

where a is the switching activity, C the total switched capacitance, Vdd the power supply voltage, and f the frequency of the digital clock. Using the estimated dynamic power of the digital core, the total switched capacitance can be calculated as:

$$C = \frac{P}{a \cdot Vdd^2 \cdot f} \tag{4.2}$$

Since only part of this capacitance is switched at one time, C needs to be adjusted by multiplying with the switching factor a. The adjusted switched capacitance C_{adj} equals:

$$C_{adj} = \frac{P}{Vdd^2 \cdot f} \tag{4.3}$$

The adjusted switched capacitance C_{adj} is charged from *0 V* to *Vdd* during rise time and discharged back to *0 V* during fall time. The rise and fall times for the digital core and I/O cells are specified in the digital library, or can be easily obtained from Hspice simulations of the digital library models. The 20-80% rise time of waveform (a), $tr_{20\text{-}80\%}$, is marked in Figure 4.2. The first simplification creates waveform (c), which has a constant slope assumed to be equal to the maximum *dV/dt* of waveform (a), and a transition time equal to the 20-80% rise time of waveform (a). Assuming waveform (c) represents the voltage on the switched capacitance, the corresponding charging current is an ideal square wave pulse shown by waveform (d). Since the slope of (c) equals the maximum *dV/dt* of (a), the amplitude of the square wave pulse charging current (d) equals the peak value of the charging current (b). Thus, the maximum charging current of waveform (b) can be calculated as:

$$I_{MAX} = C_{adj}\frac{dV}{dt} = C_{adj}\frac{Vdd}{tr_{20-80\%}} \tag{4.4}$$

The second simplification assumes that the slope of waveform (e), equals the maximum *dI/dt* of the charging current (b). Based on this assumption, waveform (e) has the amplitude equal to the peak value of the charging current (b), and the rising and falling slopes equal to the maximum *dI/dt* of the charging current (b). Thus, waveform (e) represents the worst case charging current transient, and can be used to construct the digital switching noise current. This current is represented in Figure 4.2 by waveform (f). Inserting C_{adj} expression (4.3) in equation (4.4), the amplitude of the switching current, I_{SW}, can be calculated as:

$$I_{SW} = I_{MAX} = \frac{P}{Vdd \cdot f \cdot tr_{20-80\%}} \tag{4.5}$$

The rise and fall times are equal to:

$$tr_{SW} = tf_{SW} = \frac{tr_{20-80\%}}{2} \tag{4.6}$$

It can be noticed that all parameters needed to construct the digital switching noise model are typically available in the early stages of the design process.

In some cases the dynamic power estimate consists of two components: the digital core power, and the input-output (I/O) cells power, thus, two values of the switched capacitance can be calculated. The digital core switched capacitance is charged and discharged with shorter rise and fall times compared to the I/O capacitance. Thus, when the power estimate is split between digital core and I/Os, the switching noise is modeled by two pulsed current sources mounted in parallel. For simplicity the two current sources are assumed to operate at the same frequency and phase, only the amplitudes and rise and fall times are different.

4.5 Model Construction

4.5.1 Analog Region

The mesh model presented in this section applies to flip chip mounted on BGA package technology, but other types of chips and packages can be derived in a similar way. The analog region is divided in squares centered on the chip pins, as shown in Figure 4.3, and named macro-cells.

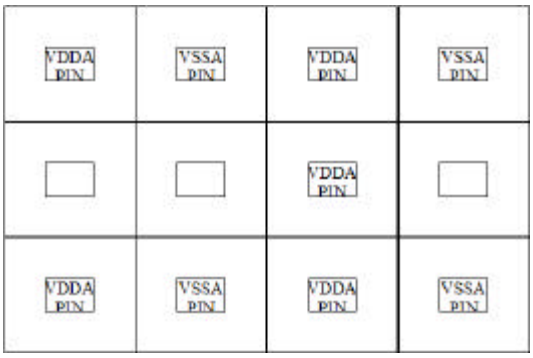


Figure 4.3: Analog region mesh model divided in squares centered on the chip pins

Each macro-cell is further divided in N^2 small-cells, choosing N depending on the desired granularity. Figure 4.4 shows an example of a macro-cell centered on an analog power pin, VDDA, and containing 25 small-cells. Small-cells have three terminals on each side, representing power, ground, and substrate. Two additional terminals for power and ground, *VDDLOC* and *VSSLOC*, are placed in the middle. Macro-cells centered on a power or ground pin, have the center *VDDLOC* or *VSSLOC* terminal connected to the corresponding power or ground in the chip model. Macro-cells centered on signal pins leave *VDDLOC* and *VSSLOC* pins open. If noise suppression guard rings are implemented, the corresponding center terminals are connected to the guard ring model.

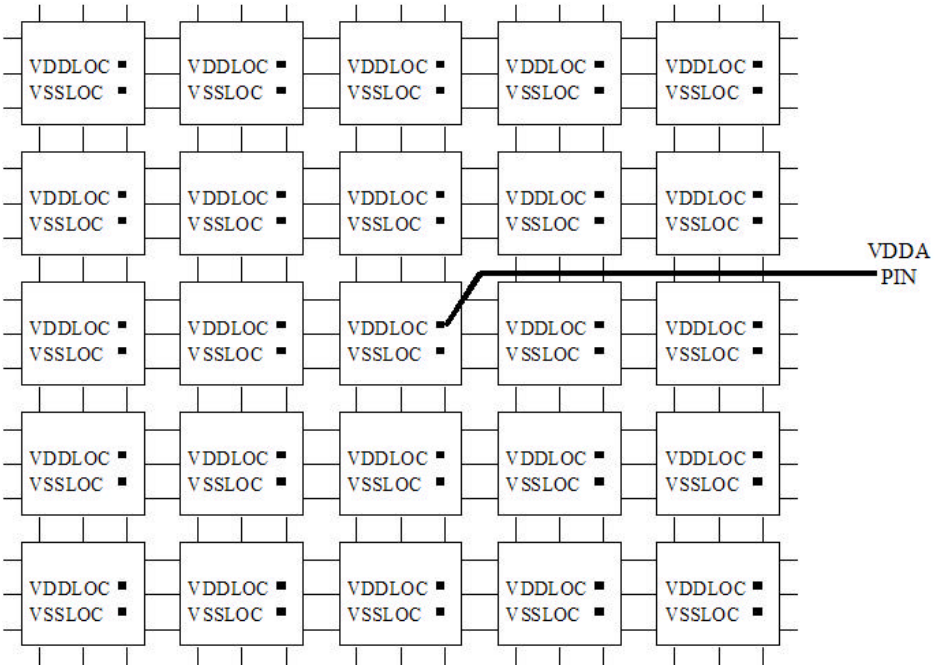


Figure 4.4: An example of a macro-cell centered on an analog power pin, VDDA, and containing 25 small cells.

Figure 4.5 shows the schematic of a small-cell. *R_VDD*, *R_VSS*, and *R_SUB* are the resistances of the power, ground, and substrate. *R_NWELL* and *Cj_NWELL* represent the n-well vertical resistance and junction capacitance. *R_SUBC* represents the total substrate contact vertical resistance, and *CJ_NDIFF* the total n-type diffusion

capacitance. Pins *VDD_LOC* and *VSS_LOC* represent the power and ground nodes in the center of the cell.

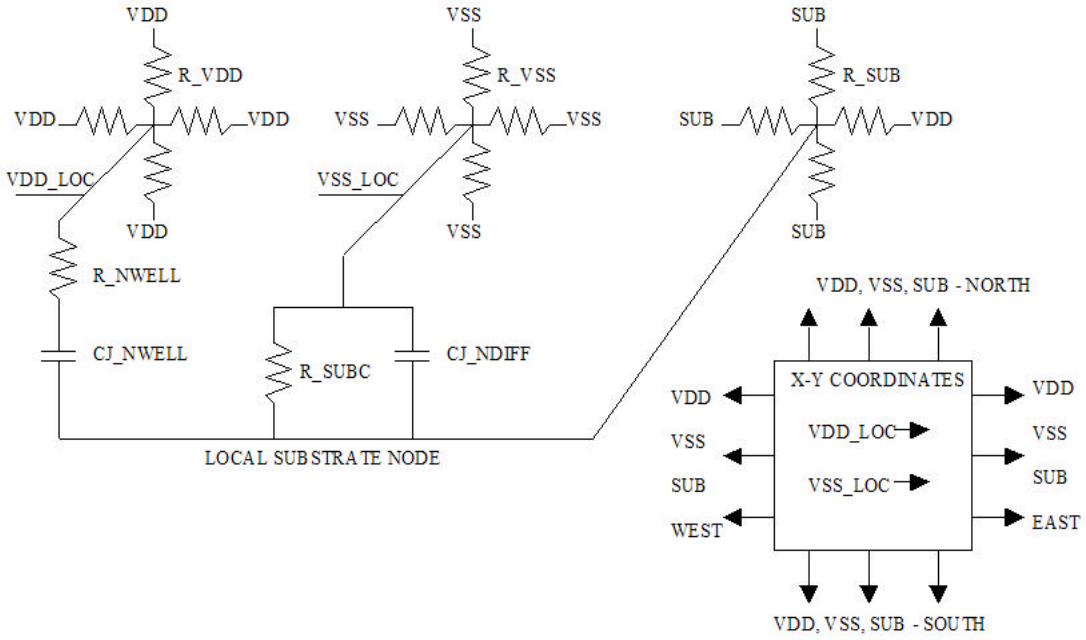


Figure 4.5: Schematic diagram of a single cell of the analog region mesh model.

The resistances *R_VDD* and *R_VSS* can be calculated from the geometry of a typical power grid cell, shown in Figure 4.6. The power grid cell can be developed based on the specifications of the thick metal wires available in the process design manual.

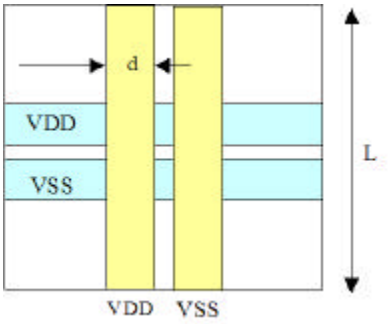


Figure 4.6: Physical layout of a typical power grid cell.

R_VDD and *R_VSS* can be calculated from the geometrical dimensions *L* and *d*, and the metal layer resistance *Rm*, using the following equations:

$$R\_VDD = \frac{1}{2} Rm \frac{L}{d} \tag{4.7}$$

$$R\_VSS = \frac{1}{2} Rm \frac{L}{d} \tag{4.8}$$

The other elements are sized using the technology parameters listed in Table 4.2 and three statistical parameters estimated from typical or previous designs.

Table 4.2: Technology parameters used in the derivation of model elements

Parameter	Notation
Metal layer resistance <O/square>	*Rm*
Substrate sheet resistance < O /square>	*Rsub*
Vertical p-well resistance < O - μm^2>	*Rp*
Vertical n-well resistance < O - μm^2>	*Rn*
Cja ndiff <fF/ μm^2>	*Cja*
Cjp ndiff <fF/ μm^2>	*Cjp*

$$R\_SUB = \frac{1}{2} Rsub \tag{4.9}$$

$$R\_SUBC = \frac{Rp}{ksubc \cdot L^2} \tag{4.10}$$

where *ksubc* is a statistical constant representing the fraction of substrate contact area in a L x L square of layout, estimated from typical or previous designs.

$$R\_NWELL = \frac{Rn}{knwell \cdot L^2} \tag{4.11}$$

$$Cj\_NWELL = knwell \cdot L^2 \cdot Cja + 4 \cdot \sqrt{knwell \cdot L^2} \cdot Cjp \tag{4.12}$$

$$Cj\_NDIFF = kndiff \cdot L^2 \cdot Cja + 4 \cdot \sqrt{kndiff \cdot L^2} \cdot Cjp \tag{4.13}$$

where *knwell* and *kndiff* are statistical constants representing the fraction of n-well and respectively n-type diffusion areas in a L x L square of layout, estimated from typical or previous designs.

The size of the resulting netlist depends on the mesh granularity N. For higher granularities, the simulation may take a long time or may not be able to run at all. In these cases the granularity needs to be reduced. For chips having the analog region placed symmetrically on one side of the chip, a simplified one-dimensional distributed mesh can be used. In this case the result is a cross-sectional distribution of substrate noise in the analog region. The simplified model consists of a sequence of macro-cells, each representing the region centered on a column of chip pins, as shown in Figure 4.7. The choice of power or ground connection on each column may not represent the real chip, since power and ground pins typically alternate across the column, but it can be assumed to be a close approximation.

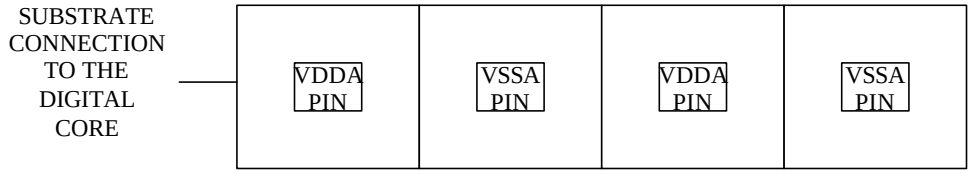


Figure 4.7: Simplified model consists of a sequence of macro-cells, each representing the region centered on a column of chip pins.

Each macro-cell is made out of *N* small-cells, as shown in Figure 4.8, where *N* is the granularity of the model.

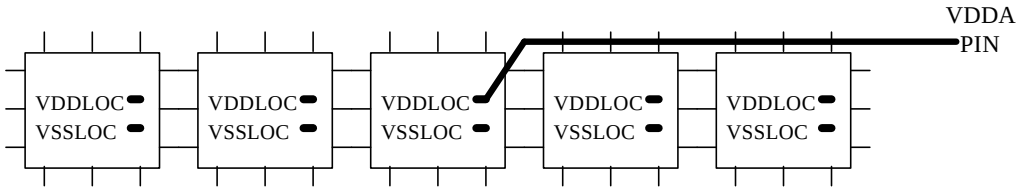


Figure 4.8: Schematic diagram of a macro-cell is made out of N small cells, each representing a vertical slice of the chip substrate and power distribution.

Each small-cell represents the model of a column having the width of a power grid cell, *L*, and the height equal to the height of the chip. The schematic of a small-cell is shown in Figure 4.9.

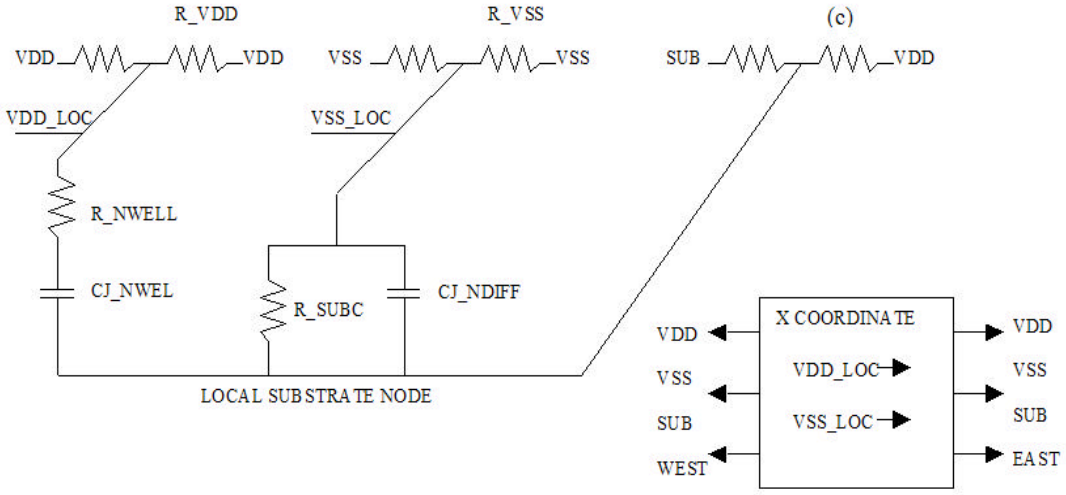


Figure 4.9: Schematic diagram of a small cell used in the simplified one-dimensional mesh model.

Similarly to the two-dimensional model, the parameters of this cell can be calculated from parameters available in the design manual and statistical data from previous designs using the following equations, where *H* is the height of the chip:

$$R\_VDD = \frac{1}{2} Rm \frac{L}{d} \cdot \frac{L}{H} \tag{4.14}$$

$$R\_VSS = \frac{1}{2} Rm \frac{L}{d} \cdot \frac{L}{H} \tag{4.15}$$

$$R\_SUB = \frac{1}{2} Rsub \cdot \frac{L}{H} \tag{4.16}$$

$$R\_SUBC = \frac{Rp}{ksubc \cdot L \cdot H} \tag{4.17}$$

where *ksubc* is a statistical constant representing the fraction of substrate contact area in a L x L square of layout

$$R\_NWELL = \frac{Rn}{knwell \cdot L \cdot H} \tag{4.18}$$

$$Cj\_NWELL = (knwell \cdot L^2 \cdot Cja + 4 \cdot \sqrt{knwell \cdot L^2} \cdot Cjp) \cdot \frac{H}{L} \tag{4.19}$$

$$Cj\_NDIFF = (kndiff \cdot L^2 \cdot Cja + 4 \cdot \sqrt{kndiff \cdot L^2} \cdot Cjp) \cdot \frac{H}{L} \tag{4.20}$$

where *knwell* and *kndiff* are statistical constants representing the fraction of n-well and respectively n-type diffusion areas in a L x L square of layout.

It can be noticed that for both two-dimensional and one-dimensional models all the components of the analog region mesh have been calculated using information typically available in early stages of the design process.

4.5.2 Digital Circuits, Package and PCB Power Distribution

For simplification it has been assumed that the digital power and ground noise couples into the substrate mainly through two mechanisms. First, digital ground noise couples into substrate through the total substrate contact resistance and the total n-diffusion capacitance, modeled by the parallel *RC* network (c) in Figure 4.1. Second, digital power noise couples into the substrate through the total n-well vertical resistance and the total junction capacitance modeled by the series *RC* network (d) in Figure 4.1. The resistor and capacitor of network (c) are calculated using the equations:

$$R\_SUBD = \frac{Rp}{ksubd \cdot X \cdot Y} \tag{4.21}$$

$$Cj\_NDIFFD = kndiffd \cdot X \cdot Y \cdot Cja + 4 \cdot \sqrt{kndiffd \cdot X \cdot Y} \cdot Cjp \tag{4.22}$$

where *ksubd* and *kndiffd* are statistical constants representing the fraction of substrate contact and n-diffusion areas in the digital region, estimated from typical or previous designs, and *X* and *Y* are the dimensions of the digital region.

The resistor and capacitor of network (d) are calculated using the equations:

$$R\_NWELLD = \frac{Rn}{knwelld \cdot X \cdot Y} \tag{4.23}$$

$$Cj\_NWELLD = knwelld \cdot X \cdot Y \cdot Cja + 4 \cdot \sqrt{knwelld \cdot X \cdot Y} \cdot Cjp \tag{4.24}$$

where *knwelld* is a statistical constant representing the fraction of n-well area in the digital region, estimated from typical or previous designs, and *X* and *Y* are the dimensions of the digital region. The resistor (e) is typically equal to zero, since it

represents the physical interface between the digital and analog substrate regions, but it can be set to higher values if high resistance guard rings are placed between the digital and analog regions.

The package parameters include the series resistance and inductance representing the interconnect to the chip, and the resistance and inductance associated to the interface to the PCB. These parameters are specific to each package and mounting technology, and are usually available in the package specification datasheet. For custom packages these parameters are usually available in the design specification documents. The models of the decoupling capacitors placed on chip and on PCB are found in the manufacturer data sheets.

4.5.3 Experimental Model

The experiment has been implemented on Test Chip 3, built in 0.13 µm IBM CMOS technology on a lightly doped substrate. Figure 4.10 shows a simplified diagram of the physical placement of sensors and digital noise emulators (DNEs).

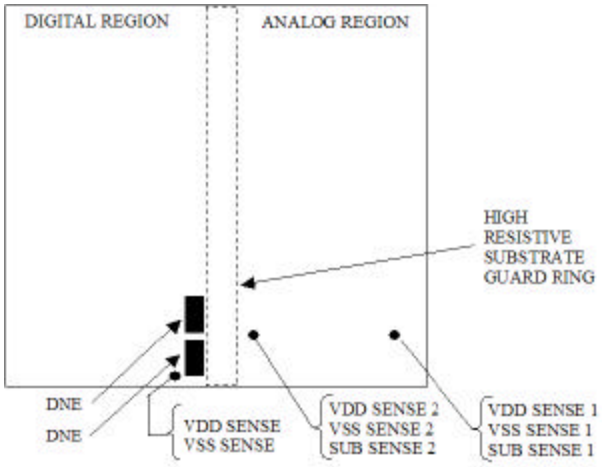


Figure 4.10: Simplified diagram of the physical placement of sensors and digital noise emulators (DNEs) in the noise coupling prediction experiment.

The digital noise emulators are placed in the digital side, which is separated from the analog side by a 100 μm wide high resistive substrate guard ring. Sense lines

connected to an external oscilloscope probe the power, ground and substrate. The test chip is 4200 *µm* wide and 4800 *µm* tall, and the analog region is 2000 *µm* wide. The power grid physical layout is shown in Figure 4.6, and has the dimensions 14.06 *µm* x 14.06 *µm*. The C4 pins are spaced 225 *µm* apart, and thus, 16 power grid cells fit in the space between two C4s. The mesh model is made of macro-cells centered on the C4 pin locations, each consisting of an array of 16 x 16 small-cells. The schematic of a small cell has been shown in Figure 4.5, and physically it represents the model of a square substrate and power grid region measuring 14.06 *µm* x 14.06 *µm*. The parameters of the model have been calculated following the procedure described in Section 4.5.1, and are shown in Table 4.3 for both the one and two-dimensional models.

Table 4.3: Parameters for the one and two dimensional mesh cell models.

Parameter	2D Values	1D Values
R_VDD	0.24 O	7 mO
R_VSS	0.24 O	7 mO
R_SUB	130 O	0.39 O
R_SUBC	70.3 O	0.2 O
R_NWELL	105.5 O	0.31 O
Cj_NWELL	25.5 fF	8.71 pF
Cj_NDIFF	5 fF	1.71 pF

The parameters of the digital core model, package, PCB, and interconnects have been calculated following the procedure described in Section 4.5.2. These values have been placed in the overall schematic diagram of the chip, package, and PCB model, shown in Figure 4.11.

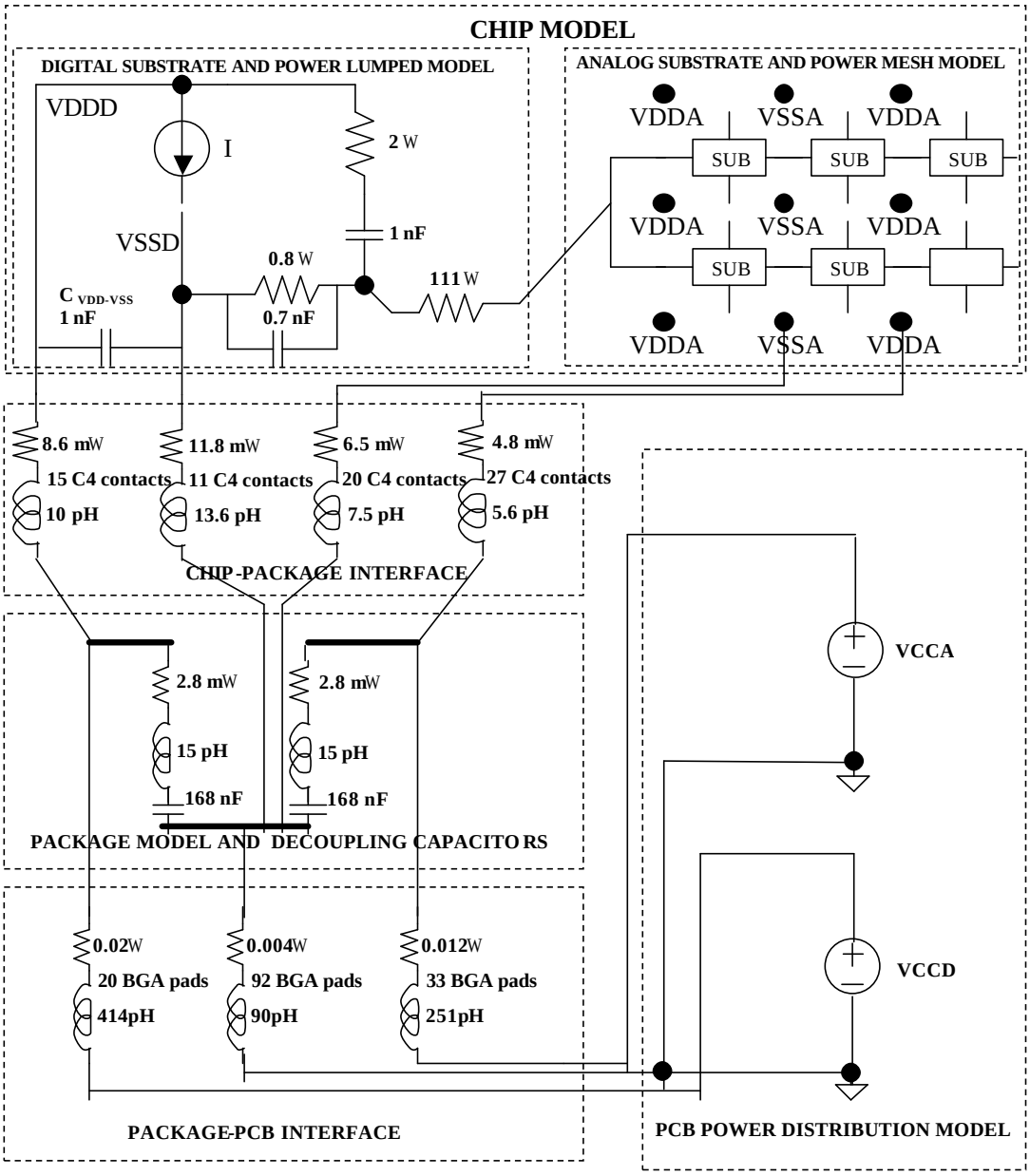


Figure 4.11: Schematic diagram of the chip, package, and PCB model, illustrating the component values for the digital core and the parasitic elements of the power distribution.

4.6. Noise Coupling Prediction Results

4.6.1. Measurement and Simulation of the Digital Switching Noise

The DNEs generate a square wave current pulse having 120 mA amplitude, 256 ns period, and about 1 ns rise time. The voltages on the digital power and ground are measured using sense lines connected to a Tektronix TDS8200 oscilloscope. Figure 4.12 shows the transient response of the digital and analog power and ground.

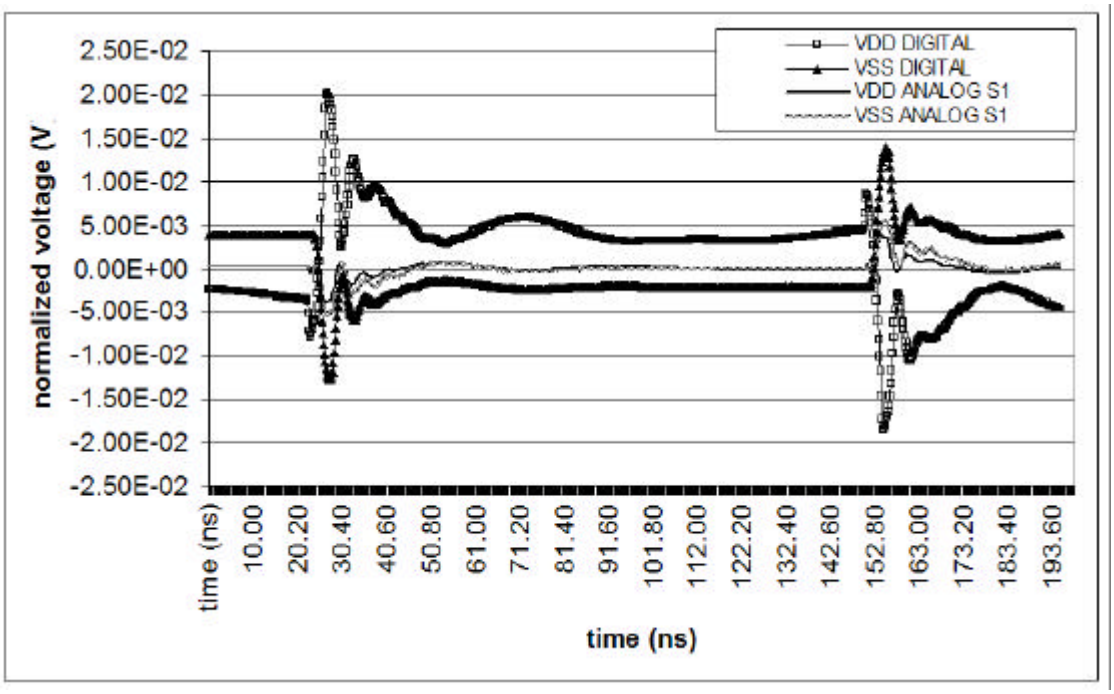


Figure 4.12: Voltage transient response at the digital and analog power and ground due to a 120 mA square wave current pulse signal injected in the digital supply.

A DC voltage drop of about 10 mV in the digital supply can be noticed when the 120 mA current is active, a high frequency ringing of about 3.5 ns period, and a low frequency ringing of about 40 ns period. The ringing on *VDD_DIGITAL* has opposite phase compared to the ringing on *VSS_DIGITAL*. The analog power and ground show the same ringing waveforms, having smaller amplitudes and the same phase as the ringing on the digital ground. This result suggests that the noise on digital ground

couples into the analog ground in the package through the shared ground impedance of the power distribution. *VSS_ANALOG* amplitude being higher than *VDD_ANALOG* amplitude suggests that the noise coupled into the analog ground couples from here into the digital ground through the decoupling capacitors. This is actually a function of the decoupling capacitors, but because of parasitic effects the *VDD_ANALOG* does not follow exactly the waveform on the *VSS_ANALOG*.

Simulation results on the model shown in Figure 4.11 confirm the experimental measurements. Figure 4.13 shows the simulated waveforms on the digital power (a), digital ground (b), package ground (c), analog ground (d), and analog power (e).

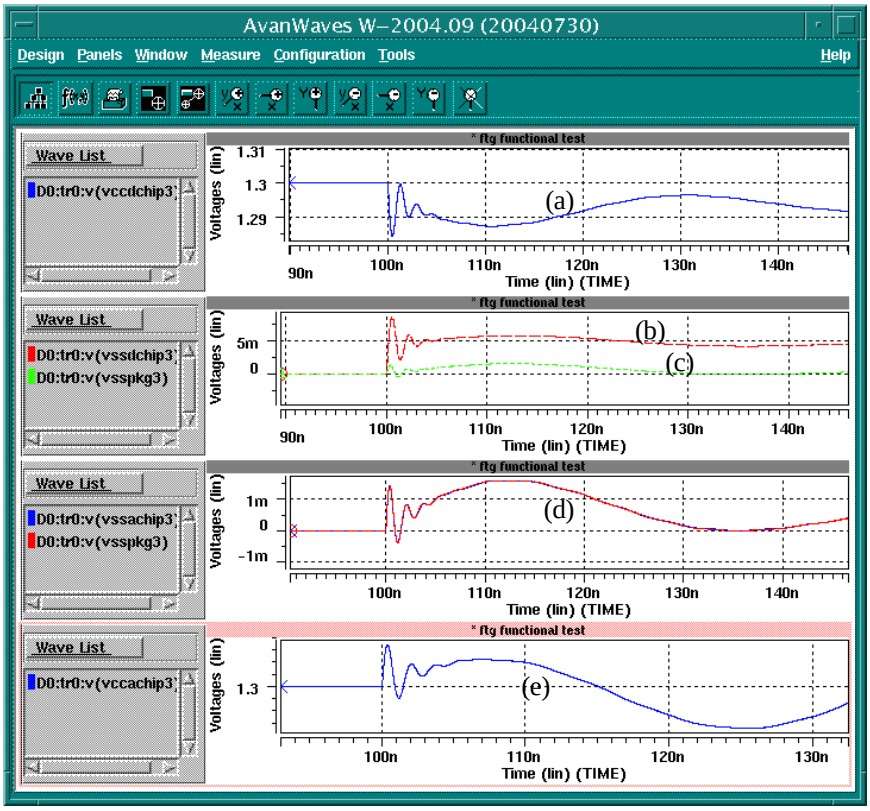


Figure 4.13 Simulated waveforms on the digital power (a), digital ground (b), package ground (c), analog ground (d), and analog power (e), illustrating the correlation with the measurement results.

Both high and low frequency ringing waveforms occur on the digital power and ground. The package and analog ground follow the digital ground, and the analog power follows the analog ground. The waveforms of the analog power and ground are

similar but not identical, differences being noticed especially in high frequency ringing. Because of this difference, the analog circuits, which are powered differentially between the analog VDD and VSS, are affected more by high frequency switching noise.

4.6.2. Measurement and Simulation of Noise Coupling into Analog Power, Ground, and Substrate

The DNE generates a square wave current pulse of amplitude 60 mA, with a period of 180 ns, and rise/fall times of about 1 ns. The coupled noise into the analog power, ground, and substrate lines is measured through sense lines with a Tektronix TDS8200 oscilloscope. Figure 4.14 shows the waveforms measured by sensors group 1 located about 1000 µm from the digital region.

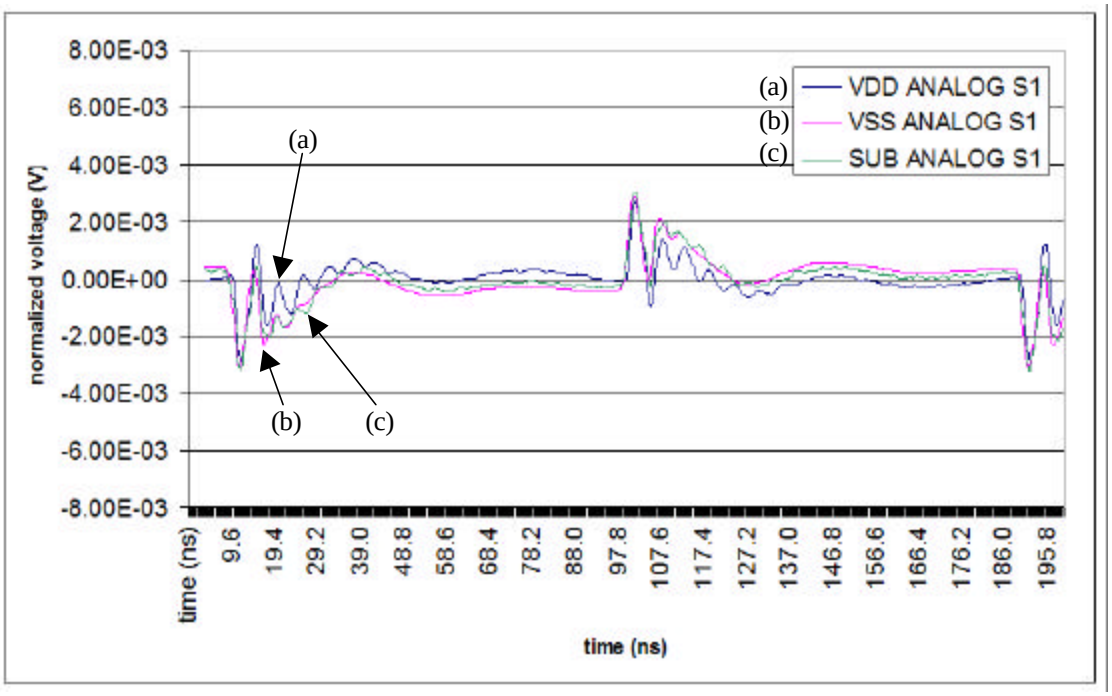


Figure 4.14: Analog power, ground, and substrate waveforms at group 1 of sensors.

It can be noticed the high and low frequency ringing, and the differences in waveforms especially right after the switching edges. Figure 4.15 shows the waveforms measured by sensors group 2, located 50 µm from the digital region.

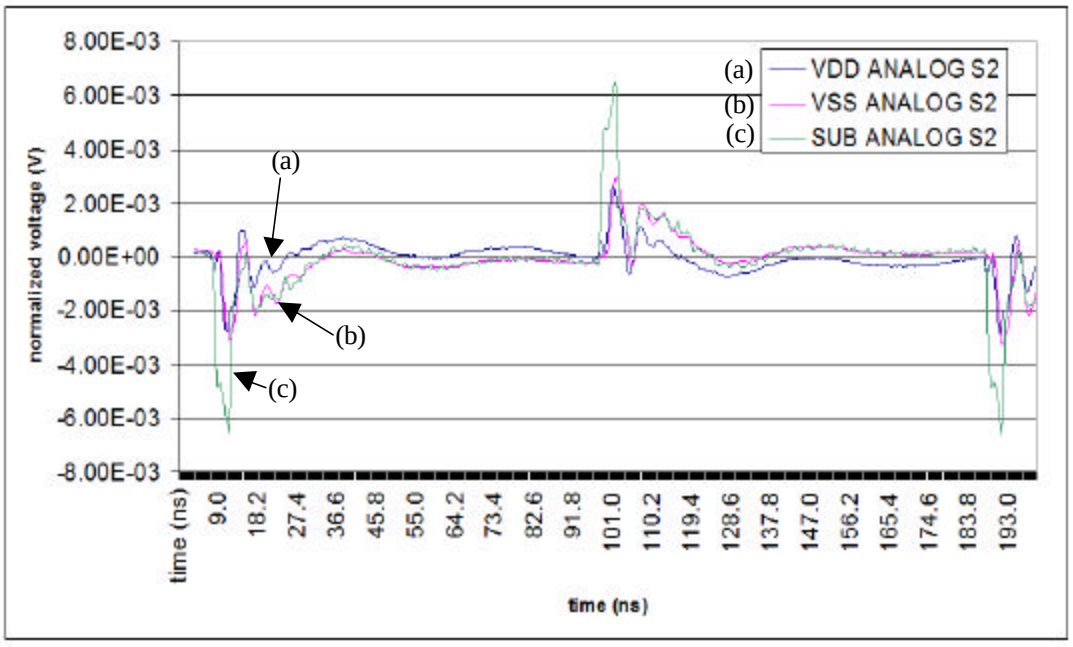


Figure 4.15: Analog power, ground, and substrate waveforms at group 2 of sensors, located 50 µm from the digital region.

It can be noticed the ringing is similar to the waveforms at 1000 µm distance, and a much higher amplitude of substrate overshoot is observed right at the transition edge. This overshoot is caused by digital noise coupling through the resistance of the substrate. After the overshoot, the substrate follows the *VSS* waveform, which suggests a delayed shunting of substrate to VSS through substrate contacts. The delay may be caused by parasitic inductance and resistance of the substrate contacts interconnect to the VSS power grid. The substrate waveform at 1000 µm does not have overshoot because the coupling has been attenuated by the long distance. For this group of sensors the differences between the voltages on ground, power, and substrate are generated mainly by the noise injected through the power and ground pins. The substrate receives noise from ground and power through the substrate contacts and n-well junction capacitance. This conclusion agrees with the results published in [11] and [12].

Hspice transient simulation results of the one-dimensional mesh model are shown in Figure 4.16, and a magnified image of the first transition edge in Figure 4.17.

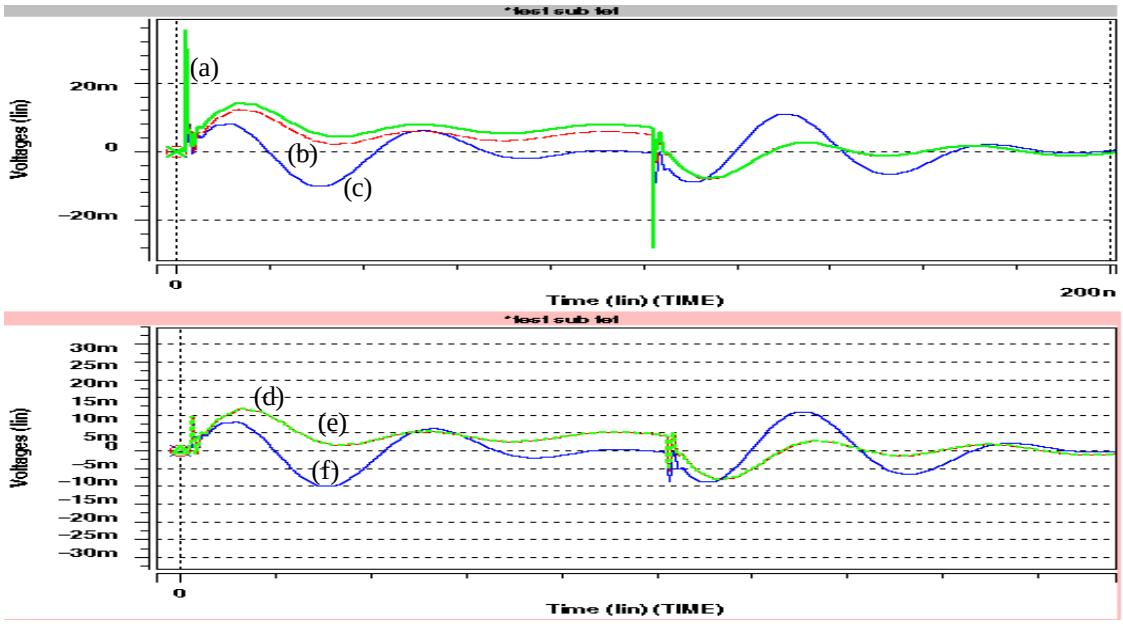


Figure 4.16: Analog power, ground, and substrate simulated transient waveforms using the one-dimensional mesh model.

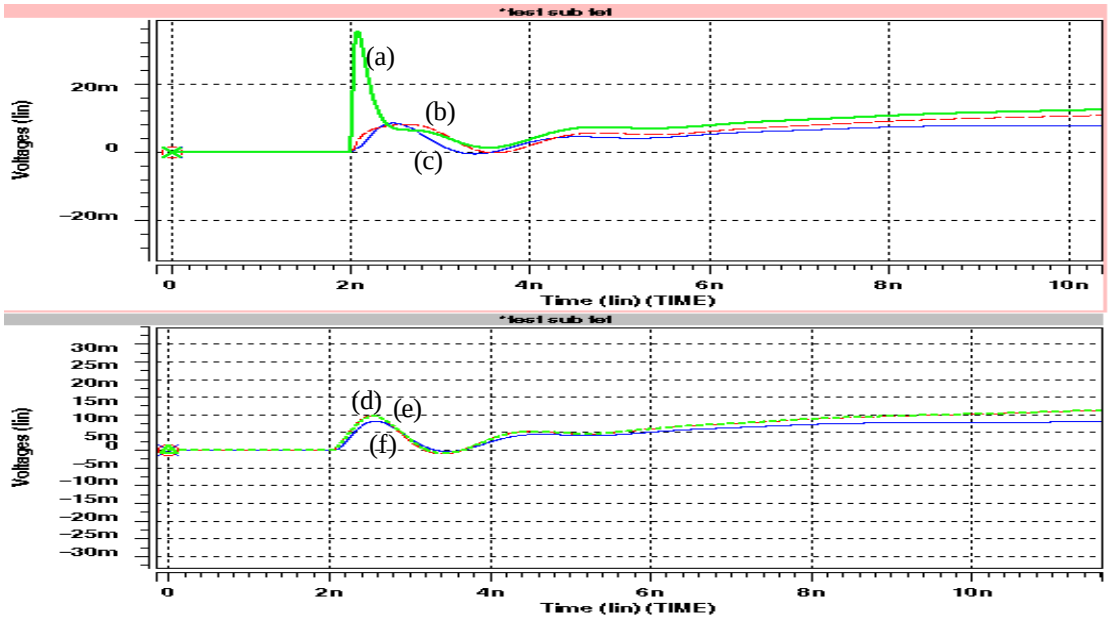


Figure 4.17: Magnified view of analog power, ground, and substrate simulated transient waveforms using the one-dimensional mesh model.

Waveforms (a), (b), and (c) show the substrate, ground, and power at 50 µm distance from the digital region, and waveforms (d), (e), and (f) show substrate, ground, and

power at 1000 μm distance. The high and low frequency ringing correlates with the measured waveforms. The substrate waveform at 50 μm distance first overshoots and then follows the ground, similar to the experimental measurements. The simulated amplitudes are higher than the measurements; however differences are expected considering the simplifying approximations made to develop this model. Since the main components of the measured waveforms are also present in the simulation results, it can be concluded that the one-dimensional model can be used to predict the noise coupling in early stages of the design process.

The two-dimensional mesh model was too large for transient simulations, and thus, it has been simulated only in frequency domain. Since correlation could not be established directly with the transient measurements, a correlation with the frequency analysis of the one-dimensional model has been performed. Figure 4.18 shows the results of 1 GHz ac Hspice simulations for the two-dimensional model, and the correlation with the ac simulations of the one-dimensional model. Figure 4.19 shows similar simulation results and correlation between the one and two-dimensional models at 10 GHz.

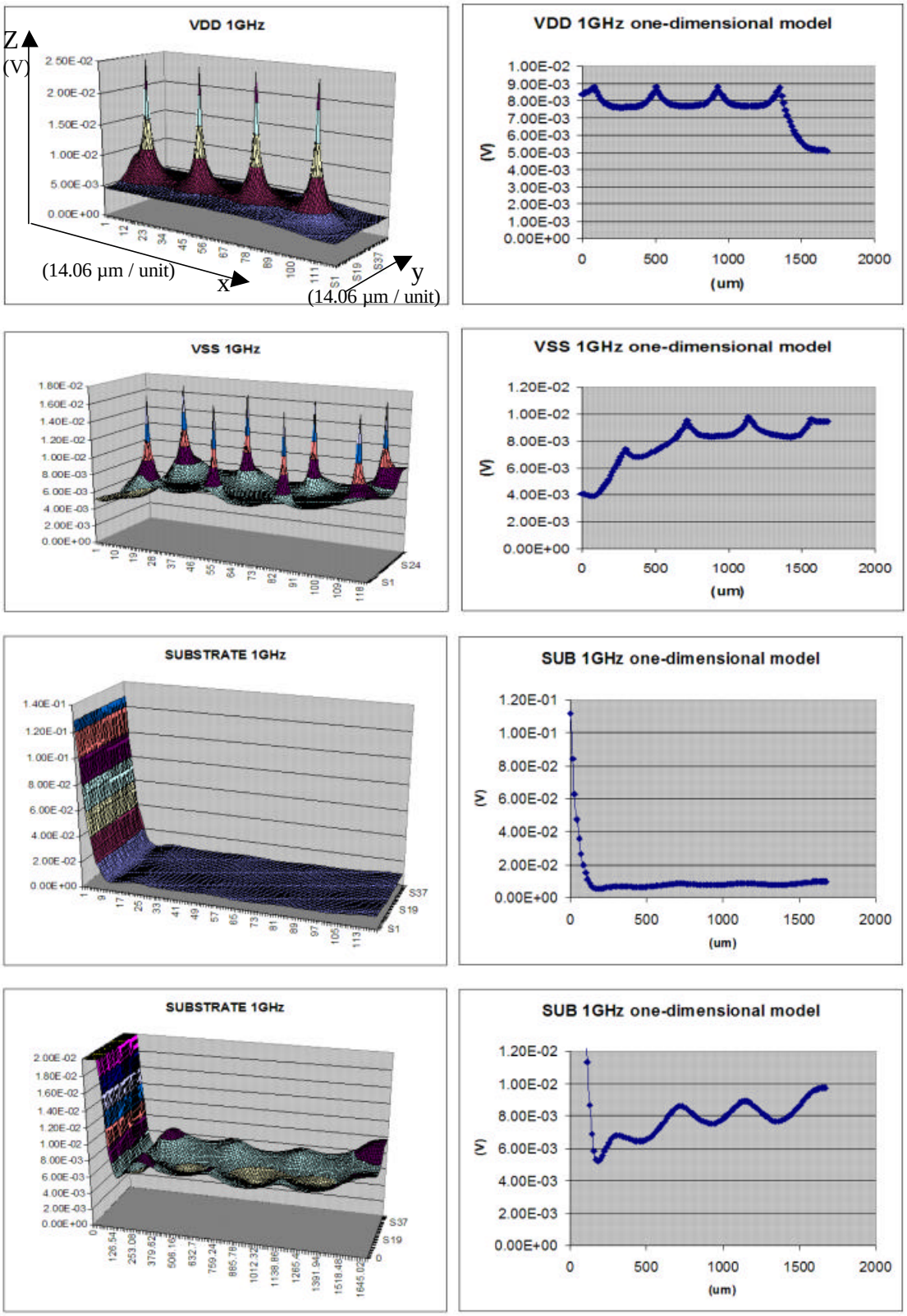


Figure 4.18: Correlation between the one and two-dimensional models at 1 GHz

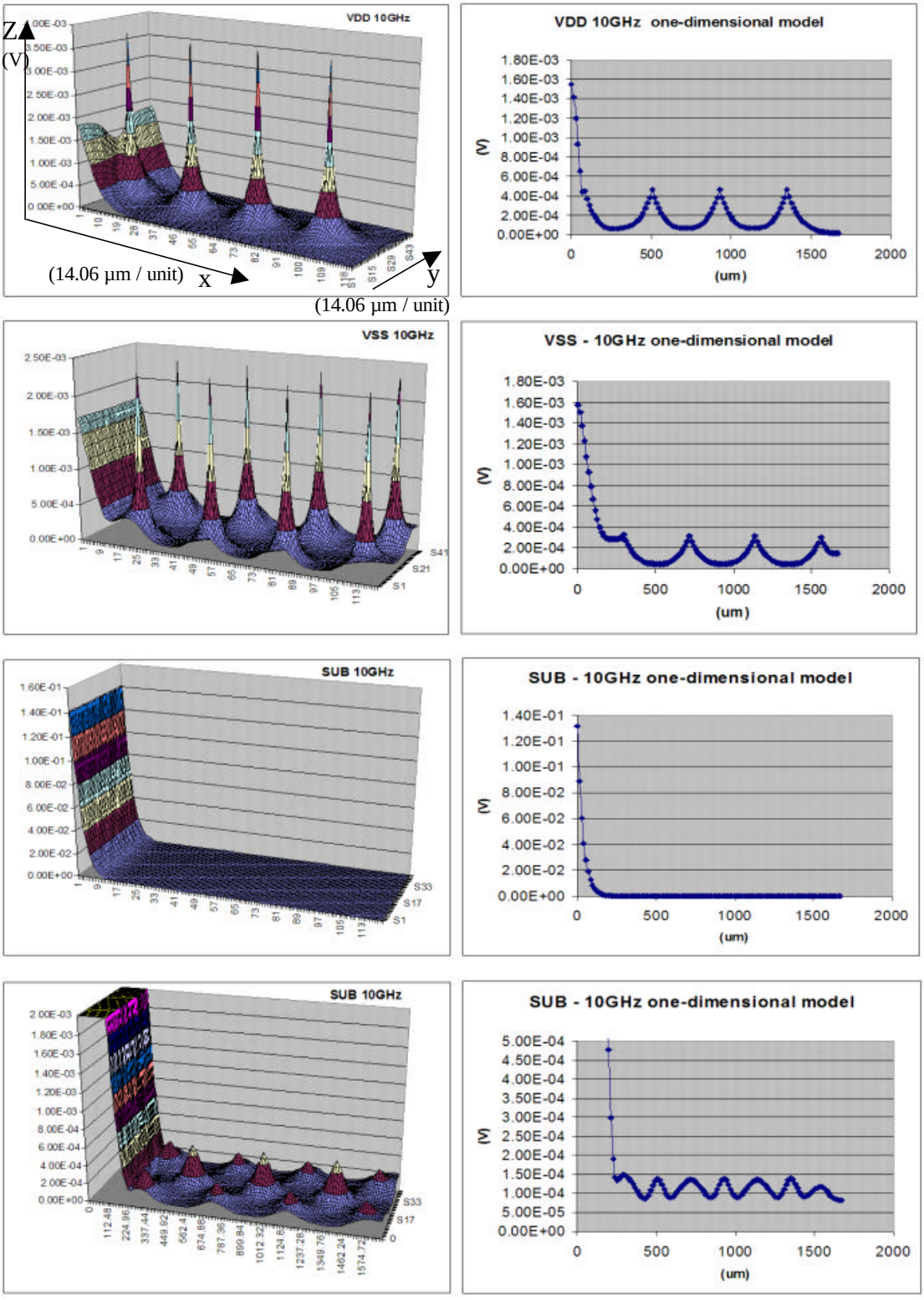


Figure 4.19: Correlation between the one and two-dimensional models at 10 GHz

The grid units on both horizontal axes represent 14.06 μm in the physical layout, and on the vertical axes Volts. The height of the simulated mesh covered seven C4 pins, out of which three where power or ground. The spikes correspond to the location of these power and ground pins. The left side of the surface corresponds to the physical interface between the analog and digital regions.

It can be noticed, in Figure 4.18 the amplitude correlation between the one and two-dimensional models at $x = 0$ for each *VDD*, *VSS*, and *SUB*. Correlation also exists in the amplitude variation along the x-axes, which represents the amplitude variation for increased distance from the digital region. Similar correlation can be noticed at 10 GHz.

The ac simulations show that there is a good correlation between the two-dimensional and the one-dimensional models. Since the one-dimensional model has been previously correlated in transient simulations with the measured data, it can be assumed that the two-dimensional model can be used to predict the noise coupling in the analog region. As it is seen in Figures 4.18 and 4.19, the two-dimensional prediction technique provides a surface potential map of the noise coupled into power, ground, and substrate at each location within the analog region of the chip.

4.7 Conclusion

This chapter has presented a hybrid lumped-distributed model that can be used to predict the substrate and power supply noise coupling in early stages of a design process. The development of the model is based only on information typically available in the architectural stages of design, when schematics, verilog code, and layout are not yet defined. The two-dimensional map of noise coupling in the analog region allows the analog design engineers to simulate the performance of critical circuits early in the design process. It also identifies the quiet regions for physical placement of sensitive circuits, and allows the evaluation of noise coupling suppression techniques such as guard rings, and power and ground pins assignment.

Chapter 5

Conclusions

Coupling of digital switching noise into analog circuits in SoC applications has become a tremendous challenge. Technology scaling has worsened the problem by increasing the complexity and speed of digital cores, which consequently generates more switching noise, and by reducing the voltage supply headroom of analog circuits, which makes them more sensitive to substrate and power supply noise. To overcome these issues, research effort in recent years has been invested in reducing the noise coupling effects on analog circuits. Work has focused on identifying the noise generation, propagation, and coupling mechanisms, developing accurate substrate and power supply noise measurement techniques, and modeling the noise coupling in various stages of the design process. This research work has focused on measurement, modeling, and suppression of noise coupling. This dissertation has presented improved substrate and power supply noise measurement techniques, active substrate noise cancellation circuit structures, and a noise coupling modeling technique for early prediction during the architectural stages of the design process. This chapter summarizes the results and contributions, and suggests directions for future work in this field.

5.1 Summary

Noise coupling measurement in mixed-signal SoC applications has been addressed in Chapter 2. The importance of measuring both substrate and power supply noise was emphasized since the analog circuits sense the combined effect. Also mentioned was the importance to not affect the noise propagation or inject additional noise into substrate or power supply. A set of requirements for making accurate measurements

in complex SoCs has been created, and a comparison of published work referred to these requirements has been performed. Driven by these requirements, a proposed measurement technique using compact sensors and an on-chip digitizing sampler has been presented. The sensors have been designed to minimally affect the noise coupling, and not to inject additional noise in the substrate or power supply. Resistive coupling to substrate and power supply lines allows the measurement of very low frequency and DC components. The on-chip waveform digitizing reduces the bandwidth limitation and signal contamination due to off-chip routing, and eliminates additional analog output pins. Experimental evaluation of this technique in a 0.13 µm CMOS test chip showed the bandwidth coverage from DC to 1.6 GHz for both substrate and power supply sensors. The overall performance evaluation has proved that the sensors and the on-chip waveform recorder can measure successfully the substrate and power supply noise in complex SoC applications.

Chapter 3 covered techniques of noise coupling suppression in mixed-signal SoCs. Previous published methods of reducing noise generation, propagation, and reception by analog circuits have been discussed. It has been emphasized that while these methods help reduce noise coupling they don't completely solve the problem. For example the isolation using guard rings reduces the coupling, but substrate noise still exists and varies with physical location inside guard rings. To reduce even more the noise coupling effects, this research work proposed three active cancellation structures that can be used in addition to conventional guard ring methods. The first technique addresses the common-source NMOS amplifier stage, and senses the substrate noise through a source-follower PMOS transistor, which generates a noise cancellation current. The second technique is a derivation of the first one for active loads made of a current source and a diode-connected transistor. The third technique addresses the NMOS in common-source configuration with degeneration, and uses a negative feedback loop to cancel out the substrate noise effect. The experimental implementations of these techniques in a 0.13 µm CMOS test chip have been evaluated.

Chapter 4 discussed the noise coupling modeling and prediction in SoCs, and the application coverage to various stages of the design process. It has been mentioned the correlation between modeling accuracy and the stage of design where the methods can be applied. Also, it has been emphasized that the most accurate methods use the complete layout which is available only late in the design process, and the problems found at this stage often require major rework that significantly impacts cost and schedule. Driven by the desire to predict the noise coupling problems early in the design process, this work has proposed a novel hybrid lumped-distributed model of the chip substrate and power distribution, which has been integrated in a macro-model of the chip, package, and PCB. The model construction procedure, and experimental validation through test chip measurements and simulations have been presented. Despite the fact that the accuracy is lower than techniques using physical layout information, or schematics and behavior models, this technique can be used to predict major noise coupling issues during the architectural stage of the design process.

5.2 Recommendations for Future Work

While novel techniques for measurement, suppression, and prediction of substrate and power supply noise have been developed, there are some issues outside the scope of this research work that may be of interest for future investigation.

First, the work presented in this dissertation has covered only the CMOS on lightly-doped bulk substrate technology, and only BGA packages. While successful results have been presented for this technology, it would be interesting to evaluate the proposed techniques on heavily doped substrate with lightly doped epitaxial layer, silicon-on-insulator (SOI), and triple-well option. The evaluation of other types of packages, may also be of interest of future investigation. The particularities of these technologies may redefine the noise coupling mechanisms, and thus may drive adjustments to the prediction and suppression techniques.

Second, this research work focused primarily on the effect on noise coupling on NMOS transistors, but other components, like PMOS transistors, diffused resistors,

and capacitors are also affected by noise coupling. By similarity, part of the results can be extrapolated to PMOS. It may be in the interest of future work to adjust and validate the proposed techniques for these components.

Third, this dissertation presented a coupling prediction technique for the architectural stage of the design process. This technique expands the coverage of previous published modeling methods, but does not solve the entire modeling problem. Because decisions that affect noise coupling are taken at various stages in the design process, it is desirable to model the noise coupling at each of these stages. While this can be achieved by using previous published and commercial modeling techniques, which each focus on different stages of design, it would be more beneficial to integrate a set of techniques that cover all design stages in a single tool. This way the noise coupling modeling and prediction can be performed in an automatic mode during the entire design process.

Bibliography

[1] G. E. Moore, “Progress in digital integrated electronics,” *International Electron Devices Meeting 1975*, Volume 21, Pages: 11 – 13, 1975

[2] International Technology Roadmap for Semiconductors, ITRS, web site: http://www.itrs.net

[3] R. Singh and S. Sali, “Modeling of electromagnetically coupled substrate noise in FLASH A/D converters,” IEEE Transactions on Electromagnetic Compatibility, Volume 45, Issue 2, Pages: 459 – 468, May 2003

[4] Z. Zhangming and Y. Yintang, “Characterization of substrate noise coupling in high speed CMOS current-steering D/A converter,” *Proceedings of 2005 IEEE International VLSI Workshop on Design and Video Technology, 2005*, Pages :48 – 51, 28-30 May 2005

[5] P. Heydari, "Analysis of the PLL jitter due to power/ground and substrate noise," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Volume 51, Issue 12, Pages: 2404 – 2416, Dec. 2004

[6] N. Checka, D. D. Wentzloff, A. Chandrakasan and R. Reif, "The effect of substrate noise on VCO performance," *IEEE Radio Frequency integrated Circuits (RFIC) Symposium, 2005*, Pages :523 – 526, June 12-14, 2005

[7] C. Soens, G. Van der Plas, P. Wambacq and S. Donnay, "Performance degradation of an LC-tank VCO by impact of digital switching noise," *Proceeding of the 30th European Solid-State Circuits Conference, 2004. ESSCIRC 2004*, Pages:119 – 122, Sept. 21-23, 2004

[8] Xu Min, D. K. Su, D. K. Shaeffer, T. H. Lee and B. A. Wooley, "Measuring and modeling the effects of substrate noise on the LNA for a CMOS GPS receiver," *IEEE Journal of Solid-State Circuits*, Volume 36, Issue 3, Pages: 473 – 485, March 2001

[9] H. Lan and R. Dutton, "Synthesized compact models (SCM) of substrate noise coupling analysis and synthesis in mixed-signal Ics," *Proceedings of the Design, Automation and Test in Europe Conference and Exhibition*, Volume: 2 , Pages:836 - 841, 16-20 Feb. 2004.

[10] T. Blalack, J. Lau, F.J.R. Clement and B.A. Wooley, "Experimental results and modeling of noise coupling in a lightly doped substrate," *Electron Devices Meeting*, Pages:623 – 626, 8-11 Dec. 1996.

[11] X. Aragones and A. Rubio, “Experimental comparison of substrate noise coupling using different wafer types,” *IEEE Journal of Solid-State Circuits*, Volume: 34 , Issue: 10 , Pages:1405 – 1409, Oct. 1999.

[12] M. Nagata, Y. Kashima, D. Tamura, T. Morie and A. Iwata, “Measurements and analyses of substrate noise waveform in mixed signal IC environment,” *Proceedings of the IEEE Custom Integrated Circuits*, Pages:575 – 578, 16-19 May 1999.

[13] K. Makie-Fukuda, T. Anbo, T. Tsukada, T. Matsuura and M. Hotta, “Voltage-comparator-based measurement of equivalently sampled substrate noise waveforms in mixed-signal integrated circuits,” *IEEE Journal of Solid-State Circuits*, Volume: 31 , Issue: 5 , Pages:726 – 731, May 1996.

[14] Xu Weize and E.G. Friedman, “A substrate noise circuit for accurately testing mixed-signal ICs,” *Proceedings of the IEEE International Symposium on Circuits and Systems*, 2002, Volume: 1 , Pages:I-145 - I-148, 26-29 May 2002.

[15] M. Nagata and A. Iwata, “Substrate crosstalk analysis in mixed signal CMOS integrated circuits,” *Proceedings of the Design Automation Conference Asia and South Pacific* , Pages:623 – 629, 25-28 Jan. 2000.

[16] B.E. Owens, S. Adluri, P. Birrer, R. Shreeve, S.K. Arunachalam, K. Mayaram and T.S. Fiez, “Simulation and Measurement of Supply and Substrate Noise in Mixed-Signal Ics,” *IEEE Journal of Solid-State Circuits*, Volume: 40 , Issue: 2 , Pages:382 – 391, Feb. 2005.

[17] M. Van Heijningen, J. Caomiet, P. Wambacq, S. Donnay and I. Bolsens, “A design experiment for measurement of the spectral content of substrate noise in mixed-signal integrated circuits,” *Southwest Symposium on Mixed-Signal Design*,

Pages:27 – 32, 11-13 April 1999.

[18] M. Van Heijningen, M. Badaroglu, S. Donnay, M. Engels and I. Bolsens, "High-level simulation of substrate noise generation including power supply noise coupling," *Proceedings of the Design Automation Conference*, Pages:446 – 451, June 5-9, 2000.

[19] N. Barton, D. Ozis, T. Fiez and K. Mayaram, "The effect of supply and substrate noise on jitter in ring oscillators," *Proceedings of the IEEE Custom Integrated Circuits Conference*, Pages:505 – 508, 12-15 May 2002.

[20] S.P. Debnath, J. Sukumar and H. Udaykumar, "A Methodology for Fast Vector Based Power Supply and Substrate Noise Analyses," *Proceedings of the 18th International Conference on VLSI Design*, Pages:808 – 811, 03-07 Jan. 2005.

[21] J. Briaire and S. Krisch, "Principles of substrate crosstalk generation in CMOS circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Volume 19, Issue 6, Pages: 645 – 653 June 2000.

[22] C. Andrei, O. Valorge, F. Calmon, J. Verdier and C. Gontrand, "Impact of substrate perturbation on a 5 GHz VCO spectrum," *Proceedings of the 16th International Conference on Microelectronics*, Pages: 684 – 687, 6-8 Dec. 2004.

[23] M. A. Mendez, D. Mateo, X. Aragones and J. L. Gonzalez, "Phase noise degradation of LC-tank VCOs due to substrate noise and package coupling," *Proceedings of the 31st European Solid-State Circuits Conference*, Pages: 105 – 108, 12-16 Sept. 2005.

[24] C. Soens, G. Van der Plas, P. Wambacq, S. Donnay and M. Kuijk, "Performance degradation of LC-tank VCOs by impact of digital switching noise in lightly doped

substrates," *IEEE Journal of Solid-State Circuits*, Volume 40, Issue 7, Pages: 1472 – 1481, July 2005.

[25] F. Herzel and B. Razavi, "A study of oscillator jitter due to supply and substrate noise," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, Volume 46, Issue 1, Pages: 56 – 62, Jan. 1999.

[26] V. Venkatesan, Q. Nguyen, A. Bose and P. Parris, "DC substrate coupling between LDMOS and CMOS devices in Hyperintegration I technology," *Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting*, Pages: 57 – 60, 27-29 Sept. 1998.

[27] L. Deferm, S. Decoutere, C. Claeys and G. Declerck, "Latch-up in a BiCMOS technology," *Proceedings of the International Electron Devices Meeting*, Pages: 130 – 133, 11-14 Dec. 1988.

[28] A. Hermann, M. Olbrich and E. Barke, "Placing substrate contacts into mixed-signal circuits controlling circuit performance," *Proceedings of the IEEE Custom Integrated Circuits Conference*, Pages :373 – 376, 21-24 Sept. 2003.

[29] R. M. Secareanu, S. Warner, S. Seabridge, C. Burke, T. E. Watrobski, C. Morton, W. Staub, T. Tellier and E. G. Friedman, "Placement of substrate contacts to alleviate substrate noise in epi and non-epi technologies," *Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems*, Volume 3, Pages: 1314 - 1318, 8-11 Aug. 2000.

[30] L. Varga, "Electronic circuit analogue model for CMOS devices," *Proceedings of the 6th European Conference on Radiation and Its Effects on Components and Systems*, Pages: 266 - 268 , 10-14 Sept. 2001.

[31] T. Aoki, “A new latch-up test structure for practical design methodology for internal circuits in the standard cell-based CMOS/BiCMOS LSIs,” *Proceedings of the International Conference on Microelectronic Test Structures,* Pages: 18 – 23, 16-19 March 1992.

[32] S. Ardalan and M. Sachdev, “An overview of substrate noise reduction techniques,” *Proceedings 5th International Symposium on Quality Electronic Design*, pp. 291 - 296, 2004

[33] M. Badaroglu, P. Wambacq, G. Van der Plas, S. Donnay, G. Gielen and H. De Man, “Digital ground bounce reduction by phase modulation of the clock,” *Proceedings Design, Automation and Test in Europe Conference and Exhibition*, vol 1, pp. 88 – 93, Feb. 2004

[34] C. Hwan-Mei, W. Ming-Hwei, B.C. Liau, L. Chang and W. Ching-Fu, “The study of substrate noise and noise-rejection-efficiency of guard-ring in monolithic integrated circuits,*” IEEE International Symposium on Electromagnetic Compatibility*, vol.1, pp. 123 – 128, Aug. 2000

[35] L. Forbes, W.T. Lim and K.T. Yan, “Guard ring diodes for suppression of substrate noise and improved reliability in mixed-mode CMOS circuits,” *Proceedings of the 5th International Symposium on the Physical and Failure Analysis of Integrated Circuits*, pp. 145 – 148, Dec. 1995

[36] N.R. Agung, S. Takagi and N. Fujii, “Improving the immunity to substrate noise using active noise cancellation circuit in mixed-signal integrated circuits,” *Asia-Pacific Conference on Circuits and Systems*, vol. 1, pp. 135 – 140, Oct. 2002

[37] W. Winkler and F. Herzel, "Active substrate noise suppression in mixed-signal circuits using on-chip driven guard rings," *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 357 – 360, May 2000

[38] K. Makie-Fukuda and T. Tsukada, "On-chip active guard band filters to suppress substrate-coupling noise in analog and digital mixed-signal integrated circuits," *Symposium on VLSI Circuits, Digest of Technical Papers*, pp. 57 – 60, June 1999

[39] H.H.Y. Chan and Z. Zilic, "Substrate coupled noise reduction and active noise suppression circuits for mixed-signal system-on-a-chip designs," *Proceedings of the 44th IEEE Midwest Symposium on Circuits and Systems*, vol.1, pp. 154 – 157, Aug. 2001

[40] F. Herzel and B. Razavi, "A study of oscillator jitter due to supply and substrate noise," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, pp. 56 – 62, Jan. 1999

[41] B. Razavi, "Design of Analog CMOS Integrated Circuits," McGraw-Hill, 2001, pp. 124-125.

[42] B. Razavi, "Design of Analog CMOS Integrated Circuits," McGraw-Hill, 2001, pp. 21-27 and 33-35.

[43] B. Razavi, "Design of Analog CMOS Integrated Circuits," McGraw-Hill, 2001, pp. 296-297.

[44] G. Blakiewicz and M. Chrzanowska-Jeske, " Modeling of substrate noise block properties for early prediction," *IEEE International Symposium on Circuits and Systems*, 2005. ISCAS 2005, Vol. 3, Pages:3015 – 3018, May 2005

[45] L. Elvira, F. Martorell, X. Aragones and L. Gonzalez, “A macromodelling methodology for efficient high-level simulation of substrate noise generation,” *Design, Automation and Test in Europe Conference and Exhibition*, Volume 2, Pages:1362 – 1363, 16-20 Feb. 2004

[46] J. Lundgren, T. Ytterdal, P. Eriksson, B. Oelmann, M. Abdalla and M. O'Nils, “A power-line noise coupling estimation methodology for architectural exploration of mixed-signal systems,” *Southwest Symposium on Mixed-Signal Design, 2003*, Page(s):133 – 137, 23-25 Feb. 2003

[47] A. Nardi, J. L. Haibo Zeng; Garrett, L. Daniel and A. L. Sangiovanni-Vincentelli, “A methodology for the computation of an upper bound on noise current spectrum of CMOS switching activity,” *International Conference on Computer Aided Design, 2003*, Pages:778 – 785, 9-13 Nov. 2003

[48] R. Zhe Wang; Murgai and J. Roychowdhury, “ADAMIN: automated, accurate macromodeling of digital aggressors for power and ground supply noise prediction,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Volume 24, Issue 1, Pages:56 – 64, Jan. 2005

[49] M. Badaroglu, G. Van der Plas, P. Wambacq, L. Balasubramanian, K. Tiri, I. Verbauwhede, S. Donnay, G. G. E. Gielen and H. J. De Man, “Digital circuit capacitance and switching analysis for ground bounce in ICs with a high-ohmic substrate,” *IEEE Journal of Solid-State Circuits*, Volume 39, Issue 7, Pages:1119 – 1130, July 2004

[50] J. M. Casalta, X. Aragones and A. Rubio, “Substrate coupling evaluation in BiCMOS technology,” *IEEE Journal of Solid-State Circuits*, Volume 32, Issue 4, Pages: 598 – 603, April 1997

[51] D. L. Cheng, D. C. Kwang-Ting Cheng; Wang and M. Marek-Sadowska, "A hybrid methodology for switching activities estimation," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Volume 17, Issue 4, Pages:357 – 366, April 1998

[52] N. Checka, A. Chandrakasan and R. Reif, "Substrate noise analysis and experimental verification for the efficient noise prediction of a digital PLL," *Proceedings of the IEEE Custom Integrated Circuits Conference*, 2005, Pages:473 – 476, 18-21 Sept. 2005

[53] A. Sharma, P. Birrer, S. K. Arunachalam, Chenggang Xu; T. S. Fiez and K. Mayaram, "Accurate Prediction of Substrate Parasitics in Heavily Doped CMOS Processes Using a Calibrated Boundary Element Solver," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Volume 13, Issue 7, Pages:843 – 851, July 2005

[54] S. Kristiansson, F. Ingvarson, S. P. Kagganti, N. Simic, M. Zgrda and K. O. Jeppson, "A surface potential model for predicting substrate noise coupling in integrated circuits," *IEEE Journal of Solid-State Circuits*, Volume 40, Issue 9, Pages:1797 – 1803, Sept. 2005

[55] X. Aragones, J. L. Gonzalez, F. Moll and A. Rubio, "Noise generation and coupling mechanisms in deep-submicron ICs," *IEEE Design & Test of Computers*, Volume 19, Issue 5, Pages:27 – 35, Sept.-Oct. 2002

[56] G. Van der Plas, M. Badaroglu, G. Vandersteen, P. Dobrovoiny, P. Wambacq, S. Donnay, G. Gielen and H. De Man, "High-level simulation of substrate noise in high-ohmic substrates with interconnect and supply effects," *Proceedings of the 41st Design Automation Conference, 2004*, Pages:854 – 859, 2004

[57] Hai Lan, Zhiping Yu and R. W. Dutton, "A CAD-oriented modeling approach of frequency-dependent behavior of substrate noise coupling for mixed-signal IC design," *Proceedings of the Fourth International Symposium on Quality Electronic Design, 2003*,
Pages:195 – 200, 24-26 March 2003

[58] A. Koukab, C. Dehollain and M. Declercq, "HSpeedEx: a high-speed extractor for substrate noise analysis in complex mixed-signal SOC," *Proceedings of the 39th Design Automation Conference, 2002*, Pages:767 – 770, 10-14 June 2002

[59] P. Birrer, T. S. Fiez and K. Mayaram, "Silencer!: a tool for substrate noise coupling analysis," *Proceedings of the IEEE International SOC Conference, 2004*, Pages:105 – 108, 12-15 Sept. 2004

[60] T. Brandtner and R. Weigel, "Hierarchical simulation of substrate coupling in mixed-signal ICs considering the power supply network," *Proceedings of the Design, Automation and Test in Europe Conference and Exhibition, 2002*, Pages:1028 – 1032, 4-8 March 2002

[61] Chenggang Xu; T. Fiez and K. Mayaram, "An improved Z-parameter macro model for substrate noise coupling," *Proceedings of the 2004 International Symposium on Circuits and Systems ISCAS 2004*, Volume 5, Pages:V-161 - V-164, 23-26 May 2004

[62] G. Veronis, Yi-Chang Lu and R. W. Dutton, "Modeling of wave behavior of substrate noise coupling for mixed-signal IC design," *Proceedings of the 5th International Symposium on Quality Electronic Design, 2004*, Pages:303 – 308, 2004

[63] Y. Murasaka, M. Nagata, T. Ohmoto, T. Morie and A. Iwata, "Chip-level substrate noise analysis with network reduction by fundamental matrix computation," *Proceedings of the International Symposium on Quality Electronic Design, 2001*, Pages:482 – 487, 26-28 March 2001

[64] M. van Heijningen, M. Badaroglu, S. Donnay, G. G. E. Gielen and H. J. De Man, "Substrate noise generation in complex digital systems: efficient modeling and simulation methodology and experimental verification," *IEEE Journal of Solid-State Circuits*, Volume 37, Issue 8, Pages:1065 – 1072, Aug. 2002

[65] S. Mitra, R. A. Rutenbar, L. R. Carley and D. J. Allstot, "A methodology for rapid estimation of substrate-coupled switching noise," *Proceedings of the IEEE Custom Integrated Circuits Conference, 1995*, Pages:129 – 132, 1-4 May 1995

[66] H. W. Johnson and M. Graham, "High-Speed Digital Design," *PTR Prentice Hall*, 1993, ISBN: 0133957241, Pages: 8-9