HIGH FREQUENCY NOISE IN CMOS LOW NOISE AMPLIFIERS

A DISSERTATION
SUBMITTED TO THE DEPARTMENT OF
ELECTRICAL ENGINEERING
AND THE COMMITTEE ON GRADUATE STUDIES OF
STANFORD UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

Jung-Suk Goo

August 2001

© Copyright by Jung-Suk Goo 2001

All Rights Reserved

I certify that I have read this dissertation and that in my opinion it is fully adequate, in scope and in quality, as a dissertation for the degree of Doctor of Philosophy.

Robert W. Dutton
(Principal Advisor)

I certify that I have read this dissertation and that in my opinion it is fully adequate, in scope and in quality, as a dissertation for the degree of Doctor of Philosophy.

Thomas H. Lee
(Associate Advisor)

I certify that I have read this dissertation and that in my opinion it is fully adequate, in scope and in quality, as a dissertation for the degree of Doctor of Philosophy.

Zhiping Yu

Approved for the University Committee on Graduate Studies:

Abstract

THE IMPORTANCE OF CMOS TECHNOLOGY is increasing in RF design applications owing to the promise of integrating electronic systems on a single silicon chip. While complete broad band characterization and accurate modeling of the MOSFET noise are critical requirements for circuit designs, the noise behavior and physics in short channel MOSFETs is not well understood. This dissertation explores the physical origin and contributing mechanisms of noise in MOSFETs, as well as a design methodology to minimize the impact of noise on fully integrated LNAs.

Investigating the physical noise sources in the MOSFET imposes significant computational requirements, due to the multi-dimensional nature of the device. In addition, higher order transport models need to be considered due to aggressive channel-length scaling. This dissertation presents a quasi two-dimensional noise simulation technique which provides an accurate and fast solution for MOSFET noise analysis by combining a 1-D active transmission line model with rigorous 2-D device simulation.

The physical origin of the excess noise in short channel MOSFETs has been identified. Source-side contributions dominate drain current noise; non-local transport behavior causes higher local ac resistance near the source junction and in turn generates extra noise contributions which are amplified by the channel transconductance. This phenomenon is directly reflected in excess values and a strong gate length dependence of γ and δ in scaled submicron MOSFETs. Higher order transport models are essential to capture this effect in

noise simulation.

Contrary to the common assumption that drain current exhibits only $1/f$ and white channel thermal noise contributions, this study demonstrates that the substrate generates thermal fluctuations that produce additive channel noise, amplified by the substrate transconductance. This component produces another plateau and frequency dependence in the noise spectrum of the drain current. Moreover, the effect tends to exaggerate the drain noise factor at low frequencies.

The high frequency noise modeling for MOSFET devices generally requires at least three parameters. This study demonstrates that while other two-parameter approaches, such as developed by Pospieszalski and those used in BSIM4 model, lead to errors, the results do not cause noticeable discrepancies for most practical circuit topologies. The modeling approach used in BSIM4 has been independently validated and is shown to be sufficient in capturing the physical origin of the excess noise.

Explicit guidelines for LNA design have been presented based directly on measured noise parameters and two-port noise theory; the approach requires neither sophisticated noise modeling nor circuit simulation. An 800MHz LNA test chip has been designed based on the proposed methodology. With 3.75mA of bias current, the LNA achieves about 0.9dB of noise figure, which adds just 0.3dB to the NF_{min} of the intrinsic MOSFET device. It is competitive with that of GaAs and bipolar LNAs and also quite close to the values predicted using the analysis presented in this work.

Acknowledgments

I WOULD like to thank many people who made my life at Stanford memorable and enjoyable. First and foremost, I wish to acknowledge my advisor, Professor Robert W. Dutton. He has been a great research mentor with his management skills and enthusiasm. He also has been an exceptional role model of a senior of life. He has done his utmost to help with every concern that his advisees have. I cannot forget how he encouraged and supported me while I was lying in bed for long time due to a back injury.

I also would like to thank my associate advisor, Professor Thomas H. Lee, who gave me strong motivation in my research. I am indebted to Dr. Zhiping Yu, who served on my oral exam and reading committees and whose incisive comments were a great help in numerical noise simulation tool development. I am also grateful for Professor John M. Cioffi, who agreed to chair my oral committee despite his busy schedule.

The staff of the Center for Integrated Systems have offered good support, and I want to thank Fely Barrera, Miho Nishi, Maria Perea, Carmen Miraflor, Maureen Rochford, Kate Gibson, and Dr. Richard Dasher. I also want to acknowledge the help of Greg Gorton, Ali Tabatabaei, and Hamid Rategh with CAD tools on the Jupiter project. Special thanks go to Dr. Daniel Yergeau, whose computational expertise has kept the research in phase. I thank friends in the Stanford TCAD group for their helpful discussions and friendship: Chang-Hoon Choi, Kwanghoon Oh, Tae-Young Oh, SoYoung Kim, Dr. Olof Tornblad, Xin-Yi Zhang, Xiaoning Qi, Michael Kwong, Yi-Chang Lu, Atsushi Kawamoto, Choshu Ito, and

Mr. Hiroyuki Sakai.

In addition to those in the Stanford community, I want to acknowledge a number of industrial people who contributed directly to research. In particular, I would like to thank: Dr. Tom Vrotsos, Dr. Keith R. Green, Dr. William Liu, and Mr. Donald J. Ladwig of Texas Instruments for providing access to noise measurement equipment; Mr. Thomas P. Redfern, Mr. Peter Hopper, Mr. Michael P. Schwartz, Mr. Robert Farmer, Dr. Hee-Tae Ahn, Mr. Rich Taylor, and Ms. Linda Smith of National Semiconductor for fabricating chips, lending wafers, and test equipment; Dr. Marek Mierzwinski of Agilent Technologies and Professor François Danneville of University of Lille in France for collaboration in noise simulation tool development; Dr. Conor Rafferty and Dr. Muhammad A. Alam of Agere Systems and Professor Simona Donati of Politecnico Di Torino in Italy for providing PADRE as well as cooperating in noise simulation. I also want to thank several people for providing noise measurement data: Dr. Alexander Rahm and Dr. Gerhard Knoblinger of Infineon Technologies; Dr. Fariborz Assaderaghi and Dr. Lawrence Wagner of IBM; and Professor Hiroshi Iwai of Tokyo Institute of Technology and Ms. Hisayo S. Momose and Mr. Eiji Morifuji of Toshiba Corporation. I would like to acknowledge that this research was initiated by the Defense Advanced Research Projects Agency and then supported by Texas Instruments through customized research of SRC.

Finally, I must reserve special thanks for my significant others. I appreciate all the friends: Yoon, Jung-Won, Youngmi, Wonil, Hyun Jin, Kern, Hyongsok, Jungsang, Nahm-suk, Moon-Jung, Seong Taek, Dong-Hyun, Ki Young, Sang-Min, Jaewon, and folks in *Korea town* in the basement of CIS. I would like thank my sisters – Hyun, Nan, Jung, and Young – for their genial favor. I am deeply indebted to my mom in heaven and dad who gave me unconditional support. I also want to thank my son, Timothy, for his hilarity that refreshed me from the overload of research. At last, my sincere thanks are reserved for my wife, Inseong, who has sacrificed her career for the family before and now begins a new

student life at Stanford.

This work is dedicated to my God.

Contents

Abstract . . . v

Acknowledgments . . . vii

List of Tables . . . xvi

List of Figures . . . xvii

1 Introduction **1**

1.1 Motivation . . . 1

1.2 Overview . . . 2

2 Fundamentals of Noise **5**

2.1 Thermal Noise . . . 6

2.1.1 Thermal Noise in Electronic Devices . . . 7

2.1.2 Thermal Noise in MOSFETs . . . 8

2.2 Shot Noise . . . 10

2.3 Flicker Noise . . . 11

2.4 Generation-Recombination Noise . . . 12

2.5 Noise Figure . . . 12

2.6 Four Noise Parameters . . . 15

3 Numerical Noise Simulation **17**

3.1 Basic Theory for Noise Calculation . . . 21
3.1.1 Impedance Field Method . . . 21
3.1.2 Impedance Field Formulation . . . 22
3.1.3 Network Analysis . . . 22
3.1.4 Device Segmentation . . . 25
3.2 Noise Simulator Implementation . . . 28
3.2.1 2-D Device Simulator . . . 28
3.2.2 2-D to 1-D Transformation . . . 29
3.2.3 Microscopic Noise Source Calculation . . . 31
3.3 Simulation Results . . . 33
3.4 Summary . . . 37

4 Parasitic Noise Components 39
4.1 Deembedding . . . 40
4.2 DUT Implications . . . 42
4.2.1 Bonding Pad . . . 42
4.2.2 Gate Poly Resistance . . . 43
4.3 Substrate Induced Drain Current Noise . . . 45
4.3.1 Noise Simulation . . . 46
4.3.2 Noise Contribution Model . . . 47
4.3.3 Simulation Results . . . 49
4.4 Summary . . . 52

5 Excess Channel Noise 55
5.1 Physical Origin . . . 56
5.2 Summary . . . 60

6 Compact Noise Modeling **63**

6.1 van der Ziel Model 65

6.2 Pospieszalski Model 66

6.3 BSIM4 Model 69

6.4 Impact of Errors in Correlation Modeling 72

6.5 Physical Noise Modeling 80

6.6 Summary 82

7 LNA Design **83**

7.1 High Frequency Intrinsic Noise Performance of MOSFETs 84

7.1.1 Scaling of the Noise Parameters 86

7.1.2 Conversion of Noise Characteristics into Common-Gate Mode . . . 87

7.2 Design Guidelines for a Tuned Amplifier 89

7.2.1 Basic Architecture 89

7.2.2 Power Constrained Design 92

7.2.3 Cascode Stage Design 93

7.2.4 Design with A Fixed Source Impedance 94

7.2.5 Secondary Considerations 98

7.3 Experimental Results 98

7.4 Summary 102

8 Conclusions **103**

8.1 Summary 103

8.2 Recommendations for Future Work 105

Appendix A

Two-Port Theory 109

A.1 General Two-Port Matrices . . . 110
A.2 Noise Correlation Matrices . . . 111
A.2.1 Admittance Representation . . . 113
A.2.2 Impedance Representation . . . 114
A.2.3 $ABCD$ Representation . . . 114
A.2.4 Transformation into Other Representations . . . 116
A.2.5 Noise Analysis for Circuits . . . 117
A.3 Derivation of Four Noise Parameters . . . 117
A.3.1 How the Four Noise Parameters Are Defined . . . 117
A.3.2 Relationship between $F_{min} - R_n - G_{opt} - B_{opt}$ and $\overline{v_n^2} - \overline{i_n^2}$ . . . 120
A.3.3 Relationship between $F_{min} - R_n - G_{opt} - B_{opt}$ and $\overline{i_g^2} - \overline{i_d^2}$ . . . 120
A.4 Two-Port Parameters of the MOSFET . . . 122
A.4.1 Y Paramters . . . 122
A.4.2 $ABCD$ Paramters . . . 124
A.4.3 Conversion from Common-Gate Y to Common-Source $ABCD$ . . . 125

Appendix B

MOSFET Noise Analysis . . . 127
B.1 Impedance Field Formulation . . . 127
B.2 Unsegmented MOSFET Noise Spectra . . . 128
B.2.1 General Uniform Transmission Line . . . 128
B.2.2 Lossy Active Transmission Line . . . 130
B.2.3 Impedance Field . . . 131
B.2.4 Noise Power Spectra . . . 132

Appendix C

MEDICI Input Deck for Noise Simulation . . . 135

Appendix D

On the Validity of the Pospieszalski Model 137

Appendix E

Noise Model Description 139

E.1 BSIM4 Noise Model 139

E.2 Knoblinger Noise Model 140

E.3 Klein Noise Model 140

Appendix F

LNA Analysis Method 141

F.1 Input Impedance 141

F.2 Noise Analysis Based on Two-Port Theory 142

F.3 Analytical Calculation of Noise Figure 143

Bibliography **145**

List of Tables

7.1 Measured Performance of an 800MHz LNA 101

A.1 Conversions between Two-Port Network Parameters [1] 112

A.2 Transformation Matrices to Calculate Noise Matrices of Other Representations [2] 115

List of Figures

2.1 Numerous noise sources. 5

2.2 Induced gate noise effects in MOSFET devices. 9

2.3 Typical architecture of a radio receiver. 13

2.4 Typical dependence of the noise figure on source admittance 14

3.1 Original device representation with a noisy segment. 19

3.2 Modified device representation based on the Langevin method. 20

3.3 Another modified device representation adopting the Impedance Field Method. 20

3.4 Basic principle of the impedance field calculation. The MOSFET is divided into two subdevice blocks that are represented by two-port networks. (b) General two-port network diagram. 23

3.5 Small-signal equivalent representation for a MOSFET at high frequency in a common-gate configuration. 24

3.6 Local small-signal equivalent circuit for a segment of the MOSFET. 25

3.7 Frequency evolution of drain current noise spectral power density terms for a uniform transmission line. 26

3.8 Frequency evolution of gate current noise spectral power density terms for a uniform transmission line. 27

3.9 Drain current noise calculation error by segmentation for a uniform transmission line case. The MOSFETs are divided into 20 segments. 28

3.10 Gate current noise calculation error by segmentation for a uniform transmission line case. The MOSFETs are divided into 20 segments. 29

3.11 Illustration for local quantity extraction from a 2-D device simulation result. 30

3.12 Gate length dependence of γ and δ comparing HD and DD model results. . 32

3.13 Gate length dependence of the imaginary part of c comparing HD and DD model results. 33

3.14 Comparison of de-embedded measurement data (circles) to the simulated equivalent noise resistance (dots) for a 0.25 μm nMOSFET. Solid lines refer to smoothed simulation results of the HD model. 34

3.15 Gate bias dependence comparison of de-embedded measurement data (circles) to simulated minimum noise figures (dots) with correction for the loss due to G_{opt} for a 0.25 μm nMOSFET. Solid lines refer to smoothed simulation results of HD model. 35

3.16 Frequency dependence comparison of de-embedded measurement data (circles) to simulated minimum noise figures (dots) with correction for the loss due to G_{opt} for a 0.25 μm nMOSFET. Solid lines refer to smoothed simulation results of HD model. 36

4.1 Parasitic resistance generating thermal noise in MOSFETs. 39

4.2 Equivalent circuit model of the DUT for de-embedding. 40

4.3 Calculation of distributed resistance for a MOSFET with a multi-fingered gate structure. 43

4.4 Cross-section of the MOSFET structure used for simulation. 46

4.5 Commonly assumed drain current noise power spectrum for MOSFETs. . . 47

4.6 Anticipated general drain current noise power spectrum for bulk MOSFETs. The solid line is total noise power, the circle symbol is the $1/f$ noise component ($S_{i_d,1/f}$), the triangle symbol is the additive component induced by the substrate ($S_{i_d,sub}$), and the diamond symbol is the channel thermal noise component ($S_{i_d,channel}$). The inset circuit diagram explains the contribution mechanism of the substrate thermal noise to the drain current noise. 48

4.7 Simulation results of drain current noise power spectrum of a 0.5μm MOSFET for different drain bias conditions. The gate oxide thickness is 60nm, N_{chan} is 5.0×10^{17}cm^{-3}, N_{sub} is 1.0×10^{15}cm^{-3}, L_{sd} is 0.01μm, and V_{GS} is 1.5V. The symbols are PADRE simulation results and lines are calculated using Equation (4.21). 50

4.8 Simulation results of drain current noise power spectrum for MOSFETs with different gate lengths. The gate oxide thickness is 60nm, N_{chan} is 5.0×10^{17}cm^{-3}, N_{sub} is 3.2×10^{16}cm^{-3}, L_{sd} is 0.01μm, V_{GS} is 1.5V, and V_{DS} is 2.5V. The symbols are PADRE simulation results and lines are calculated using Equation (4.21). 51

4.9 Distributed effect of the substrate network. 52

4.10 Drain current noise spectrum for different number of poles. 53

5.1 Comparing the HD model with the DD model along the channel for noise spectral density distribution of the local noise source (S_{i_n} [A^2/Hzμm]) and its actual contribution to the drain noise (S_{i_d} [A^2/Hzμm]); and the impedance field ($|\Delta A_d|^2$ [no unit]). 56

5.2 Local ac resistance distribution, comparing the HD model (solid line) with the DD model (dashed line). 58

5.3 Carrier response to the electric field changes. 59

5.4 Car analogy to explain the carrier transport in the channel. 60
6.1 Noise figure of a MOSFET connected to Z_s=50Ω 63
6.2 Noise performance of a tuned LNA 64
6.3 MOSFET thermal noise models. (a) van der Ziel model (b) Pospieszalski Model. 65
6.4 Schematic for model comparison. (a) van der Ziel model (b) Pospieszalski Model. 66
6.5 Gate bias dependence of the correlation factor of the Pospieszalski model for an nMOSFET ($W/L = 96/0.25\mu$m). 67
6.6 MOSFET thermal noise models. (a) BSIM4 as implemented. (b) Simplified BSIM4 (assuming R_s is negligible) 69
6.7 Schematic for BSIM4 model comparison. 70
6.8 Comparison for the correlated noise power spectrum. (a) real part (b) imaginary part 71
6.9 Model comparison procedure. 72
6.10 Frequency dependence of four noise parameters. Generated using noise sources extracted at 5GHz. (a) NF_{min} (b) R_n 74
6.11 Frequency dependence of four noise parameters. Generated using noise sources extracted at 5GHz. (a) G_{opt} (b) B_{opt} 75
6.12 Shunt-series feedback broadband amplifier. (a) Architecture (b) Power-constrained noise performance. 76
6.13 $1/g_m$ termination broadband amplifier. (a) Architecture (b) Noise performance. 77
6.14 Inductively degenerated tuned amplifier. (a) Architecture (b) Power-constrained noise performance. 78

6.15 Inductively degenerated tuned amplifier with cascode stage. (a) Architecture (b) Power-constrained noise performance. 79

6.16 Physical noise sources in MOSFET devices. 80

6.17 Comparison between physical effects and BSIM4 noise model. 81

7.1 Intrinsic noise performance for the entire operating range of a 0.25 μm nMOSFET. (a) Minimum noise figure (NF_{min} [dB]) (b) Equivalent noise resistance (R_n [Ω]). 85

7.2 Noise power of the MOSFET in a common-gate configuration. (a) Original (b) Equivalent 87

7.3 (a) Tuned LNA architecture employing inductive source degeneration. (b) Dependence of output noise power components on $\Re[Z_A]$ where Z_A is the input impedance at the gate electrode of M_1. 88

7.4 The noise performance of the LNA for varying L_s. The noise contributions of M_1 substrate and M_2 are excluded and C_p=0. (a) Optimum source impedance (b) Noise figure. 90

7.5 (a) Optimum L_s yielding the best noise figure of the LNA for the given bias condition under the power constraint. (b) The best noise figure of the LNA with optimum L_s. The noise contributions of M_1 substrate and M_2 are excluded and C_p=0. 91

7.6 The impact of the cascode transistor on the overall noise figure under the power constraint. $R_s = Z_{in} = 50\Omega$. 93

7.7 Power constrained noise figure of the tuned amplifier when $R_s = Z_{in} = 50\Omega$. The solid line is the actual noise figure; the dashed line is an approximation calculated from (7.15). 94

7.8 Optimum source impedance of a power constrained LNA at f=4GHz when $R_s = Z_{in} = 50\Omega$. The noise contributions of M_1 substrate and M_2 are included and C_p=0. 95

7.9 Optimum source impedance of a power constrained LNA at f=800MHz when $R_s = Z_{in} = 50\Omega$. The noise contributions of M_1 substrate and M_2 are included and C_p=0. 96

7.10 The power constrained noise performance of the LNA when $R_s = Z_{in} = 50\Omega$. The noise contributions of M_1 substrate and M_2 are included and C_p=0. (a) Equivalent noise resistance (b) Noise figure 97

7.11 The power constrained noise performance of the LNA when $R_s = Z_{in} = 50\Omega$ for different pad capacitance. The noise contributions of M_1 substrate and M_2 are included. (a) Noise figure (b) Gain. 99

7.12 Die photo of the LNA 100

7.13 Wire-bonding illustration of the LLP package 101

8.1 Gate oxide tunneling current in MOSFETs. (a) Fowler-Nordheim tunneling current. (b) Direct tunneling current. 106

8.2 Local small-signal equivalent circuit for a segment of MOSFET in which the direct tunneling current is significant. 107

A.1 General two-port diagram. 109

A.2 Equivalent noise circuit of a two-port. (a) Admittance representation (b) Impedance representation (c) $ABCD$ representation. 113

A.3 Circuit decomposition for noise analysis (a) Entire circuit (b) Cascode decomposition (c) Series decomposition (d) Parallel decomposition 116

A.4 Circuit diagram for the noise figure calculation of general two port networks 118

A.5 Y parameters of a MOSFET for different configurations. 123

B.1 Equivalent circuit for a differential length Δx of a two-conductor transmission line. 129
F.1 Schematic diagram for input impedance calculation of the LNA 142
F.2 Noise performance evaluation sequence for the LNA 143

Chapter 1

Introduction

WIRELESS COMMUNICATIONS has thrived in the last decade, owing to exploding user demand for information and the commensurate need for connectivity. Substantial research effort has focused on many application areas, such as cellular phones, cordless phones, GPS (global positioning system), and WLANs (wireless local area networks). The RF ICs (radio frequency integrated circuits) have been the primary domain of GaAs or bipolar technologies since those technologies provide relatively high cutoff frequencies (f_T). However, as continuous scaling of CMOS makes f_T in excess of 30GHz readily achievable in typical quarter micron technology, CMOS becomes an attractive alternative for RF applications in the low GHz frequency range.

1.1 Motivation

In comparison to other technologies, CMOS is the most cost-effective solution to date for large-scale digital applications and it enables system-on-a-chip owing to its capability of providing large-scale subsystems with high levels of integration. A number of fully integrated tranceivers, up to 5GHz, are being implemented using standard CMOS processes;

typical protocols are Bluetooth, IEEE 802.11, IEEE 802.15.3, IEEE 802.11a, and HiperLAN. Nevertheless, the real design of CMOS RF circuits is still a challenge due to severe constraints on power consumption and noise that impose stringent margins to the design process. Accurate models are critical in order to reduce design cycles and to achieve first-time success in implementation. Unfortunately, available MOSFET compact models – such as BSIM3v3 [3], MOS Model 9 [4], or EKV [5] – are typically not applicable for the GHz range of frequencies.

Modeling of noise provides critical information in the design of RF circuits, especially for LNA (low noise amplifier) blocks. The LNA is typically the first stage of a radio receiver and needs to provide sufficient gain while introducing the least noise possible. Since it is indispensable to understand the physical phenomena of broadband noise and to incorporate this information into the models, lack of understanding of MOSFET noise presents a substantial barrier to the implementation of CMOS receivers.

1.2 Overview

The following chapters provide extensive and detailed information about MOSFET noise both in terms of device physics and detailed design guidelines for circuits. To achieve these goals, this dissertation tackles various areas such as physics based numerical simulation, noise characterization, compact modeling, and finally LNA design methodologies.

Chapter 2 gives an introduction to the definition and classification of device noise. It also introduces fundamental concepts of system noise performance. Chapter 3 begins with a survey of numerical simulation methods for studying device noise and then presents an efficient simulation technique for deep submicron MOSFETs, including discussion of practical concerns related to the implementation.

Chapter 4 discusses parasitic noise sources in MOSFETs and implications of the results

on intrinsic noise characterization. This chapter also brings attention to substrate induced noise, which has been known for some time but in practice has been neglected. Chapter 5 explores the subject of the excess channel thermal noise, including a survey of recent approaches to modeling and practical limitations. In this chapter, the physical origin of the excess noise is investigated based on the numerical simulation methodology discussed in Chapter 3. Chapter 6 examines existing compact noise models and makes critical comparison of the results with physics discussed in Chapters 4 and 5. A physically sound noise modeling approach is then proposed.

Chapter 7 discusses LNA design in detail. This includes the development of an intuitive noise optimization procedure along with an actual circuit implementation example with experimental results for a CMOS LNA. These results demonstrate that CMOS is a good candidate for high performance LNA design. Finally Chapter 8 concludes with a summary and suggestions for future work.

Several appendices provide more detailed explanation of certain subjects. Appendix A introduces two-port theory that offers a means to model the performance of the noisy system macroscopically. Appendix B describes the impedance field formulation procedure and noise spectra of a uniform transmission line. Appendix C provides a sample input deck for the commercial device simulator MEDICI, specifically for the case where a hydrodynamic model for carrier transport is incorporated. Appendix D validates the assumption of the Pospieszalski noise model. Appendix E describes several noise models including BSIM4. Finally, Appendix F presents the LNA analysis method, including input impedance calculations and noise performance analysis.

Chapter 2

Fundamentals of Noise

THE GENERAL DEFINITION OF NOISE in the Webster dictionary includes "loud, confused , or senseless shouting or outcry" or "any sound that is undesired or interferes with one's hearing of something." In electronics, noise is usually referred as an opposite

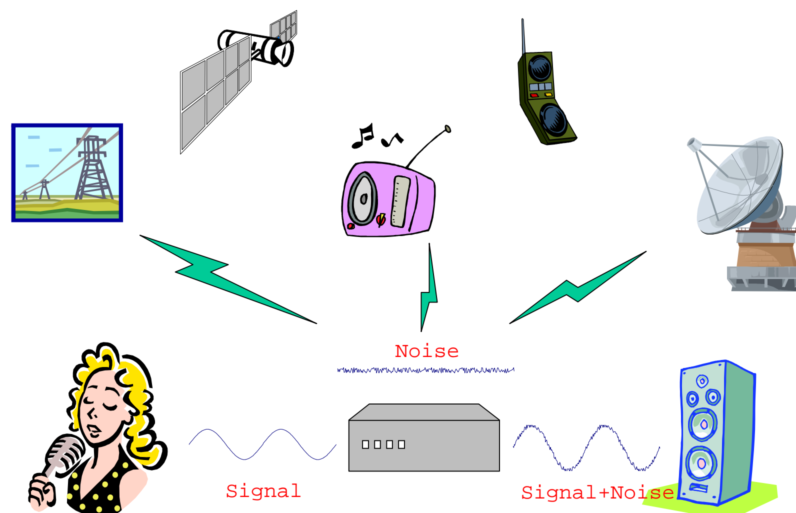


Figure 2.1: Numerous noise sources.

term to the *signal*[1]. Thus noise can be defined as "everything except for the desired signal" [6]. There are numerous noise sources interfering with the desired signal in electronic systems, including: power-line, broadcasting signals for radio and TV, signal cross-talk, and other electromagnetic waves, as illustrated in Figure 2.1. Most of them are classified as *artificial noise*, which can be reduced or eliminated using good shielding scheme.

By contrast, other noise sources, classified as *fundamental noise*, are irreducible by shielding since they are inherent in the system or device itself. These fundamental noise sources impose a lower limit of the performance of electronics, which manifests itself as a continuous hissing sound in audio systems, snowy pictures in analog TV sets, or the ultimate sensitivity of measurement systems. The process of fundamental noise is random yet can be characterized statistically.

The microscopic noise theory at the material level is straightforward and well established. Physically, two types of noise can be identified: thermal and quantum. However phenomenologically several types of noise sources are observed, such as thermal, shot, generation-recombination, and flicker noise.

2.1 Thermal Noise

Thermal noise refers to the kinetic energy of particles as a result of their finite temperature. A thermally-excited electron in a conductor undergoes a *random walk* Brownian motion via collisions with the lattice of the conductor; as a result it produces fluctuations in the terminal characteristics. The statistical properties of such Brownian particles were studied by Einstein in 1906 [7]. In 1927, Johnson discovered that the noise power spectrum of a

[1]The signal is an object to transmit or convey information. By contrast noise is an obstacle to transmitting or conveying information.

conductor is independent of its material and the measurement frequency[2]; noise properties are determined only by the temperature and electrical resistance under thermal equilibrium [8], [9]:

$$\overline{v_n^2} = S_{v_n}\Delta f = 4kT\Delta f R \quad (2.1)$$

$$\overline{i_n^2} = S_{i_n}\Delta f = 4kT\Delta f / R \quad (2.2)$$

This noise is referred as thermal noise, which is the most fundamental and important noise in electronic devices. Johnson's colleague Nyquist explained the original observations based on the equi-partition theorem of thermodynamics and a transmission line cavity, without going into the details of the microscopic electron transport process [10]. In honor of these pioneers, thermal noise is often called *Johnson noise* or *Nyquist noise*.

2.1.1 Thermal Noise in Electronic Devices

Thermal noise assumes that the system is in thermal equilibrium, which only applies strictly if no bias is applied to the device. When there is a bias, the carrier collisions produce noise called either *diffusion noise* or *velocity-fluctuation noise*. Since behavior of these kinds of noise agrees well with Johnson's thermal noise model, they are often called *thermal noise* as well, especially for resistors.

In general, macroscopic thermal noise measured at the electrodes of a non-linear device is different from the formulae given in Equations (2.1) and (2.2). However the microscopic spectral density generated at a local point still conforms to the thermal noise form as follows

[2]This is true only if $kT \gg \hbar\omega$ is satisfied.

[11], [12]:

$$S_{i_n} = \frac{\overline{i_n^2}}{\Delta f} = 4kT\,\Re[\sigma]\frac{A}{l} = 4\,q^2\,n\,\Re[D_n]\frac{A}{l} = 4\,k\,T_n\frac{q\,n\,\Re[\mu_{ac}]\,A}{l} \quad (2.3)$$

where Δ denotes a differential quantity, f is the operating frequency, $\Re[\ ]$ denotes the real part of a complex number, σ is the conductivity, A and l are the cross-sectional area and length of a device segment, q is the electronic charge, n is the carrier density, D_n is the noise diffusion coefficient[3], k is Boltzmann's constant, T_n is the noise temperature, and μ_{ac} is the ac mobility.

2.1.2 Thermal Noise in MOSFETs

Thermal noise of the MOSFET imposes a fundamental limitation on CMOS LNAs [13]. Based on the fact that the MOSFET is a modulated resistor, capacitively coupled to the gate, van der Ziel has proposed a thermal noise model for MOSFETs, which consists of drain current noise, *induced gate current noise*, and their cross-correlation coefficient as follows [6]:

$$\overline{i_d^2} \triangleq 4kT\Delta f\,\gamma\,g_{d0} \quad (2.4)$$

$$\overline{i_g^2} \triangleq 4kT\Delta f\,\delta\,g_g \quad (2.5)$$

$$\overline{i_g i_d^*} \triangleq c\sqrt{\overline{i_g^2}\,\overline{i_d^2}} \quad (2.6)$$

$$g_g \triangleq \zeta\frac{\omega^2 C_{gs}^2}{g_{d0}} \quad (2.7)$$

[3] In comparison to the spreading diffusion coefficient (D_s), D_n has the same value at thermal equilibrium while its field ($\mathcal{E}$) or energy (E) dependency is different in general. Although D_s may be used as an approximation of D_n [12], it would be questionable for extremely small devices where ballistic transport assumes an important role.

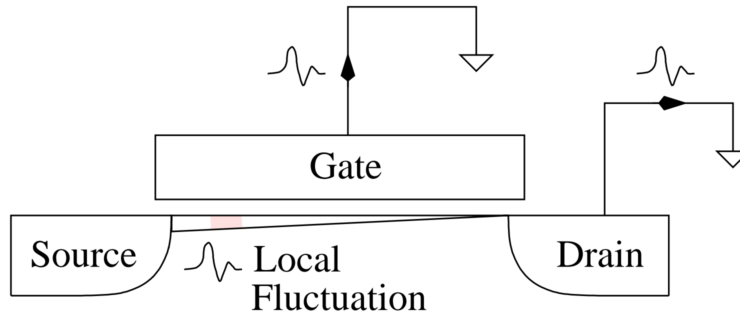


Figure 2.2: Induced gate noise effects in MOSFET devices.

where γ, δ, and ζ are bias-dependent factors; g_{d0} is the drain output conductance under zero drain bias; g_g is the real part of the gate-to-source admittance; and c is the cross correlation coefficient.

Note that the induced gate current noise is thermal noise that is induced by local fluctuations in the channel via capacitive coupling through the gate oxide, as illustrated in Figure 2.2. Induced gate noise is proportional to f^2, owing to the ωC dependence, while drain noise is frequency independent (*white*). As discussed in Chapter 6, the induced gate noise dominates noise performance of MOSFETs at high frequencies.

For long channel MOSFETs, γ satisfies the inequality $\frac{2}{3} \leq \gamma \leq 1$. The value of 2/3 holds when the MOSFET is in the channel pinch-off region, and the value of 1 is valid when the drain bias is zero [11]. Also for long channel MOSFETs in saturation, δ, c, ζ are reportedly 4/3, $j0.395$, and 0.2 [14], respectively. This model agrees well with long channel MOSFETs down to 1.7μm. Substantial increases have been observed in γ and δ for MOSFETs with shorter channel length [15], [16], [17], [18], [19]. However, the amount of the increase is still controversial [18]; the physical mechanism responsible for such excess noise has remained an open question. This issue is discussed in detail in Chapters 4 and 5.

2.2 Shot Noise

Shot noise was first described by Schottky in 1918 [20] as:

$$\overline{i_n^2} = 2q\, I_{DC} \Delta f \tag{2.8}$$

where I_{DC} is the dc current flowing across the device. It is white noise and occurs when quantized carriers cross barriers with random spacing as in Schottky diodes or $p-n$ junctions. The arrival of one unit charge at a boundary is independent of when the previous unit arrived or when the succeeding unit will arrive. Therefore, two conditions are required for shot noise to occur: a flow of direct current and a potential barrier over which the carriers are extracted. Thus linear devices do not generate shot noise. In the case of MOSFETs, shot noise dominates the noise characteristics only when the device is in the subthreshold region owing to the carrier transport in this region, which is very similar to conditions in bipolar transistors.

Physically, shot noise consists of a mixture of thermal and generation-recombination components. There are two environments for a $p-n$ junction: lattice vibration (thermal phonon) reservoirs which are responsible for thermal diffusion noise and electromagnetic field (thermal photon) reservoirs which are responsible for generation-recombination noise. Under forward bias, two-thirds of the full shot noise is due to thermal diffusion noise and one-third is due to recombination noise by spontaneous emission, which is of quantum mechanical origin. If the $p-n$ junction is under reverse bias, shot noise is dominated by generation noise caused by thermal photon absorption.

2.3 Flicker Noise

The first obervation of flicker noise in an electronic system was made by Johnson [21]. It is also known as $1/f$ noise since its spectral density is inversely proportional to the frequency. Flicker noise is ubiquitous but no universal mechanism has been proved definitively as the cause. Thus its model contains various empirical parameters unlike thermal and shot noise. In other words, flicker noise can be modeled empirically but cannot be predicted *a priori*.

Carbon composition resistors exhibit current-dependent excess noise due to the random formation and extinction of *macro arcs* among neighboring carbon granules [22]. The amount of excess noise is much smaller in carbon film resistors and smallest in metal-film resistors. It is also important to minimize the dc drop across a resistor since excess noise increases for the larger dc bias [6].

Flicker noise is significantly larger in MOSFETs than in other types of devices since it is quite closely related to surface phenomena. This fact is usually explained based on charge trapping behavior of defects and impurities that are plentiful at the Si/SiO_2 interface. Larger MOSFETs exhibit less flicker noise since larger gate oxide capacitance smooths the fluctuations in channel charge. The typical model is given as:

$$\overline{i_n^2} = \frac{K}{f}\frac{g_m^2}{WLC_{ox}^2}\Delta f \tag{2.9}$$

where K is a device-specific constant, g_m is transconductance, W is the device width, L is the device length, and C_{ox} is the gate oxide capacitance per unit area. Smaller K can be obtained from buried channel devices like p-MOSFETs, but largely varies from process to process, and lot to lot.

2.4 Generation-Recombination Noise

Generation-recombination noise is caused by the carrier density fluctuation due to emission and capture of carriers by traps. It manifests itself as resistance fluctuations. Thus generation-recombination noise is observed only if external bias voltage is applied, although the fluctuations are present whether the device is in thermal equilibrium or not.

Since this noise is closely related to the localized energy states, its behavior depends largely on the temperature, frequency, and bias conditions. In modern MOSFET technologies, this component is usually much smaller than flicker noise and generally can be neglected.

2.5 Noise Figure

An important measure of system noise performance is a parameter known as the *noise figure* (NF) or *noise factor* (F) [23]. This parameter came into popular use in the 1940's when Friis [24] defined the noise figure of a network to be the ratio of the signal-to-noise power ratio at the input to the signal-to-noise power ratio at the output:

$$F \triangleq \frac{(S/N)_{in}}{(S/N)_{out}} \tag{2.10}$$

where the ambient temperature must be 290°K by convention[4]. Thus the noise figure of a network is the decrease or degradation in the signal-to-noise ratio as the signal goes through the network. A perfectly noise-free amplifier would maintain the same signal-to-noise ratio at its input and output. A realistic amplifier, however, also adds extra noise from its own components and degrades the signal-to-noise ratio. Therefore a low noise figure means that

[4]Simply because kT becomes a good round number 4.00×10^{-21}J when the temperature T is 290°K.

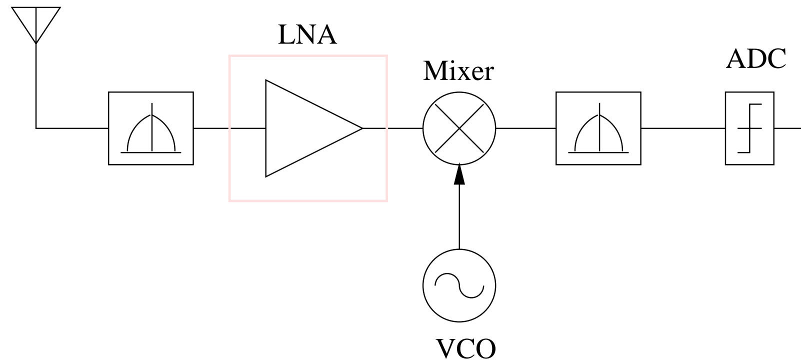


Figure 2.3: Typical architecture of a radio receiver.

little noise is added by the network. Modern usage of *noise figure* is usually reserved for the quantity NF, expressed in dB units:

$$NF = 10 \log F \tag{2.11}$$

Other definitions of the noise factor are:

$$F = \frac{\text{Total Output Noise Power}}{\text{Output Noise Power by Source Impedance}} \tag{2.12}$$
$$= \frac{\text{Total Equivalent Input Noise Power}}{\text{Noise Power of Source Impedance}} \tag{2.13}$$

When n blocks are cascaded as illustrated in Figure 2.3, the noise figure for the entire system is given by [24]:

$$F_{tot} = 1 + (F_1 - 1) + \frac{F_2 - 1}{A_1} + \cdots + \frac{F_n - 1}{A_1 \cdots A_{n-1}} \tag{2.14}$$

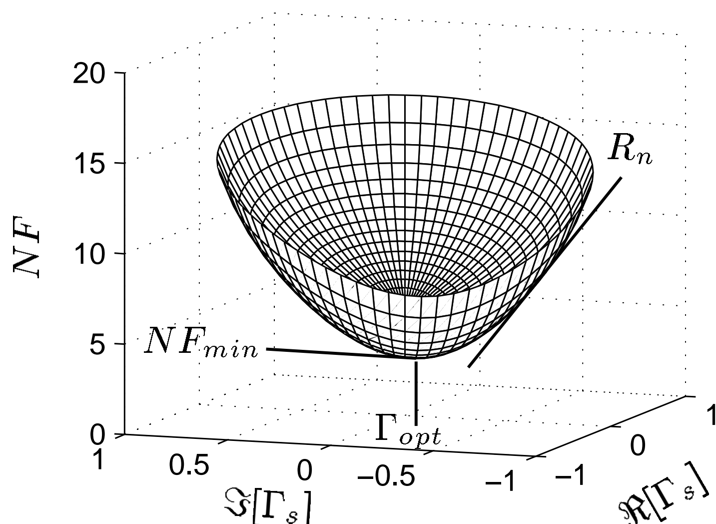


Figure 2.4: Typical dependence of the noise figure on source admittance

where A_i is available power gain[5] and the noise figure of each stage is evaluated with the output impedance of the preceding stage. This is known as the Friis formula and typical results show that the first few stages in a cascade are the most critical in noise performance since the given equation shows that the noise contributed by each stage decreases as the gain preceding the stage increases. Therefore, the noise figure of the low-noise amplifier basically dominates the entire receiver sensitivity[6]. Consequently, the LNA has to be designed to have the lowest possible NF and the highest possible gain.

[5]Available power gain is defined as the available power at the output, that the circuit delivers to a conjugate-matched load, divided by the available source power, that the source delivers to a conjugate-matched circuit.

[6]The sensitivity of an RF receiver is defined as the minimum signal level that the system can detect with acceptable signal-to-noise ratio.

2.6 Four Noise Parameters

The noise figure of a system is not only determined by noise sources inside of the system but also determined by the source admittance driving the system. The noise performance of a linear system typically exhibits a parabolic dependence on source admittance at one frequency as shown in Figure 2.4. The x-y plane of Figure 2.4 is the source reflection coefficient Γ_s as used in the Smith chart and the z axis is the resulting noise figure; contours for a set of constant noise figures result in circles on a Smith chart. Such a behavior can be completely characterized by four noise parameters $F_{min} - R_n - Y_{opt}$ [25]:

$$F = F_{min} + \frac{|Y_s - Y_{opt}|^2 R_n}{G_s} \tag{2.15}$$

$$= F_{min} + \frac{4R_n}{Z_0} \cdot \frac{|\Gamma_{opt} - \Gamma_s|^2}{|1 + \Gamma_{opt}|^2(1 - |\Gamma_s|^2)} \tag{2.16}$$

$$\Gamma_{opt} = \frac{1 - Z_0 Y_{opt}}{1 + Z_0 Y_{opt}} \tag{2.17}$$

where Y_s is the source admittance, Z_0 is the characteristic impedance (usually 50Ω), F_{min} is the minimum noise factor that the network can achieve with the optimum source admittance condition ($Y_s = Y_{opt} = G_{opt} + jB_{opt}$), and noise resistance R_n determines the sensitivity of the noise figure when Y_s differs from Y_{opt}. This representation is widely used in RF circuit design since it offers a more intuitive way to deal with noise properties. These four noise parameters are determined by intrinsic noise sources of the given system; thus they are equivalent[7] to intrinsic noise sources.

It is important to note that the optimum source admittance (Y_{opt}) is generally different from the conjugate power match condition ($Y_{conj} = Y_{in}^*$). Thus those two conditions quite often need to be traded off. To achieve a good noise figure, it is desired to have low NF_{min}

[7] See Appendix A.3 for the detailed derivation.

(hopefully below 1dB), small R_n, and a close proximity between Y_s and Y_{opt}.

Chapter 3

Numerical Noise Simulation

SIMULATION OF MOSFET NOISE can play an important role in realizing optimal CMOS RF circuit design by providing *a priori* noise performance metrics of devices which in turn help reveal underlying technology issues. A very popular technique in device noise simulation is the IFM (*Impedance Field Method*) [26] with *Langevin stochastic noise source*. Even though the IFM was theoretically extended up to 3-D (three-dimensions) [27], [28], its practical application has been limited to 1-D (one-dimensional) devices [12]. The 1-D simulation conveys simple and insightful results at reasonable computational cost; unfortunately, its accuracy is limited. Recently an alternative technique, using a 1-D Boltzmann Transport Equation, has been proposed to improve model accuracy for short channel MOSFETs [29]. Nevertheless, the primary weakness involves difficulty in incorporation of 2-D (two-dimensional) dependencies. This problem is particularly acute for state-of-the-art MOSFET technologies because of various second-order effects caused by complex processing such as new drain structures, gate overlap effects, nonuniform doping profiles in the substrate, etc. Hence, in conjunction with process simulation, the capability to exploit multi-dimensional device simulations to extract physical dependencies of noise is highly attractive.

Recently several studies have reported full 2-D noise simulation results implementing the IFM in a DD (Drift-Diffusion) based device simulator [30],[31]. The 2-D noise simulation is well suited for investigating the noise contribution from the substrate, discussed in Chapter 4. However, in the case of channel noise, unsatisfactory agreement with experimental data implies that the noise modeling of deep submicron MOSFETs requires not only multi-dimensional features but also higher order transport models to capture essential dispersive non-equilibrium effects [12], [31]. The problem is that the expansion to higher order moments of the BTE (Boltzmann transport equation) in 2-D noise simulation requires substantially increased cost both for implementation and simulation. For example, the HD (Hydro-Dynamic) formulation involves at least four times larger matrices [30] and to date has not been used for 2-D noise analysis.

Fortunately, the nature of the MOSFET provides an important clue that reconciles the tough requirements of MOSFET noise simulation with limited computational resources. The primary issue in understanding noise performance of FETs is the knowledge of the small-signal behavior [32]. Based on Shockley's theory [33], van der Ziel and Ero [34] have proposed a modeling approach that considers the FET as an active, distributed, nonuniform transmission line. This approach has been refined by Klaassen [35] and has provided basic insight into the behavior of FETs. Such an approach is based on the fact that small-signal transport in MOSFETs is a linear process confined to the shallow inversion layer. In a multi-dimensional simulation, once coupled equations converge, the solution at each node contains structural information of the whole system, along with the underlying physics. Namely, the 2-D solutions of the substrate are redundant in the channel noise simulation of MOSFETs. Thus if accurate local solutions for the inversion layer are provided by multi-dimensional device simulations, the required second-order effects can be incorporated in noise analysis by means of the transmission line analogy, also known as the quasi 2-D approach.

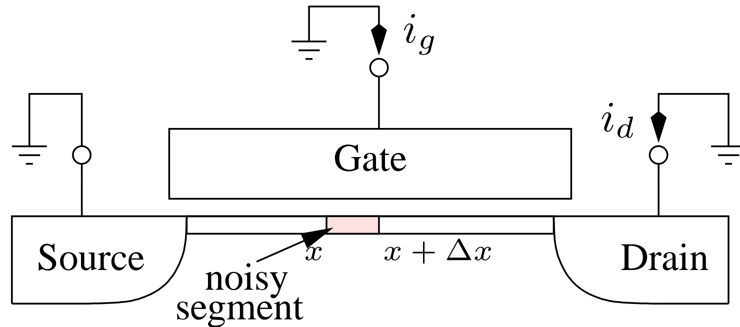


Figure 3.1: Original device representation with a noisy segment.

Hence, while a full 2-D noise simulation is necessary for investigating the substrate noise contribution due to the importance of structural information, a quasi 2-D simulation can be a good alternative for channel noise investigation due to the importance of higher order dispersive effects. Since the full 2-D noise simulation methodology is well established, this chapter presents a hybrid quasi 2-D approach for MOSFET channel noise modeling that combines a 1-D active transmission line model with a 2-D device simulation. Since this approach utilizes only a limited number of local solutions, imported from the device simulator, it imposes neither extra simulation time nor more complexity in implementation, regardless of the carrier transport model.

This chapter is constructed as follows: Section 3.1 offers the basic concept of the IFM and Langevin stochastic noise source and introduces practical concerns related to the implementation such as the impedance field formulation and device segmentation error. Then Section 3.2 explains how the noise simulation is actually implemented using a commercial device simulator. Finally, Section 3.3 demonstrates noise simulation results for MOSFETs as well as comparisons to measured data using an industrial technology.

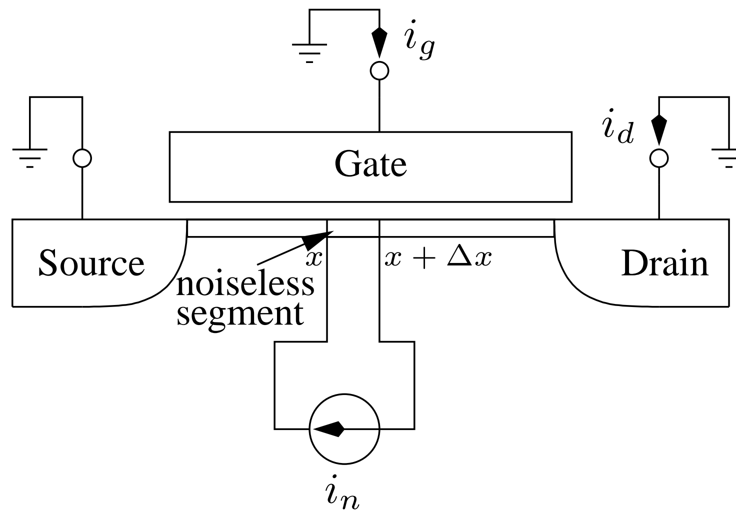


Figure 3.2: Modified device representation based on the Langevin method.

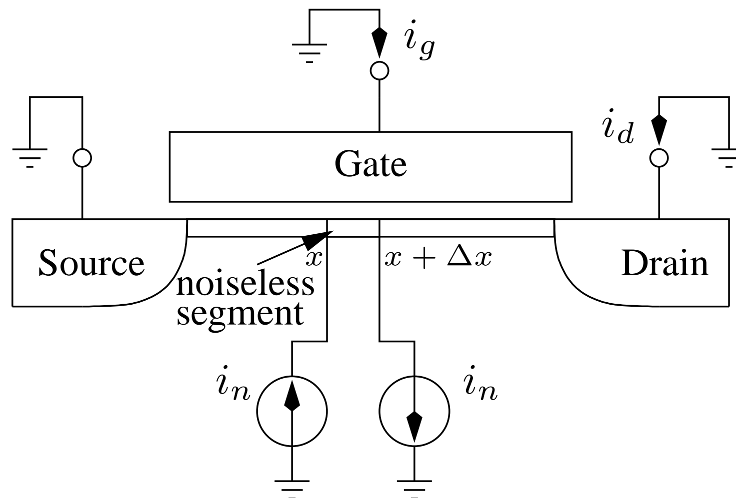


Figure 3.3: Another modified device representation adopting the Impedance Field Method.

3.1 Basic Theory for Noise Calculation

3.1.1 Impedance Field Method

From the microscopic point of view, noise is due to local random events of the carriers, which produce fluctuations of carrier velocity or in the number of carriers. These local fluctuations can be modeled by a *Langevin stochastic source term* superimposed on the dc current or bias voltage. The resulting fluctuations propagate to the electrodes and produce noise at the terminal electrodes. The propagation is called the *impedance field* [12]. Usually the local noise source is represented by a current source, otherwise the noise voltage sources across different sections are correlated [28]. Then, depending on termination of the electrodes, the impedance field is given either by an impedance Z or a dimensionless factor A [32]. Since the primary interest of this research is on current representations for the drain and gate noise, the respective two electrodes should be short-circuited for ac analysis and the impedance fields should become dimensionless factors.

The basic concept of the IFM [28] is illustrated in Figures 3.1 – 3.3. The current source i_n is the local noise source; i_d and i_g are short-circuited currents induced by i_n at the drain and gate electrodes, respectively. The noisy segment of a MOSFET in Figure 3.1 can be modeled as a noiseless segment with a Norton generator representing the local fluctuation as shown in Figure 3.2. Again it can be reconfigured as Figure 3.3. If the spectral density of a noisy segment is given by S_{i_n}, its subsequent noise power spectral density at two electrodes and their cross-correlation coefficient are given by:

$$S_{i_d} = |\Delta A_d|^2 S_{i_n} \tag{3.1}$$

$$S_{i_g} = |\Delta A_g|^2 S_{i_n} \tag{3.2}$$

$$S_{i_g i_d} = \Delta A_g \Delta A_d^* S_{i_n} \tag{3.3}$$

where * denotes a complex conjugate; and,

$$\Delta A_d \triangleq \frac{i_d}{i_n} = [A_d(x) - A_d(x + \Delta x)] \tag{3.4}$$

$$\Delta A_g \triangleq \frac{i_g}{i_n} = [A_g(x) - A_g(x + \Delta x)] \tag{3.5}$$

Hence the total noise power spectral density and cross-correlation coefficient for the entire MOSFET become simply the sum of the components for all segments.

3.1.2 Impedance Field Formulation

One of the key issues in our approach is how to formulate the dimensionless impedance field A. Figure 3.4 (a) shows a two-port network representing the MOSFET in the common-gate configuration and with a current source i_n added at x. Analysis[1] for the given network gives:

$$A_d(x) \triangleq \frac{i_d}{i_n} = \frac{Y_{21_{CG}}(x, L)}{Y_{22_{CG}}(0, x) + Y_{11}(x, L)} \tag{3.6}$$

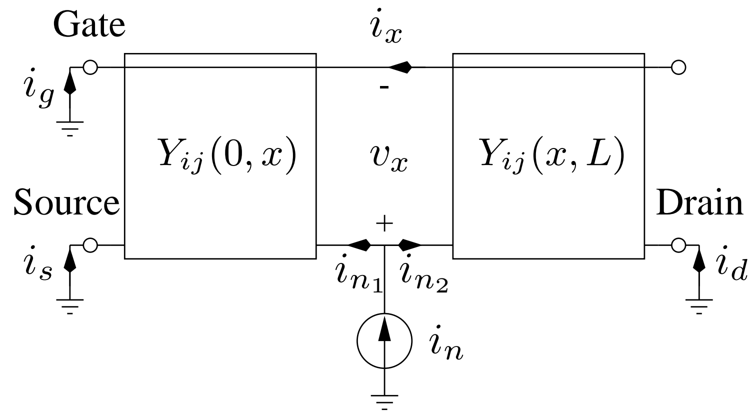
$$A_g(x) \triangleq \frac{i_g}{i_n} = -1 - \frac{Y_{12_{CG}}(0, x) + Y_{21_{CG}}(x, L)}{Y_{22_{CG}}(0, x) + Y_{11_{CG}}(x, L)} \tag{3.7}$$

where the subscript CG denotes that the two-port network is in the common-gate configuration.

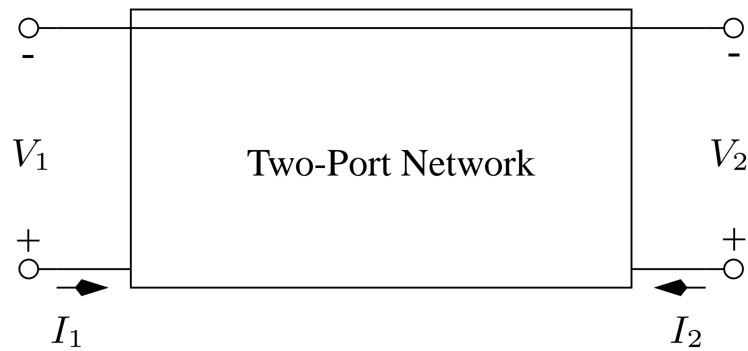
3.1.3 Network Analysis

To derive the network parameter Y_{ij} terms at x, suppose a MOSFET is divided into n segments as shown in Figure 3.5. Each segment of the MOSFET can be represented by its

[1]See Appendix B.1 for the detailed analysis.



(a)



(b)

Figure 3.4: Basic principle of the impedance field calculation. The MOSFET is divided into two subdevice blocks that are represented by two-port networks. (b) General two-port network diagram.

localized small-signal circuit illustrated in Figure 3.6, equivalent to a simple MOS device

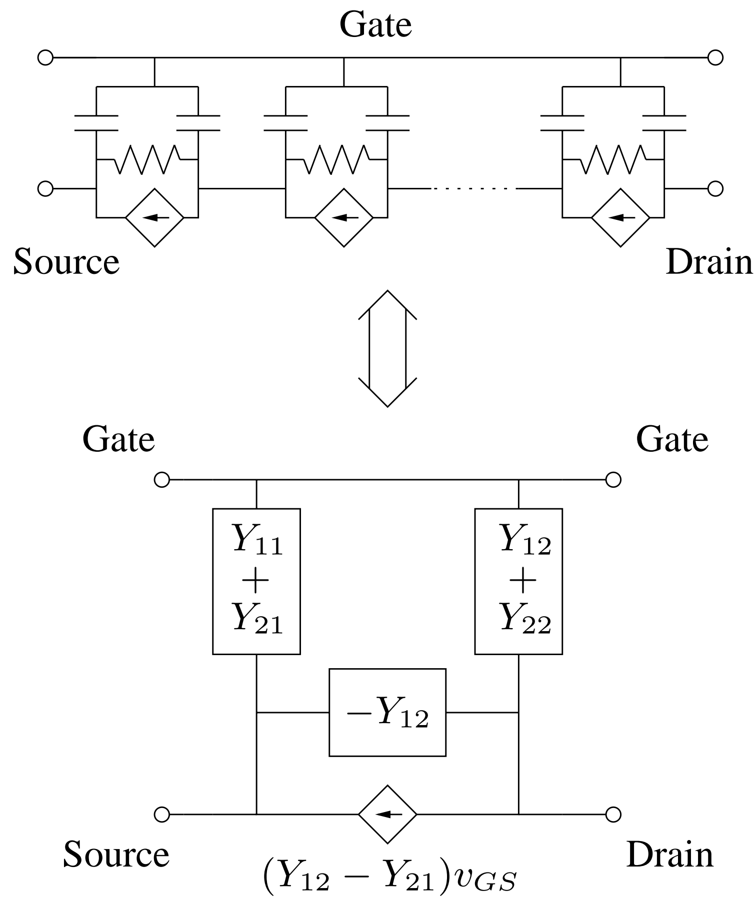


Figure 3.5: Small-signal equivalent representation for a MOSFET at high frequency in a common-gate configuration.

commonly used in SPICE, where the following parameters are applicable:

C_{gs} : The gate-to-source capacitance

C_{gd} : The gate-to-drain capacitance

r_o : The output resistance

g_m : The transconductance

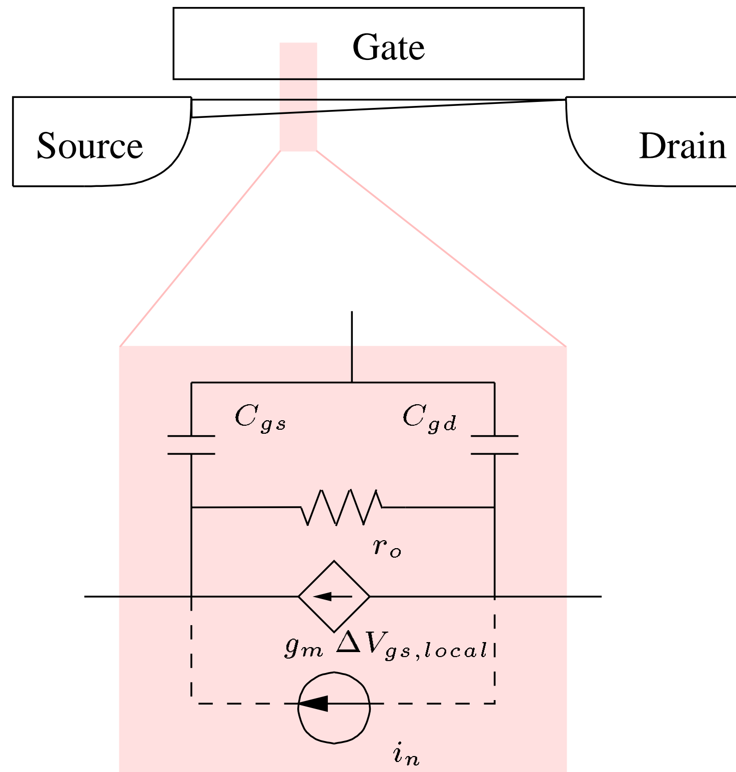


Figure 3.6: Local small-signal equivalent circuit for a segment of the MOSFET.

Then using a simple transformation[2] and subsequent matrix multiplications, the desired network parameters for the impedance field calculation are obtained.

3.1.4 Device Segmentation

An important issue to be considered is how dense the segmentation should be. Although the MOSFET is a nonuniform transmission line under actual operating conditions, a uniform

[2]See Appendix A.4.2 and Table A.1 for $ABCD$ parameters of a MOSFET segment and subsequent conversion of network parameters.

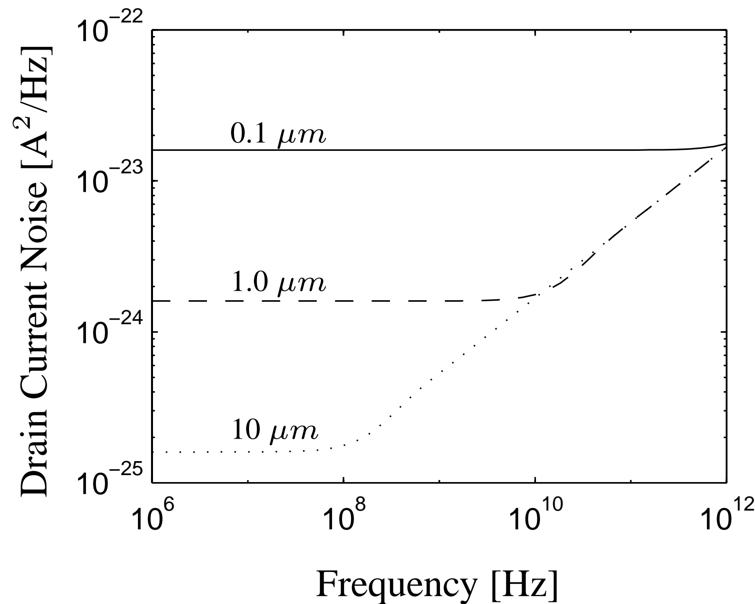


Figure 3.7: Frequency evolution of drain current noise spectral power density terms for a uniform transmission line.

transmission line analysis can provide a crude idea about the segmentation issue. The MOSFET can be considered as a uniform transmission line only under zero drain bias. In such a case, we can derive the noise characteristic for an *assumption-free unsegmented* transmission line.

Figures 3.7 and 3.8 show the calculated noise power spectra for an *unsegmented* uniform transmission line[3]. In contrast to common circuit design assumptions [13], at very high frequencies, the drain noise has frequency dependence and the gate noise is not proportional to the square of the frequency. Obviously the correlation between drain noise and gate noise will also differ across this frequency range. Nevertheless, this would not be important in most practical situations because these changes take place in a range far above

[3]See Appendix B.2 for the details of an unsegmented uniform transmission line.

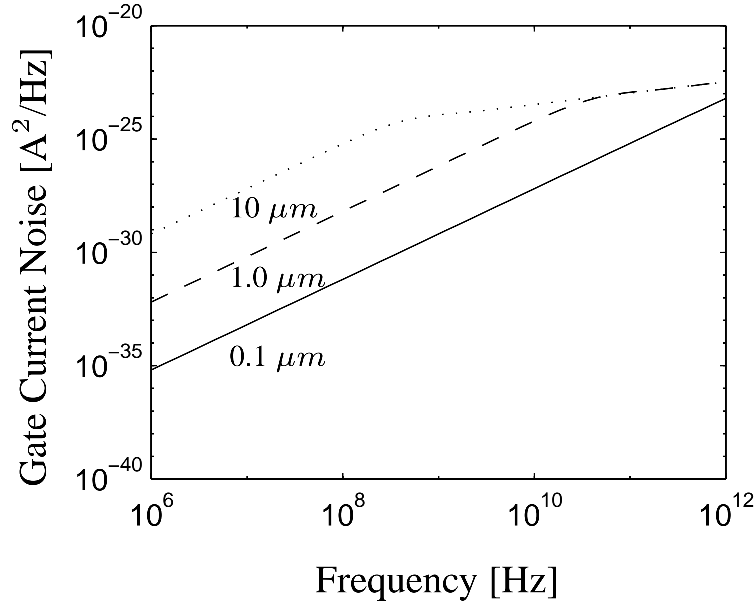


Figure 3.8: Frequency evolution of gate current noise spectral power density terms for a uniform transmission line.

the cutoff frequency (f_T).

To examine the segmentation limit, a segmented case has been compared with unsegmented results of Figures 3.7 and 3.8. Figures 3.9 and 3.10 respectively show the error in drain and gate noise calculation caused by segmentation for different sizes and frequencies. It is obvious that the smaller error is achieved by a denser segmentation and smaller ratio of the device length to the wavelength. For example, to maintain an error of less than 1 percent, $\frac{\Delta x L}{\lambda}$ should be less than $10^{-5}\mu$m, which corresponds to an upper frequency limit of 280 GHz for a 0.25 μm device that has been divided into 20 segments. If the numbers of segments are 4 and 10, the lower limits of error are 6.2 percent and 1.0 percent, respectively. Note that the number of segments imposes a lower limit on the error of gate noise calculation in Figure 3.10 due to the distributed nature of the device. By comparing these

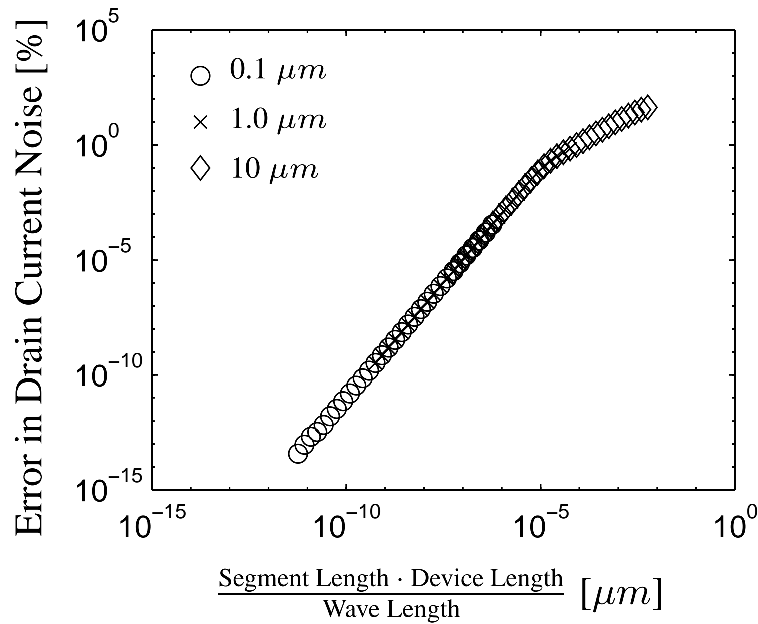


Figure 3.9: Drain current noise calculation error by segmentation for a uniform transmission line case. The MOSFETs are divided into 20 segments.

indices to the average meshing distance of device simulators and the cutoff frequency of the 0.25 μm MOSFET (about 30GHz in the actual operation region), we can conclude that the segmentation itself imposes practically no limits on modeling accuracy.

3.2 Noise Simulator Implementation

3.2.1 2-D Device Simulator

The proposed noise simulation method has been implemented as a post-processor for MEDICI [36], a commercial 2-D numerical device simulator. MEDICI works in conjunction with

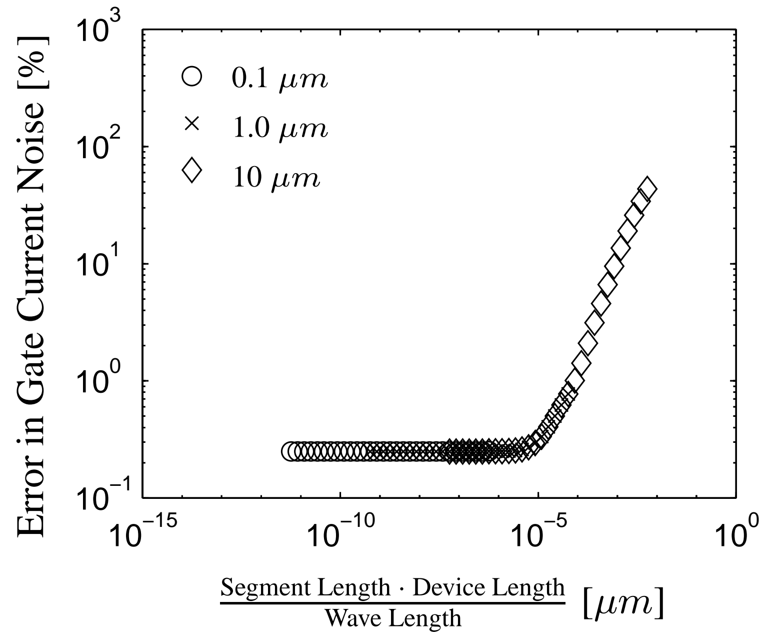


Figure 3.10: Gate current noise calculation error by segmentation for a uniform transmission line case. The MOSFETs are divided into 20 segments.

TSUPREM4 [37], a commercial 2-D numerical process simulator. Field-dependent mobility models [38], [39] are used in the device simulation. The simulator also provides self-consistent solutions of carrier density, mobility, and carrier temperature [4] based on carrier-temperature-dependent mobility and thermal diffusion current models as well as a carrier-temperature-based impact ionization model used for the HD model [40].

3.2.2 2-D to 1-D Transformation

The noise analysis of devices is based on ac sensitivity analysis. To take advantage of the 1-D transmission line analogy, we thus need to extract the 1-D ac equivalent circuit using

[4] A sample input deck is provided in Appendix C.

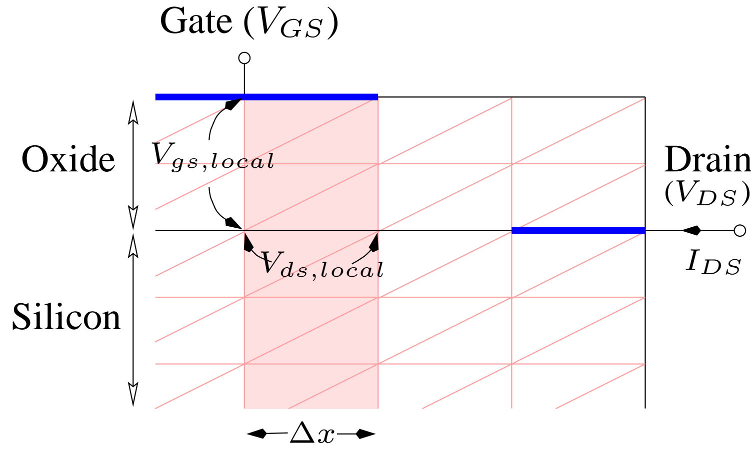


Figure 3.11: Illustration for local quantity extraction from a 2-D device simulation result.

2-D solutions. Assuming that the local small-signal parameters are frequency independent, the model emulates the ac behavior using local perturbations of dc quantities acquired from three bias conditions: the desired bias ([V_{DS},V_{GS}]) and two adjacent biases ([$V_{DS} + \Delta V_{DS}$,V_{GS}] and [V_{DS},$V_{GS} + \Delta V_{GS}$]). The same technique has been adopted in HELENA [41] and is known to be valid up to $2f_T$, which sets the applicable frequency limit of the proposed mixed approach.

The small-signal parameters associated with Figure 3.5 are deduced as follows:

$$C_{gs} + C_{gd} = \frac{\Delta Q_{inv}}{\Delta V_{gs,local}} \tag{3.8}$$

$$r_o = \frac{\Delta V_{ds,local}}{\Delta I_{DS}} \tag{3.9}$$

$$g_m = \frac{\Delta I_{DS}}{\Delta V_{gs,local}} \tag{3.10}$$

where Δ denotes a differential quantity for different sets of bias, Q_{inv} is the sum of inversion charge in the channel, $V_{gs,local}$ is the difference between the gate electrode potential

and the local source potential, $V_{ds,local}$ is the potential difference between the local drain potential and source potential, and I_{DS} is the current at the drain electrode. Note that changing V_{DS} affects not only $V_{ds,local}$ but also $V_{gs,local}$ and vice versa.

Figure 3.11 illustrates how local quantities are determined. The local potential has been obtained from the nodal quasi-fermi level along the Si/SiO_2 interface; the inversion charge has been calculated by summing up the product of the nodal carrier density and its associated area along the y-direction. MEDICI uses the finite-box discretization method [42] with a triangular mesh structure. While MEDICI allows irregular triangular meshes, only right-angled ones were used in the implementation to simplify the summing procedure for the inversion charge. The extracted 1-D small-signal equivalent circuit has been verified by comparing terminal characteristics of the 2-D device — capacitance, transconductance, and output resistance — to the first-order terms of Y_{ij}s deduced for the entire MOSFET as shown in Figure 3.5.

3.2.3 Microscopic Noise Source Calculation

The local noise source has been approximated using the spreading diffusion coefficient. Since MEDICI implicitly assumes the Einstein relationship, the local noise spectrum can be obtained as follows:

$$S_{i_n} \approx 4\,k\,T_c \frac{q\,n\,\mu_{dc}\,A}{l} \tag{3.11}$$

$$\approx 4\,k\,T_c\,\frac{1}{R_{dc}} = 4\,k\,T_c\,\frac{I_{DS}}{V_{ds,local}} \tag{3.12}$$

where T_c is the carrier temperature, μ_{dc} is the dc mobility, A and l are the cross-sectional area and length of a device segment, and R_{dc} is the dc resistance of a segment. We have assumed that a segment is a homogeneous resistor with the carrier temperature set by the

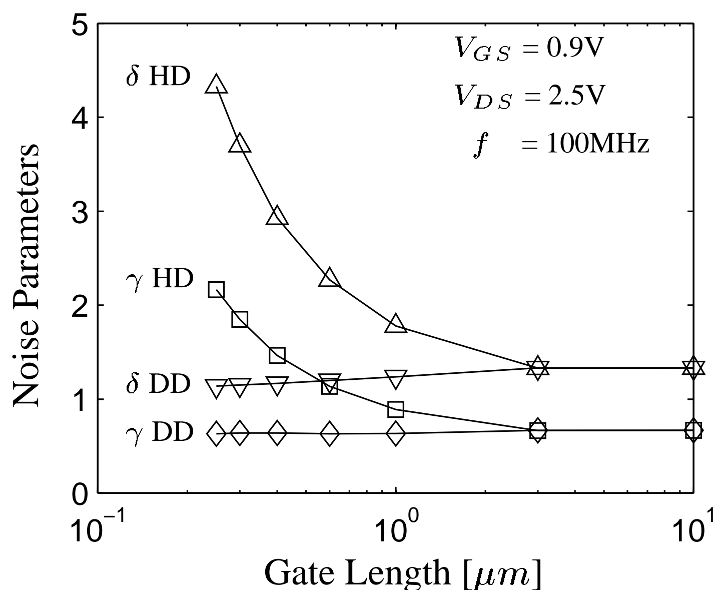


Figure 3.12: Gate length dependence of γ and δ comparing HD and DD model results.

Si/SiO$_2$ interface since the inversion layer is only tens of angstroms in thickness and its temperature distribution is almost homogeneous. For a piece of silicon, this approximation successfully predicts the reported field dependence of the diffusion coefficient [12]. For more precise simulations, D_n needs to be acquired through either Monte Carlo simulations [41] or experiments [12], as a function of the electric field or energy. Nevertheless, the above approximation causes a negligible error in the MOSFET noise calculation because, as will be discussed in Section 5.1, the actual contribution to the drain or gate noise is dominated by the source junction side, where D_n is about the same as D_s.

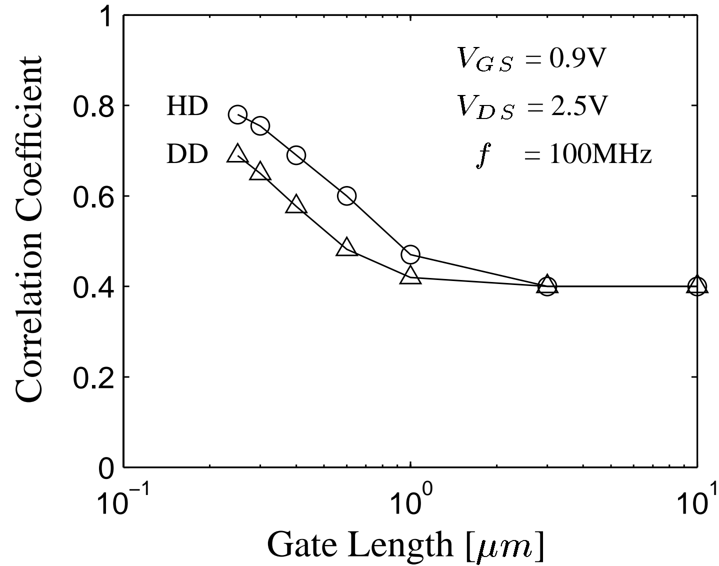


Figure 3.13: Gate length dependence of the imaginary part of c comparing HD and DD model results.

3.3 Simulation Results

We have performed noise simulations for nMOSFETs from an industrial 0.25 μm CMOS process. No optimization was done except for determining the doping profile calibration process. The structure and doping of the device were directly imported from TSUPREM4 and all model parameters were kept at the default values in the MEDICI simulator. Simulated dc characteristics showed good agreement with measured results for both the DD and HD transport models.

As shown in Figures 3.12 and 3.13, the long channel simulation results exhibit good agreement with the classical values[5], regardless of the transport model used in device simulation. As the channel length decreases, as shown in Figure 3.12, only the HD simulation

[5]See Section 2.1.2 for the classical van der Ziel model.

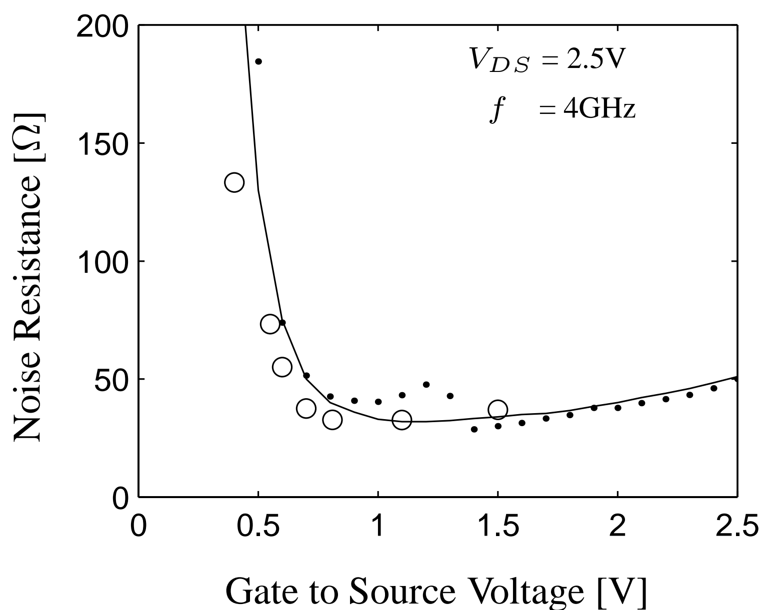


Figure 3.14: Comparison of de-embedded measurement data (circles) to the simulated equivalent noise resistance (dots) for a 0.25 μm nMOSFET. Solid lines refer to smoothed simulation results of the HD model.

results show an increase in γ and δ, similar to that which Jindal [16] and Abidi [15] have reported. Both models yield an increased correlation factor in Figure 3.13, which would in turn mitigate the impact of larger values of γ and δ on the noise figure. Some oscillatory behavior was observed in the bias dependence of the HD results and may be caused by the numerical stability problem related to the HD model implemented in MEDICI.

A 0.25 μm nMOSFET with W = 200 μm was measured using the ATN NP5B system [43] to examine the validity of the noise simulations. To compare the intrinsic part only, the pad loss [44] has been de-embedded by removing the parasitic components[6] of the noise correlation admittance matrix from that of the total matrix as proposed by Morifuji *et al.*

[6]More detailed deembedding issues are discussed in Chapter 4.

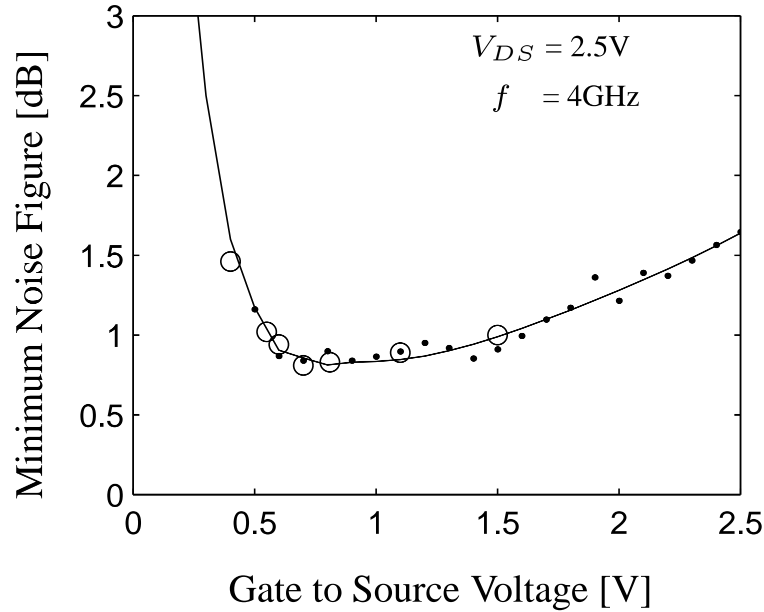


Figure 3.15: Gate bias dependence comparison of de-embedded measurement data (circles) to simulated minimum noise figures (dots) with correction for the loss due to G_{opt} for a 0.25 μm nMOSFET. Solid lines refer to smoothed simulation results of HD model.

[45]. The distributed resistance of the MOSFET gate electrode [46] has been neglected because it was silicided and divided into 5 μm-width-fingers during layout. Finally the simulation results are transformed[7] into four noise parameters from the noise power spectral density and their cross-correlation coefficient based on the equivalent circuit in Figure 3.5. The transformed intrinsic data for the DD model largely underestimates the noise performance, achieving less than half that of HD model in terms of F_{min} and R_n. The HD case also shows some discrepancy in F_{min} and Y_{opt}, while R_n is in good agreement [47] as shown in Figure 3.14. Since Y_{opt} is mainly determined by the small signal equivalent

[7]See Appendix A.3.3 and A.4.3 for the transformation.

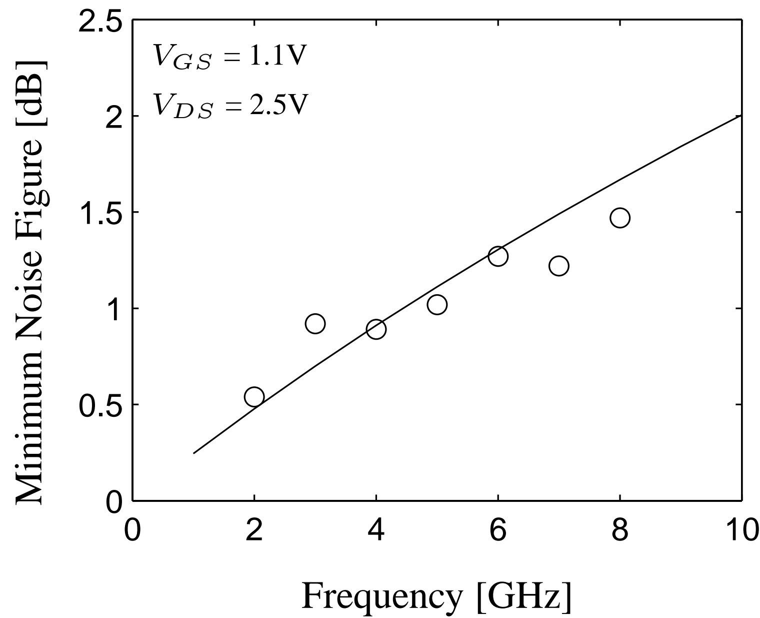


Figure 3.16: Frequency dependence comparison of de-embedded measurement data (circles) to simulated minimum noise figures (dots) with correction for the loss due to G_{opt} for a 0.25 μm nMOSFET. Solid lines refer to smoothed simulation results of HD model.

circuit of the MOSFET, which is verified using the current and capacitance of the device, a large discrepancy in Y_{opt} implies that the de-embedding procedure was not satisfactory. In Figures 3.15 and 3.16, an artificial increase in G_{opt} by a factor of 1.7 is used in the transformation to fit model results with the measured G_{opt}; excellent agreement of F_{min} is then observed in both bias and frequency dependencies. The accuracy of intrinsic noise simulation is thus clearly satisfactory and it is possible to estimate circuit level noise performance, based on technology parameters contained in the simulation model.

3.4 Summary

An accurate and computationally efficient simulation technique for high frequency noise performance of deep submicron MOSFETs is proposed. This technique is based on an active transmission line concept but uses 2-D device simulation. The Langevin stochastic source term is introduced as a local noise source and the small-signal behavior of the MOSFET is represented by a cascaded two-port network, characterized in a common gate configuration. Since the local static quantities required for noise calculation are imported from a 2-D numerical device simulator using advanced transport models, this technique is able to capture dispersive non-equilibrium effects and incorporate second-order effects caused by complex processing. Background of the proposed approach includes details of the impedance field formulation. Segmentation itself does not cause significant error in the noise calculations within a practical range of frequencies and meshing distances. The long channel noise simulation results are in good agreement with classical values; short channel results based on the HD model successfully describe the reported excess noise in short channel MOSFETs. The transformed simulation results of the HD model show excellent agreement with the de-embedded measurement data, both in bias and frequency dependencies, while the DD model largely underestimates the experimental results. This chapter demonstrates and explains the importance of advanced (i.e. HD) transport models for 2-D noise analysis and also verifies the use of the model, based on noise simulation results for deep submicron MOSFETs. The proposed simulation technique is accurate and fast enough for practical RF noise performance analysis of deep submicron MOSFETs.

Chapter 4

Parasitic Noise Components

COMPLETE BROADBAND CHARACTERIZATION is indispensable for accurate modeling as well as future RF circuit designs. In measurements of intrinsic noise, the de-embedding procedure is critical since the measured noise parameters are influenced significantly by parasitic components, such as distributed resistance of each of the electrodes and other resistive terms. This chapter discusses parasitic noise sources in MOSFETs and their implications on intrinsic noise characterization.

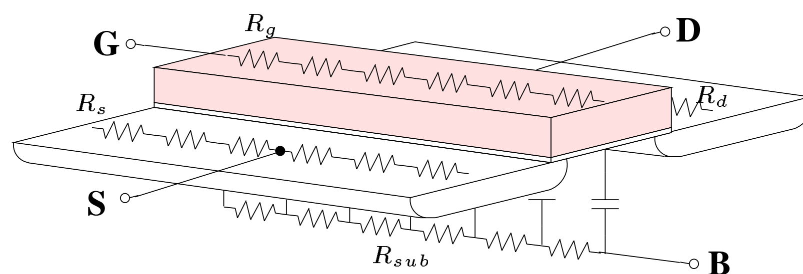


Figure 4.1: Parasitic resistance generating thermal noise in MOSFETs.

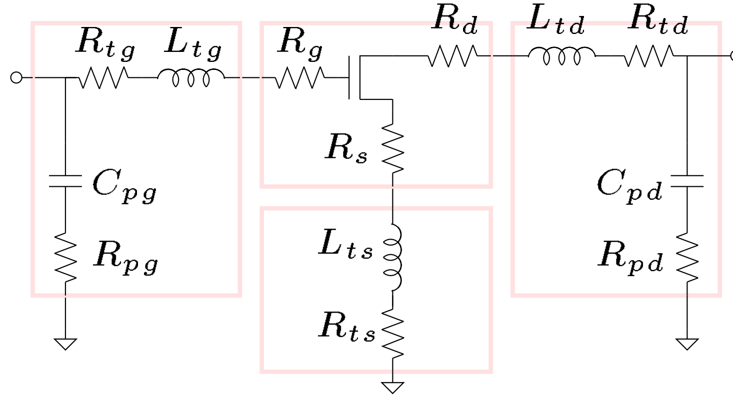


Figure 4.2: Equivalent circuit model of the DUT for de-embedding.

4.1 Deembedding

Most parasitic contributions can be deembedded based on two port theory explained in Appendix A [44], [2]. The equivalent circuit of the DUT is illustrated in Figure 4.2. While most de-embedding studies adopt an equivalent circuit for the intrinsic MOSFET too, it is more appropriate that the MOSFET be left as a blackbox because an accurate modeling of the intrinsic device behavior is not trivial and it can directly contribute errors in intrinsic noise power extraction. Depending on the extraction method of parasitic elements, the de-embedding of R_g, R_d, and R_s can be done either together with or separately from the de-embedding of other parasitics:C_{pg}, R_{pg}, R_{tg}, L_{tg}, R_{ts}, L_{ts}, C_{pd}, R_{pd}, R_{td}, and L_{td}. However, the basic principles are the same.

First, the DUT consists of three cascading stages: gate parasitics (stage-1), intrinsic plus source parasitics (stage-2), and drain parasitics (stage-3). The impedance matrices of

gate and drain parasitics are:

$$\overrightarrow{Z}_G = \begin{bmatrix} Z_{pg} & Z_{pg} \\ \\ Z_{pg} & Z_{pg} + Z_{tg} \end{bmatrix} \quad (4.1)$$

$$\overrightarrow{Z}_D = \begin{bmatrix} Z_{pd} + Z_{td} & Z_{pd} \\ \\ Z_{pd} & Z_{pd} \end{bmatrix} \quad (4.2)$$

where

$$Z_{pg} = R_{pg} + 1/(j\omega C_{pg}) \quad (4.3)$$

$$Z_{tg} = R_g + R_{tg} + j\omega L_{tg} \quad (4.4)$$

$$Z_{pd} = R_{pd} + 1/(j\omega C_{pd}) \quad (4.5)$$

$$Z_{td} = R_d + R_{td} + j\omega L_{td} \quad (4.6)$$

The corresponding noise matrices ($\overrightarrow{C}_{Z_G}$ and $\overrightarrow{C}_{Z_D}$) are easily calculated and then transformed into ABCD representation ($\overrightarrow{C}_{A_G}$ and $\overrightarrow{C}_{A_D}$) using Equation (A.14). Since the measured four noise parameters give the noise matrix of the DUT ($\overrightarrow{C}_{A_{DUT}}$), the noise matrix for stage 2 is:

$$\begin{aligned} \overrightarrow{C}_{A_{MS}} = {} & \overrightarrow{A}_G^{-1}[\overrightarrow{C}_{A_{DUT}} - \overrightarrow{C}_{A_G}](\overrightarrow{A}_G^{\dagger})^{-1} \\ & -\overrightarrow{A}_{MS}\overrightarrow{C}_{A_D}\overrightarrow{A}_{MS}^{\dagger} \end{aligned} \quad (4.7)$$

Stage-2 is a series connection of two parts: the intrinsic MOSFET and source parasitics.

The impedance matrix of source parasitics is:

$$\overrightarrow{Z}_S = \begin{bmatrix} Z_{ts} & Z_{ts} \\ \\ Z_{ts} & Z_{ts} \end{bmatrix} \quad (4.8)$$

$$Z_{ts} = R_s + R_{ts} + j\omega L_{ts} \quad (4.9)$$

Then the noise matrix of the intrinsic MOSFET is simply:

$$\overrightarrow{C}_{Z_M} = \overrightarrow{C}_{Z_{MS}} - \overrightarrow{C}_{Z_S} \quad (4.10)$$

A direct transformation of $\overrightarrow{C}_{Z_M}$ to the admittance representation yields the self- and cross-power spectral densities of drain and gate noise.

$$\overline{i_g^2} = 2\Delta f \overrightarrow{C}_{Y_M}(1,1) \quad (4.11)$$

$$\overline{i_g i_d^*} = 2\Delta f \overrightarrow{C}_{Y_M}(1,2) \quad (4.12)$$

$$\overline{i_d^2} = 2\Delta f \overrightarrow{C}_{Y_M}(2,2) \quad (4.13)$$

4.2 DUT Implications

4.2.1 Bonding Pad

The ac current path from the bonding pad, via the conductive substrate to ground, causes a significant influence on measured F_{min}, especially for bulk silicon technologies [44], [45]. To minimize this component, several techniques can be employed such as making the input pad smaller, using a semi-insulating substrate, and using a substrate with extremely low resistivity. The most effective solution is to replace the bottom plate of the pad capacitor

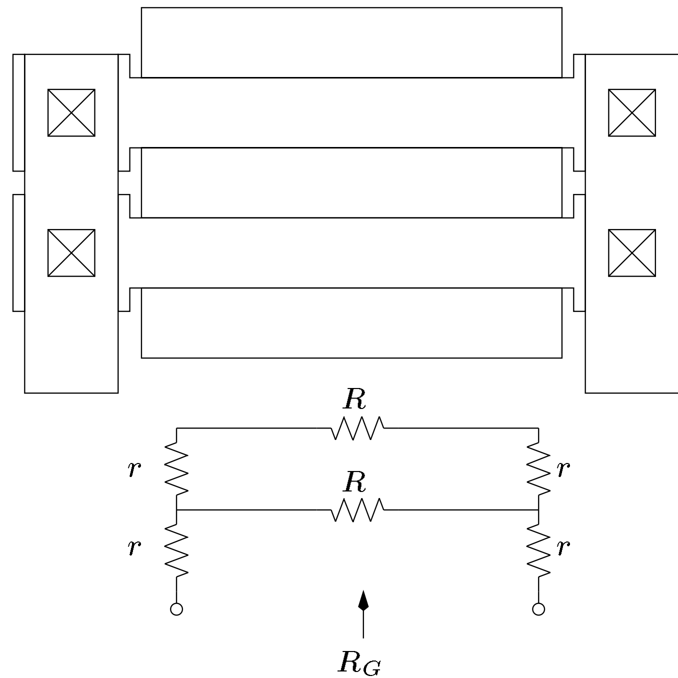


Figure 4.3: Calculation of distributed resistance for a MOSFET with a multi-fingered gate structure.

with a grounded metal layer. The additional capacitance caused by this method can be deembedded easily and also can be utilized in LNA design[1].

4.2.2 Gate Poly Resistance

In modern MOSFET technologies, the gate electrode is made of polysilicon. Since its resistivity is relatively high, the noise contribution often exceeds the channel noise. Due to

[1]Discussed in Section 7.2.5.

the distributed effect, the equivalent resistance of the gate electrode is given by:

$$R_G \approx \frac{K R_\square W}{n^2 L} \tag{4.14}$$

where $R_\square$ is the sheet resistance of the gate material, W is the total gate width of the device, L is the gate length, and n is the number of gate fingers. The factor K is 1/3 when each gate finger is contacted only at one end, and reduces to 1/12 by contacting at both ends [13]. Thus this contribution can be reduced by lowering the resistivity of the gate and interdigitating the gate electrodes.

In state-of-the-art MOSFET technologies, owing to the use of silicided gates, $R_\square$ is improved by a factor of 10 compared with the pure polysilicon process. Nevertheless, the noise contribution is substantial in MOSFETs with gate length below 0.23μm [48]. Figure 4.3 illustrates a MOSFET with interdigitated gates contacting at both ends. The equivalent resistance is given by:

$$R_G = \frac{1}{12}\left[\left(2n + 3 + \frac{1}{n}\right)r + \frac{1}{n}R\right] \tag{4.15}$$

$$\approx \frac{n}{4}r + \frac{1}{12n}R \tag{4.16}$$

where $R = \frac{R_\square W}{nL}$ is the resistance of a gate finger and r is interconnect resistance, which is usually routed in a metal layer that has significantly lower sheet resistance than polysilicon [46]. Since R_G directly adds to noise resistance[2] R_n, ideally $R_G \ll R_n$ must be satisfied. In other words,

$$4kTR_G\, g_m^2 \ll 4kTg_{d0}\gamma \tag{4.17}$$

[2] $R_n \triangleq \frac{S_{i_d}}{4kT|Y_{21}|^2}$. See Section 2.6 for details.

is desirable. Hence a rough rule of thumb is:

$$R_G\, g_m \ll 1 \tag{4.18}$$

$$n \gg \sqrt{\frac{R_\Box\, W^2\, v_{sat}\, C_{ox}}{24\, L}} \tag{4.19}$$

4.3 Substrate Induced Drain Current Noise

It is known that short channel MOSFETs yield larger drain current noise (S_{i_d}) [15], [16], [17], [18], [19], [49], [50] than the value predicted by the van der Ziel model [11], which agrees with long channel MOSFETs. However, the amount of the increase is still controversial. Some studies have demonstrated a substantial increase while other studies have claimed less than a factor of two increase for 0.17μm MOSFETs [18], [19].

According to common circuit design assumptions, the drain current noise is white (i.e. frequency independent). In many experimental studies, however, the measured noise resistance that directly represents the drain current noise in MOSFETs, has shown a frequency dependence in the GHz frequency range [45], [51], [52], [53]. Since this phenomenon cannot be explained by any frequency dependence of Y_{21}, it has been totally ignored or attributed to measurement errors [53]. However, R_n is not prone to errors; moreover it shows excellent linearity with a logarithmic frequency dependence. A device level noise simulation study has qualitatively demonstrated that such a frequency dependence can be attributed to the substrate resistance [31] but the physical mechanism has not been identified.

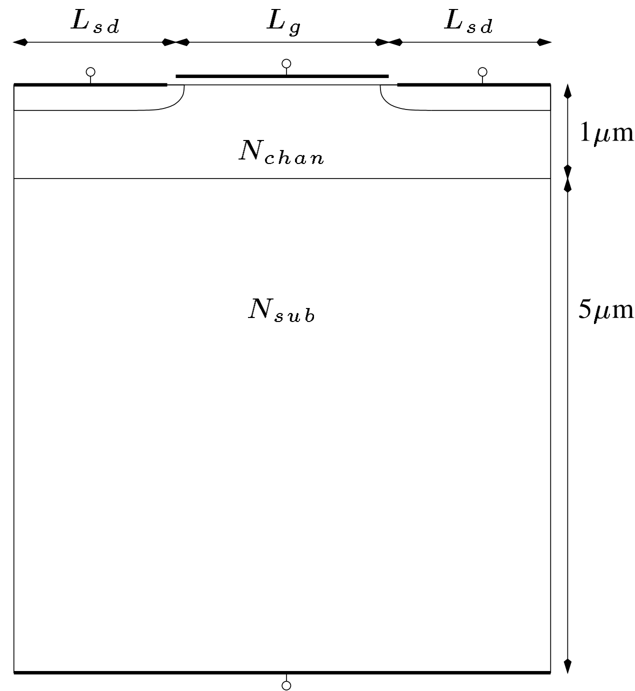


Figure 4.4: Cross-section of the MOSFET structure used for simulation.

4.3.1 Noise Simulation

The physical origin of the frequency dependence for drain current noise has been investigated using PADRE, a general-purpose multi-dimensional device simulator, in which the IFM (Impedance Field Method) [26] is implemented [31],[54],[55]. Since the primary interest in the present work focuses on the substrate induced thermal noise, the drift-diffusion model is used and other noise sources, such as $1/f$ noise and generation-recombination noise, are ignored. The MOSFET structure used for noise simulation is illustrated in Figure 4.4. This structure, while quite simple, still provides useful analysis results and physical insight. To minimize secondary effects, the junction length (L_{sd}) is reduced and the bulk contact is located at the bottom through a low-doping substrate.

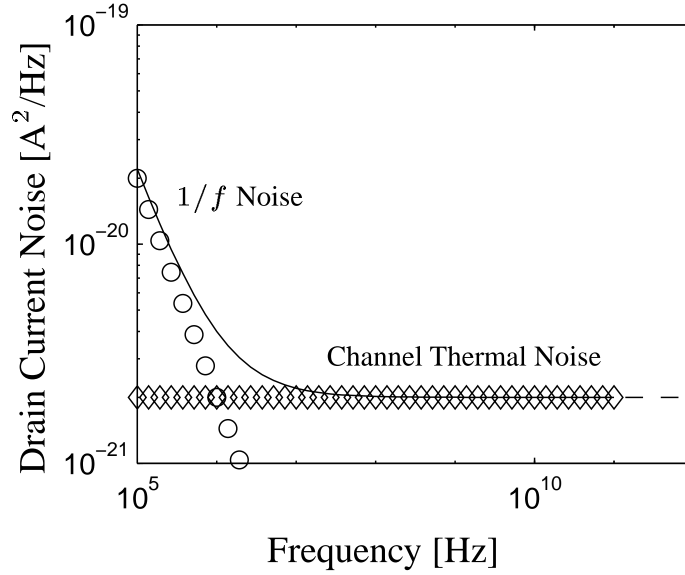


Figure 4.5: Commonly assumed drain current noise power spectrum for MOSFETs.

4.3.2 Noise Contribution Model

It has been a common assumption that the drain current noise only exhibits $1/f$ noise ($S_{i_d,1/f}$) and white channel thermal noise ($S_{i_d,channel}$) contributions as illustrated in Figure 4.5. They correspond to regions I and III in Figure 4.6, respectively. Although local noise sources generate white noise up to the quantum limit, as frequency becomes much higher than the cutoff frequency, the capacitive coupling between the channel and gate makes propagation of local fluctuations stronger, consequently channel thermal noise increases as shown in region IV in Figure 4.6 [32],[56].

In addition, spreading resistance (R_{sub}) of the substrate generates thermal fluctuations given by:

$$S_{v_{sub}} = 4kTR_{sub} \tag{4.20}$$

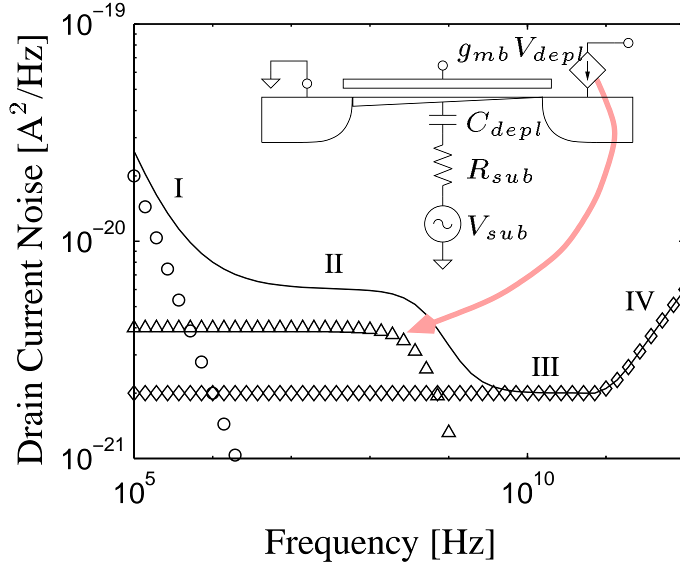


Figure 4.6: Anticipated general drain current noise power spectrum for bulk MOSFETs. The solid line is total noise power, the circle symbol is the $1/f$ noise component ($S_{i_d,1/f}$), the triangle symbol is the additive component induced by the substrate ($S_{i_d,sub}$), and the diamond symbol is the channel thermal noise component ($S_{i_d,channel}$). The inset circuit diagram explains the contribution mechanism of the substrate thermal noise to the drain current noise.

where k is Boltzmann's constant and T is the lattice temperature [57]. These fluctuations in the substrate potential modulate the channel charge of the depletion capacitor (C_{depl}) and subsequently produce additive channel noise ($S_{i_d,sub}$), amplified by substrate transconductance (g_{mb}). Since the $R_{sub}C_{depl}$ network in Figure 4.6 acts as a low-pass filter, the amount of additive channel noise is given by

$$S_{i_d,sub} = \frac{4kTR_{sub}g_{mb}^2}{1+(\omega R_{sub}C_{depl})^2} \tag{4.21}$$

This equation suggests that $S_{i_d,sub}$ has a low frequency noise plateau ($4kTR_{sub}g_{mb}^2$) dominating region II in Figure 4.6 and a pole at $f = (2\pi R_{sub}C_{depl})^{-1}$. Thus $S_{i_d,sub}$ effectively increases the drain current noise factor γ.

This phenomenon was first discussed by Jindal [57], but only the low frequency noise plateau was considered. In the case of SOI MOSFETs, the partially-depleted body leads to large R_{sub} and subsequently produces a component with a higher plateau and much lower pole location than for bulk MOSFETs. Faccio *et al.* have modeled this effect by introducing a parallel shunting capacitor, which is the sum of the capacitances of the front gate oxide (C_{ox}) and buried oxide (C_{BOx}) [58]. For bulk MOSFETs, using similar physical reasoning, Kishore *et al.* have explained the phenomenon by adding an RC network between the gate and substrate [52]. However, the channel charge shields the substrate network from the gate electrode under strong inversion conditions [59]. Therefore C_{ox} must be replaced with C_{depl}.

4.3.3 Simulation Results

In Figures 4.7 and 4.8, the noise spectra are reproduced by including the additive component, calculated based on Equation (4.21), to the simulation results for MOSFETs with a highly doped substrate ($N_{sub} = N_{chan}$). The calculated spectra fit the low frequency noise plateau and pole location, introducing less than 30% error, with C_{depl}-R_{sub}-g_{mb} values extracted from ac and dc simulation results of PADRE. R_{sub} is extracted from a structure without junctions and gate oxide; C_{depl} is approximately equal to $C_{db} + C_{sb}$ if the junction area becomes negligibly small. It is important to note that $S_{v_{sub}}$ indirectly contributes to S_{i_d} via the channel depletion capacitor. Due to the bias dependence of g_{mb}, $S_{i_d,sub}$ is zero under zero drain bias, increases as drain bias increases, and finally saturates for higher drain bias, as shown in Figure 4.7. It also largely increases the drain noise factor at low gate bias

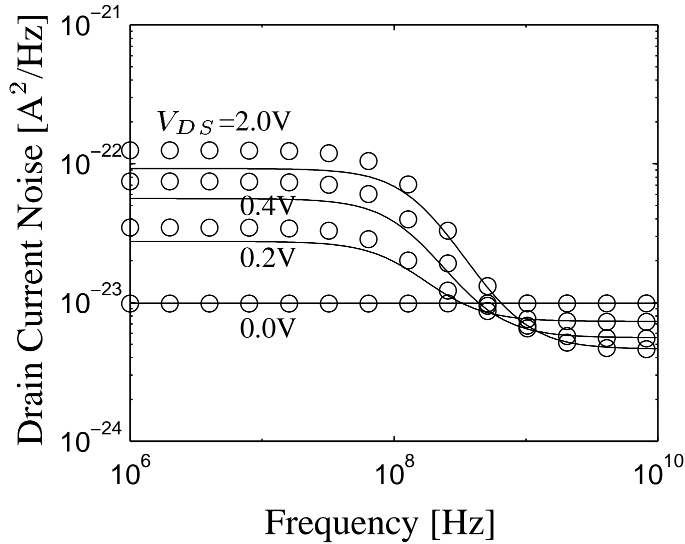


Figure 4.7: Simulation results of drain current noise power spectrum of a 0.5μm MOSFET for different drain bias conditions. The gate oxide thickness is 60nm, N_{chan} is 5.0$\times10^{17}$cm^{-3}, N_{sub} is 1.0$\times10^{15}$cm^{-3}, L_{sd} is 0.01μm, and V_{GS} is 1.5V. The symbols are PADRE simulation results and lines are calculated using Equation (4.21).

conditions. Moreover $S_{i_d,sub}$ becomes more significant as the channel length decreases in Figure 4.8 since $S_{i_d,sub}$ is proportional to g_{mb}^2 while $S_{i_d,channel}$ is proportional to g_m. Interestingly, these tendencies conform with the reported description of excess drain current noise in short channel MOSFETs [15], [16], [17], [49].

It is worth mentioning that those studies reporting a substantial increase of the drain noise factor have collected data at frequencies below 100MHz due to the bandwidth limits of the transimpedance amplifier. Moreover the samples used relatively primitive technologies, that employ only shallow threshold adjustment doping on a highly resistive substrate.

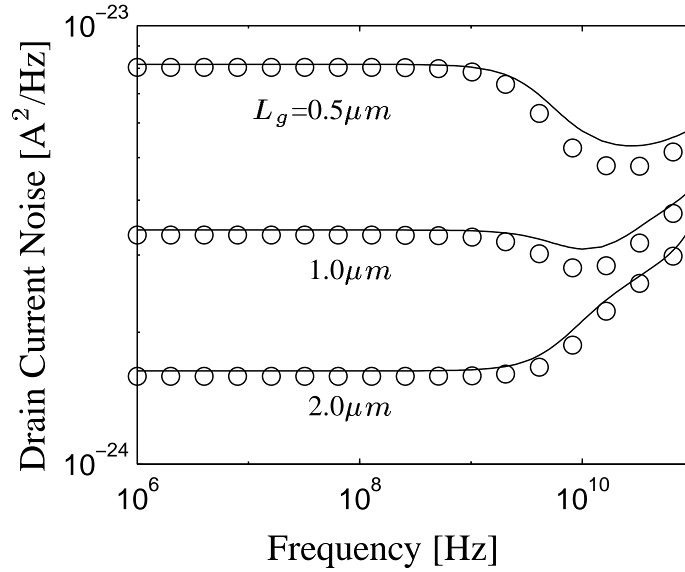


Figure 4.8: Simulation results of drain current noise power spectrum for MOSFETs with different gate lengths. The gate oxide thickness is 60nm, N_{chan} is 5.0×10^{17}cm^{-3}, N_{sub} is 3.2×10^{16}cm^{-3}, L_{sd} is 0.01μm, V_{GS} is 1.5V, and V_{DS} is 2.5V. The symbols are PADRE simulation results and lines are calculated using Equation (4.21).

Therefore, it is now suggested that the amount of channel thermal noise has been exaggerated due to the additive thermal noise contribution from the substrate. Thus to characterize the pure channel thermal noise, data needs to be obtained either in region III or from MOSFETs with a highly doped substrate.

As the transition between regions II and III approaches the GHz range in modern bulk CMOS technologies, modeling using a single RC lump may not be successful. Due to the three-dimensional distributed effect of the substrate network, illustrated in Figure 4.9, the actual $S_{i_d,sub}$ spectrum is the sum of multiple components with different poles; as shown in

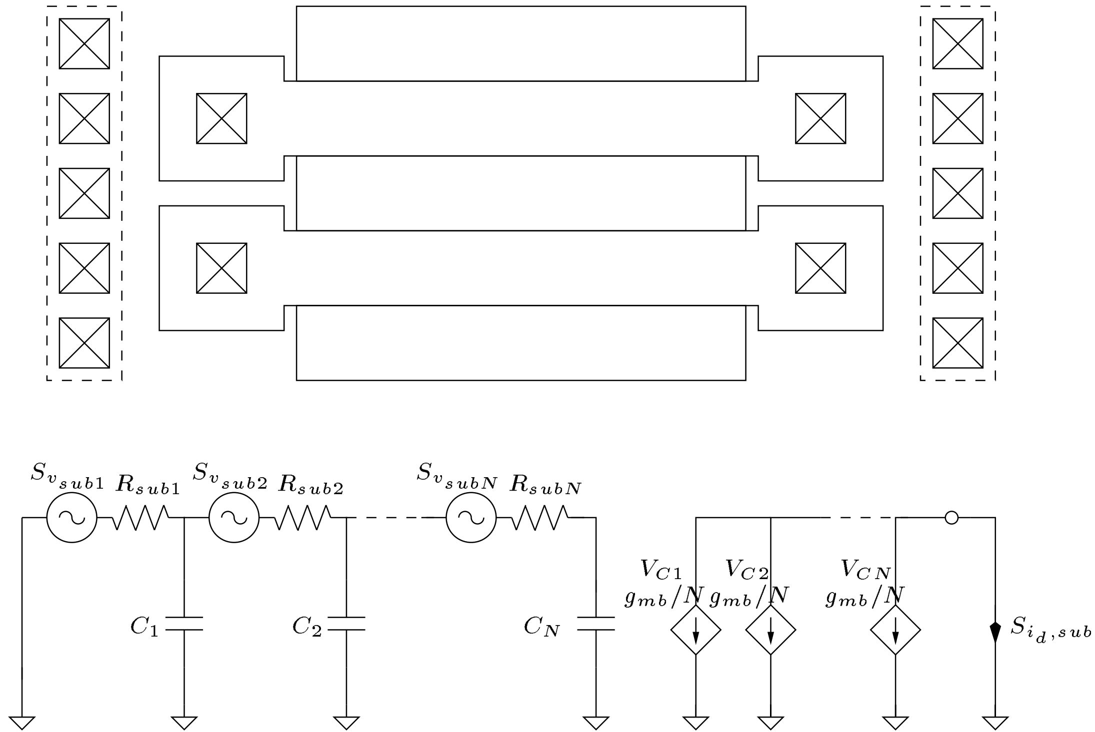


Figure 4.9: Distributed effect of the substrate network.

Figure 4.10, the slope of the transition is much smoother than -20dB/decade, typically below -5dB/decade. Thus prediction of the $S_{i_d,sub}$ characteristic poses an ongoing challenge; the use of three-dimensional noise simulations can be expected to provide additional data in support of new compact modeling.

4.4 Summary

This chapter discusses how parasitic noise sources in MOSFETs can be deembedded, what influences noise data significantly in DUTs, and how the substrate resistance increases channel thermal noise. The parasitic noise sources can be separated using two port theory.

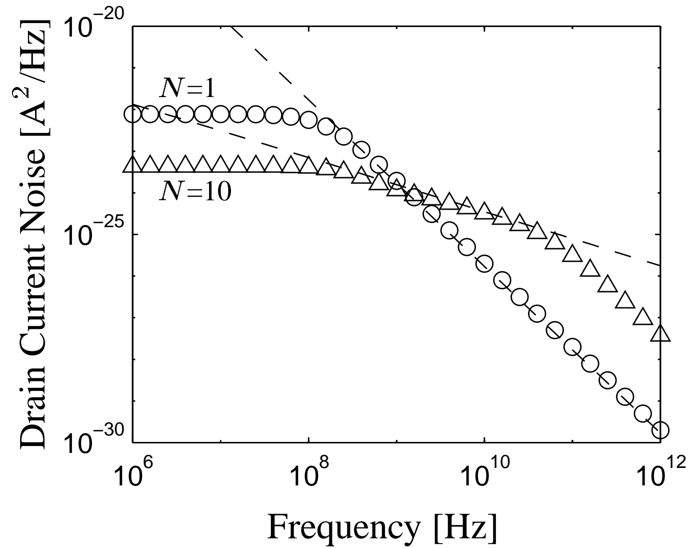


Figure 4.10: Drain current noise spectrum for different number of poles.

The most significant parasitic components are the bonding pad on a conductive substrate and distributed resistance of the gate poly. Both can be minimized by changing the process and optimizing the layout. Resistance of the substrate generates potential fluctuations that in turn produce additive channel noise by modulating the inversion charge via the channel depletion capacitor. For low-doped substrates, the additive noise may result in a frequency dependence of the drain current noise due to a pole associated with the R_{sub}-C_{depl} network. Since it conforms to the tendency of the reported excess noise, it may exaggerate the value being reported for the channel thermal noise factor. Hence, careful characterization is required to achieve accurate modeling. To minimize this component, the well doping profile needs to extend deep into the substrate.

Chapter 5

Excess Channel Noise

RECENT COMPACT MODELING APPROACHES have explained excess channel noise, observed in MOSFETs with channel lengths below 1.7μm [16],[17], [18],[19], using local *voltage* noise sources [18], [19],[49],[50]. However, the use of local voltage noise sources in device modeling suffers from the spatial correlation of the noise sources [60], [61]. This results in a dominant noise contribution near the drain junction, which is more significant when hot carrier effects are included [19], [49],[50]. By contrast, quasi-2D numerical simulation results for HEMT devices have revealed that the drain noise of the FET is not in fact dominated by the drain-side but rather by the source-side contributions [62]. Numerical noise simulation results in Figure 3.12 have qualitatively demonstrated the observed excess thermal noise in 0.25μm MOSFETs based on the Hydrodynamic (HD) formulation [47],[56],[63]. This chapter investigates the physical origin of the excess noise by comparing the differences between local and non-local carrier transport models in noise simulation.

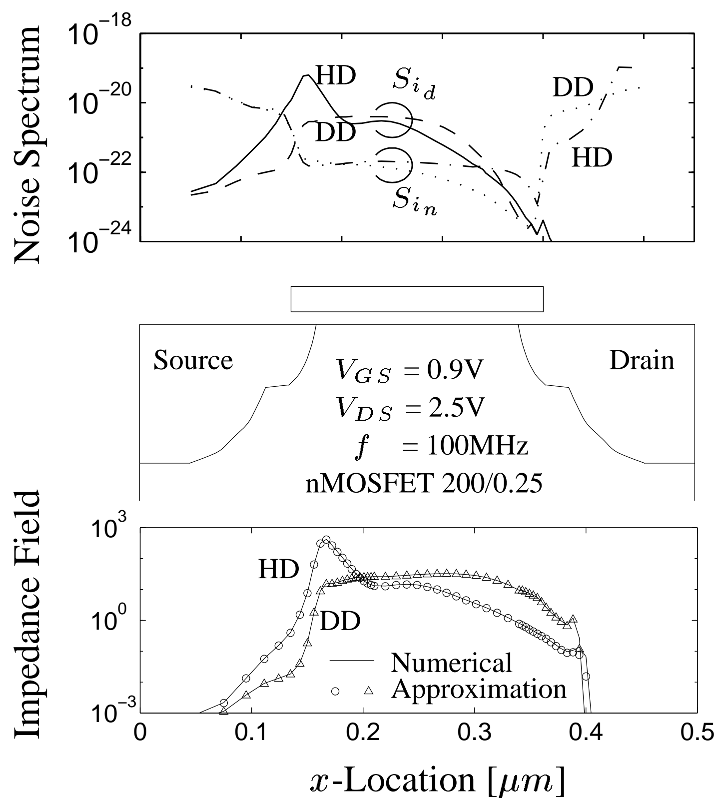


Figure 5.1: Comparing the HD model with the DD model along the channel for noise spectral density distribution of the local noise source (S_{i_n} [A^2/Hzμm]) and its actual contribution to the drain noise (S_{i_d} [A^2/Hzμm]); and the impedance field ($|\Delta A_d|^2$ [no unit]).

5.1 Physical Origin

Excess noise is defined as deviation from the van der Ziel model [1] [11]. As emphasized in Figure 3.12, for decreasing channel length, the *non-local* HD formulation shows a significant deviation from the long channel value of γ whereas the purely *local* Drift-Diffusion

[1]See Section 2.1.2.

(DD) model remains constant. The spatial distribution of S_{i_d} in Figure 5.1 shows clearly that the excess noise in the HD results originates due to a peak at the metallurgical source junction. In the framework of the *impedance field* representation [26],[32],[56], device noise at the electrodes is determined by two independent factors: local fluctuations and their propagation to the terminal electrodes. Given noise sources (S_{i_n}) representing local fluctuations and the impedance field (ΔA_d) representing the propagation, current noise power at the drain electrode is:

$$S_{i_d} \;=\; |\Delta A_d|^2 \, S_{i_n} \tag{5.1}$$

The fact that the two models yield almost the same values of S_{i_n} in the location near the source in Figure 5.1, implies that the impedance field (ΔA_d) differentiates the effects between the two models on noise simulation. The impedance fields, shown in the bottom of Figure 5.1, reveal significant differences between the HD and DD models across the entire device channel. The impedance field is numerically calculated based on network analysis principles, but it can be conceptually explained by cascading three sub-MOSFETs : $M_S(0, x)$, $M_C(x, x + \Delta x)$, and $M_D(x + \Delta x, L)$. Nodal analysis yields the following simplified approximation (symbols in Figure 5.1):

$$\Delta A_d \;\approx\; \frac{r_{o_C} g_{m_D}}{1 + r_{o_S} g_{m_D}} \;\approx\; r_{o_C} g_{m_D} \tag{5.2}$$

The given equation is basically a closed-loop gain of a feedback system and the parameterization in Equation (5.2) suggests that the local ac resistance (r_{o_C}) is primarily responsible for the source side peak of the impedance field; additionally, the impact of r_{o_C} is amplified by g_{m_D} as the device length becomes smaller. Figure 5.2 shows that the

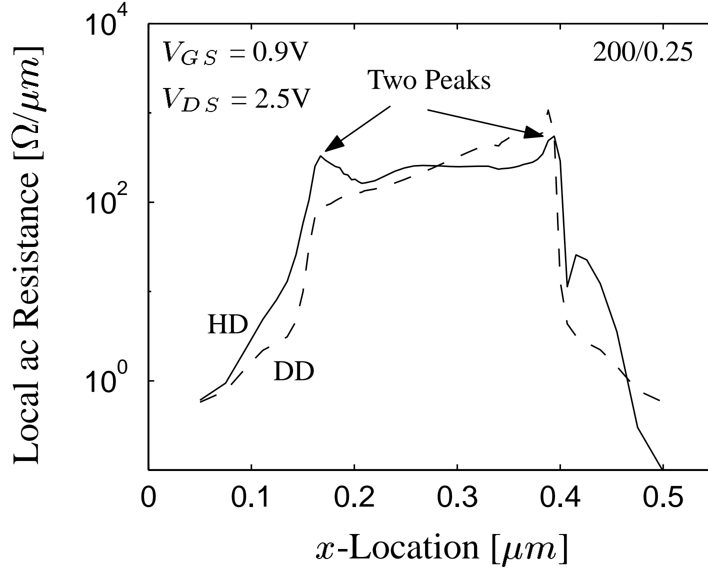


Figure 5.2: Local ac resistance distribution, comparing the HD model (solid line) with the DD model (dashed line).

HD results exhibit two peaks in the ac resistance distribution, localized at the metallurgical junctions. For any segment within the semiconductor, higher ac resistance directly represents a smaller derivative of the velocity with respect to field ($\frac{\partial v}{\partial \mathcal{E}}$) because

$$R_{ac} = -\frac{\partial \mathcal{E}}{qn\partial v}\frac{l}{A} \tag{5.3}$$

Unfortunately, the direct measurement of $\frac{\partial v}{\partial \mathcal{E}}$ is difficult since the electric field changes near the source junction are extremely small and vary two dimensionally with drain bias.

Suppose an electric field is applied and then removed as illustrated in Figure 5.3. In terms of physical effects, as reflected by the DD model, the carrier velocity instantaneously follows the electric field change. The DD model assumes that carrier velocity is directly

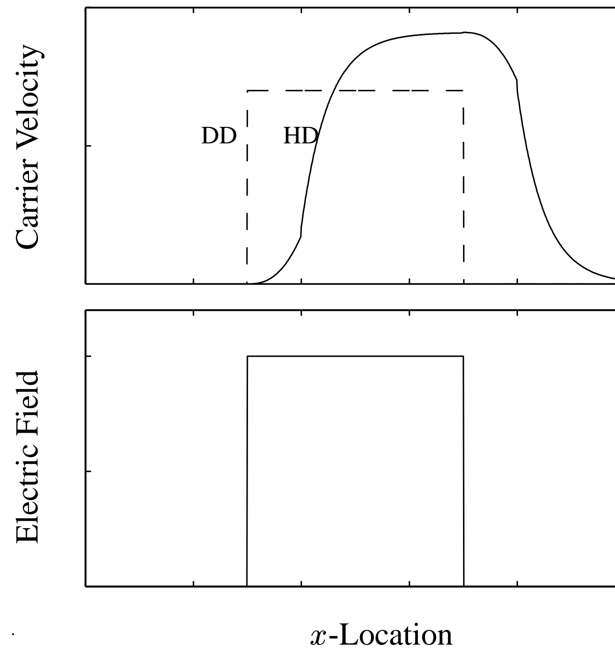


Figure 5.3: Carrier response to the electric field changes.

determined by the electric field. In reality, carriers need a certain amount of time to accelerate and to decelerate due to inertia; thus the carrier velocity has latency in response to the electric field change, as shown in Figure 5.3. This phenomenon is referred to as the *non-local* effect and is primarily reflected in higher order transport models [64] such as the HD formulation, in which latency is modeled by a parameter called *carrier relaxation time*. A good analogy is a heavy car with a weak engine: the carrier is a car, the electric field is an accelerator, and the carrier velocity is speed. A car experiences latency as it goes from an initial start through exit or as it goes into highway ramps as illustrated in Figure 5.4. Likewise, the electric field variation near the source junction is quite small; the HD model

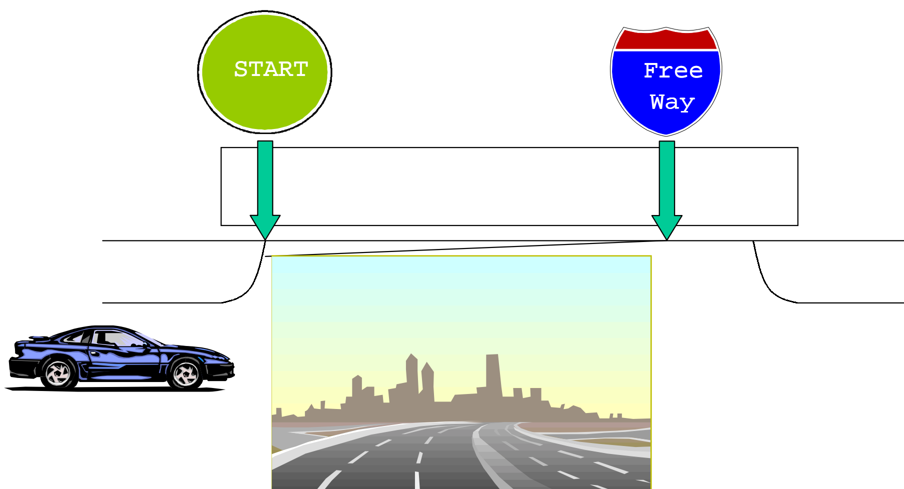


Figure 5.4: Car analogy to explain the carrier transport in the channel.

gives almost the same value of velocity as can be extracted based on the classical $v-\mathcal{E}$ relationship. However, the non-local effect produces spatial latency in the response of carriers to the electric field change, and effectively makes their velocity less sensitive to the field at the source-end compared to that predicted using the DD model. Hence, the HD model exhibits a smaller derivative of the velocity with respect to the field, which subsequently causes a higher local ac resistance and larger impedance field.

5.2 Summary

This chapter analyzes excess thermal noise in short channel MOSFETs, using a hybrid numerical noise simulation method. Drain current noise is dominated by the source-side contributions. Moreover, the excess noise is caused not by the individual local noise sources but by the effects of the impedance field. While both the DD and HD models show almost the same values of velocity due to small electric field at the source, the non-local transport

behavior causes a smaller derivative of velocity with respect to the electric field for the HD formulation. The resulting higher local ac resistance near the source junction increases the impedance field which is directly reflected in excess noise and a strong gate length dependence of γ and δ in scaled submicron MOS devices. This phenomenon cannot be accounted for using the conventional DD model because of the local nature in the $v - \mathcal{E}$ relationship. Thus higher order transport models, such as the HD formulation, are essential in considering noise simulation for scaled MOSFET devices. Equation (5.3) suggests that the improvement of γ can be achieved either using a different material with lighter carrier mass or employing a broader channel carrier profile. Structures such as buried channel, JFETs, and MESFETs are possible candidate devices to be considered.

Chapter 6

Compact Noise Modeling

MOST EXISTING MOSFET NOISE MODELS have not adequately accounted for excess drain current noise, observed in short channel MOSFETs. Some models allow the user to adjust drain current noise but the bias or geometry dependences are

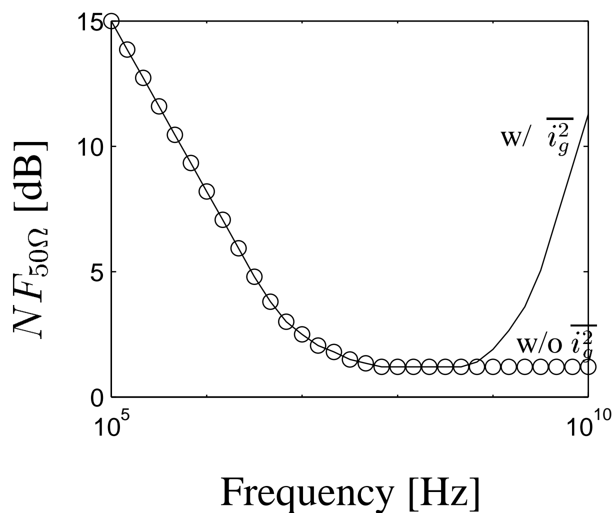


Figure 6.1: Noise figure of a MOSFET connected to Z_s=50Ω

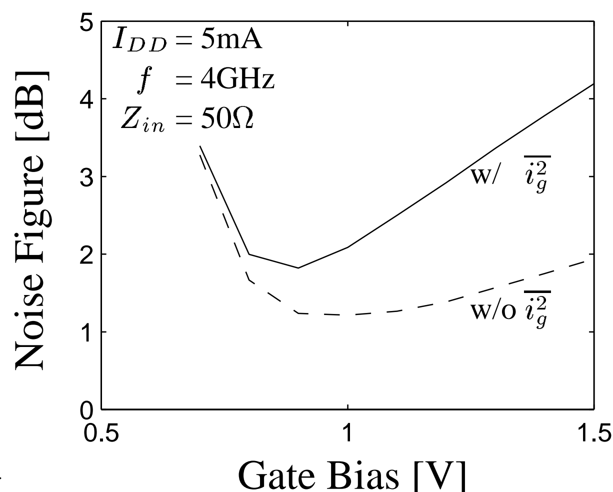


Figure 6.2: Noise performance of a tuned LNA

not modeled. Besides drain current noise, as discussed in Section 2.1.2, MOSFETs have induced gate current noise. Since it is proportional to f^2, it is not significant at low frequencies and has long been neglected in digital-application-oriented modeling. Even the *de facto* industry standard model BSIM3 has not accounted for the induced gate noise. As CMOS is increasingly used for RF applications, however, it is apparent that the inclusion of induced gate noise is necessary. Figure 6.1 illustrates the frequency dependence of the noise figure of a MOSFET connected to 50Ω source resistance. This bathtub-shaped characteristic is dominated by $1/f$ noise at low frequencies, limited by drain current thermal noise at mid frequencies, and induced gate noise prevails at high frequencies, starting from one tenth of f_T. Hence, if the induced gate noise in excluded, the noise figure of high frequency amplifiers is largely underestimated as shown in Figure 6.2.

This chapter reviews existing high frequency noise models, validates their assumptions, and proposes a physically sound modeling approach for MOSFETs.

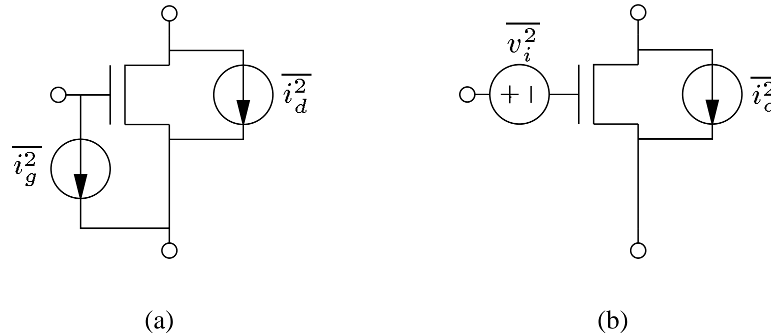


Figure 6.3: MOSFET thermal noise models. (a) van der Ziel model (b) Pospieszalski Model.

6.1 van der Ziel Model

The most broadly accepted noise model for MOSFETs is the van der Ziel model [11]. This model also has a solid physical basis since it is simply based on the admittance representation of classical two-port theory[1]. Since the cross-correlation is a complex number in general, this approach has *four* parameters that correspond to $F_{min} - R_n - G_{opt} - B_{opt}$ introduced in Section 2.6.

In the case of the MOSFET, the real part of the cross-correlation is much smaller than the imaginary part under most practical operating conditions; van der Ziel proposed a *three*-parameter model by assuming $\Re[\overline{i_1 i_2^*}] = 0$. In such a case, the correlation admittance (Y_c) is purely imaginary and F_{min} becomes a subordinate factor of R_n and G_{opt} [62].

[1]Detailed discussion is presented in Appendix A.2.

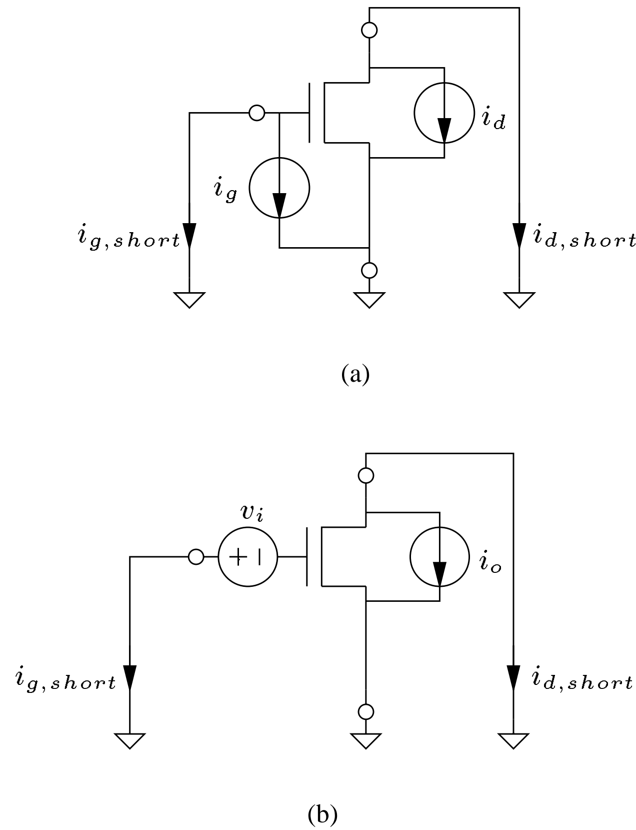


Figure 6.4: Schematic for model comparison. (a) van der Ziel model (b) Pospieszalski Model.

6.2 Pospieszalski Model

Another widely accepted noise model in the GaAs community is the Pospieszalski model [65], which is based on the hybrid representation ($\overrightarrow{H}$). Figures 6.3 (a) and (b) compares the Pospieszalski model with the van der Ziel model. While the gate current noise in the van der Ziel model is frequency dependent and correlated with the drain current noise, the Pospieszalski model uses an input voltage noise source $\overline{v_i^2}$, which is frequency-independent.

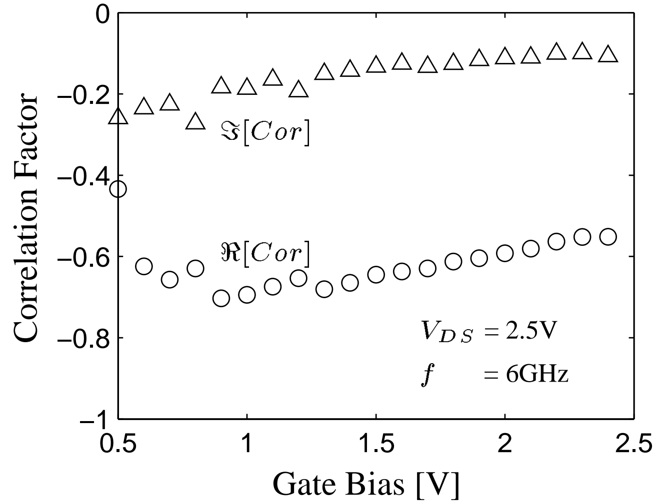


Figure 6.5: Gate bias dependence of the correlation factor of the Pospieszalski model for an nMOSFET ($W/L = 96/0.25\mu$m).

Reducing the number of variables further, Pospieszalski proposed a *two*-parameter model by assuming that two noise sources have negligible correlation ($\overline{v_i i_o^*} \approx 0$). Thus this approach has the advantage that it is easily implementable in typical SPICE simulators. Further investigations demonstrated that the given assumption is well satisfied in GaAs devices [62]. However, no study has shown that it is valid for MOSFET devices.

If this model is equivalent to the van der Ziel model, both models should yield the same amount of short-circuit noise current at the input and output electrodes as illustrated in Figures 6.4 (a) and (b):

$$i_{g,short} = -i_g = Y_{11} v_i \quad (6.1)$$

$$i_{d,short} = -i_d = (Y_{21} - Y_{12}) v_i - i_o \quad (6.2)$$

The given assumption means that the following correlation factor needs to be nearly zero:

$$Cor = \frac{\overline{v_i i_o^*}}{\sqrt{\overline{v_i^2}\,\overline{i_o^2}}} \quad (6.3)$$

where

$$\overline{v_i^2} = \frac{1}{|Y_{11}|^2}\overline{i_g^2} \quad (6.4)$$

$$\overline{v_i i_o^*} = \frac{Y_{21}^* - Y_{12}^*}{|Y_{11}|^2}\overline{i_g^2} - \frac{1}{Y_{11}}\overline{i_g i_d^*} \quad (6.5)$$

$$\overline{i_o^2} = \frac{|Y_{21} - Y_{12}|^2}{|Y_{11}|^2}\overline{i_g^2} + \overline{i_d^2} - 2\Re\left[\frac{Y_{21} - Y_{12}}{Y_{11}}\overline{i_g i_d^*}\right] \quad (6.6)$$

Figure 6.5 demonstrates that the correlation-free assumption is not applicable in general to short channel MOSFETs. Even in long channel devices, the MOSFET does not satisfy conditions which make the correlation negligible[2]. Thus, the given model introduces errors in modeling MOSFET noise behavior. The noise spectra reproduced by the Pospieszalski model are as follows:

$$\overline{i_{g,Pos}^2} = |Y_{11}|^2\overline{v_i^2} \quad (6.7)$$

$$\overline{i_g i_{d,Pos}^*} = Y_{11}[(Y_{21}^* - Y_{12}^*)\overline{v_i^2} - \overline{v_i i_o^*}] \quad (6.8)$$

$$\overline{i_{d,Pos}^2} = |Y_{21} - Y_{12}|^2\overline{v_i^2} + \overline{i_o^2} - 2\Re[(Y_{21} - Y_{12})\overline{v_i i_o^*}] \quad (6.9)$$

[2]Appendix D explains why the correlation is not negligible in long channel MOSFETs.

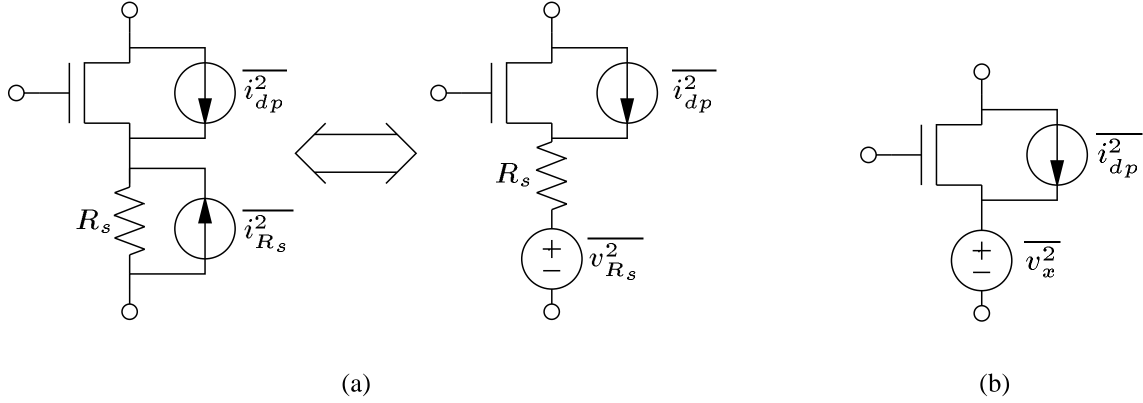


Figure 6.6: MOSFET thermal noise models. (a) BSIM4 as implemented. (b) Simplified BSIM4 (assuming R_s is negligible)

.

With the given correlation-free assumption, the above formulae become:

$$\overline{i_{g,Pos}^2} = |Y_{11}|^2\overline{v_i^2} \approx \omega^2(C_{gs}+C_{gd})^2\overline{v_i^2} \tag{6.10}$$

$$\overline{i_g i_{d,Pos}^*} = Y_{11}(Y_{21}^* - Y_{12}^*)\overline{v_i^2} \approx j\omega(C_{gs}+C_{gd})g_m\overline{v_i^2} \tag{6.11}$$

$$\overline{i_{d,Pos}^2} = |Y_{21}-Y_{12}|^2\overline{v_i^2}+\overline{i_o^2} \approx g_m^2\overline{v_i^2}+\overline{i_o^2} \tag{6.12}$$

Equations (6.10) and (6.11) suggest that the model assumes $\overline{i_g i_d^*} = \overline{i_g^2}(Y_{21}-Y_{12})^*/Y_{11}^*$.

6.3 BSIM4 Model

The next generation MOS model BSIM4 [66], [67] released for public use in March 2000, amends the shortcomings of BSIM3 predecessor by addressing induced gate noise. The BSIM4 model shown in Figure 6.6 (a) and (b) are somewhat similar to the Pospieszalski

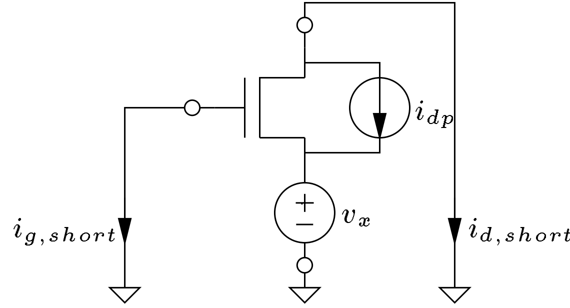


Figure 6.7: Schematic for BSIM4 model comparison.

model since the noise sources are frequency-independent and uncorrelated ($\overline{v_{R_s} i_{dp}^*} = 0$); this topology is easier to implement in a circuit simulator. On the other hand, it adopts a drastically different modeling strategy by connecting a noise source to the *source electrode* instead of the gate. This approach differs from other models since it is not based on any equivalent two-port representation.

While the exact implementation uses $\overline{v_{R_s}^2} = 4kT\Delta f(R_x + R_s)$[3] as shown in Figure 6.6 (a), this chapter uses a simplified BSIM4 model shown in Figure 6.6 (b) for sake of simplicity. It assumes that the source resistance (R_s) can be neglected, since the condition that $R_x \gg R_s$ is generally satisfied.

Again, comparing the short-circuited noise current at two electrodes identifies the underlying assumption of the BSIM model. Comparing Figures 6.4 (a) and 6.7 gives:

$$i_{g,short} = -i_g = (Y_{11} + Y_{12})v_x \tag{6.13}$$

$$i_{d,short} = -i_d = (Y_{21} + Y_{22})v_x - i_{dp} \tag{6.14}$$

Thus the BSIM4 model replicates the frequency dependence and correlation of the induced

[3]A complete model description is presented in Appendix E.1.

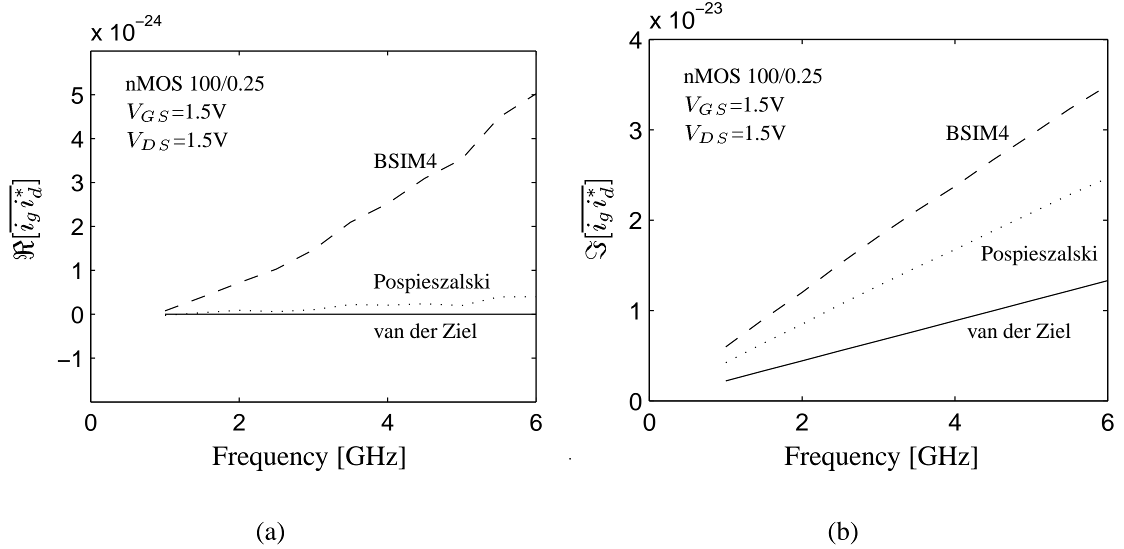


Figure 6.8: Comparison for the correlated noise power spectrum. (a) real part (b) imaginary part

gate noise as follows:

$$\overline{i^2_{g,BSIM4}} = |Y_{11} + Y_{12}|^2 \overline{v_x^2} \approx \omega^2 C_{gs}^2 \overline{v_x^2} \tag{6.15}$$

$$\overline{i_g i^*_{d,BSIM4}} = (Y_{11} + Y_{12})(Y_{21} + Y_{22})^* \overline{v_x^2} \approx j g_m \omega C_{gs} \overline{v_x^2} \tag{6.16}$$

$$\overline{i^2_{d,BSIM4}} = |Y_{21} + Y_{22}|^2 \overline{v_x^2} + \overline{i^2_{dp}} \approx g_m^2 \overline{v_x^2} + \overline{i^2_{dp}} \tag{6.17}$$

Equations (6.15) and (6.16) suggest that the BSIM4 model assumes $\overline{i_g i_d^*} = \overline{i_g^2}(Y_{21} + Y_{22})^*/(Y_{11} + Y_{12})^*$. Due to this assumption, the BSIM4 model also causes errors in modeling the term $\overline{i_g i_d^*}$.

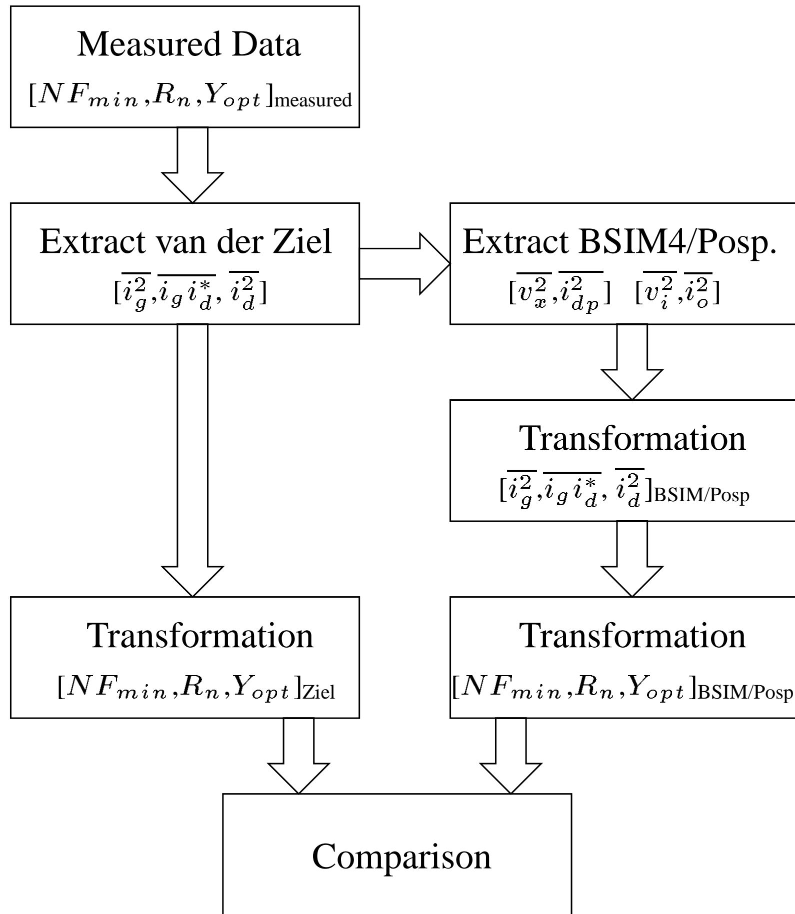


Figure 6.9: Model comparison procedure.

6.4 Impact of Errors in Correlation Modeling

As discussed in the previous sections, two-parameter models do not describe successfully the noise characteristics of MOSFETs. As compared in Figure 6.8 (a) and (b), the Pospieszalski and BSIM4 models introduce a substantial amount of errors in $\overline{i_g i_d^*}$ term. On the other hand, they can replicate perfectly $\overline{i_g^2}$ and $\overline{i_d^2}$. Therefore the question becomes to what degree the $\overline{i_g i_d^*}$ term affects the entire noise characteristics.

According to the two-port noise theory [68], as long as the two different models reproduce the same four noise parameter sets, they should yield exactly the same noise performance for various circuit topologies. To examine how much the noise characteristics are affected by the errors in the correlated noise term, measured four noise parameters are compared with characteristics that are reproduced by extracted noise sources. The procedure is illustrated in Figure 6.9. First, noise sources for the van der Ziel model are extracted at 5GHz by directly converting the noise matrix. Second, noise sources of the Pospieszalski and BSIM4 models are chosen to fit $\overline{i_g^2}$ and $\overline{i_d^2}$ values as follows:

$$\overline{v_x^2} = \frac{1}{|Y_{11}+Y_{12}|^2}\overline{i_g^2} \tag{6.18}$$

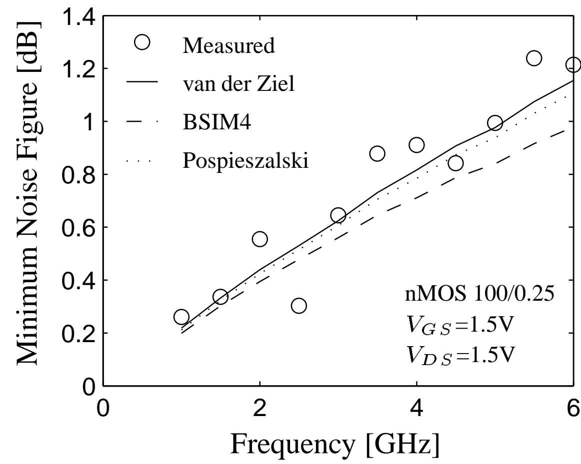
$$\overline{i_{dp}^2} = \overline{i_d^2} - \frac{|Y_{21}+Y_{22}|^2}{|Y_{11}+Y_{12}|^2}\overline{i_g^2} \tag{6.19}$$

$$\overline{v_i^2} = \frac{1}{|Y_{11}|^2}\overline{i_g^2} \tag{6.20}$$

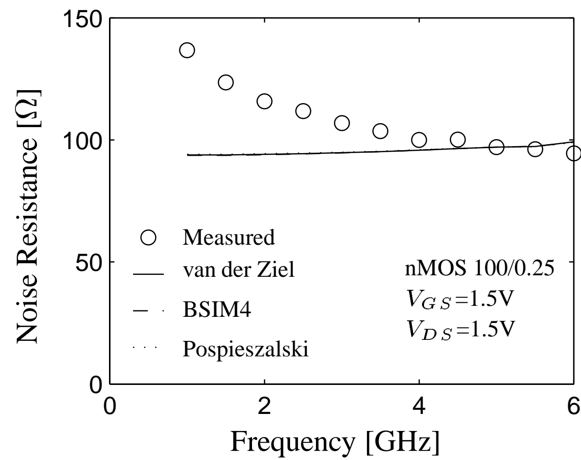
$$\overline{i_o^2} = \overline{i_d^2} - \frac{|Y_{21}-Y_{12}|^2}{|Y_{11}|^2}\overline{i_g^2} \tag{6.21}$$

Then equivalent gate-drain current noise spectra are reproduced using Equations (6.10) – (6.12) and (6.15) – (6.17). For the van der Ziel model, $\overline{i_g^2}$ and $\overline{i_g i_d^*}$ are adjusted based on their frequency dependence. Finally, each set of $\overline{i_g^2} - \overline{i_g i_d^*} - \overline{i_d^2}$ is transformed back into four noise parameters for comparison.

In Figures 6.10 and 6.11, the frequency dependence of the four noise parameters are compared. These results demonstrate that the frequency independent noise sources $\overline{v_x^2}$ and $\overline{v_i^2}$ reproduce the behavior of the frequency dependent noise $\overline{i_g^2}$ at the device level. Since R_n is determined by $\overline{i_d^2}$, all the models should yield exactly the same value in Figure 6.10 (b). The error in $\overline{i_g i_d^*}$ term leads to discrepancies in other parameters in Figures 6.10 (a), 6.11 (a), and 6.11 (b) but the differences are acceptably small. These results imply that, despite substantial errors in $\overline{i_g i_d^*}$ term, the two-parameter models can be used as a practical means

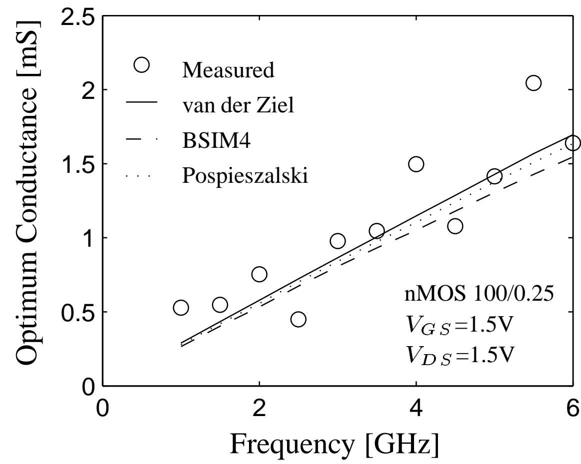


(a)

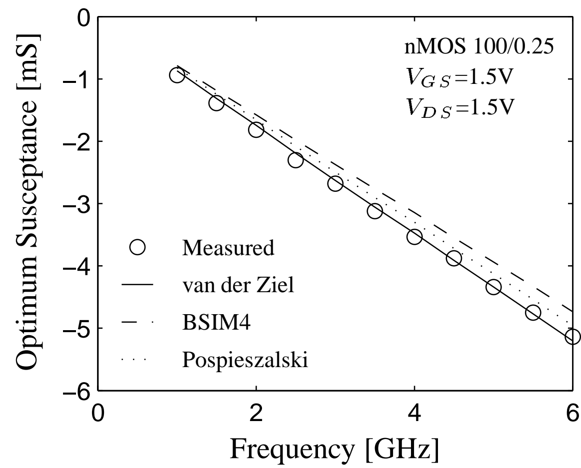


(b)

Figure 6.10: Frequency dependence of four noise parameters. Generated using noise sources extracted at 5GHz. (a) NF_{min} (b) R_n



(a)



(b)

Figure 6.11: Frequency dependence of four noise parameters. Generated using noise sources extracted at 5GHz. (a) G_{opt} (b) B_{opt}

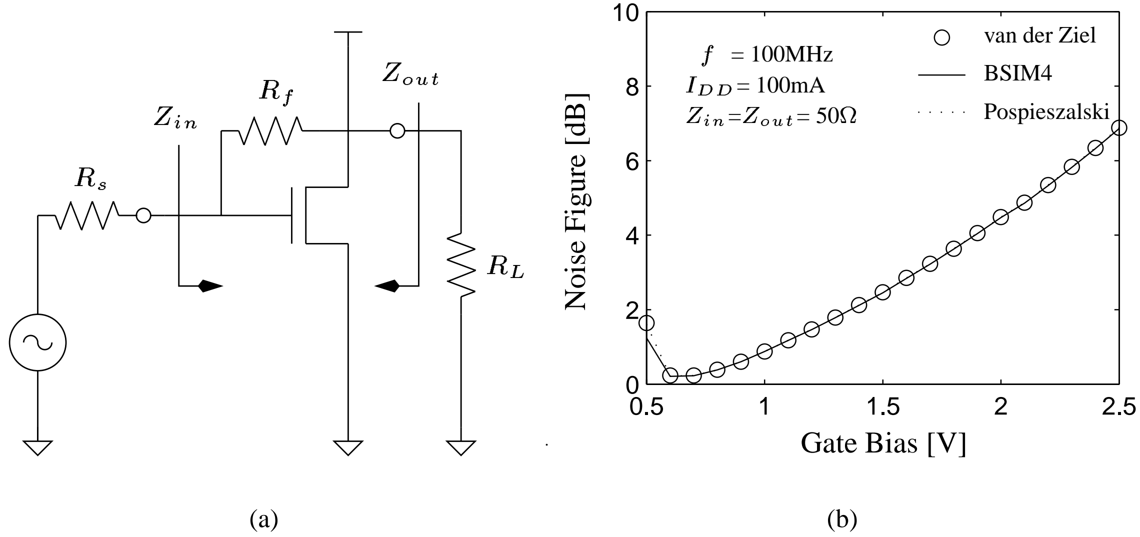


Figure 6.12: Shunt-series feedback broadband amplifier. (a) Architecture (b) Power-constrained noise performance.

for implementing MOSFET noise models.

Next, turning to actual circuit applications, the noise figure is calculated for various circuit topologies using the noise analysis method for linear networks described in Appendix A.2.5. Noise parameters are reproduced for the three models as described previously.

Figure 6.12 (a) shows a broadband amplifier with feedback (R_f) used to achieve impedance matching at input and output. In the case of the van der Ziel model, the induced gate noise has negligible impact on the noise figure, up to moderately high frequencies. By contrast, the drain current noise $\overline{i_o^2}$ for the Pospieszalski model and $\overline{i_{dp}^2}$ for BSIM4 are smaller by $g_m^2\overline{v_i^2}$ and $g_m^2\overline{v_x^2}$, respectively, than $\overline{i_d^2}$ from the van der Ziel model. However, the broadband contribution of $\overline{v_i^2}$ and $\overline{v_x^2}$ compensate for this difference. Thus all the models yield the same overall noise performance. In other words, NF_{min} is close to zero in the frequency

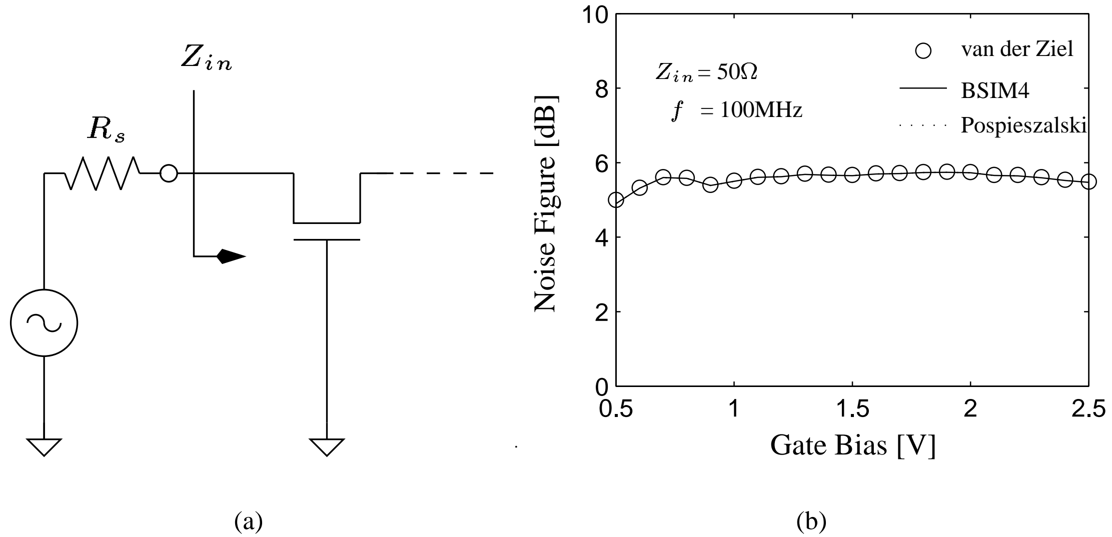


Figure 6.13: $1/g_m$ termination broadband amplifier. (a) Architecture (b) Noise performance.

range below 1GHz; R_n is the same for both models; the key factor that differentiates the noise performance is Y_{opt}. In Figure 6.12 (b), $Y_{opt} \ll 1/50$ except in the very low gate bias range, thus the different models yield the same results.

Another broadband amplifier architecture, whose input impedance is adjusted by its g_m, is shown in Figures 6.13 (a). The Pospieszalski and BSIM4 models again exhibit an identical noise figure to the van der Ziel model in Figure 6.13 (b), with the same physical differences as noted above. This case validates the non-grounded source condition of operation.

A good example that highlights the impact of induced gate noise is the power-constrained design of the tuned amplifier, illustrated in Figure 6.14 (a). Usually this architecture exhibits valley-shaped noise characteristics for a power-constraint as shown in Figure 6.14

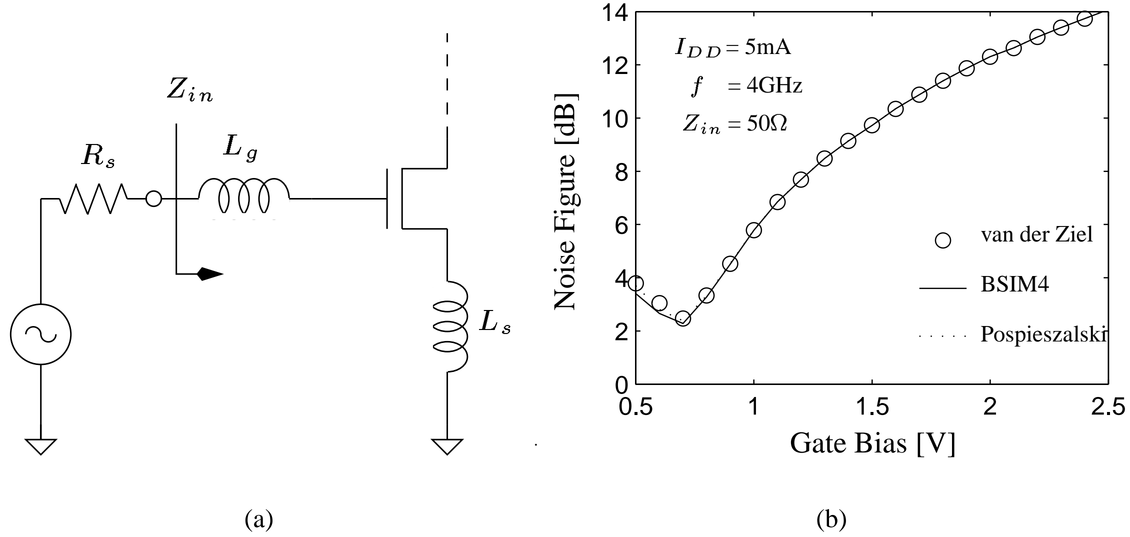


Figure 6.14: Inductively degenerated tuned amplifier. (a) Architecture (b) Power-constrained noise performance.

(b); the drain noise is dominant as the gate bias becomes lower while the induced gate noise becomes dominant at high gate bias. The correlated term $\overline{i_g i_d^*}$ affects the noise performance at low gate bias but it is less significant than the drain noise [69]. Therefore the noise figure shows excellent agreement and again validates further the non-grounded source conditions in modeling noise. This can also be explained based on the four noise parameters. When the gate bias is high, the mismatch of Y_{opt} to Y_s is so large that the noise performance equation can be approximated as:

$$F = F_{min} + \frac{|Y_s - Y_{opt}|^2 R_n}{G_s} \tag{6.22}$$

$$\approx \frac{|Y_s|^2 R_n}{G_s} \tag{6.23}$$

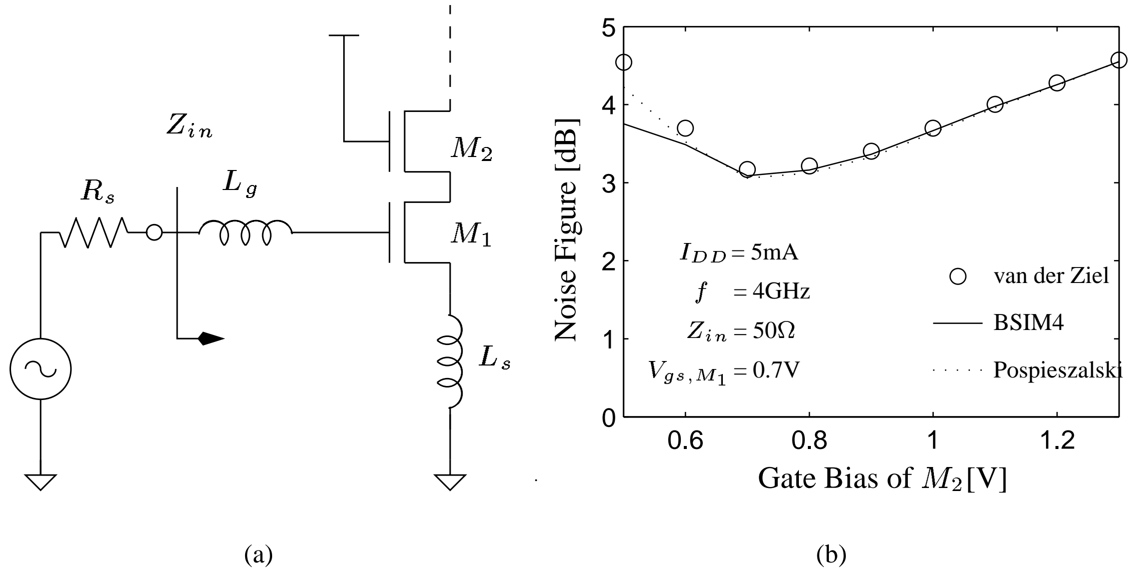


Figure 6.15: Inductively degenerated tuned amplifier with cascode stage. (a) Architecture (b) Power-constrained noise performance.

As the gate bias becomes lower, Y_{opt} gets closer to Y_s so imperfect reproduction of noise parameters in Figures 6.10 and 6.11 results in observable differences. These differences become more noticeable when the cascoded stage is taken into account as shown in Figure 6.15. Nevertheless, the error is acceptably small.

Therefore, the Pospieszalski and BSIM4 noise models can be considered as being equivalent to the van der Ziel model in most practical circuits, including non-grounded source conditions of operation.

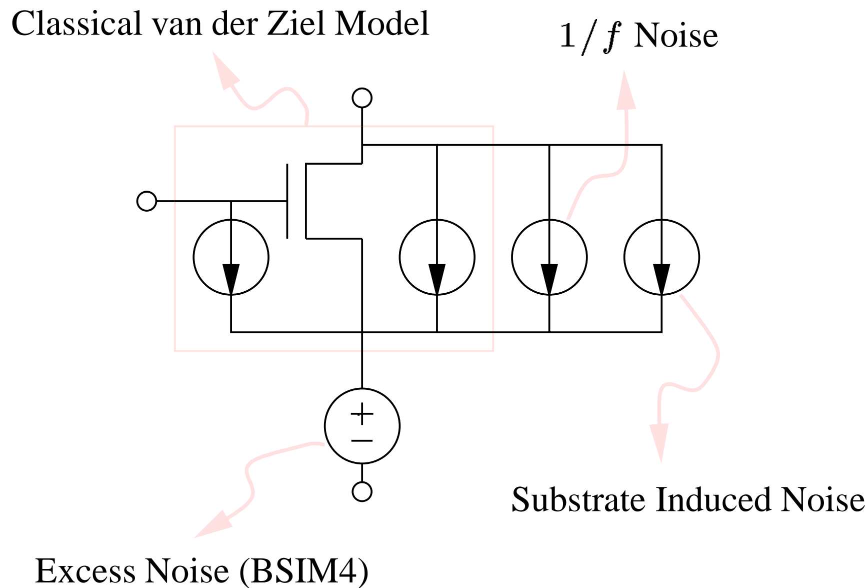


Figure 6.16: Physical noise sources in MOSFET devices.

6.5 Physical Noise Modeling

Figure 6.16 illustrates noise sources, accounting all the physical phenomena addressed in Chapters 2, 4, and 5. Local fluctuations in the channel generate current noise at the electrodes; this effect is captured by the classical van der Ziel model with long channel coefficients[4]. Charge trapping behavior of defects and impurities at the Si/SiO_2 interface introduces $1/f$ noise spectrum in drain current noise that can be modeled only empirically[5].

In many technologies, spreading resistance of the substrate generates an indirect contribution via the channel depletion capacitor. Due to the three-dimensional distributed effect

[4] Refer to Section 2.1.2.
[5] Refer to Section 2.3.

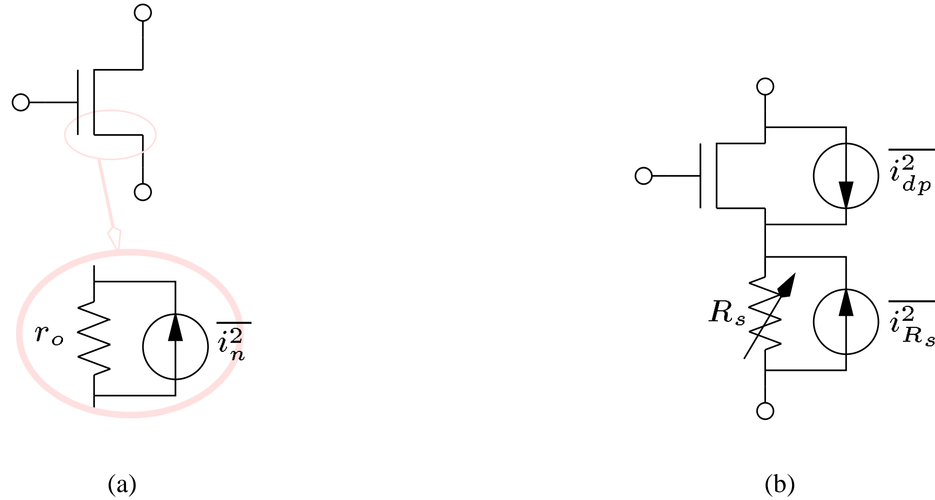


Figure 6.17: Comparison between physical effects and BSIM4 noise model.

of the substrate network, this component also needs to be modeled empirically[6] as follows:

$$S_{i_d,sub} = \frac{4kTR_{sub}g_{mb}^2\,\alpha}{1+(\omega R_{sub}C_{depl})^n} \tag{6.24}$$

where α is usually below 0.1 and n is around 0.4.

Finally, the excess noise in short channel devices can be accounted for by a voltage noise source connected to the source electrode, as adopted in BSIM4. Physical simulations[7] demonstrate that non-local transport behavior results in higher local ac resistance near the source junction, which in turn causes excess noise as illustrated in Figure 6.17 (a). In BSIM4, as shown in Figure 6.17 (b), the source resistance R_s is arbitrarily increased in the noise analysis to capture the excess noise in short channel MOSFETs. Interestingly, as

[6] Refer to Section 4.3.3.
[7] See Section 5.1.

this approach describes exactly what simulation results explain, it is thus quite adequate in physical modeling.

The excess noise generated by the higher local ac resistance, in combination with transconductance, manifest bias and geometry dependences quite similar to those of hot carrier effects. Thus, despite their seemingly inappropriate physics, recent compact models[8] reproduce macroscopically drain current noise very well. They usually consist of two portions: one captured by the long channel noise theory ($\overline{i_{d,0}^2}$) and the other one incorporating the short channel effect ($\overline{i_{d,e}^2}$). Hence the amount of the voltage noise source in Figure 6.16 should be $\overline{i_{d,e}^2}/g_m^2$.

6.6 Summary

The high frequency noise characteristics are dominated by induced gate noise, which is not accounted for in most MOSFET noise models. To describe MOSFET noise behavior at high frequencies, three parameters are required, as incorporated in the van der Ziel model. Two-parameter models, such as the Pospieszalski and BSIM4 models, introduce errors in the correlated noise term in general. Nevertheless such errors do not impose significant problems in most practical circuit topologies. Thus they can be considered as being functionally equivalent to the van der Ziel model. The modeling strategy of BSIM4 is particularly attractive in physical modeling since it captures the physical phenomena identified by numerical simulations.

[8]Refer to Appendix F for model descriptions.

Chapter 7

LNA Design

THE TRADITIONAL NOISE OPTIMIZATION TECHNIQUE for LNA design starts with a given device with fixed characteristics; the optimum bias condition and source impedance are then determined. Hence, this technique often results in poor input matching or unacceptably large power consumption. By contrast, in full custom ICs, the designer can choose the desired device geometries, which offers an important degree of freedom. Nevertheless most designers still rely on classical optimization techniques because no explicit guidance is generally available on how to best exercise the IC designer's freedom in tailoring device geometries. Recently proposed noise optimization techniques for CMOS RF circuits permit greater flexibility in the selection of device geometries as well as matching elements and biasing conditions to minimize the noise figure for a specified gain or power dissipation [13], [69]. However, they use simplified small-signal models as well as constant noise characteristics. These techniques also rely heavily on mathematical derivations that provide limited intuitive design guidance.

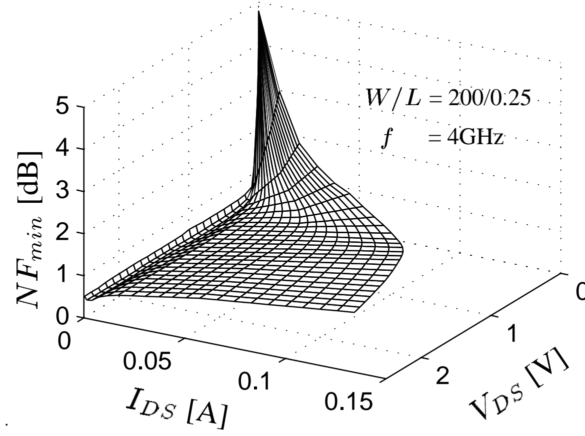
This chapter presents explicit guidelines for LNA design based directly on measured noise parameters and noisy two-port theory; the approach requires neither sophisticated noise modeling nor circuit simulation to be used. All the analyses are based on MOSFET

designs but the same methodology can be applied to other IC technologies as well, for example, design using more advanced HBT technology [70]. Section 7.1 considers the intrinsic noise performance of the MOSFET in relation to LNA design. Section 7.2 explains how the noise performance of the LNA differs from that of the intrinsic device; explicit design guidelines for a CMOS tuned LNA with power constraints are presented. Finally Section 7.3 presents experimental results for an implementation using integrated CMOS technology to realize an LNA.

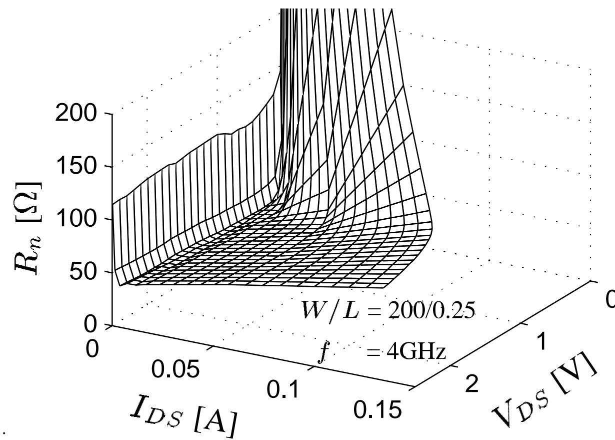
7.1 High Frequency Intrinsic Noise Performance of MOSFETs

The intrinsic noise parameters of a MOSFET are shown in Figure 7.1 for the entire operating range: the $x-y$ plane spans the $I-V$ operating characteristic curves and z axis gives the noise parameter at the respective bias points. These characteristics are transformed from simulated noise factors by combining them with network parameters that are secondary outputs of the noise simulator. In the linear region ($V_{DS} < V_{Dsat}$), NF_{min} and R_n show drastic increases; a similar increase of R_n is observed for low gate bias ($V_{GS} \approx V_{th}$). Such results are mainly attributed to the low g_m as well as a poor correlation factor (c) in this regime, and suggest that those bias conditions are highly undesirable for circuit implementation. Even in the saturation region, despite a good value for NF_{min} (below 1dB), actual circuit noise performance can easily degrade due to small G_{opt} (corresponding $|\Gamma_{opt}|$ is nearly 1) as well as large R_n (three to ten times larger than that observed for HEMT devices [71]). Another observation is that NF_{min} in Figure 7.1 (a) shows negligible drain bias dependence while γ and δ usually exhibit substantial drain bias dependence.

In the saturation region for MOSFETs, the four noise parameters can be approximated



(a)



(b)

Figure 7.1: Intrinsic noise performance for the entire operating range of a 0.25 μm nMOSFET. (a) Minimum noise figure (NF_{min} [dB]) (b) Equivalent noise resistance (R_n [Ω]).

as[1]:

$$F_{min} \approx 1 + \frac{\omega}{\omega_T}\sqrt{\gamma\delta\zeta(1-|c|^2)} \tag{7.1}$$

[1]See Appendix A.3.3 for derivations.

Equation (7.1) suggests that shorter devices yield better noise figures because ω_T is proportional to $1/L_{eff}$ while $\sqrt{\gamma\delta\zeta(1-|c|^2)}$ becomes at most 6.5 times larger than the long channel case, down to 0.25 μm [69]. The small drain bias dependence of NF_{min} also can be explained by (7.1) since increases of γ and δ are mitigated by increasing g_m and c.

7.1.1 Scaling of the Noise Parameters

In realizing a fully custom IC design of the LNA, one of the key issues is to understand the device scaling effects on the noise parameters. Since shorter devices yield better noise figures, the selection of device geometries for the LNA design requires width scaling, consistent with the shortest channel length that can be realized. The four noise parameters can be derived from current noise spectral power, given in Equations (2.4) – (2.6), as follows:

$$F_{min} = 1 + 2R_n(G_{opt} + G_c) \tag{7.2}$$

$$R_n = \left|\frac{1}{Y_{21}}\right|^2 \frac{\overline{i_d^2}}{4\,k\,T\,\Delta f} \tag{7.3}$$

$$G_{opt} = \sqrt{\frac{G_u}{R_n} + G_c^2} \tag{7.4}$$

$$B_{opt} = -B_c \tag{7.5}$$

$$G_u = \frac{\overline{i_g^2}(1-|c|^2)}{4\,k\,T\,\Delta f} \tag{7.6}$$

$$Y_c = Y_{11} - Y_{21}c\sqrt{\frac{\overline{i_g^2}}{\overline{i_d^2}}} \tag{7.7}$$

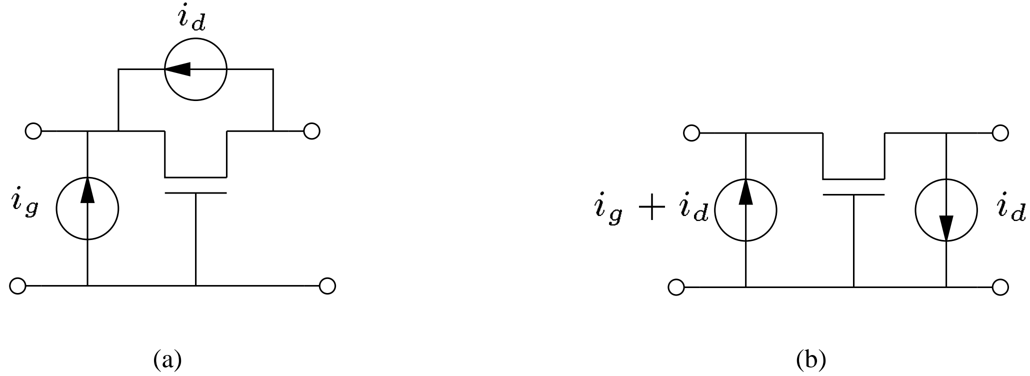


Figure 7.2: Noise power of the MOSFET in a common-gate configuration. (a) Original (b) Equivalent

These results suggest the dependence of the four noise parameters with respect to device width as follows:

$$F_{min} \quad \text{no width dependence} \tag{7.8}$$

$$R_n \propto 1/W \tag{7.9}$$

$$G_{opt} \propto W \tag{7.10}$$

$$B_{opt} \propto W \tag{7.11}$$

7.1.2 Conversion of Noise Characteristics into Common-Gate Mode

Adding a cascode stage is a common practice in amplifier design because it improves the stability by shielding the input device from voltage variations at the output. The four noise parameters of the cascode stage can be directly obtained by measuring the common-gate mode MOSFET. The equivalent I/O noise power also can be obtained from characteristics

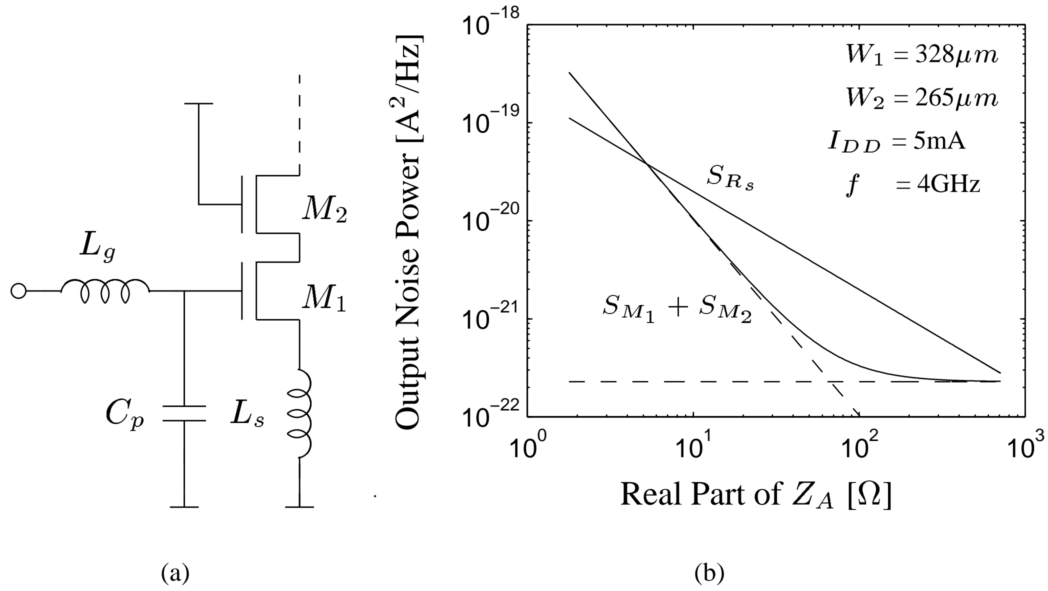


Figure 7.3: (a) Tuned LNA architecture employing inductive source degeneration. (b) Dependence of output noise power components on $\Re[Z_A]$ where Z_A is the input impedance at the gate electrode of M_1.

of the common-source model, using Figure 7.2 as a reference for the parameters.

$$\overline{i_1^2} = \overline{i_g^2} + \overline{i_g i_d^*} + \overline{i_d i_g^*} + \overline{i_d^2} \tag{7.12}$$

$$\overline{i_1 i_2^*} = -\overline{i_g i_d^*} - \overline{i_d^2} \tag{7.13}$$

$$\overline{i_2^2} = \overline{i_d^2} \tag{7.14}$$

The four noise parameters of the cascode stage in turn can be obtained using the noisy two-port theory [2], described in Appendix A.2. Note that the body effect is not taken into account in these calculations.

7.2 Design Guidelines for a Tuned Amplifier

The four noise parameters and s-parameters were measured for a 0.24 μm nMOSFET with W = 100 μm, using the ATN NP5B system [43]. The resulting data were then smoothed for the frequency as well as the bias dependences, and in turn used in the following analyses.

7.2.1 Basic Architecture

The tuned amplifier illustrated in Figure 7.3 (a) is one of the most broadly used LNA architectures because it offers the potential of achieving the best noise performance. The desired input impedance[2] of the amplifier is obtained for a narrow frequency band by choosing L_s and L_g independently. It is known that the source degeneration inductance (L_s) controls the noise performance of a given architecture [72] yet the reasons are not well understood. Figure 7.3 (b) shows that each component contributing output noise[3] has a different dependence on the real part of the input impedance ($\Re[Z_A] \approx \omega_T L_s$) when the source impedance offers a conjugate power match. Since the feedback of L_s reduces the current gain, as L_s increases, the output noise contributions from the source resistance (S_{R_s}) and the induced gate noise of M_1 (S_{i_g,M_1}) monotonically decrease but their slopes are different due to different feedback effects. On the other hand, the contribution from the induced gate noise of M_2 (S_{i_g,M_2}) is negligibly small; the contributions from drain current noise (S_{i_d,M_1} and S_{i_d,M_2}) have almost unity gain thus result in an L_s-independent term. Hence the LNA yields the best noise figure when the L_s-dependent term and L_s-independent term give equal contributions, as shown in Figure 7.3 (b).

Figures 7.4 (a) and (b) graphically explain how L_s changes the performance of the

[2]The input impedance calculation is explained in Appendix F.1.
[3]Derivations for each component are available in Appendix F.3.

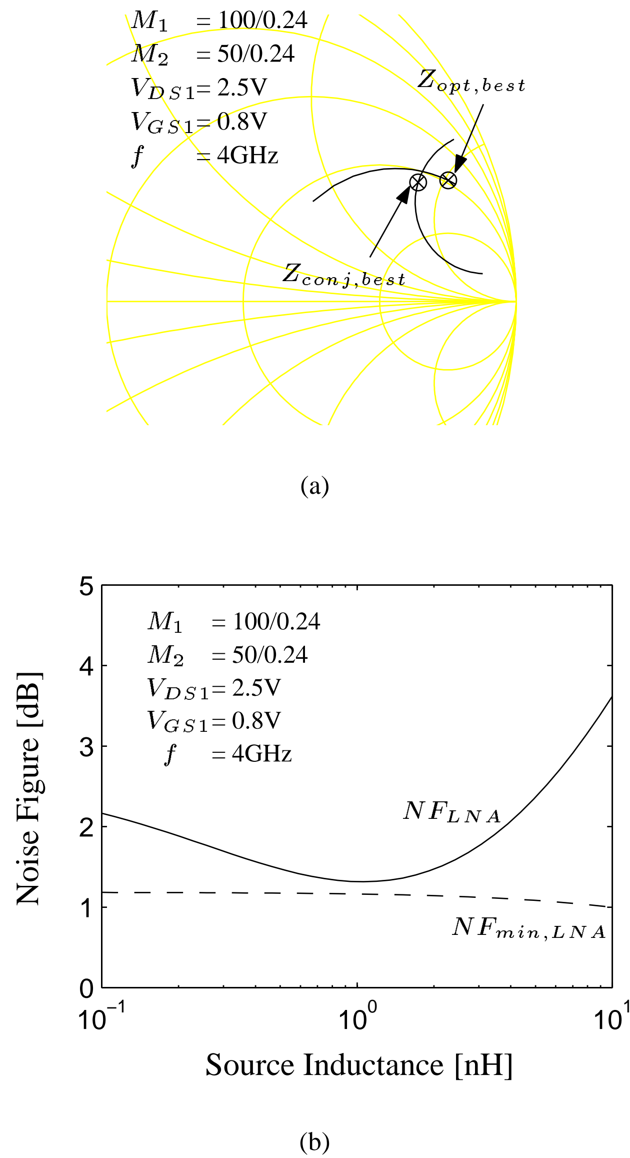
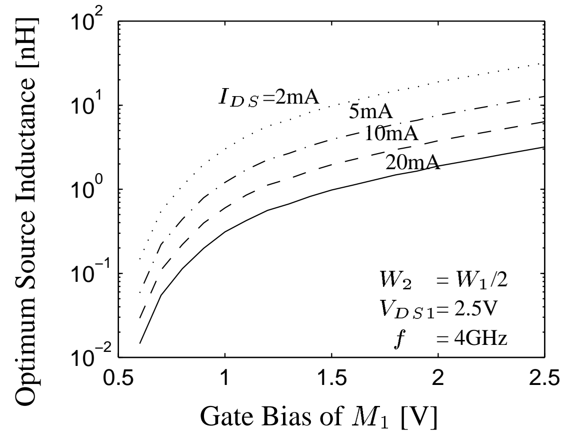
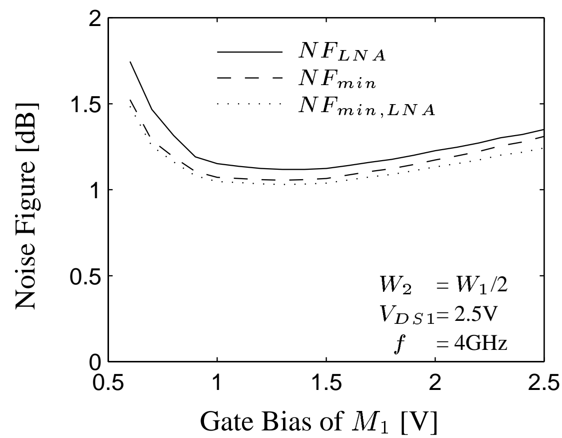


Figure 7.4: The noise performance of the LNA for varying L_s. The noise contributions of M_1 substrate and M_2 are excluded and C_p=0. (a) Optimum source impedance (b) Noise figure.



(a)



(b)

Figure 7.5: (a) Optimum L_s yielding the best noise figure of the LNA for the given bias condition under the power constraint. (b) The best noise figure of the LNA with optimum L_s. The noise contributions of M_1 substrate and M_2 are excluded and C_p=0.

LNA[4]. As L_s increases, the optimum noise matching condition (Z_{opt}) and the power matching condition ($Z_{conj} = Z_{in}^*$) exhibit independent trajectories as shown in Figure 7.4 (a). Therefore, when L_s brings Z_{opt} and Z_{conj} to the point where they are in the closest proximity, the best achievable noise figure with a power match is obtained as shown in Figure 7.4 (b). This fact implies that an accurate calculation of the input impedance is critical in the noise optimization process; approximate values are of limited use. Another beneficial impact of using a source inductance is the resulting improvement of NF_{min} and R_n. Thus the LNA can in principle achieve a better noise figure than NF_{min} of the MOSFET alone if Z_{opt} coincides with Z_{conj}.

7.2.2 Power Constrained Design

The power budget is usually constrained for integrated circuit implementations, thus a design approach oriented toward low power is very important. When the supply voltage and power consumption are fixed, the device width of the input stage corresponding to each bias condition can be easily calculated from the current density. Since the measured four noise parameters are valid only for one device size, they need to be properly scaled based on the width dependences as noted in Equations (7.8) – (7.11). Figure 7.5 (a) demonstrates the optimum L_s is bias dependent and scales linearly with the specified current. However, the noise figure achieved by optimizing L_s is independent of the current specification and very close to the intrinsic NF_{min} as shown in Figure 7.5 (b). Therefore, an arbitrary value of the source impedance, in conjunction with the proper choice of inductance used for source degeneration, offers the possibility of simultaneously achieving a good noise figure as well as a perfect power match.

[4] The analysis procedure is described in Appendix F.2.

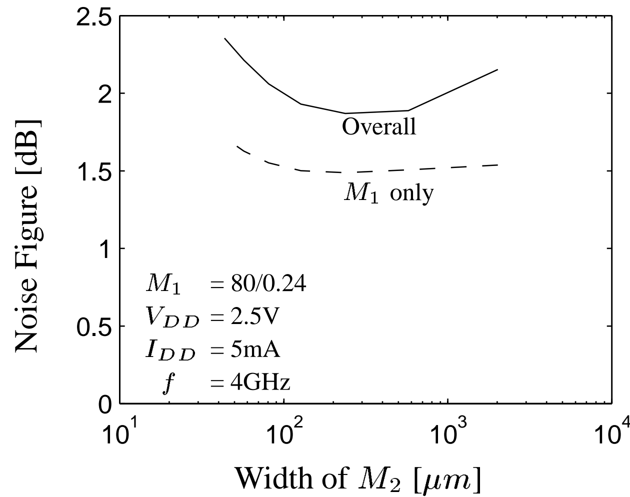


Figure 7.6: The impact of the cascode transistor on the overall noise figure under the power constraint. $R_s = Z_{in} = 50\Omega$.

7.2.3 Cascode Stage Design

While it is known that increasing the width of the cascode device monotonically improves shielding from the output, its impact on the noise performance is not well understood. As the width of the cascode stage increases, the generated noise power from the cascode stage also increases, but the required L_s for a specific Z_{in} decreases. Thus, the different width of the cascode stage consequently yields a different noise match condition as well as different value of noise resistance; an optimal width exists as shown in Figure 7.6. For the given topology, with $W_2 \approx 3W_1$, the cascode stage introduces 40% extra noise power to the input stage, which in turn increases NF by about 0.5dB.

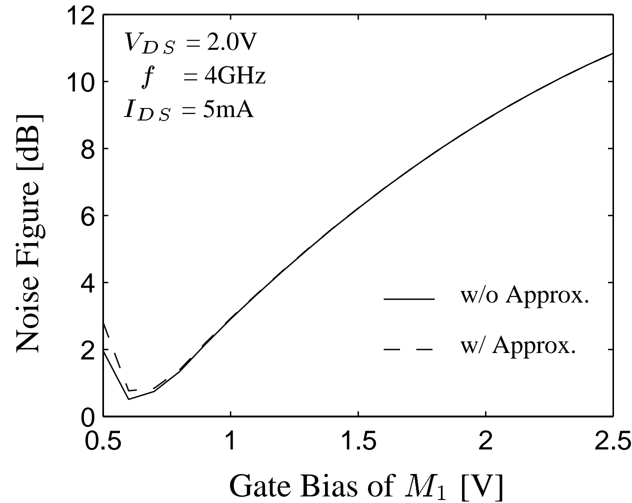


Figure 7.7: Power constrained noise figure of the tuned amplifier when $R_s = Z_{in} = 50\Omega$. The solid line is the actual noise figure; the dashed line is an approximation calculated from (7.15).

7.2.4 Design with A Fixed Source Impedance

In many RF applications, the source impedance has a fixed value of 50Ω, thus $NF_{50\Omega}$ is considered to be a more reasonable parameter than NF_{min}. Even if the source impedance is 50Ω, however, $NF_{50\Omega}$ does not represent the power-matched noise performance unless the input impedance is also adjusted to 50Ω. In this section, the MOSFET sizes are adjusted to satisfy the given power constraint and the inductors L_s and L_g are chosen to provide a 50Ω input impedance for the LNA.

Figure 7.7 is calculated analytically using formulae in Appendix F.3. It exhibits a deep valley-shaped noise figure profile, and suggests that choosing an appropriate gate bias is critical. If we can ignore the correlated portion in (F.19), the amplifier noise figure can be

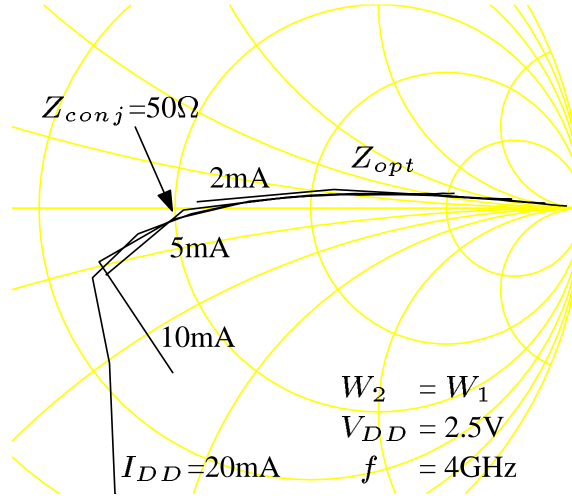


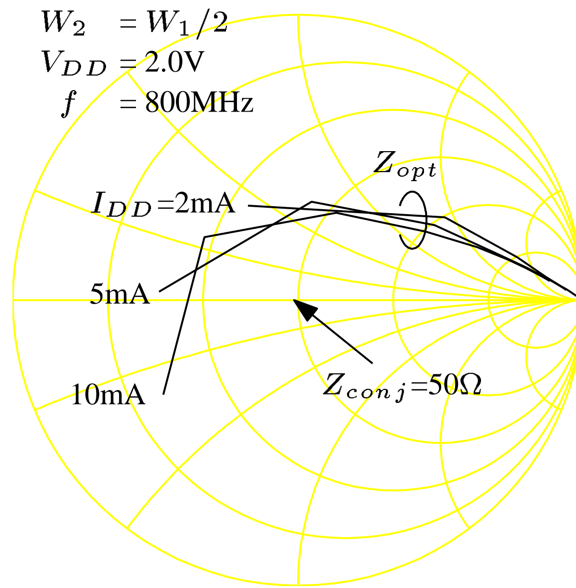
Figure 7.8: Optimum source impedance of a power constrained LNA at f=4GHz when $R_s = Z_{in} = 50\Omega$. The noise contributions of M_1 substrate and M_2 are included and C_p=0.

approximated as follows:

$$F \approx 1 + \frac{\gamma g_{d0}}{G_s}\left(\frac{\omega_0}{\omega_T}\right)^2 + G_s\frac{\delta\zeta}{g_{d0}} \tag{7.15}$$

The comparison in Figure 7.7 shows that the approximate formula replicates the original noise characteristics. This formula explains the valley-shaped noise behavior using two independent noise contributions. One originates from the drain noise and is dominant when the gate bias is low. The other contribution originates from the induced gate noise and becomes dominant at higher gate bias. When the current is fixed, these two components have opposing gate bias dependencies. The noise figure thus has a minimum where they contribute equally to the noise figure. This fact highlights the importance of accurate gate noise modeling for circuit design.

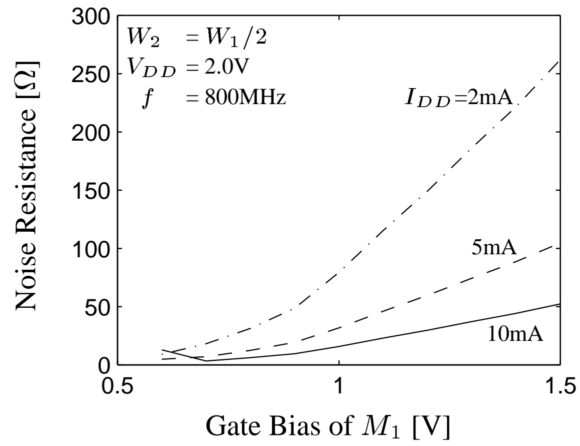
Figure 7.8 demonstrates that Z_{opt} of the LNA is almost purely real at 4GHz, unlike



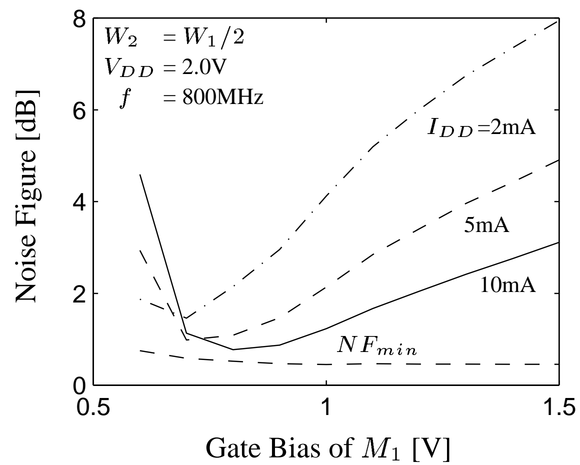
(a)

Figure 7.9: Optimum source impedance of a power constrained LNA at f=800MHz when $R_s = Z_{in} = 50\Omega$. The noise contributions of M_1 substrate and M_2 are included and C_p=0.

the intrinsic MOSFET. It also suggests that a proper choice of the width makes Z_{opt} so close to 50Ω that a simultaneous matching of the impedance and noise can be achieved. Another Z_{opt} for a different topology, shown in Figure 7.9, exhibits larger deviation from the power match condition, which is caused not by the operating frequency but by the poorly optimized cascode stage. Nevertheless, this deviation does not substantially degrade the noise figure since the noise resistance of the LNA shown in Figure 7.10 (a) is reduced by a factor of as much as 5, in comparison to the MOSFET by itself. As a result, noise figures close to NF_{min} can be achieved as shown in Figure 7.10 (b). The achievable noise



(a)



(b)

Figure 7.10: The power constrained noise performance of the LNA when $R_s = Z_{in} = 50\Omega$. The noise contributions of M_1 substrate and M_2 are included and C_p=0. (a) Equivalent noise resistance (b) Noise figure

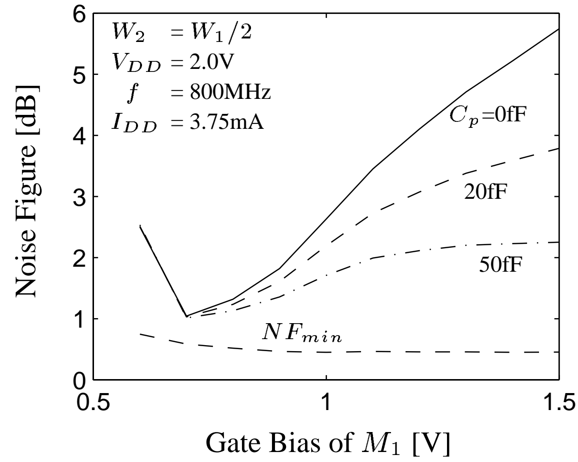
figure is primarily limited by the extra noise contribution from the cascode stage which is also subject to the given power constraint.

7.2.5 Secondary Considerations

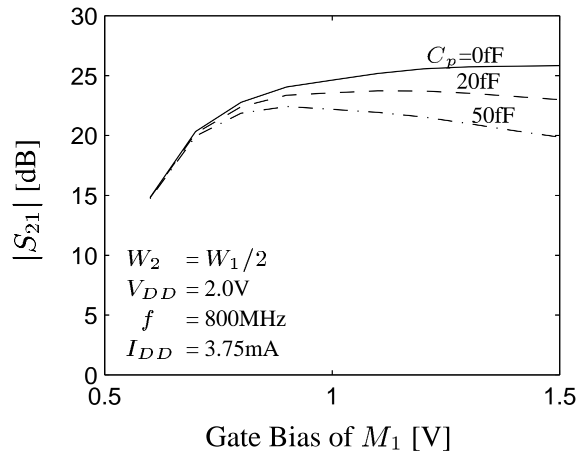
In the process of practical LNA design, as illustrated in Figure 7.3, the bonding pad introduces an extra ac current path to ground. In silicon technology, this can deteriorate severely the noise figure if the path contains a resistive component, such as the conductive substrate [44]. If the resistive component is suppressed, however, the bonding capacitance simply increases the required inductance value for the designated input impedance. This consequently brings the noise match condition closer to 50Ω and also makes the noise resistance smaller. Figures 7.11 (a) – (b) demonstrate that a proper choice of bonding pad size can be utilized to improve the gate bias dependence by trading-off the noise figure with the gain.

7.3 Experimental Results

To evaluate the LNA performance, a single-ended LNA targeting sub-1.0dB of noise figure was designed using a 0.24μm silicide CMOS technology. The die photo of the LNA is given in Figure 7.12. The LNA was designed based on the characteristic in Figure 7.11 (a). First, the supply voltage and power consumption were chosen to 2.0V and 7.5mW, respectively. The gate bias was set to 0.7V to achieve the best noise figure based on the characteristic in Figure 7.11 (a); its corresponding size of M_1 was 90/0.24 for the given power budget. At the time of design, the cascode stage was not fully optimized; the sizes of M_2 was chosen to be 45/0.24. For the given topology, it is expected to improve the noise figure by 0.1dB with W_2 = 80μm. To minimize the distributed gate resistance, the MOSFETs were segmented into 5μm-long gate fingers and each of the fingers was contacted at both ends [46]. The



(a)



(b)

Figure 7.11: The power constrained noise performance of the LNA when $R_s = Z_{in} = 50\Omega$ for different pad capacitance. The noise contributions of M_1 substrate and M_2 are included. (a) Noise figure (b) Gain.

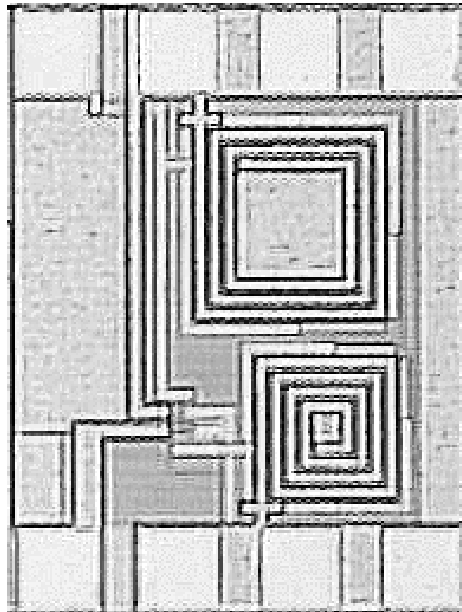


Figure 7.12: Die photo of the LNA

spiral inductor L_s was implemented using the metal-5 layer and its value was chosen to be 1.1nH to provide 50Ω of real part of the input impedance, in combination with C_p. The inductor was designed based on the compact model presented by [73]; a patterned ground shield was employed to reduce the substrate parasitics of the spiral inductor [74]. To suppress extra noise, the pad capacitor was implemented using metal-5 and metal-1 layers, giving 47fF of capacitance. Since the required gate inductor L_g to cancel out the imaginary part of the input impedance was 36nH, which is too large to be integrated, an external inductor was used along with a bondwire inductor. Finally, to control the parasitic inductance from L_s to ground, the die was mounted on a special LLP package [75], that allows direct downbonding to the large ground plane as shown in Figure 7.13.

The real term of the input impedance of the fabricated LNA was 54Ω and was adjusted to 50Ω using an off-chip tuner. Table 7.1 summarizes the performance of the LNA. With

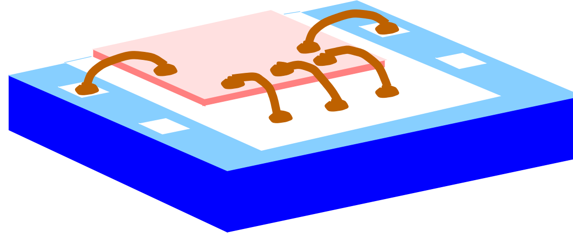


Figure 7.13: Wire-bonding illustration of the LLP package

3.75mA of bias current, the LNA achieves about 0.9dB of noise figure, which is the lowest reported noise figure with a perfect power match for a CMOS LNA [76] and adds just 0.3dB to the NF_{min} of the intrinsic MOSFET device. The measured noise figure is also quite close to the expected value and demonstrates that the proposed methodology accurately predicts the noise performance of custom integrated LNA designs. Since the threshold voltage is

Table 7.1: Measured Performance of an 800MHz LNA

Parameters	Measured Value
Frequency	800 MHz
Supply Voltage	2.0 V
Power Consumption	7.5 mW
Noise Figure	0.9±0.2 dB
Available Gain	8.8 dB
s_{11}	-38.1 dB
IIP3	7.1 dBm
1dB Compression	-6.5 dBm
Die Area	0.19 mm^2

relatively high in the given technology, further process adjustments can potentially reduce the supply voltage as well as the power consumption.

7.4 Summary

Based on the measured noise parameters of the 0.24μm MOSFET, and on the results derived from noisy two-port theory, explicit guidelines for a fully integrated LNA design are presented. The measured noise parameters can be scaled directly with the device width; device sizing can be utilized for power-constrained design. The noise performance of the tuned LNA is primarily controlled by the source degeneration inductance, which determines both the power matching and the noise matching conditions. Therefore, if arbitrary values of source impedance are allowed, the optimal LNA design can be obtained by adjusting the source inductance. Even if the source impedance is fixed, the fully integrated LNA can achieve noise performance near NF_{min} by choosing an appropriate device geometry and optimizing the bias conditions. The cascode stage usually introduces at least 40% extra noise power to the input stage; thus its width needs to be optimized.

Although the demonstrated LNA uses a single-ended architecture, future LNA designs will require differential operation since further scaling of the device sizes requires smaller values of source inductance. The results demonstrate that CMOS can be a good candidate for high performance LNA designs, competitive with GaAs and bipolar LNAs.

Chapter 8

Conclusions

THIS DISSERTATION has explored high frequency noise behavior of MOSFETs, addressing issues ranging from the physical origin and contribution mechanism of fundamental noise sources to actual circuit implementation of a CMOS LNA. The presented information should help lower substantially the barrier to the implementation of fully integrated CMOS receivers. To conclude, this chapter summarizes briefly the key contributions presented in the previous chapters.

8.1 Summary

Numerical simulation helps reveal underlying physics and technology issues behind macroscopic noise behavior. The impedance field method is a very popular technique in device noise simulation and it was theoretically extended up to three dimensions (3-D). Due to substantial cost for implementation and simulation, however, it has been used only for two-dimensional analysis; higher order transport models, such as the hydrodynamic formulation, were not used in multi-dimensional simulations. Investigating the separate noise sources in the MOSFET imposes different requirements; to date there has been no unified

simulation method proposed. In Chapter 3, a quasi two-dimensional simulation technique for the analysis of channel noise is proposed. This technique is based on an active transmission line concept but uses two-dimensional device simulation. It is also the first known attempt to use the hydrodynamic model in two-dimensional noise simulations.

Chapter 4 discusses the importance of parasitic noise components in the MOSFET and how they can be deembedded. The additive noise component induced from the substrate is shown to interlink the substrate component to the issue of excess channel noise. The results of full two-dimensional noise simulations demonstrate that the commonly assumed noise spectrum needs to be modified and the substrate component leads to controversy in understanding and quantifying of excess noise. Chapter 5 investigates the physical origin of the excess channel noise based on quasi two-dimensional simulations. The results confront the conventional modeling approaches, typically based on the hot-carrier effects, and propose that higher local ac resistance near the source junction is developed due to the non-local transport behavior of carriers which in turn results in the excess noise. The conclusions of Chapters 4 and 5 offer important clues, both in terms of how to improve compact noise models and also improve noise performance of intrinsic MOSFET devices as well as to develop novel device structures yielding better noise characteristics. Chapter 6 surveys existing compact noise models and proposes a physically sound modeling approach for MOSFET noise.

The design of the LNA is the subject of Chapter 7. A new design approach and explicit guidelines for a fully integrated LNA design are presented. Compared with prior approaches, the proposed approach is highly intuitive since it is based on noisy two-port theory. The noise matching condition is primarily determined by the source degeneration inductance, under a perfect power match. The optimum source inductance determines both the power matching and the noise matching conditions and, on the other hand, it is determined by bias conditions and the size of the device. Thus, the optimum design condition

can be found either by changing the power match condition or by changing the device size. This theoretical development enables a 0.9dB noise figure for a single ended LNA, operating at 800MHz with 3.75mA of bias current.

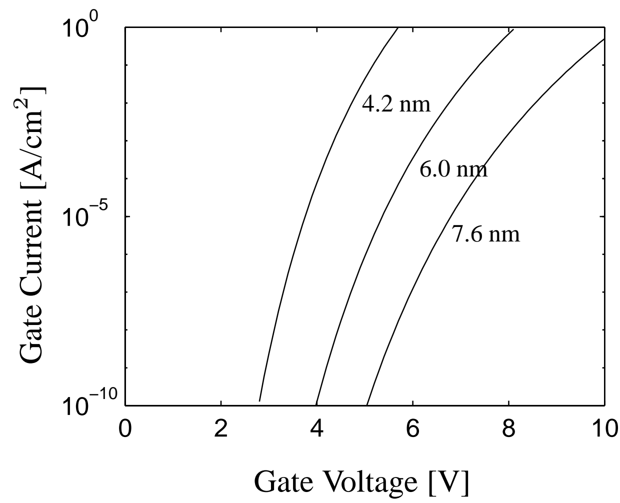
8.2 Recommendations for Future Work

There are various challenging issues that await exploration in future research. Noise characterization is one area that needs more work. Although reliable data acquisition is the backbone of the entire research, measurement of ultra low noise is not satisfactory yet.

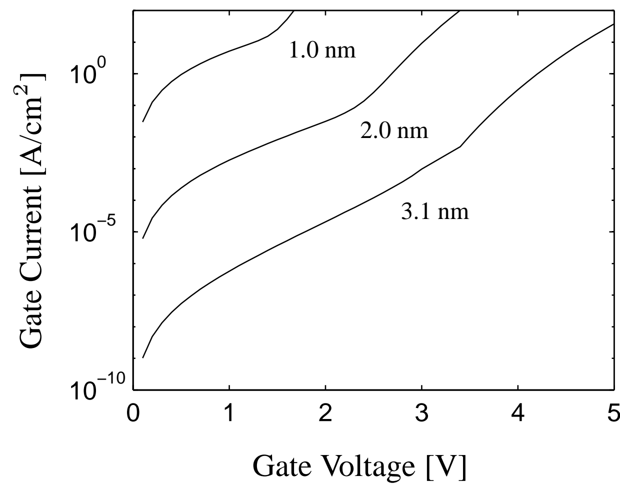
Numerical noise simulation poses several ongoing challenges. First, it is strongly desirable to fully exploit multidimensional features available in advanced transport models. This provides a means to investigate the substrate induced channel noise and new device structures for noise improvement.

Another challenge for numerical simulation is inclusion of tunneling current into the simulator. Traditionally, the gate oxide of a MOSFET has been considered as a perfect barrier for carriers allowing no current flow between the gate and silicon. In fact, there is tunneling of electrons from the vicinity of the electrode Fermi level through the forbidden energy gap into the conduction band of the oxide. Such a phenomenon is called Fowler-Nordheim tunneling [77]. The perfect barrier assumption has been valid in most practical situations because the Fowler-Nordheim tunneling current has been negligibly small as shown in Figure 8.1 (a).

As demonstrated in Figure 8.1 (b), however, ultra-thin oxides below 4 nm exhibit drastic increase of leakage current, so called direct tunneling current [78]. In this regime, the gate oxide capacitor would introduce an extra noise current source, possibly a shot noise current source, besides the two classical noise sources considered here: drain and gate current noise. Fortunately, the IR drop along the gate polysilicon due to the leakage current is



(a)



(b)

Figure 8.1: Gate oxide tunneling current in MOSFETs. (a) Fowler-Nordheim tunneling current. (b) Direct tunneling current.

negligible; also, the additional conductances ($1/r_{gs}$ and $1/r_{gd}$ in Figure 8.2) associated with this tunneling across the gate oxide are small compared with ωC_{gs} and ωC_{gd} in the range above the $1/f$ corner frequency, which is usually few MHz in MOSFETs.

By contrast, the impact of the direct tunneling current on high frequency noise performance is becoming critical. The gate shot noise current generated in each segment of the MOSFET flows along the channel and subsequently creates drain shot noise current as well, because it is uncorrelated with the origins of the drain and gate current noise [79]. Since

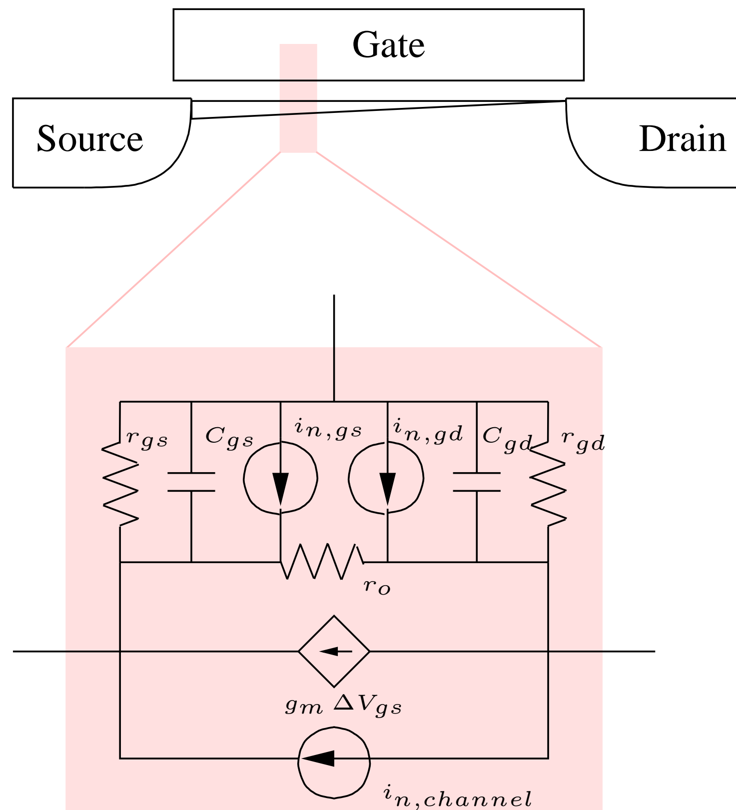


Figure 8.2: Local small-signal equivalent circuit for a segment of MOSFET in which the direct tunneling current is significant.

the direct tunneling current can be substantial, the drain shot noise becomes comparable to the drain current noise in MOSFETs with oxides below 2 nm. While a rigorous modeling of the direct tunneling current is a prerequisite to accounting for this effect, accurate modeling of tunneling in MOSFETs involves evaluation of the multi-dimensional Schrödinger equation – an unsolved problem to date.

In circuit design, it is desirable to have a new CAD tool incorporating the proposed intuitive approach for LNA design. Besides, further device scaling leads to a reduction in supply voltage and presents a challenge to new circuit topologies for overcoming limited voltage headroom.

Appendix A

Two-Port Theory

A TWO-PORT is simply the circuit theory representation for a network inside a black box as illustrated in Figure A.1, considered to consist of only *two pairs* of accessible terminals – usually representing the input and output respectively. It is a powerful and widely used technique for analyzing low-frequency circuits, along with the Kirchhoff laws. In general, this technique cannot be directly applied to microwave circuits. Nevertheless

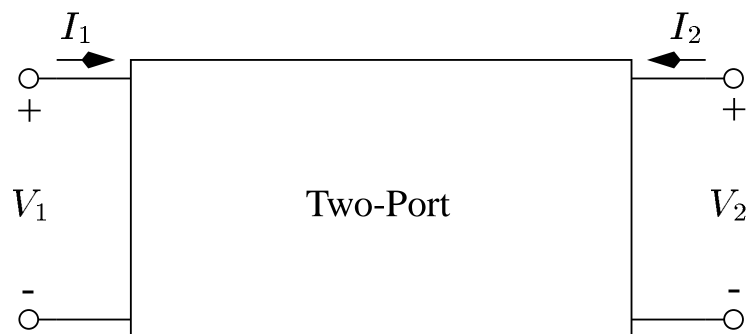


Figure A.1: General two-port diagram.

it can be extended to handle many cases that arise in microwave analysis. Thus analysis includes noise properties of networks since the primary concerns are usually some type of *global quantities*, such as the voltage and current at terminals or the power flow through a device.

A.1 General Two-Port Matrices

Once voltages and currents have been defined at various points in a network, the *impedance* ($\overrightarrow{Z}$) and *admittance* ($\overrightarrow{Y}$) matrices can be acquired as follows:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \qquad \overrightarrow{Z} \triangleq \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \tag{A.1}$$

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \qquad \overrightarrow{Y} \triangleq \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \tag{A.2}$$

These matrices are very popular since they lend themselves directly to the development of equivalent circuits.

Other popular matrices include $ABCD$ ($\overrightarrow{A}$, also known as *transmission* or *chain* matrix) and *hybrid* ($\overrightarrow{H}$) matrices:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \qquad \overrightarrow{A} \triangleq \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} \tag{A.3}$$

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix} \qquad \overrightarrow{H} \triangleq \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix} \tag{A.4}$$

Note that one variable used in $\overrightarrow{A}$ matrix is $-I_2$ rather than I_2; for historical reasons it is

preferred in modeling cascaded connections.

As the frequency approaches to the microwave range, equivalent voltages and currents and the related matrices become an abstracted sum since direct measurements involve the magnitude as well as phase of a traveling wave or a standing wave. A representation more in accordance with the ideas of incident, reflected, and transmitted waves is given by the *scattering* matrix ($\overrightarrow{S}$), defined in relation to these incident and reflected voltage waves as:

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix} \qquad \overrightarrow{S} \triangleq \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \tag{A.5}$$

Useful conversions for two-port network parameters are given in Table A.1.

A.2 Noise Correlation Matrices

Two-port theory provides a means to represent a noisy two-port in terms of a noiseless two-port and its corresponding two noise sources [68] as illustrated in Figure A.2. Depending on the type of noise sources, six representations can be derived but the following three representations are particularly useful: admittance for parallel connections, impedance for series connections, and $ABCD$ for a cascade of stages [2].

Mathematically each representation defines noise sources in terms of so-called *correlation matrices*, denoted by $\overrightarrow{C}$ and a subscript which specifies the representation. The elements of matrices are denoted by the spectral densities $C_{s_1 s_2^*}$, which are defined as the Fourier transform of their auto- and cross-correlation functions, with a subscript referring to the noise sources s_1 and s_2.

Noise sources are usually characterized by their mean fluctuations, that are related to

Table A.1: Conversions between Two-Port Network Parameters [1]

	$\overrightarrow{S}$	$\overrightarrow{Z}$	$\overrightarrow{Y}$	$\overrightarrow{A}$
$\overrightarrow{S}$	S_{11}	$\frac{(Z_{11}-Z_0)(Z_{22}+Z_0)-Z_{12}Z_{21}}{\Delta Z}$	$\frac{(Y_0-Y_{11})(Y_0+Y_{22})+Y_{12}Y_{21}}{\Delta Y}$	$\frac{A_{11}+A_{12}/Z_0-A_{21}Z_0-A_{22}}{A_{11}+A_{12}/Z_0+A_{21}Z_0+A_{22}}$
	S_{12}	$\frac{2Z_{12}Z_0}{\Delta Z}$	$\frac{-2Y_{12}Y_0}{\Delta Y}$	$\frac{2(A_{11}A_{22}-A_{12}A_{21})}{A_{11}+A_{12}/Z_0+A_{21}Z_0+A_{22}}$
	S_{21}	$\frac{2Z_{21}Z_0}{\Delta Z}$	$\frac{-2Y_{21}Y_0}{\Delta Y}$	$\frac{2}{A_{11}+A_{12}/Z_0+A_{21}Z_0+A_{22}}$
	S_{22}	$\frac{(Z_{11}+Z_0)(Z_{22}-Z_0)-Z_{12}Z_{21}}{\Delta Z}$	$\frac{(Y_0+Y_{11})(Y_0-Y_{22})+Y_{12}Y_{21}}{\Delta Y}$	$\frac{-A_{11}+A_{12}/Z_0-A_{21}Z_0+A_{22}}{A_{11}+A_{12}/Z_0+A_{21}Z_0+A_{22}}$
$\overrightarrow{Z}$	$Z_0\frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$	Z_{11}	$\frac{Y_{22}}{\|Y\|}$	$\frac{A_{11}}{A_{21}}$
	$Z_0\frac{2S_{12}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$	Z_{12}	$\frac{-Y_{12}}{\|Y\|}$	$\frac{A_{11}A_{22}-A_{12}A_{21}}{A_{21}}$
	$Z_0\frac{2S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$	Z_{21}	$\frac{-Y_{21}}{\|Y\|}$	$\frac{1}{A_{21}}$
	$Z_0\frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$	Z_{22}	$\frac{Y_{11}}{\|Y\|}$	$\frac{A_{22}}{A_{21}}$
$\overrightarrow{Y}$	$Y_0\frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$	$\frac{Z_{22}}{\|Z\|}$	Y_{11}	$\frac{A_{22}}{A_{12}}$
	$Y_0\frac{-2S_{12}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$	$\frac{-Z_{12}}{\|Z\|}$	Y_{12}	$\frac{A_{12}A_{21}-A_{11}A_{22}}{A_{12}}$
	$Y_0\frac{-2S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$	$\frac{-Z_{21}}{\|Z\|}$	Y_{21}	$\frac{-1}{A_{12}}$
	$Y_0\frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$	$\frac{Z_{11}}{\|Z\|}$	Y_{22}	$\frac{A_{11}}{A_{12}}$
$\overrightarrow{A}$	$\frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{2S_{21}}$	$\frac{Z_{11}}{Z_{21}}$	$\frac{-Y_{22}}{Y_{21}}$	A_{11}
	$Z_0\frac{(1+S_{11})(1+S_{22})-S_{12}S_{21}}{2S_{21}}$	$\frac{\|Z\|}{Z_{21}}$	$\frac{-1}{Y_{21}}$	A_{12}
	$\frac{1}{Z_0}\frac{(1-S_{11})(1-S_{22})-S_{12}S_{21}}{2S_{21}}$	$\frac{1}{Z_{21}}$	$\frac{-\|Y\|}{Y_{21}}$	A_{21}
	$\frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{2S_{21}}$	$\frac{Z_{22}}{Z_{21}}$	$\frac{-Y_{11}}{Y_{21}}$	A_{22}

$$|Z| = Z_{11}Z_{22} - Z_{12}Z_{21} \qquad |Y| = Y_{11}Y_{22} - Y_{12}Y_{21}$$

$$\Delta Z = (Z_{11} + Z_0)(Z_{22} + Z_0) - Z_{12}Z_{21} \qquad \Delta Y = (Y_{11} + Y_0)(Y_{22} + Y_0) - Y_{12}Y_{21}$$

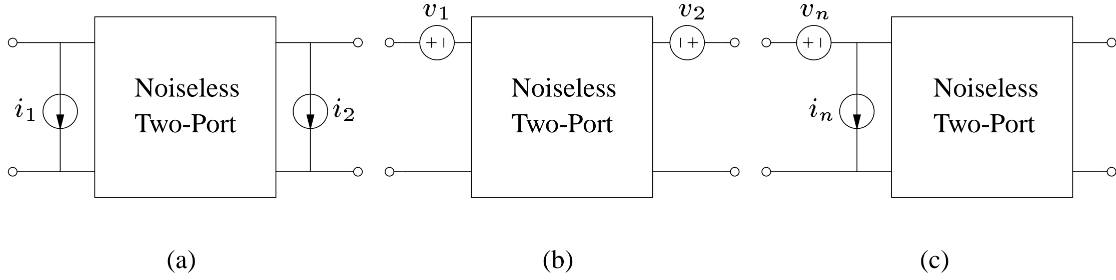


Figure A.2: Equivalent noise circuit of a two-port. (a) Admittance representation (b) Impedance representation (c) $ABCD$ representation.

power spectral densities as follows:

$$\overline{s_i s_j^*} \;=\; 2\Delta f C_{s_i s_j^*} \qquad i, j = 1, 2 \tag{A.6}$$

The factor 2 occurs since the frequency range has been taken from $-\infty$ to $+\infty$.

A.2.1 Admittance Representation

This representation is useful when two networks $\overrightarrow{Y}_1$ and $\overrightarrow{Y}_2$ are connected in parallel:

$$\overrightarrow{C}_Y \;=\; \overrightarrow{C}_{Y_1} + \overrightarrow{C}_{Y_2} \tag{A.7}$$

$$\overrightarrow{C}_Y \;\triangleq\; \begin{bmatrix} C_{i_1 i_1^*} & C_{i_1 i_2^*} \\ C_{i_2 i_1^*} & C_{i_2 i_2^*} \end{bmatrix} = 2kT\Re[\overrightarrow{Y}] \tag{A.8}$$

where $\Re[\ ]$ denotes the real part of a complex number and $\overrightarrow{C}_Y$ denotes the correlation matrix of the admittance representation, in which $C_{i_m i_n^*}$ are the self- or cross-power spectral

densities of the input and output current noise sources, as illustrated in Figure A.2 (a).

A.2.2 Impedance Representation

This representation is useful when two networks $\overrightarrow{Z}_1$ and $\overrightarrow{Z}_2$ are connected in series:

$$\overrightarrow{C}_Z = \overrightarrow{C}_{Z_1} + \overrightarrow{C}_{Z_2} \tag{A.9}$$

$$\overrightarrow{C}_Z \triangleq \begin{bmatrix} C_{v_1v_1^*} & C_{v_1v_2^*} \\ C_{v_2v_1^*} & C_{v_2v_2^*} \end{bmatrix} = 2kT\Re[\overrightarrow{Z}] \tag{A.10}$$

where $\overrightarrow{C}_Z$ denotes the correlation matrix of the impedance representation, in which $C_{v_mv_n^*}$ are the self- or cross-power spectral densities of the input and output voltage noise sources, as illustrated in Figure A.2 (b).

A.2.3 $ABCD$ Representation

This representation is useful when two networks $\overrightarrow{A}_1$ and $\overrightarrow{A}_2$ are cascaded:

$$\overrightarrow{C}_A = \overrightarrow{A}_1\overrightarrow{C}_{A_2}\overrightarrow{A}_1^{\dagger} + \overrightarrow{C}_{A_1} \tag{A.11}$$

$$\overrightarrow{C}_A \triangleq \begin{bmatrix} C_{v_nv_n^*} & C_{v_ni_n^*} \\ C_{i_nv_n^*} & C_{i_ni_n^*} \end{bmatrix} \tag{A.12}$$

$$= 2kT \begin{bmatrix} R_n & \frac{F_{min}-1}{2} - R_nY_{opt}^* \\ \frac{F_{min}-1}{2} - R_nY_{opt} & R_n|Y_{opt}|^2 \end{bmatrix} \tag{A.13}$$

where $\overrightarrow{C}_A$[1] denotes the correlation matrix of the $ABCD$ representation, in which $C_{v_n i_n^*}$ are the self- or cross-power spectral densities of the input referred noise sources, as illustrated in Figure A.2 (c). This representation is particularly useful since the correlation matrix can be directly obtained from the measured noise characteristics, even in cases when the correlation matrix cannot be derived from theory. Also this representation is simpler than others since the noise sources are located at the input port, thus they are totally separated from the gain and matching parameters.

[1]There is a typographical error in [2], which is corrected in [80].

Table A.2: Transformation Matrices to Calculate Noise Matrices of Other Representations [2]

		Original Representation		
		Admittance	Impedance	$ABCD$
Resulting Representation	Admittance	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}$	$\begin{bmatrix} -Y_{11} & 1 \\ -Y_{21} & 0 \end{bmatrix}$
	Impedance	$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & -Z_{11} \\ 0 & -Z_{21} \end{bmatrix}$
	$ABCD$	$\begin{bmatrix} 0 & A_{12} \\ 1 & A_{22} \end{bmatrix}$	$\begin{bmatrix} 1 & -A_{11} \\ 0 & -A_{21} \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$

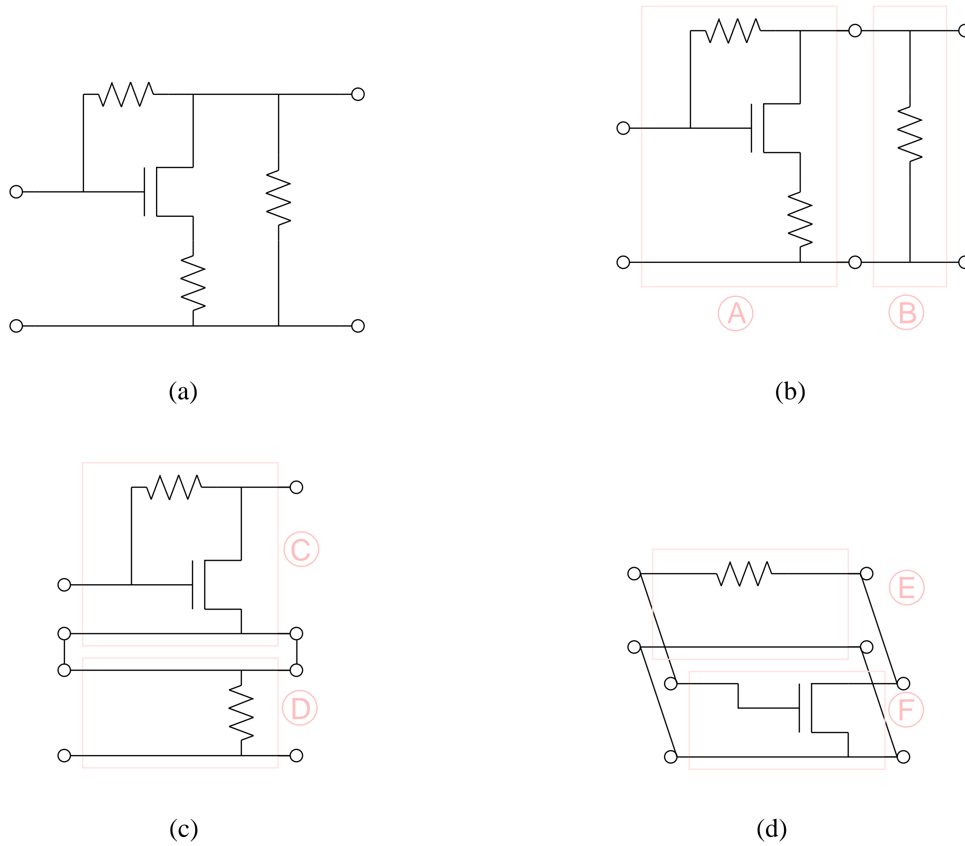


Figure A.3: Circuit decomposition for noise analysis (a) Entire circuit (b) Cascode decomposition (c) Series decomposition (d) Parallel decomposition

A.2.4 Transformation into Other Representations

Each representation can be transformed into another by the matrix operation:

$$\overrightarrow{C}' = \overrightarrow{T}\,\overrightarrow{C}\,\overrightarrow{T}^{\dagger} \tag{A.14}$$

where $\overrightarrow{C}$ and $\overrightarrow{C}'$ are the noise correlation matrices of the original and resulting representations respectively, $\overrightarrow{T}$ is the transformation matrix given in Table A.2, and $\overrightarrow{T}^{\dagger}$ is the transpose conjugate of $\overrightarrow{T}$.

A.2.5 Noise Analysis for Circuits

Based on two-port theory, the net noise performance can be calculated based on correlation matrices of each building block; or, conversely parasitic noise components can be deembedded to get intrinsic noise performance of a specific block. The circuit illustrated in Figure A.3 (a) consists of a MOSFET and three resistors: basic two-port blocks B, D, E, and F. Once each basic two-port is specified by their electrical and correlation matrices, the noise performance of the entire circuit is obtained by adding block by block. For example, the block C in Figure A.3 (c) results from a parallel connection of block E and F as shown in Figure A.3 (d); block A is determined by connecting block C and D in series as shown in Figure A.3 (c); finally, the entire circuit is obtained by cascading block A and B as shown in Figure A.3 (b). Depending on the kind of connection, the noise matrices of the given sub-blocks need to be transformed to a designated form as discussed previously.

A.3 Derivation of Four Noise Parameters

A.3.1 How the Four Noise Parameters Are Defined

The four noise parameters represent a behavior-level modeling of the $ABCD$ representation. When a noisy network is connected to a noise source $\overline{i_s^2}$ as illustrated in Figure A.4, based on Equation (2.13), the noise figure of the network can be derived in terms of $R_n - G_u - G_c - B_c$ representation as follows:

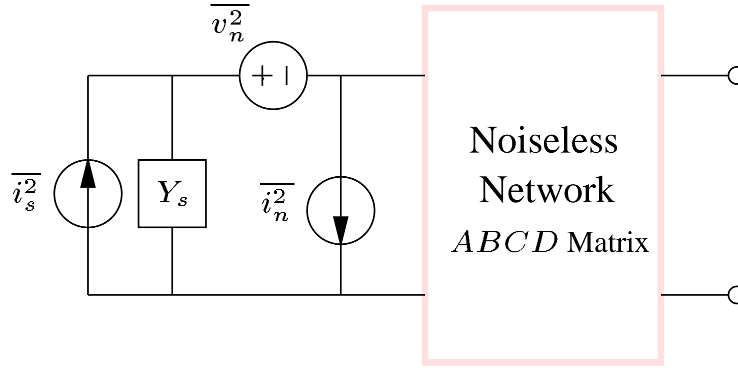


Figure A.4: Circuit diagram for the noise figure calculation of general two port networks

$$F = \frac{\overline{i_s^2} + \overline{|i_n + Y_s v_n|^2}}{\overline{i_s^2}} \tag{A.15}$$

$$= \frac{\overline{i_s^2} + \overline{|(i_c + i_u) + Y_s v_n|^2}}{\overline{i_s^2}} \tag{A.16}$$

$$= \frac{\overline{i_s^2} + \overline{|(Y_c v_n + i_u) + Y_s v_n|^2}}{\overline{i_s^2}} \tag{A.17}$$

$$= \frac{\overline{i_s^2} + \overline{|i_u + (Y_c + Y_s) v_n|^2}}{\overline{i_s^2}} \tag{A.18}$$

$$= 1 + \frac{\overline{i_u^2} + |Y_c + Y_s|^2 \overline{v_n^2}}{\overline{i_s^2}} \tag{A.19}$$

$$= 1 + \frac{\overline{i_u^2} + [(G_c + G_s)^2 + (B_c + B_s)^2] \overline{v_n^2}}{\overline{i_s^2}} \tag{A.20}$$

$$\triangleq 1 + \frac{G_u + [(G_c + G_s)^2 + (B_c + B_s)^2] R_n}{G_s} \tag{A.21}$$

$$\overline{i_s^2} \triangleq 4kT\Delta f G_s \tag{A.22}$$

$$\overline{i_u^2} \triangleq 4kT\Delta f G_u \tag{A.23}$$

$$\overline{v_n^2} \triangleq 4kT\Delta f R_n \tag{A.24}$$

where i_c is the component of i_n that is correlated with v_n, i_u is the component of i_n that is uncorrelated with v_n, and Y_c is the correlation admittance.

Since the derived expression of the noise figure is a function of the source admittance (Y_s), taking the derivative of Equation (A.21) with respect to Y_s yields the condition to achieve the minimum noise figure:

$$\frac{\partial F}{\partial G_s} = \frac{-G_u - [G_c^2 - G_s^2 + (B_c + B_s)^2]R_n}{G_s^2} \tag{A.25}$$

$$\frac{\partial F}{\partial B_s} = \frac{2(B_c + B_s)R_n}{G_s} \tag{A.26}$$

The source admittance which results in Equations (A.25) and (A.26) going to zero is determined by:

$$G_{opt} \triangleq \sqrt{\frac{G_u}{R_n} + G_c^2} \tag{A.27}$$

$$B_{opt} \triangleq -B_c \tag{A.28}$$

Introducing these two newly defined quantities removes G_u from Equation (A.21):

$$F = 1 + \frac{(G_{opt}^2 - G_c^2)R_n}{G_s} + \frac{[(G_c + G_{opt}) + (G_s - G_{opt})]^2 R_n}{G_s} + \frac{[(B_c + B_{opt}) + (B_s - B_{opt})]^2 R_n}{G_s} \tag{A.29}$$

Since $B_c + B_{opt} = 0$, rearranging Equation (A.29) yields another representation of the noise

figure, $F_{min} - R_n - G_{opt} - B_{opt}$, as follows:

$$F = 1 + 2R_n(G_{opt} + G_c) + \frac{[(G_s - G_{opt})^2 + (B_s - B_{opt})^2]R_n}{G_s}$$

$$\triangleq F_{min} + \frac{|Y_s - Y_{opt}|^2 R_n}{G_s} \quad \text{(A.30)}$$

$$F_{min} \triangleq 1 + 2R_n(G_{opt} + G_c) \quad \text{(A.31)}$$

A.3.2 Relationship between $F_{min} - R_n - G_{opt} - B_{opt}$ and $\overline{v_n^2} - \overline{i_n^2}$

The relationship between the four noise parameters and noise sources can be found by solving Equations (A.6), (A.12), and (A.13) as follows:

$$F_{min} = 1 + \frac{\overline{v_n i_n^*} + \overline{v_n^2}\, Y_{opt}^*}{2\, k\, T\, \Delta f} \quad \text{(A.32)}$$

$$R_n = \frac{\overline{v_n^2}}{4kT\Delta f} \quad \text{(A.33)}$$

$$Y_{opt} = \sqrt{\frac{\overline{i_n^2}}{\overline{v_n^2}} - \left(\Im\left[\frac{\overline{v_n i_n^*}}{\overline{v_n^2}}\right]\right)^2} + j\Im\left[\frac{\overline{v_n i_n^*}}{\overline{v_n^2}}\right] \quad \text{(A.34)}$$

A.3.3 Relationship between $F_{min} - R_n - G_{opt} - B_{opt}$ and $\overline{i_g^2} - \overline{i_d^2}$

Direct transformation using Table A.2 gives:

$$\overline{v_n^2} = |A_{12}|^2 \overline{i_d^2} \quad \text{(A.35)}$$

$$\overline{v_n i_n^*} = A_{12}\overline{i_d i_g^*} + A_{12}A_{22}^*\overline{i_d^2} \quad \text{(A.36)}$$

$$\overline{i_n^2} = \overline{i_g^2} + A_{22}\overline{i_d i_g^*} + A_{22}^*\overline{i_g i_d^*} + |A_{22}|^2\overline{i_d^2} \quad \text{(A.37)}$$

Substituting them into Equations (A.33) and (A.34) yields:

$$F_{min} = 1 + \frac{|A_{12}|^2\overline{i_d^2}}{2kT\Delta f}\left[\sqrt{\frac{\overline{i_g^2} - |\overline{i_g i_d^*}|^2/\overline{i_d^2}}{|A_{12}|^2\overline{i_d^2}} + \Re\left(\frac{A_{22}}{A_{12}} + \frac{1}{A_{12}}\frac{\overline{i_g i_d^*}}{\overline{i_d^2}}\right)^2} \quad \text{(A.38)}$$

$$+ \Re\left(\frac{A_{22}}{A_{12}} + \frac{1}{A_{12}}\frac{\overline{i_g i_d^*}}{\overline{i_d^2}}\right)\right] \quad \text{(A.39)}$$

$$R_n = |A_{12}|^2\frac{\overline{i_d^2}}{4kT\Delta f} \quad \text{(A.40)}$$

$$Y_{opt} = \sqrt{\frac{\overline{i_g^2} - |\overline{i_g i_d^*}|^2/\overline{i_d^2}}{|A_{12}|^2\overline{i_d^2}} + \Re\left(\frac{A_{22}}{A_{12}} + \frac{1}{A_{12}}\frac{\overline{i_g i_d^*}}{\overline{i_d^2}}\right)^2} - j\Im\left(\frac{A_{22}}{A_{12}} + \frac{1}{A_{12}}\frac{\overline{i_g i_d^*}}{\overline{i_d^2}}\right) \quad \text{(A.41)}$$

If the distributed and Miller effects are negligible, the network parameters can be approximated as:

$$A_{12} \approx -\frac{1}{g_m} \quad \text{(A.42)}$$

$$A_{22} \approx -\frac{j\omega C_{gs}}{g_m} \quad \text{(A.43)}$$

Combining these equations with the drain and gate current noise power spectrum given in

Equations (2.4) – (2.7) yields:

$$F_{min} \approx 1 + \frac{\omega}{\omega_T}\sqrt{\gamma\delta\zeta(1-|c|^2)} \tag{A.44}$$

$$R_n \approx \frac{\gamma g_{d0}}{g_m^2} \tag{A.45}$$

$$G_{opt} \approx \frac{g_m \omega C_{gs}}{g_{d0}}\sqrt{\frac{\delta\zeta(1-|c|^2)}{\gamma}} \tag{A.46}$$

$$B_{opt} \approx -\omega C_{gs}\left(1 - c\frac{g_m}{g_{d0}}\sqrt{\frac{\delta\zeta}{\gamma}}\right) \tag{A.47}$$

Inversely, $\overline{i_g^2} - \overline{i_g i_d^*} - \overline{i_d^2}$ can be expressed in terms of $F_{min} - R_n - G_{opt} - B_{opt}$:

$$\overline{i_g^2} = 4kT\Delta f R_n\Big(|Y_{opt}|^2 + |Y_{11}|^2 - 2\Re[Y_{11}Y_c^*]\Big) \tag{A.48}$$

$$\overline{i_g i_d^*} = 4kT\Delta f R_n (Y_{11} - Y_c)Y_{21}^* \tag{A.49}$$

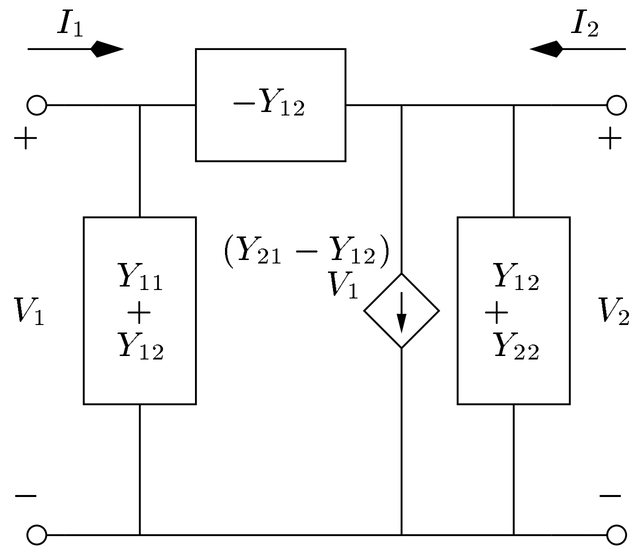
$$\overline{i_d^2} = 4kT\Delta f R_n |Y_{21}|^2 \tag{A.50}$$

$$Y_c = \frac{F_{min} - 1}{2R_n} - Y_{opt} \tag{A.51}$$

A.4 Two-Port Parameters of the MOSFET

A.4.1 Y Paramters

Since the FET has a π-configuration by its nature, the Y parameters are widely used in modeling of FETs. Figure A.5 illustrates two different configurations that are particularly useful for noise analysis. At high frequencies, all the parameters have second-order terms due to the distributed nature of the device. At low frequencies, the Y parameters of the



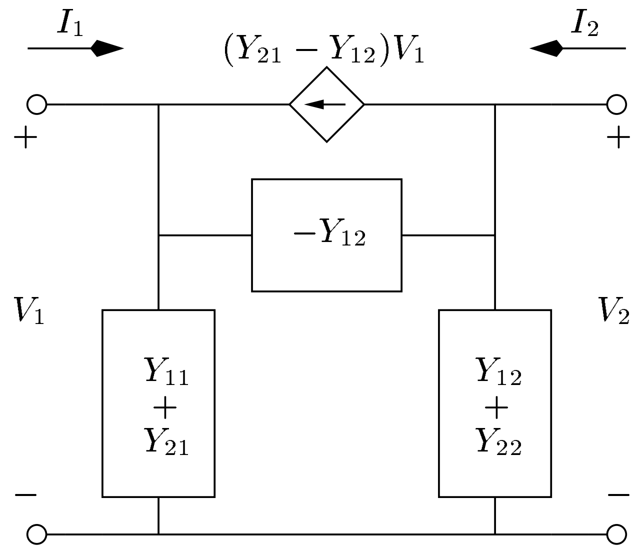


Figure A.5: Y parameters of a MOSFET for different configurations.

MOSFET in a common-source configuration can be approximated as:

$$Y_{11} = j\omega(C_{gs} + C_{gd}) \tag{A.52}$$

$$Y_{12} = -j\omega C_{gd} \tag{A.53}$$

$$Y_{21} = g_m - j\omega C_{gd} \tag{A.54}$$

$$Y_{22} = g_{ds} + j\omega C_{gd} \tag{A.55}$$

where $j = \sqrt{-1}$ and $\omega = 2\pi f$. In the common-gate configuration, the Y parameters are:

$$Y_{11_{CG}} = j\omega C_{gs} - g_m + g_{ds} \tag{A.56}$$

$$Y_{12_{CG}} = -g_{ds} \tag{A.57}$$

$$Y_{21_{CG}} = g_m - g_{ds} \tag{A.58}$$

$$Y_{22_{CG}} = j\omega C_{gd} + g_{ds} \tag{A.59}$$

A.4.2 $ABCD$ Paramters

The $ABCD$ parameters of a MOSFET segment in the common-gate configuration, described in Section 3.1.3, are given by:

$$A_{11_{CG}} = \frac{1 + j\omega\, r_o\, C_{gd}}{1 + g_m\, r_o} \tag{A.60}$$

$$A_{12_{CG}} = \frac{r_o}{1 + g_m\, r_o} \tag{A.61}$$

$$A_{21_{CG}} = -\frac{\omega^2\, r_o\, C_{gs}\, C_{gd}}{1 + g_m\, r_o} + \frac{j\omega[C_{gs} + (1 + g_m\, r_o)C_{gd}]}{1 + g_m\, r_o} \tag{A.62}$$

$$A_{22_{CG}} = \frac{1 + g_m\, r_o + j\omega\, r_o\, C_{gs}}{1 + g_m\, r_o} \tag{A.63}$$

Given $ABCD$ matrices ($\overrightarrow{A}_{CG_i}$, $i = 1 \sim n$) for n segments, the required matrices at abscissa x ($i = k$) are simply

$$T(0, x) = T_1 T_2 \cdots T_{i-1} \quad \text{(A.64)}$$

$$T(x, L) = T_i T_{i+1} \cdots T_n \quad \text{(A.65)}$$

A.4.3 Conversion from Common-Gate Y to Common-Source $ABCD$

When the simulation results are compared with measured data in Section 3.3, the Y parameters, which are the secondary output of the simulator, need to be transformed from the common-gate configuation to the common-source configuation as:

$$A_{11} = \frac{Y_{22_{CG}}}{Y_{21_{CG}} + Y_{22_{CG}}} \quad \text{(A.66)}$$

$$A_{12} = \frac{1}{Y_{21_{CG}} + Y_{22_{CG}}} \quad \text{(A.67)}$$

$$A_{21} = \frac{Y_{11_{CG}} Y_{22_{CG}} - Y_{12_{CG}} Y_{21_{CG}}}{Y_{21_{CG}} + Y_{22_{CG}}} \quad \text{(A.68)}$$

$$A_{22} = \frac{Y_{11_{CG}} + Y_{12_{CG}}}{Y_{21_{CG}} + Y_{22_{CG}}} + 1 \quad \text{(A.69)}$$

Simulation results give common-gate Y parameters while measured data is in common-source configuration.

Appendix B

MOSFET Noise Analysis

B.1 Impedance Field Formulation

As illustrated in Figure 3.4 (a), all electrodes are short-circuited to ground for noise calculations. The noise current i_n is divided into i_{n_1} and i_{n_2}, and subsequently induces v_x (voltage across the local node and gate node), i_x (current flows from the left to right blocks), and three short-circuited electrode currents (i_g, i_d, and i_s). Basic KCL conditions governing the network are:

$$i_n = i_{n_1} + i_{n_2} \tag{B.1}$$

$$i_{n_1} + i_g + i_s + i_x = 0 \tag{B.2}$$

$$i_{n_2} + i_d - i_x = 0 \tag{B.3}$$

Simple two-port network analysis for the left block yields:

$$v_x = V_2(0,x)\big|_{V_1(0,x)=0} = \frac{I_2(0,x)}{Y_{22}(0,x)} = \frac{i_{n_1}}{Y_{22}(0,x)} \tag{B.4}$$

$$i_s = I_1(0,x)\big|_{V_1(0,x)=0} = Y_{12}(0,x)\, v_x \tag{B.5}$$

where the $Y_{ij}(0,x)$s are admittance parameters of the sub-device located between the source and equipotential line passing by x. Also, network analysis for the right block gives:

$$v_x = V_1(x,L)\big|_{V_2(x,L)=0} = \frac{I_1(x,L)}{Y_{11}(x,L)} = \frac{i_{n_2}}{Y_{11}(x,L)} \tag{B.6}$$

$$i_d = I_2(x,L)\big|_{V_2(x,L)=0} = Y_{21}(x,L)\, v_x \tag{B.7}$$

where $Y_{ij}(x,L)$s are admittance parameters of the sub-device located between the equipotential line passing by x and the drain. Then combining Equations (B.1) – (B.7) leads to the impedance field Equations (3.6) and (3.7).

B.2 Unsegmented MOSFET Noise Spectra

Under actual operating conditions, the MOSFET is a nonuniform-lossy-active transmission line where the coefficients are not constant along the channel. However, for the special case under zero drain bias, which can be considered as a uniform transmission line, results can be used for checking validity of the simulation results.

B.2.1 General Uniform Transmission Line

Consider an increamental length Δx for a two-conductor uniform transmission line [81] as shown in Figure B.1, described by the following four parameters:

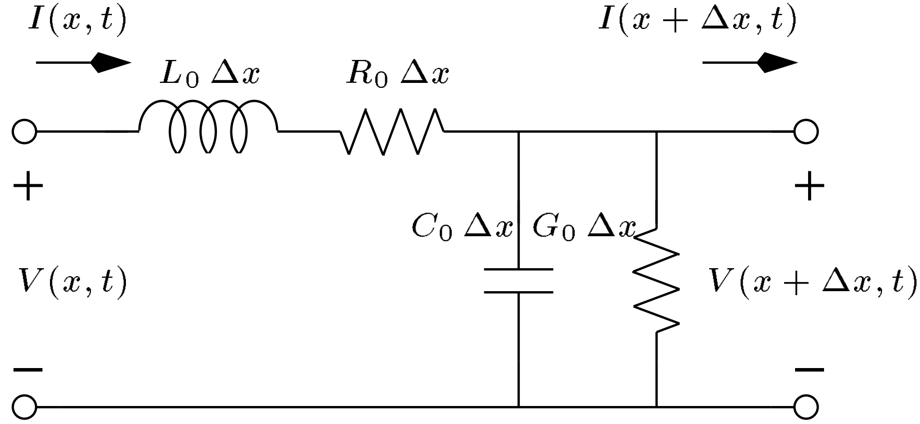


Figure B.1: Equivalent circuit for a differential length Δx of a two-conductor transmission line.

R_0 : resistance per unit length, in Ω/m.

L_0 : inductance per unit length, in H/m.

G_0 : conductance per unit length, in S/m.

C_0 : capacitance per unit length, in F/m.

Based on the coupled time-harmonic uniform transmission line equations using phasor representation, one obtains:

$$\frac{d^2V(x)}{dx^2} = \gamma_p^2 V(x) \tag{B.8}$$

$$\frac{d^2I(x)}{dx^2} = \gamma_p^2 I(x) \tag{B.9}$$

$$\gamma_p = \alpha + j\beta = \sqrt{(R_0 + j\omega L_0)(G_0 + j\omega C_0)} \tag{B.10}$$

where γ_p is the propogation constant whose real and imaginary parts, α and β, are the attenuation constant and phase constant of the line, respectively. The general solutions of

the time-harmonic 1D Helmholtz equations given above are

$$V(x) = V_0^+ e^{-\gamma_p x} + V_0^- e^{+\gamma_p x} \tag{B.11}$$

$$I(x) = I_0^+ e^{-\gamma_p x} + I_0^- e^{+\gamma_p x} \tag{B.12}$$

and the characteristic impedance of the line – the ratio of the voltage and the current at any x for an *infinitely long line* – is given by:

$$Z_0 = \frac{V_0^+ e^{-\gamma_p x}}{I_0^+ e^{-\gamma_p x}} = \frac{R_0 + j\omega L_0}{\gamma_p} = \frac{\gamma_p}{G_0 + j\omega C_0} = \sqrt{\frac{R_0 + j\omega L_0}{G_0 + j\omega C_0}} \tag{B.13}$$

Introducing boundary conditions at the load Z_L yields voltage and current equations at any point along the transmission line as follows:

$$V(x) = I_L(Z_L \cosh \gamma_p x + Z_0 \sinh \gamma_p x) \tag{B.14}$$

$$I(x) = \frac{I_L}{Z_0}(Z_0 \cosh \gamma_p x + Z_L \sinh \gamma_p x) \tag{B.15}$$

Therefore, at a distance x from the load Z_L, the impedance seen looking toward the load at the end of the transmission line, is given by

$$Z_{in}(x) = \frac{V(x)}{I(x)} = Z_0 \frac{Z_L + Z_0 \tanh \gamma_p x}{Z_0 + Z_L \tanh \gamma_p x} \tag{B.16}$$

B.2.2 Lossy Active Transmission Line

As discussed above, at high frequencies a MOSFET must be considered as a distributed RC network, with capacitive coupling to the gate representing a distributed capacitance and the channel itself representing a distributed resistance. The conductance G of the gate insulator and the inductance L of the gate can be neglected. The gate resistance may be

ignored as well, since it is smaller by several orders of magnitude than the inversion layer resistance. In addition to the RC, a transconductance component is needed for FETs to represent their active region gain behavior, but this term is zero under zero drain bias.

When L is the channel length, $R_{channel}$ is the channel resistance, and C_{OX} is the total oxide capacitance, the characteristic properties are:

$$\gamma_p = (1+j)\sqrt{\frac{\omega R_{channel} C_{OX}}{2L^2}} \triangleq \alpha + j\beta \tag{B.17}$$

$$Z_0 = (1-j)\sqrt{\frac{R_{channel}}{\omega C_{OX}}} \tag{B.18}$$

where γ_p is the propogation constant whose real and imaginary parts, α and β, are the attenuation constant and phase constant of the line, respectively; and, Z_0 is the characteristic impedance of the line.

B.2.3 Impedance Field

Based on (B.14) and (B.15), the required network parameters for the impedance field calculation are easily derived:

$$Y_{12}(0,x) = \left.\frac{I_1(0,x)}{V_2(0,x)}\right|_{V_1(0,x)=0} = \left.\frac{-I(0)}{V(x)}\right|_{Z_L=0} = -\frac{1}{Z_0 \sinh \gamma_p x} \tag{B.19}$$

$$Y_{22}(0,x) = \left.\frac{I_2(0,x)}{V_2(0,x)}\right|_{V_1(0,x)=0} = \left.\frac{I(x)}{V(x)}\right|_{Z_L=0} = \frac{\cosh \gamma_p x}{Z_0 \sinh \gamma_p x} \tag{B.20}$$

$$Y_{11}(x,L) = \left.\frac{I_1(x,L)}{V_1(x,L)}\right|_{V_2(0,x)=0} = \left.\frac{I(L-x)}{V(L-x)}\right|_{Z_L=0} = \frac{\cosh \gamma_p (L-x)}{Z_0 \sinh \gamma_p (L-x)} \tag{B.21}$$

$$Y_{21}(x,L) = \left.\frac{I_2(x,L)}{V_1(x,L)}\right|_{V_2(0,x)=0} = \left.\frac{-I(0)}{V(L-x)}\right|_{Z_L=0} = -\frac{1}{Z_0 \sinh \gamma_p (L-x)} \tag{B.22}$$

Taking derivatives after substituting these results into (3.6) and (3.7) yields:

$$\frac{dA_d}{dx} = \frac{\gamma_p \cosh \gamma_p x}{\sinh \gamma_p L} \tag{B.23}$$

$$\frac{dA_g}{dx} = \frac{\gamma_p[\cosh \gamma_p x - \cosh \gamma_p (L-x)]}{\sinh \gamma_p L} \tag{B.24}$$

B.2.4 Noise Power Spectra

If the segments are of infinitesimal size, Equations (3.1) – (3.3) become:

$$S_{i_d} = \int_0^L \left(\frac{dA_d}{dx}\right)\left(\frac{dA_d}{dx}\right)^* S_{i_n}(x)\, dx^2 \tag{B.25}$$

$$S_{i_g} = \int_0^L \left(\frac{dA_g}{dx}\right)\left(\frac{dA_g}{dx}\right)^* S_{i_n}(x)\, dx^2 \tag{B.26}$$

$$S_{i_g i_d} = \int_0^L \left(\frac{dA_g}{dx}\right)\left(\frac{dA_d}{dx}\right)^* S_{i_n}(x)\, dx^2 \tag{B.27}$$

Thus the terminal noise power spectral density terms and their cross correlation coefficient are:

$$K_0 \triangleq 4\, k\, T_n \frac{L}{R_{channel}} \left| \frac{\gamma_p}{\sinh \gamma_p L} \right|^2 \tag{B.28}$$

$$S_{i_d} = K_0 \int_0^L |\cosh \gamma_p x|^2 dx$$

$$= K_0 \frac{\alpha \sin 2\beta L + \beta \sinh 2\alpha L}{4\alpha\beta} \tag{B.29}$$

$$S_{i_g} = K_0 \int_0^L |\cosh \gamma_p x - \cosh \gamma_p (L-x)|^2 dx$$

$$= K_0 \frac{(\cos \beta L - \cosh \alpha L)(\alpha \sin \beta L - \beta \sinh \alpha L)}{\alpha\beta} \tag{B.30}$$

$$\begin{aligned} S_{i_g i_d} &= K_0 \int_0^L [\cosh \gamma_p x - \cosh \gamma_p (L-x)] \cosh \gamma_p^* x dx \\ &= K_0 \frac{(\cos \beta L - \cosh \alpha L)(\alpha \sin \beta L - \beta \sinh \alpha L)}{2\alpha\beta} \end{aligned} \tag{B.31}$$

Appendix C

MEDICI Input Deck for Noise Simulation

```
$=====================================================================
TITLE   MEDICI Example of LDD MOSFET Simulation

$=====================================================================
ASSIGN  NAME=FILE       C.VALUE=Sample.
MESH    IN.FILE=@FILE"mesh"

$=====================================================================
COMMENT Specify models
CONTACT NAME=Gate       WORKFUNC=4.37
MODELS  CONMOB  PRPMOB  FLDMOB  CONSRH  AUGER   TEMP=290

$=====================================================================
COMMENT There are three sets of solution methods available:
+       1. Conven DD solution:  mobility(E), impact ionization(E)
+       2. Approx HD solution:  mobility(E), impact ionization(T)
+                               no temp. enhanced diffusion
+       3. Full   HD solution:  mobility(T), impact ionization(T)
$.....................................................................
ASSIGN  NAME=ELETEMP    L.VALUE=T
ASSIGN  NAME=FULLEB     L.VALUE=T

IF COND=@ELETEMP
    IF COND=@FULLEB
        MODELS    TMPDIF  TMPMOB  II.TEMP   TEMP=290
```

```
    ELSE
        MODELS    ^TMPDIF ^TMPMOB II.TEMP   TEMP=290
    IF.END
    SYMBOL      CARR=1  NEWTON  ELECTRON  ELE.TEMP
    METHOD      ETX.TOL=0.10
ELSE
    SYMBOL      CARR=1  NEWTON  ELECTRON
IF.END

$=========================================================================
COMMENT Solve desired conditions with 2 adjacent biases for noise analysis
ASSIGN  NAME=INITSOL    C.VALUE=@FILE"vg1_0.sol"
ASSIGN  NAME=SOLFILE    C.VALUE=@FILE"sol1_0v"

$.........................................................................
SOLVE   INIT
SOLVE   V(Drain)=0.00   V(Gate)=0.00
+       ELEC=Gate       VSTEP=0.1  NSTEP=9  PREV
SOLVE   V(Gate)=1.00    PREV
+       ^TIF   ^ASCII   OUT.FILE=@INITSOL

$.........................................................................
LOAD    IN.FILE=@INITSOL
LOOP    STEP=4
    ASSIGN      NAME=VDBIAS
    +           N.VALUE=(0.5 1.0 1.5 2.0)
    ASSIGN      NAME=FNAME
    +           C1="0.5"  C2="1.0"  C3="1.5"  C4="2.0"

        SOLVE   V(Gate)=1.0     V(Drain)=@VDBIAS-0.5
        +       ELEC=Drain      VSTEP=0.1      NSTEP=4         PREV

        $...... Solve desired conditions
        SOLVE   V(Gate)=1.0     V(Drain)=@VDBIAS
        +       TIF     ^ASCII  ALL             PREV
        +       OUT.FILE=@SOLFILE@FNAME"_00.tif"
        $...... Solve 2 adjacent biases for noise analysis
        SOLVE   V(Gate)=1.02    V(Drain)=@VDBIAS
        +       TIF     ^ASCII  ALL             PREV
        +       OUT.FILE=@SOLFILE@FNAME"_g+.tif"
        LOAD    IN.FILE =@SOLFILE@FNAME"_00.tif"
        SOLVE   V(Gate)=1.0     V(Drain)=@VDBIAS+0.02
        +       TIF     ^ASCII  ALL             PREV
        +       OUT.FILE=@SOLFILE@FNAME"_d+.tif"
L.END
```

Appendix D

On the Validity of the Pospieszalski Model

As derived in Section 6.2, the correlation in the hybrid representation is:

$$\overline{v_i i_o^*} = \frac{Y_{21}^* - Y_{12}^*}{|Y_{11}|^2}\overline{i_g^2} - \frac{1}{Y_{11}}\overline{i_g i_d^*} \tag{D.1}$$

and Pospieszalski assumed that this quantity is zero.

For long-channel MOSFETs in the saturation region,

$$Y_{11} = j\omega(C_{gs} + C_{gd}) \tag{D.2}$$

$$Y_{21} - Y_{12} = g_m = g_{d0} \tag{D.3}$$

$$\overline{i_g^2} = 4kT\Delta f \, \frac{4}{3} \, \frac{\omega^2 C_{gs}^2}{5 g_{d0}} \tag{D.4}$$

$$\overline{i_g i_d^*} = j0.395\sqrt{\overline{i_g^2}\,\overline{i_d^2}} \tag{D.5}$$

$$\overline{i_d^2} = 4kT\Delta f \, \frac{2}{3} \, g_{d0} \tag{D.6}$$

Substitution these equations into Equation D.1 yields a condition:

$$\frac{C_{gs}}{C_{gs} + C_{gd}} = 0.625 \tag{D.7}$$

which is obviously not true. Thus the assumption of the Pospieszalski model is not valid in MOSFETs.

Appendix E

Noise Model Description

E.1 BSIM4 Noise Model

$$\overline{i_{dp}^2} = 4kT\Delta f \frac{V_{DS,eff}}{I_{DS}}(\beta g_m + \beta g_{mb} + g_d)^2 - 4kT\Delta f R_x (g_m + g_{mb} + g_d)^2 \quad \text{(E.1)}$$

$$\overline{v_{R_s}^2} = 4kT\Delta f (R_x + R_s) \quad \text{(E.2)}$$

$$R_x \triangleq \theta^2 \frac{V_{DS,eff}}{I_{DS}} \quad \text{(E.3)}$$

$$\beta \triangleq 0.577\left[1 + \text{TNOIA}\ L_{eff}\left(\frac{V_{GST,eff}}{\mathcal{E}_{sat}L_{eff}}\right)^2\right] \quad \text{(E.4)}$$

$$\theta \triangleq 0.37\left[1 + \text{TNOIB}\ L_{eff}\left(\frac{V_{GST,eff}}{\mathcal{E}_{sat}L_{eff}}\right)^2\right] \quad \text{(E.5)}$$

where the default values of two fitting constants TNOIA and TNOIB are respectively 1.5 and 1.0.

E.2 Knoblinger Noise Model

$$\overline{i_d^2} = \overline{i_{d,grad}^2} + \overline{i_{d,sat}^2} \tag{E.6}$$

$$\overline{i_{d,grad}^2} = \frac{4kT\Delta f}{L^2}\mu_{eff}Q_{inv} \tag{E.7}$$

$$\overline{i_{d,sat}^2} = \delta_i \frac{4kT\Delta f I_d}{L^2\mathcal{E}_{sat}} l\sinh(\Delta L/l) \tag{E.8}$$

$$\Delta L = l\ln\left[\frac{(V_{ds}-V_{dsat})/l+\mathcal{E}_m}{\mathcal{E}_{sat}}\right] \tag{E.9}$$

$$\mathcal{E}_m = \mathcal{E}_{sat}\sqrt{1+\left[\frac{V_{ds}-V_{dsat}}{l\mathcal{E}_{sat}}\right]^2} \tag{E.10}$$

$$l = \frac{1}{\lambda}\sqrt{\frac{2x_j\epsilon_{si}\epsilon_0}{3C_{ox}}} \tag{E.11}$$

where $\overline{i_{d,grad}^2}$ is the contribution from the gradual channel region, which the classical long channel model describes, and $\overline{i_{d,sat}^2}$ is the extra contribution for short channel MOSFETs. Two parameters are incorporated: λ is the channel length modulation parameter and δ_i is a fitting constant for noise [19].

E.3 Klein Noise Model

$$\overline{i_d^2} = \frac{4kT\Delta f}{L^2}\mu_{eff}Q_{inv} + \frac{8}{3}\Delta f q v_{sat}\tau_\epsilon \frac{I_d}{L} \tag{E.12}$$

where the saturation velocity v_{sat} is typically 10^5m/sec and the energy relaxation time τ_ϵ is the order of 10^{-12}sec [82].

Appendix F

LNA Analysis Method

F.1 Input Impedance

The simplified circuit diagram for input impedance calculations is illustrated in Figure F.1. Note that the output admittance has been divided into two components since the source electrode of the MOSFET is not grounded while the substrate is still grounded. Then the input impedance is:

$$Z_{in} = \frac{T_1 + T_2 + T_3}{T_4 + T_5} \tag{F.1}$$

$$T_1 = 1 - Y_{12} Z_L \tag{F.2}$$

$$T_2 = Z_{L_s}[Y_{11} + Y_{21} - Y_{12} Z_L (Y_{11} + Y_{21})] \tag{F.3}$$

$$T_3 = g_{ds}(Z_L + Z_{L_s} + Y_{11} Z_L Z_{L_s}) \tag{F.4}$$

$$T_4 = -Y_{12} Y_{21} (Z_L + Z_{L_s}) \tag{F.5}$$

$$T_5 = Y_{11}[1 + (g_{ds} - Y_{12})(Z_L + Z_{L_s})] \tag{F.6}$$

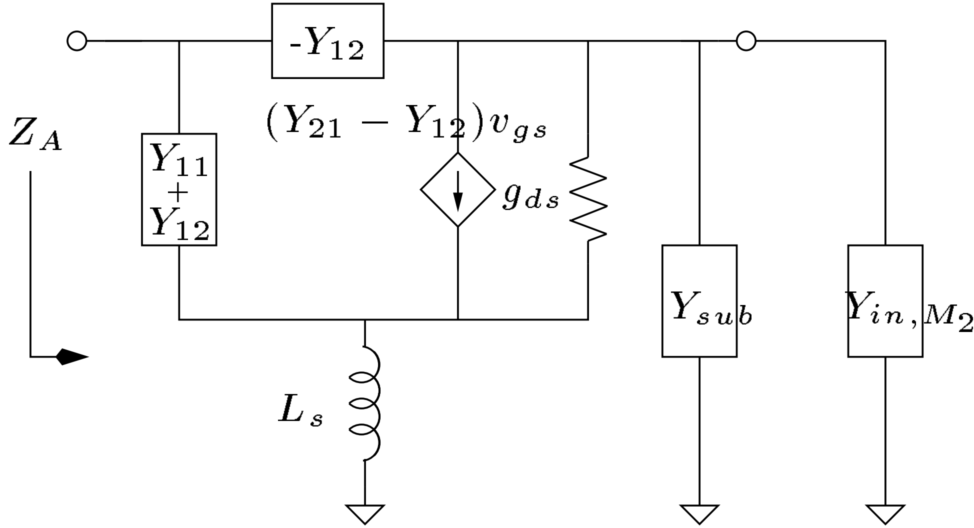


Figure F.1: Schematic diagram for input impedance calculation of the LNA

where

$$Y_{sub} = Y_{12} + Y_{22} - g_{ds} \tag{F.7}$$

$$Y_{in,M_2} \approx Y_{11,M_2} + Y_{21,M_2} \tag{F.8}$$

$$Z_L \triangleq 1/(Y_{sub} + Y_{in,M_2}) \tag{F.9}$$

$$Z_{L_s} = j\omega L_s \tag{F.10}$$

F.2 Noise Analysis Based on Two-Port Theory

As illustrated in Figure F.2, the LNA consists of three cascaded stages. The noise matrix of the first stage ($\boldsymbol{C}_{A,1st}$) can be easily found based on the network parameters. In the second stage, using Equation (A.14), the four-noise parameters of the MOSFET (M_1) need

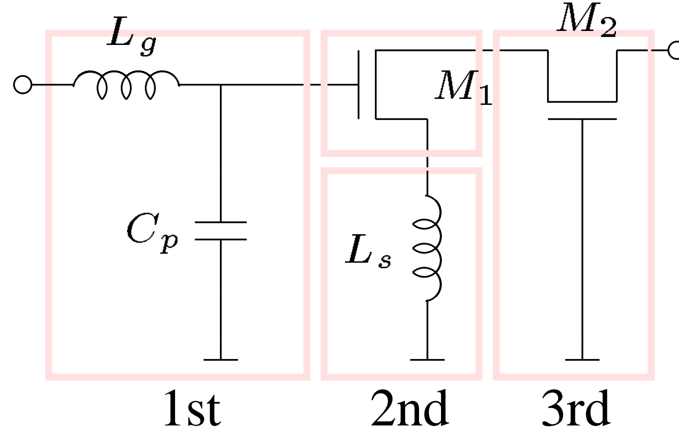


Figure F.2: Noise performance evaluation sequence for the LNA

to be transformed into the impedance noise matrix form ($\boldsymbol{C}_{Z,M_1}$) first and then added to the source inductor component ($\boldsymbol{C}_{Z,L_s}$). Finally the noise matrix of the third stage ($\boldsymbol{C}_{A,3rd}$) can be obtained using (7.12) – (7.14). Note that the noise contribution from Y_{sub} needs to be subtracted from the second stage and added to the third stage. Finally the noise performance of the entire LNA is given by cascading the three stages using (A.11):

$$\boldsymbol{C}_{A,LNA} = \boldsymbol{A}_{1st}\boldsymbol{C}_{A,2nd+3rd}\boldsymbol{A}_{1st}^{\dagger} + \boldsymbol{C}_{A,1st} \tag{F.11}$$

$$\boldsymbol{C}_{A,2nd+3rd} = \boldsymbol{A}_{2nd}\boldsymbol{C}_{A,3rd}\boldsymbol{A}_{2nd}^{\dagger} + \boldsymbol{C}_{A,2nd} \tag{F.12}$$

F.3 Analytical Calculation of Noise Figure

When an off-chip tuner performs a power match by transforming the input impedance of the LNA to 50Ω, the noise figure of the amplifier is:

$$F = \frac{S_{R_s} + S_{M_1} + S_{M_2}}{S_{R_s}} \quad \text{(F.13)}$$

$$S_{R_s} = 4kTR_s|G_{m_1}|^2|A_{i_2}|^2 \quad \text{(F.14)}$$

$$S_{M_1} = 4kT\gamma_1 g_{d0_1}\chi|A_{i_2}|^2/4 \quad \text{(F.15)}$$

$$S_{M_2} = 4kT\gamma_2 g_{d0_2}\xi \quad \text{(F.16)}$$

$$|G_{m_1}| = \frac{\omega_T}{2\omega_0\sqrt{\omega_T L_s R_s}} \quad \text{(F.17)}$$

$$A_{i_2} = i_{out_2}/i_{out_1} \quad \text{(F.18)}$$

$$\chi \triangleq 1 - 2\omega_0 L_s g_m|c|\kappa + (1 + \omega_0^2 L_s^2 g_{m_2}^2)\kappa^2 \quad \text{(F.19)}$$

$$\kappa \triangleq \frac{1}{\omega_0^2 C_{gs_1} L_s}\sqrt{\frac{\delta_1 g_{g_1}}{\gamma_1 g_{d0_1}}} \quad \text{(F.20)}$$

$$\xi \triangleq \eta(g_{ds_1}^2 + \omega_0^2 C_{tot}^2) + \eta^2\rho\tau + \eta\tau^2 \quad \text{(F.21)}$$

$$\eta \triangleq \frac{1}{(g_{ds_1} + g_{m_2})^2 + \omega_0^2 C_{tot}^2} \quad \text{(F.22)}$$

$$\rho \triangleq 2\omega_0 C_{tot} g_{m_2}|c|[(g_{ds_1} + g_{m_2})^2 + \omega_0^2 C_{tot}^2] \quad \text{(F.23)}$$

$$\tau \triangleq g_{m_2}\sqrt{\frac{\delta_2 g_{g_2}}{\gamma_2 g_{d0_2}}} \quad \text{(F.24)}$$

$$C_{tot} \triangleq C_{db_1} + C_{sb_2} + C_{gs_2} \quad \text{(F.25)}$$

In these derivations, the overlap capacitance C_{gd} is neglected for the sake of simplicity. Despite the use of a cascoded stage, this simplification introduces errors. Nevertheless, this analytical approach helps understanding the behind noise contribution mechanism of the LNA.

Bibliography

[1] D. M. Pozar, *Microwave Engineering*, Chapter 4, John Wiley & Sons, Inc., New York, NY, 2nd Edition, 1998.

[2] H. Hillbrand and P. H. Russer, "An Efficient Method for Computer Aided Noise Analysis of Linear Amplifier Networks," *IEEE Transactions on Circuits and Systems*, vol. 23, no. 4, pp. 235–238, Apr. 1976.

[3] Berkeley BSIM Group [On-line], *http://www-device.eecs.berkeley.edu/~bsim3/latenews.html*.

[4] Philips Semiconductor [On-line], *http://www.semiconductors.philips.com/Philips_Models/introduction/mosmodel9/*.

[5] The Electronics Laboratory of EPFL [On-line], *http://legwww.epfl.ch/ekv/*.

[6] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Chapter 10, Cambridge University Press, New York, NY, 1st Edition, 1998.

[7] A. Einstein, "Zur Theorie der Brownschen Bewegung (Theory of Brownian motion)," *Annalen der Physik*, vol. 19, pp. 371–379, 1906.

[8] J. B. Johnson, "Thermal Agitation of Electricity in Conductors," *Nature*, vol. 119, pp. 50–51, 1927.

[9] J. B. Johnson, “Thermal Agitation of Electricity in Conductors,” *Physical Review*, vol. 32, pp. 97–109, July 1928.

[10] H. Nyquist, “Thermal Agitation of Electric Charge in Conductors,” *Physical Review*, vol. 32, no. 7, pp. 110–113, July 1928.

[11] A. van der Ziel, *Noise in Solid State Devices and Circuits*, Chapter 5, John Wiley & Sons, New York, NY, 1986.

[12] J.-P. Nougier, “Fluctuations and Noise of Hot Carriers in Semiconductor Materials and Devices,” *IEEE Transactions on Electron Devices*, vol. 41, no. 11, pp. 2034–2049, Nov. 1994.

[13] D. K. Shaeffer and T. H. Lee, “A 1.5V, 1.5GHz CMOS Low Noise Amplifier,” *IEEE Journal of Solid-State Circuits*, vol. 32, no. 5, pp. 745–759, May 1997.

[14] A. van der Ziel, *Solid State Physical Electronics*, Chapter 18, Prentice-Hall, Englewood Cliffs, NJ, 3rd Edition, 1976.

[15] A. A. Abidi, “High-Frequency Noise Measurements on FET’s with Small Dimensions,” *IEEE Transactions on Electron Devices*, vol. 33, no. 11, pp. 1801–1805, Nov. 1986.

[16] R. P. Jindal, “Hot-Electron Effects on Channel Thermal Noise in Fine-Line NMOS Field-Effect Transistor,” *IEEE Transactions on Electron Devices*, vol. 33, no. 9, pp. 1395–1397, Sept. 1986.

[17] S. Tedja, J. Van der Spiegel, and H. H. Williams, “Analytical and Experimental Studies of Thermal Noise in MOSFET’s,” *IEEE Transactions on Electron Devices*, vol. 41, no. 11, pp. 2069–2075, Nov. 1994.

[18] A. J. Scholten, H. J. Tromp, L. F. Tiemeijer, R. van Langevelde, R. J. Havens, P. W. H. de Vreede, R. F. M. Roes, P. H. Woerlee, A. H. Montree, and D. B. M. Klaassen, "Accurate Thermal Noise Model for Deep-Submicron CMOS," in *Technical Digest of IEDM (International Electron Devices Meeting)*, Washington, DC, Dec. 1999, pp. 155–158.

[19] G. Knoblinger, P. Klein, and M. Tiebout, "A new model for thermal channel noise of deep submicron MOSFET's and its application in RF-CMOS design," in *Proceedings of the Symposium on VLSI Circuits*, Honolulu, HI, June 2000, pp. 150–153.

[20] F. H. Schottky, "Über spontane Stromschwankungen in verschiedenen Electrizitätsleitern (On Spontaneous Current Fluctuations in Various Electrical Conductors)," *Annalen der Physik*, vol. 57, pp. 541–567, 1918.

[21] J. B. Johnson, "The Schottky Effect in Low Frequency Circuits," *Physical Review*, vol. 26, pp. 71–85, 1925.

[22] C. D. Motchenbacher and F. C. Fitchen, *Low-Noise Electronic Design*, John Wiley & Sons, Inc., New York, NY, 1973.

[23] Agilent Technologies, "Fundamentals of RF and Microwave Noise Figure Measurements," *Application Note 57-1* [On-line], *http://www.agilent.com*, pp. 4–8.

[24] H. T. Friis, "Noise Figures of Radio Receivers," *Proceedings of the Institute of Radio Engineers*, vol. 32, no. 7, pp. 419–422, July 1944.

[25] H. Rothe and W. Dahlke, "Theory of Noisy Fourpoles," *Proceedings of the Institute of Radio Engineers*, vol. 44, no. 6, pp. 811–815, June 1956.

[26] W. Shockley, J. A. Copeland, and R. P. James, "The Impedance Field Method of Noise Calculation in Active Semiconductor Devices," in *Quantum Theory of Atoms, Molecules and the Solid-State*, Academic, New York, NY, 1966, pp. 537–563.

[27] K. M. van Vliet, "General Transport Theory of Noise in PN Junction-Like Devices – I. Three-Dimensional Green's Function Formulation," *Solid State Electronics*, vol. 15, pp. 1033–1053, 1972.

[28] K. M. van Vliet, A. Friedmann, R. J. J. Zijlstra, A. Gisolf, and A. van der Ziel, "Noise in single injection diodes. I. A survey of methods," *Journal of Applied Physics*, vol. 46, no. 4, pp. 1804–1813, Apr. 1975.

[29] L. M. Franca-Neto, E. Mao, and J. S. Harris Jr., "Low Noise FET Design for Wireless Communications," in *Technical Digest of IEDM (International Electron Devices Meeting)*, Washington, DC, Dec. 1997, pp. 305–308.

[30] F. Bonani, M. R. Pinto, R. K. Smith, and G. Ghione, "An Efficient Approach to Multi-Dimensional Impedance Field Noise Simulation of Bipolar Devices," in *Proceedings of 13th International Conference on Noise in Physical Systems and* $1/f$ *Noise*, Singapore, 1995, pp. 379–382.

[31] S. Donati, M. A. Alam, K. S. Krisch, S. Martin, M. R. Pinto, H. H. Vuong, F. Bonani, and G. Ghione, "Physics-Based RF Noise Modeling of Submicron MOSFETs," in *Technical Digest of IEDM (International Electron Devices Meeting)*, San Francisco, CA, Dec. 1998, pp. 81–84.

[32] A. Cappy and W. Heinrich, "High-Frequency FET Noise Performance: A New Approach," *IEEE Transactions on Electron Devices*, vol. 36, no. 2, pp. 403–409, Feb. 1989.

[33] W. Shockley, "A Unipolar Field Effect Transistor," *Proceedings of the Institute of Radio Engineers*, vol. 40, no. 11, pp. 1365–1376, Nov. 1952.

[34] A. van der Ziel and J. W. Ero, "Small-Signal, High-Frequency Theory of Field-Effect Transistors," *IEEE Transactions on Electron Devices*, vol. 11, no. 4, pp. 128–134, Apr. 1964.

[35] F. M. Klaassen, "High Frequency Noise of the Junction Field-Effect Transistor," *IEEE Transactions on Electron Devices*, vol. 14, no. 7, pp. 368–373, July 1967.

[36] Avant! Corporation [On-line], *http://www.avanticorp.com/Avant!/SolutionsProducts/Products/Item/1,1172,39,00.html*.

[37] Avant! Corporation [On-line], *http://www.avanticorp.com/Avant!/SolutionsProducts/Products/Item/1,1172,38,00.html*.

[38] D. M. Caughey and R. E. Thomas, "Carrier Mobilities in Silicon Empirically Related to Doping and Field," *Proceedings of IEEE*, vol. 55, pp. 2192–2193, 1967.

[39] K. Yamaguchi, "A Mobility Model for Carriers in the MOS Inversion Layer," *IEEE Transactions on Electron Devices*, vol. 30, no. 6, pp. 658–663, June 1983.

[40] B. Meinerzhagen and W. L. Engl, "The Influence of the Thermal Equilibrium Approximation on the Accuracy of Classical Two-Dimensional Numerical Modeling of Silicon Submicrometer MOS Transistors," *IEEE Transactions on Electron Devices*, vol. 35, no. 5, pp. 689–697, May 1988.

[41] H. Happy, G. Dambrine, J. Alamkan, F. Danneville, F. Kaptche-Tagne, and A. Cappy, "HELENA : A Friendly Software for Calculating the DC, AC, and Noise Performance of HEMTs," *International Journal of Microwave and Millimeter-Wave Computer-Aided Engineering*, vol. 3, no. 1, pp. 14–28, Jan. 1993.

[42] R. S. Varga, *Matrix Iterative Analysis*, Prentice-Hall, Englewood Cliffs, NJ, 1st Edition, 1962.

[43] ATN Microwave Inc. [On-line], *http://www.atn-microwave.com/device/np.html*.

[44] C. E. Biber, M. L. Schmatz, T. Morf, U. Lott, E. Morifuji, and W. Bächtold, "Technology Independent Degradation of Minimum Noise Figure Due to Pad Parasitics," in *IEEE MTT-S International Microwave Symposium Digest*, Baltimore, MD, June 1998, pp. 145–148.

[45] E. Morifuji, C. E. Biber, W. Bachtold, T. Ohguro, T. Yoshitomi, T. Morimoto, H. S. Momose, Y. Katsumata, and H. Iwai, "RF Noise Study of Small Gate Width Si-MOSFETs up to 8GHz Application for Low Power Consumption," in *Extended Abstracts of the International Conference on SSDM (Solid State Devices and Materials)*, Hiroshima, Japan, Aug. 1998, pp. 80–81.

[46] R. P. Jindal, "Noise Associated with Distributed Resistance of MOSFET Gate Structures in Integrated Circuits," *IEEE Transactions on Electron Devices*, vol. 31, no. 10, pp. 1505–1509, Oct. 1984.

[47] J.-S. Goo, C.-H. Choi, E. Morifuji, H. S. Momose, Z. Yu, H. Iwai, T. H. Lee, and R. W. Dutton, "RF Noise Simulation for Submicron MOSFET's Based on Hydrodynamic Model," in *Proceedings of the Symposium on VLSI Technology*, Kyoto, Japan, June 1999, pp. 153–154.

[48] H. S. Momose, R. Fujimoto, S. Otaka, E. Morifuji, T. Ohguro, T. Yoshitomi, H. Kimijima, S. Nakamura, T. Morimoto, Y. Katsumata, H. Tanimoto, and H. Iwai, "RF Noise in 1.5nm Gate Oxide MOSFETs and the Evaluation of the NMOS LNA Circuit integrated on a Chip," in *Proceedings of the Symposium on VLSI Technology*, Honolulu, HI, Aug. 1998, pp. 96–97.

[49] D. P. Triantis, A. N. Birbas, and D. Kondis, “Thermal Noise Modeling for Short-Channel MOSFET’s,” *IEEE Transactions on Electron Devices*, vol. 43, no. 11, pp. 1950–1955, Nov. 1996.

[50] C. H. Chen and M. J. Deen, “High Frequency Noise of MOSFETs I Modeling,” *Solid State Electronics*, vol. 42, no. 11, pp. 2069–2081, Nov. 1998.

[51] C. H. Chen, M. J. Deen, Z. X. Yan, M. Schroter, and C. Enz, “High Frequency Noise of MOSFETs. II. Experiments,” *Solid State Electronics*, vol. 42, no. 11, pp. 2083–2092, Nov. 1998.

[52] S. V. Kishore, G. Chang, G. Asmanis, C. Hull, and F. Stubbe, “Substrate-Induced High-Frequency Noise in Deep Sub-Micron MOSFETs for RF Applications,” in *Proceedings of IEEE CICC (Custom Integrated Circuits Conference)*, San Diego, CA, May 1999, pp. 365–368.

[53] J. J. Ou, X. Jin, C. Hu, and P. R. Gray, “Submicron CMOS thermal noise modeling from an RF perspective,” in *Proceedings of the Symposium on VLSI Technology*, Kyoto, Japan, June 1999, pp. 151–152.

[54] M. R. Pinto, C. S. Rafferty, R. K. Smith, and J. Bude, “ULSI Technology Development by Predictive Simulations,” in *Technical Digest of IEDM (International Electron Devices Meeting)*, Washington, DC, Dec. 1993, pp. 701–704.

[55] F. Bonani, G. Ghione, M. R. Pinto, and R. K. Smith, “An Efficient Approach to Noise Analysis Through Multidimensional Physics-Based Models,” *IEEE Transactions on Electron Devices*, vol. 45, no. 1, pp. 261–269, Jan. 1998.

[56] J.-S. Goo, C.-H. Choi, F. Danneville, E. Morifuji, H. S. Momose, Z. Yu, H. Iwai, T. H. Lee, and R. W. Dutton, “An Accurate and Efficient High Frequency Noise Simulation

Technique for Deep Submicron MOSFETs," *IEEE Transactions on Electron Devices*, vol. 47, no. 12, pp. 2410–2419, Dec. 2000.

[57] R. P. Jindal, "Distributed Substrate Resistance Noise in Fine-Line NMOS Field-Effect Transistors," *IEEE Transactions on Electron Devices*, vol. 32, no. 11, pp. 2450–2453, Nov. 1985.

[58] F. Faccio, F. Anghinolfi, E. H. M. Heijne, P. Jarron, and S. Cristoloveanu, "Noise Contribution of the Body Resistance in Partially-Depleted SOI MOSFET's," *IEEE Transactions on Electron Devices*, vol. 45, no. 5, pp. 1033–1038, May 1998.

[59] W. Liu, R. Gharpurey, M. C. Chang, U. Erdogan, R. Aggarwal, and J. P. Mattia, "RF MOSFET modeling accounting for distributed substrate and channel resistances with emphasis on the BSIM3v3 SPICE model," in *Technical Digest of IEDM (International Electron Devices Meeting)*, Washington, DC, Dec. 1997, pp. 309–312.

[60] K. M. van Vliet, "Markov approach to density fluctuations due to transport and scattering. II. Applications," *Journal of Mathematical Physics*, vol. 12, no. 9, pp. 1998–2012, Sept. 1971.

[61] K. K. Thornber, "Some consequences of spatial correlation on noise calculations," *Solid State Electronics*, vol. 17, no. 1, pp. 95–97, Jan. 1974.

[62] F. Danneville, H. Happy, G. Dambrine, J.-M. Belquin, and A. Cappy, "Microscopic Noise Modeling and Macroscopic Noise Models: How Good a Connection?," *IEEE Transactions on Electron Devices*, vol. 41, no. 5, pp. 779–786, May 1994.

[63] J.-S. Goo, C.-H. Choi, A. Abramo, J.-G. Ahn, Z. Yu, T. H. Lee, and R. W. Dutton, "Physical Origin of the Excess Thermal Noise in Short Channel MOSFETs," *IEEE Electron Device Letters*, vol. 22, no. 2, pp. 101–103, Feb. 2001.

[64] C. Fiegna, F. Venturi, E. Sangiorgi, and B. Riccò, "Efficient non-local modeling of the electron energy distribution in sub-micron MOSFETs," in *Technical Digest of IEDM (International Electron Devices Meeting)*, San Francisco, CA, Dec. 1990, pp. 451–454.

[65] M. W. Pospieszalski, "Modeling of Noise Parameters of MESFET's and MODFET's and Their Frequency and Temperature Dependence," *IEEE Trans. Microwave Theory and Techniques*, vol. 37, no. 9, pp. 1340–1350, Sept. 1989.

[66] Berkeley BSIM Group [On-line], *http://www-device.eecs.berkeley.edu/∼bsim3/bsim4.html*.

[67] W. Liu, *MOSFET Models for SPICE Simulation, Including BSIM3v3 and BSIM4*, John Wiley & Sons. Inc., New York, NY, 1st Edition, 2001.

[68] H. A. Haus and R. B. Adler, *Circuit Theory of Linear Noisy Networks*, John Wiley & Sons, New York, NY, 1959.

[69] J.-S. Goo, K.-H. Oh, C.-H. Choi, Z. Yu, T. H. Lee, and R. W. Dutton, "Guidelines for the Power Constrained Design of a CMOS Tuned LNA," in *Proceedings of SISPAD (International Conference on Simulation of Semiconductor Processes and Devices)*, Seattle, WA, Sept. 2000, pp. 269–272.

[70] B. Kerzar, M. Mokhtari, Y. Li, B. Hansson, K. Washio, T. Harada, and T. Lewin, "Millimeter-wave bandwidth, SiGe-HBT travelling wave amplifier," in *Technical Digest of GaAs IC Symposium*, Seattle, WA, Nov. 2000, pp. 57–59.

[71] G. Dambrine, J.-P. Raskin, F. Danneville, D. Vanhoenacker-Janvier, J.-P. Colinge, and A. Cappy, "High-Frequency Four Noise Parameters of Silicon-on-Insulator-Based

Technology MOSFET for the Design of Low-Noise RF Integrated Circuits," *IEEE Transactions on Electron Devices*, vol. 46, no. 8, pp. 1733–1741, Aug. 1999.

[72] Y. Imai, M. Tokumitsu, and A. Minakawa, "Design and Performance of Low-Current GaAs MMIC's for L-Band Front-End Applications," *IEEE Trans. Microwave Theory and Techniques*, vol. 39, no. 2, pp. 209–215, Feb. 1991.

[73] M. del Mar Hershenson, S. S. Mohan, S. P. Boyd, and T. H. Lee, "Optimization of Inductor Circuits via Geometric Programming," in *Proceedings of the 36th Design Automation Conference*, New Orleans, LA, June 1999, pp. 994–998.

[74] C. P. Yue and S. S. Wong, "On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 5, pp. 743–752, May 1998.

[75] National Semiconductor [On-line], *http://www.national.com/packaging/lqa24a.html*.

[76] P. Leroux, J. Janssens, and M. Steyaert, "A 0.8dB NF ESD-protected 9mW CMOS LNA," in *ISSCC (International Solid-State Circuits Conference) Digest of Technical Papers*, San Francisco, CA, Feb. 2001, pp. 410–411.

[77] M. Lenzlinger and E. H. Snow, "Fowler-Nordheim Tunneling into Thermally Grown SiO_2," *Journal of Applied Physics*, vol. 40, no. 1, pp. 278–283, Jan. 1969.

[78] K. F. Schuegraf and C. Hu, "Hole Injection SiO_2 Breakdown Model for Very Low Voltage Lifetime Extrapolation," *IEEE Transactions on Electron Devices*, vol. 41, no. 5, pp. 761–767, May 1994.

[79] F. Danneville, G. Dambrine, H. Happy, P. Tadyszak, and A. Cappy, "Influence of the Gate Leakage Current on the Noise Performance of MESFETs and MODFETs," *Solid State Electronics*, vol. 38, no. 5, pp. 1081–1087, May 1995.

[80] R. A. Pucel, W. Struble, R. Hallgren, and U. L. Rohde, "A General Noise De-embedding Procedure for Packaged Two-Port Linear Active Devices," *IEEE Trans. Microwave Theory and Techniques*, vol. 40, no. 11, pp. 2013–2024, Nov. 1992.

[81] D. K. Cheng, *Field and Wave Electromagnetics*, Chapter 9, Addision-Wesley, Reading, MA, 2nd Edition, 1989.

[82] P. Klein, "An Analytical Thermal Noise Model of Deep Submicron MOSFET's," *IEEE Electron Device Letters*, vol. 20, no. 8, pp. 399–401, Aug. 1999.