# ESD DESIGN CHALLENGES AND STRATEGIES IN DEEPLY-SCALED INTEGRATED CIRCUITS

A DISSERTATION
SUBMITTED TO THE DEPARTMENT OF ELECTRICAL ENGINEERING
AND THE COMMITTEE ON GRADUATE STUDIES
OF STANFORD UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

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August 2010

This dissertation is online at: http://purl.stanford.edu/mr612py6371

I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.

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# Abstract

As the semiconductor technologies advance to the nanometer regime, scaling effects adversely impact the Electrostatic Discharge (ESD) protection performance in both high-speed digital circuits and radio frequency (RF) circuits. Both the MOSFET's gate oxide breakdown voltage and the trigger voltage of the lateral bipolar junction transistor (LBJT) effect have been decreasing, contributing to significantly reduced ESD design margins. For the ESD protection and power clamping devices, the current shunting capabilities are limited by the constraints of on-chip area. Furthermore, as the interconnect metals become thinner due to the need to reduce parasitic capacitance, the failure current levels under ESD for both the human-body model (HBM) and charged device model (CDM) discharge decrease drastically. The package and functionality scaling causes considerably increased peak discharge current and exacerbates the design challenge by further lowering the capacitance budget. Overall, every element in the I/O circuit has been adversely affected by scaling, from an ESD protection perspective.

It is the main objective of this work to address the scaling and design challenges of ESD protection in deeply scaled technologies. First, the thesis introduces the on-chip ESD events, the scaling and design challenges, and the nomenclatures necessary for later chapters. The ESD design window and the I/O schematics for both rail clamping and local clamping ESD schemes are illustrated. Then, the thesis delves

into the investigation of the input and output driver devices and examines their robustness under ESD. The input driver's oxide breakdown levels are evaluated in deeply scaled technologies. The output driver's trigger and breakdown voltages are improved appreciably by applying circuit and device design techniques.

The ESD device sections first discuss rail-based clamping, a widely used protection scheme. Two diode-based devices, namely the gated diode and substrate diode, are investigated in detail with SOI test structures. Characterization is based on DC current-voltage (I-V), Very Fast Transmission Line Pulse (VF-TLP), capacitance, and leakage measurements. Improvements in performance are realized. Technology computer aided design (TCAD) simulations help understand the physical effects and design tradeoffs. Then, the following section focuses on the local clamping scheme. Two devices, the field-effect diode (FED) and the double-well FED (DWFED), are developed and optimized in an SOI technology. Trigger circuits are designed to improve the turn-on speed. The advantages of local clamping is highlighted and compared with the rail-based clamping. The results show that the FED is a suitable option for power clamping applications and the DWFED is most suitable for pad-based local clamping.

The thesis presents an ESD protection design methodology, which takes advantage of the results and techniques from pervious chapters and put each element into a useful format. Based on the correlation of package level and in-lab test results, a design process based on CDM target definition and device optimization, discharge path analysis, parasitic minimization, I/O data rate estimation and finally ESD and performance characterization is used sequentially to systematically realize the overall design goals.

# Acknowledgments

I would like to thank the many wonderful people who have enriched my experience and made my Ph.D. work at Stanford possible. First and foremost, I express my deepest gratitude to Prof. Robert Dutton. The appreciation I feel for him is beyond my ability to describe. His guidance, extraordinary insights, and unique perspectives enlightened me time and time again, inspiring me whenever I encountered difficulties. I am truly fortunate to have had him as my principal advisor during my graduate studies; he not only made me into a well-rounded researcher, but a more mature person. Dr. Dutton and the past and present members of Stanford's legendary TCAD groups whom he nurtured are role models for me. I look forward to benefiting from my collaborations with them for many years ahead.

I also express my sincere thanks to Prof. Yoshio Nishi and Prof. Krishna Saraswat for sitting on my oral committee and thoroughly reviewing this thesis. I have gained an enormous amount of knowledge about semiconductor devices from their classes and seminars, which were always infused with their pioneering views and unique approaches. Special thanks goes to Prof. Brad Osgood as well for agreeing to chair my oral defense on very short notice.

I extend my deep appreciation to Dr. Stephen Beebe (GLOBALFOUNDRIES Inc.), who provided outstanding mentorship during my research, especially during my collaborations with the semiconductor industry. The tremendous resources and insightful guidance he provided made it possible for my work to be of interest to the industry and relevant to advanced technologies.

I am truly indebted to Prof. Jung-Hoon Chun (Sungkyunkwan University) and Dr. Yang Liu for their extremely patient mentorship during my research projects and paper preparation process. They taught me important knowledge and skills I would not have learned without them. I am indebted to them for their encouragement as I climbed steep learning curves in many new areas.

Several experts from the industry have provided me with generous guidance and greatly enhanced my knowledge and perspective. I express my sincere thanks for the time extended to me by Dr. Akram Salman and Dr. Charvaka Duvvury (Texas Instruments), Dr. Timothy Maloney (Intel), Dr. Warren Anderson (AMD), Dr. Steven Voldman (Intersil), Dr. Mario Pelella (tau-Metrix Inc.) and Dr. Michael Khazhinsky (Freescale). Always willing to help, Dr. Salman taught me essential lessons during my first internship in the ESD field. Collaborating with him has been a great pleasure. I also thank Drs. Duvvury, Maloney, Anderson, Voldman, Pelella, and Khazhinsky for patiently reviewing my publications, providing critical insights, and teaching me advanced concepts.

One of the most important ways in which I have benefited from my Stanford experience has been in the wonderful opportunities the university gave me to explore both teaching and research early in my academic life. That experience is why I decided to pursue in-depth research and later communicate my results to the research community at conferences. For that early opportunity, I will extend my deep appreciation to Profs. Krishna Shenoy and Simon Wong for allowing me to serve as their teaching assistant for two years. I'd also like to thank Profs. John Hennessy, Mark Horowitz, and Bruce Lusignan for offering me opportunities to participate in the Research Experience for Undergraduates program during summers.

I must gratefully acknowledge the generous funding of the AMD-Stanford FMA Fellowship, SRC GRC research funding SRC#1784, and NanoHub (NSF), which made it financially possible for me to explore many technology areas. I'm thankful to my colleagues at GLOBALFOUNDRIES Inc. and Advanced Micro

Devices Inc. for the generous resources and technology support they provided me during my internships.

To my academic advisors, Prof. Dwight Nishimura and Prof. Umran Inan, and to the great experts who advised me during my research—Dr. Peter Griffin and Professor Zhiping Yu—I also offer my warmest gratitude. For their patient help during the past years, I also thank the TCAD group and the Electrical Engineering Department's administrative specialists, particularly Fely Barrera and Miho Nishi.

Last but not the least, I thank my parents and relatives for their emotional support, as well as my great friends and colleagues, who inspired me during discussions or encouraged me whenever I encountered obstacles: Patrick, Simone, Catherine, Tze Wee, Chia-yu, Georgi, Eric, Hitoshi, Choshu, Jae Wook, Jaeha, Moon-jung, Hai, Paul, Evelyn, Qiushi, Wei, Kevin, Gabriel, She-Hwa, and many classmates over the years.

That I have been lucky enough to know all the people who have made my Stanford life so rewarding and enjoyable I am truly grateful. You have changed me profoundly.

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# Chapter 1

# Introduction

## 1.1 Background

The large-scale manifestation of Electrostatic Discharge (ESD) in nature is lightning, which is a result of specific atmospheric conditions. In the 18$^{th}$ century [1], the demonstration of lightning as a form of electricity led to the invention of the lightning rod which helps the ionized clouds to discharge through the least resistive path to ground. In a similar mechanism, the charged human body of the chip handlers discharge through the chip to ground, or a charged chip can discharge itself when one of its I/O pins touches ground. The discharge mechanism relying on the human body is named "Human Body Model" (HBM) [2], which has a rise time of 1 to 10 ns and duration on the order of 100 ns. The discharge of a charged chip directly to ground is named "Charged Device Model" (CDM) [3], which has a rise time of about 100 ps and duration of about 1-10 ns. Very high currents (above 10 A) can occur during an ESD; therefore a path with very low resistance is needed for current shunting. The lightning rod protects the house from being damaged by lightning. Similarly, the ESD protection devices in integrated circuits (IC) protect the circuits on chip from being damaged by ESD by providing a path with high current shunting capabilities. Despite the fact that ESD devices are installed in most systems, ESD damage has been a serious issue and concern in the IC industry. It has been reported that ESD/EOS damage is responsible for nearly one third of the failures of IC [4].

As semiconductor technology advances, scaling effects adversely impact ESD protection performance in both high-speed digital circuits and radio frequency (RF) circuits [5-7]. A simplified schematic of a typical high-speed digital I/O pad with I/O devices, ESD protection devices and power clamp is illustrated in Fig. 1.1. The input device's ESD tolerance, manifested in the MOSFETs' gate oxide breakdown voltage, has been steadily decreasing due to the downscaling of oxide thickness [5]. The trigger voltage of the lateral bipolar junction transistor (LBJT) effect in the output buffer has also been decreasing [5]. The breakdown voltage ($V_{BD}$) for both input and output devices' failure mechanisms is now below 4 V, contributing to significantly reduced ESD design margins. For the ESD protection and power clamp devices, the current shunting capability is limited by the constraints on on-chip area, which is becoming very expensive. Furthermore, as the interconnect metals become thinner due to the need to reduce parasitic capacitance, failure current levels under ESD for both the human-body model (HBM) and charged device model (CDM) stresses decrease drastically. Overall, every element in the I/O schematic in Fig. 1.1 has been adversely affected by scaling, from an ESD protection perspective.

In addition to the challenges caused by technology scaling, the package scaling exacerbates the design challenge. As the average pin count for modern ICs increases to above 3000 pins, the total stored charge increases, which translates into a significantly increased peak ESD current as high as 15 A [8]. Furthermore, new applications generally require higher processing and data transmission speed. The I/O data-rate has increased to above 10 Gbit/sec for high-speed digital/O, which translates to an ultra-low capacitance budget of below 200 fF [9].

All these mentioned effects cause shrinkage in the "ESD Design Window" [8] as illustrated in Fig. 1.2; this example considers high-speed serial link designs at 15-20 Gb/sec. The window is constrained in voltage by the breakdown of the I/O devices and by the current carrying capacity of the ESD clamp. The vertical axis represents the ESD current ($I_{ESD}$), and the breakdown point can be correlated to the

HBM failure voltage level. While the decrease of $V_{dd}$ supply voltage is slowing down, the decrease of I/O transistor breakdown voltage is still considerable from one technology node to the next, causing a rapid reduction of the ESD protection design window. With only a few hundred fF capacitive budget for the ESD device used in high-speed I/O, and a very small window left beyond the 32 nm node, it becomes very challenging to develop ESD solutions that minimize the capacitive loading while achieving superior ESD robustness.

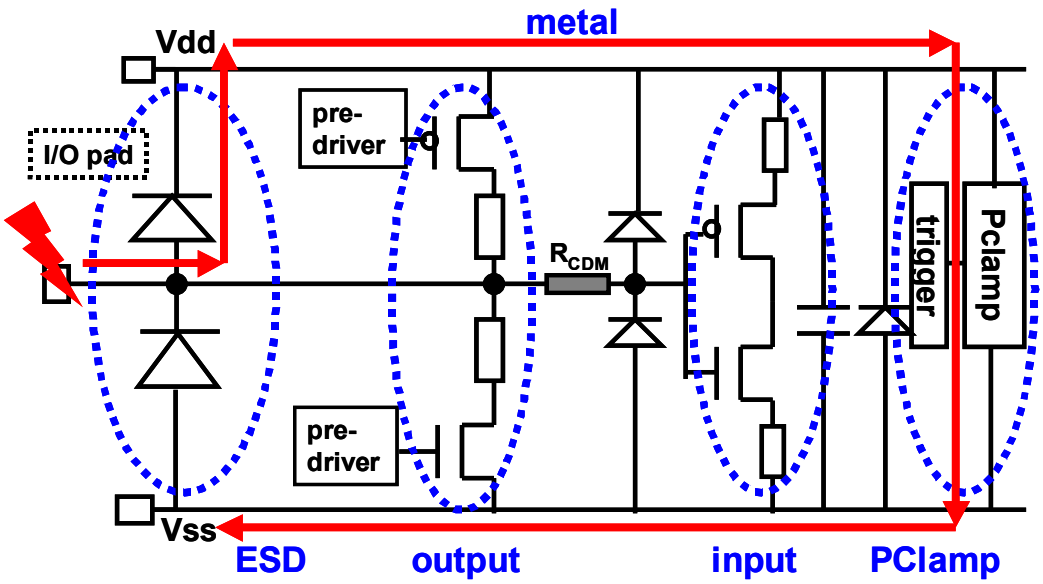



Fig. 1.1: Typical I/O circuit with ESD protection and power clamping. The core elements are marked with dashed lines. The pad-to-ground ESD path is marked using red arrows.

Choosing between the rail-based clamping and pad-based local clamping approaches [10] as protection strategies is the crux of the ESD design challenge. The choice determines the type of ESD devices to be used. In the rail-based ESD scheme (Fig. 1.1), the ESD current path for the pad-to-ground discharge is marked. A pair of diodes are connected to the pad as the primary ESD protection devices. The P/N junction diode [11], a widely used ESD protection device, boasts high current shunting capability, low resistance and low structural complexity. Due to its low turn-on voltage (below 1 V), it is usually connected in reverse-bias and is used in

rail-based schemes. Under ESD conditions, one of the diodes is forward-biased to shunt the large transient currents between two adjacent pads or along the $V_{dd}$ or $V_{ss}$ power buses and power clamp.

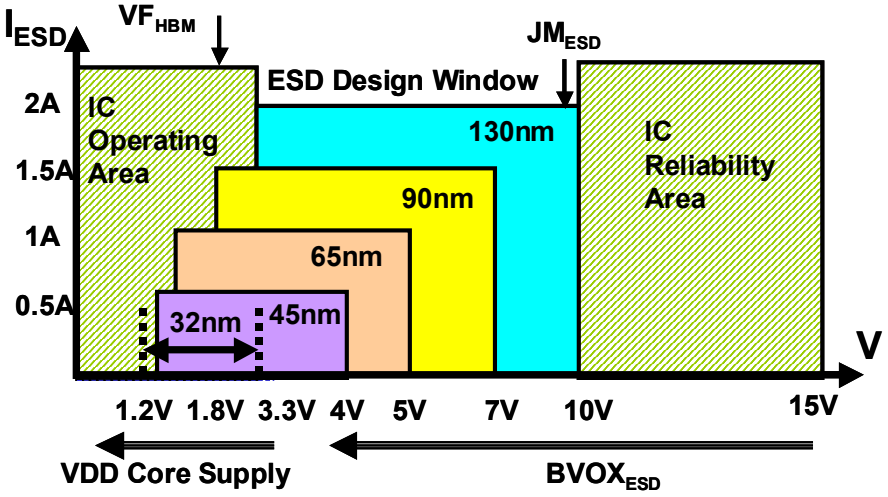



Fig. 1.2: ESD Design window from 130 nm technology to 32 nm technology.

However, this scheme is becoming insufficient in the high-current CDM domain, owing to the excessive voltage build-up along the long and resistive current paths, causing the input driver's oxide damage and the output driver's lateral bipolar junction (LBJT) effect. The dominance of CDM failures demands the exploration of other strategies and devices to circumvent the increasing voltage build-up; a pad-based local clamping protection scheme [10] is shown in Fig. 1.3. This protection circuit allows the ESD current to flow directly from the pad to ground, avoiding the long and resistive power buses and power clamp. The discharge path resistance is considerably reduced and the pad voltage build-up is minimized. However, this approach requires devices suitable for local clamping. Such protection device's turn-on voltage must be above the $V_{ss}$ to $V_{dd}$ range, in order to avoid turn-on during normal operation and to reduce leakage currents. Meanwhile, the turn-on voltage should not be high enough to damage the I/O devices and the turn-on needs to be fast enough for the short-pulsed CDM events. As usual, the ESD devices need to have low resistance and low capacitance. All these requirements need to be met.

It is the main objective of this work to address the scaling and design challenges of ESD protection in deeply scaled technologies. Both the rail clamping and local clamping are investigated with different device options. The diodes are improved and the field effect devices are developed. I/O robustness is improved and a methodology-based solution is provided.

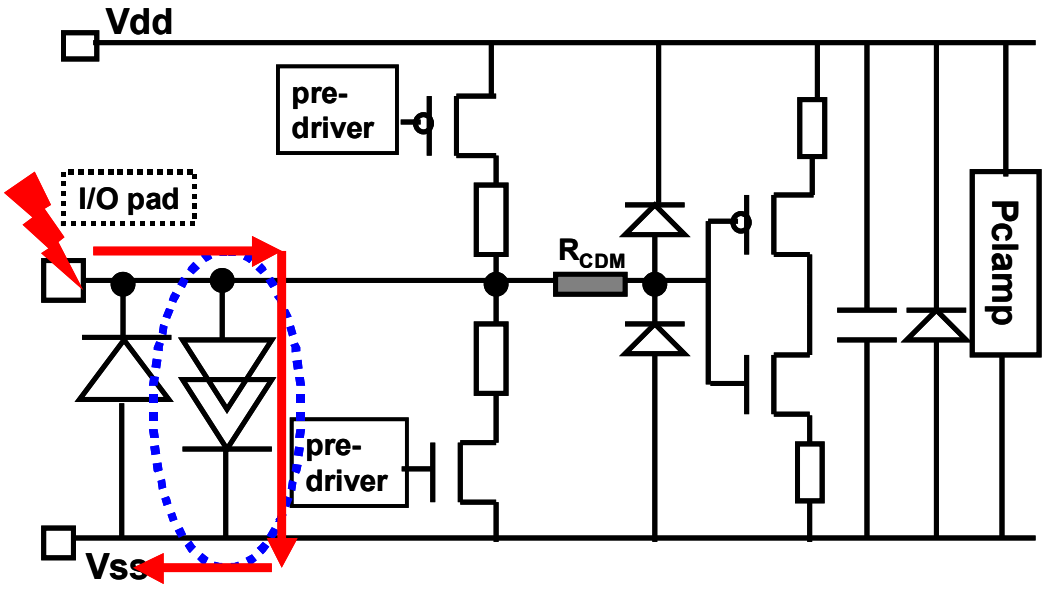



Fig. 1.3: Typical I/O circuit with ESD protection and power clamping. The local clamping protection device is marked with a dashed circle. The pad-to-ground ESD path is marked with red arrows.

To emulate the HBM and CDM ESD events for characterization, the transmission line pulsing technique (TLP) [2] and the very fast TLP (VF-TLP) [3] are applied. A simplified block diagram is shown in Fig. 1.4. A high voltage DC source charges up a piece of transmission line, and a switch discharges it into the device under test (DUT) on the wafer in the subsequent step.

Throughout this thesis, many nomenclatures related to ESD, device physics and I/O circuit are introduced and applied in various situations. Some of the most important ones are illustrated in Fig. 1.5. For a snapback device, the first turn-on voltage point is named $V_{t1}$, which marks the turn-on voltage of the ESD or I/O

device. Then the device may enter a negative resistance region. The lowest voltage in this region is named the holding voltage ($V_h$). Then both voltage and current increase, forming a resistive region. The slope in this linear region represents the conductance. The device eventually breaks down under the TLP stress. The final point corresponds to the breakdown voltage ($V_{t2}$) and second breakdown current ($I_{t2}$).

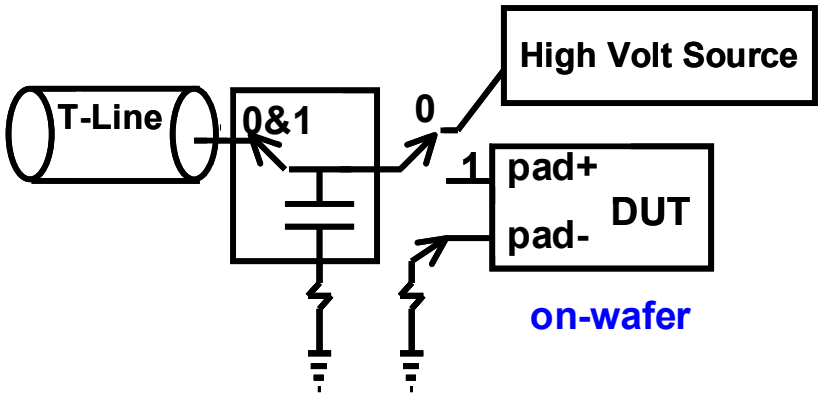



Fig. 1.4: Transmission Line Pulsing Tester Block Diagram. "0" is the charging stage and "1" is the discharging stage.

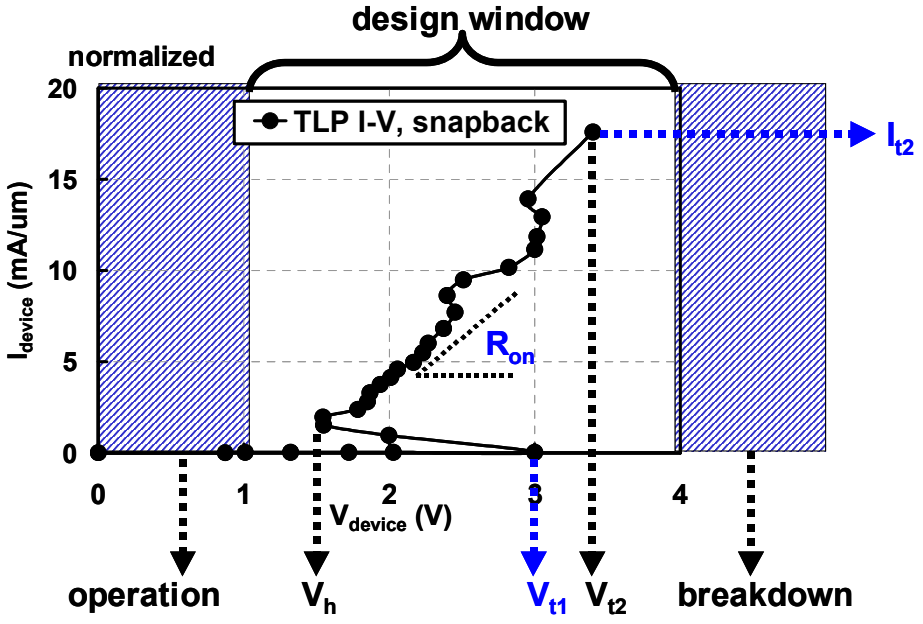



Fig. 1.5: Design window and nomenclatures. An exemplary VF-TLP I-V characteristic is plotted for illustration with the design window.

## 1.2 Thesis Outline and Contributions

This chapter introduces the on-chip ESD events, the scaling and protection design challenges, and the nomenclatures necessary for later chapters. The ESD design window and I/O schematics are illustrated for both rail clamping and local clamping ESD schemes.

Chapter 2 delves into the investigation of the input and output driver devices and examines their robustness under ESD. Input driver's oxide breakdown levels are evaluated in deeply scaled technologies. Output driver's trigger and breakdown voltages are significantly improved by applying circuit and device design techniques.

Chapter 3 focuses on the rail-based clamping, a widely used scheme. Two diode-based devices, namely the gated diode and substrate diode, are investigated in detail in SOI test structures. Characterizations are based on DC I-V, VF-TLP, capacitance, and leakage measurements. Improvements in performance are realized. Technology computer aided design (TCAD) simulations help understand the physical effects and design tradeoffs.

Chapter 4 focuses on the local clamping scheme. Two devices, namely the field-effect diode (FED) and the double-well FED (DWFED), are developed and optimized in SOI technologies. Trigger circuits are designed to improve the turn-on speed. Characterizations are based on DC I-V, VF-TLP, capacitance, and leakage measurements. TCAD simulations help guide device optimization. The advantages of the local clamping is highlighted and compared with the rail-based clamping. The results show that the FED is a suitable option for power clamping applications and the DWFED is most suitable for the pad-based local clamping.

Chapter 5 presents an ESD protection design methodology, which takes advantage of all the results and techniques developed in pervious chapters and put each element into a useful format. Based on the package level and in-lab test correlation, a design process from CDM target definition to device optimization,

discharge path analysis, I/O data rate estimation and finally ESD and performance characterization is streamlined.

Finally, Chapter 6 provides concluding remarks and discusses the future directions of ESD protection design research.

# Chapter 2

# Input and Output Drivers for ESD Design Window Engineering

This chapter discusses the I/O driver MOSFET breakdown mechanisms under ESD, and the methods for improving the I/O robustness. The breakdown levels of these devices define the ESD design window and design target, which is the first step in the ESD design methodology. The first section discusses the single MOSFET I/O robustness and ESD design window. Both the input oxide breakdown and output junction breakdown are examined. The second section focuses on improving the output buffer's breakdown, which is becoming the dominant failure mechanism for I/Os. To build more robust I/Os, stacked drivers are designed and experimented in both bulk and SOI technologies. The impact of driver sizing and pre-driver connection is examined in detail using VF-TLP and TLP measurement. It is shown that proper pre-driver configurations can double $V_{t2}$ thereby improving I/O's $I_{t2}$ [19].

## 2.1 Single I/O Device Robustness and Design Window Engineering

Technology scaling [20,21] and capacitance budget shrinkage adversely affects ESD protection performance. The increased interconnect resistance and the resulting voltage drop along the power bus further decreases the design window. This is especially a severe issue in the high current charged device model (CDM) regime, which is characterized by sub-10 ns ESD stress. The core targets of ESD protection

are the I/O devices. Therefore, it is critical to carefully design these devices and improve their characteristics in ESD, namely the input MOSFET's gate oxide breakdown level ($V_{BD}$) and the output MOSFET's trigger voltage ($V_{t1}$) of the lateral bipolar junction effect (LBJT), both of which directly limit the size of the ESD design window. These levels have been decreasing with technology scaling, contributing to significant reduced design margin.

1 ns VF-TLP [22] experiments are carried out on a variety of MOSFET devices to emulate the CDM situations. The characteristics of the commonly used I/O devices are shown in Fig. 2.1 for current SOI technology. While the thick oxide devices breakdown permanently at about 6 V, the thin oxide device for high performance I/O breaks down as low as 4 V. Similar levels are observed for bulk technologies [5].

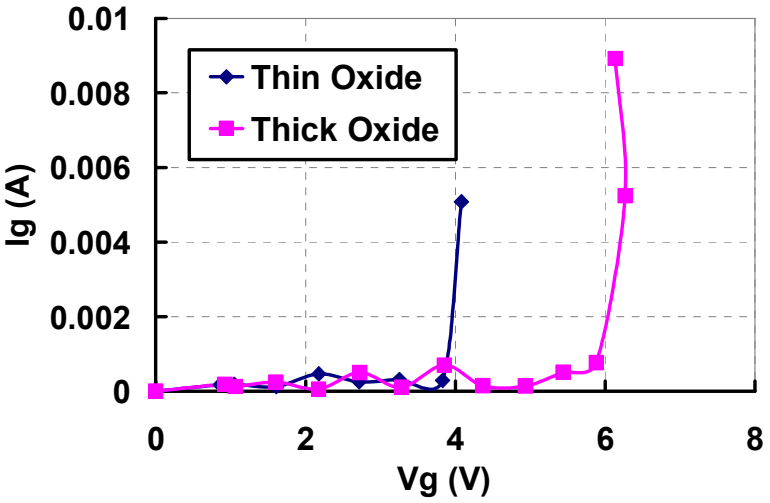



Fig. 2.1: Measured input driver oxide breakdown in 45 nm SOI technology. The device is set up with drain, source and body tied to ground, and ESD is applied across the gate. Sharp increase in gate current marks the (irreversible) breakdown.

In real I/O circuits, a pair of small diodes and a CDM resistor (Fig. 2.2) are sometimes implemented as "secondary ESD protection" elements, in addition to the "primary ESD protection" devices right next to the I/O pad. These devices are

designed to provide an extra branch to help shunt some of the ESD current, thereby protecting the input buffers whose gates are directly exposed to ESD signals, and allowing a higher than $V_{BD}$ voltage at the pad. However, such secondary protection is not applicable for very high speed I/Os since it adds extra R-C loading. More importantly, as shown in the figure, the output buffers are not protected by the secondary protection in any case. Therefore, careful characterization of the output devices' LBJT turn-on and breakdown is as critical as that of the input devices.

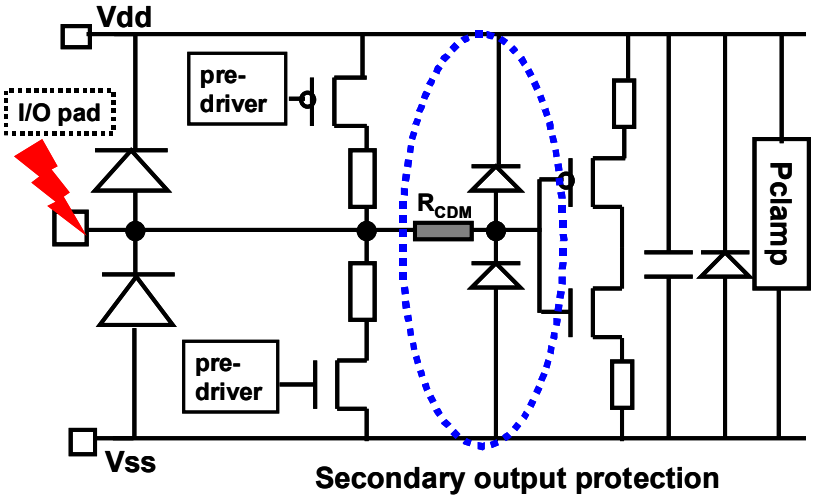



Fig. 2.2: An example of I/O circuit with ESD protection diodes and power clamp. The "secondary ESD protection" elements are marked by a dashed circle.

The VF-TLP results for the regular output single MOSFETs are shown in Fig. 2.3 for both 45 nm and 32 nm fully-silicided SOI technologies. The devices are connected in gate-grounded MOS (GGMOS) setup with gate, source and body grounded and ESD applied at the drain. In this way, the turn-on mainly relies on the LBJT. When defining design rules for output driver protection, the turn-on voltage $V_{t1}$ is the most important parameter, because for single MOSFET, a narrow device of a few micro-meters can break down shortly after it reaches the $V_{t1}$ level. In 32 nm technology, $V_{t1}$ is about 2.6 V, even lower than the $V_{BD}$. Starting from the 45 nm node, the output buffer becomes the limiting factor for the ESD design window. With a CDM current above 10 A and increasing interconnect resistance in current

technologies, I/O improvements are needed to expand the ESD design window immediately.

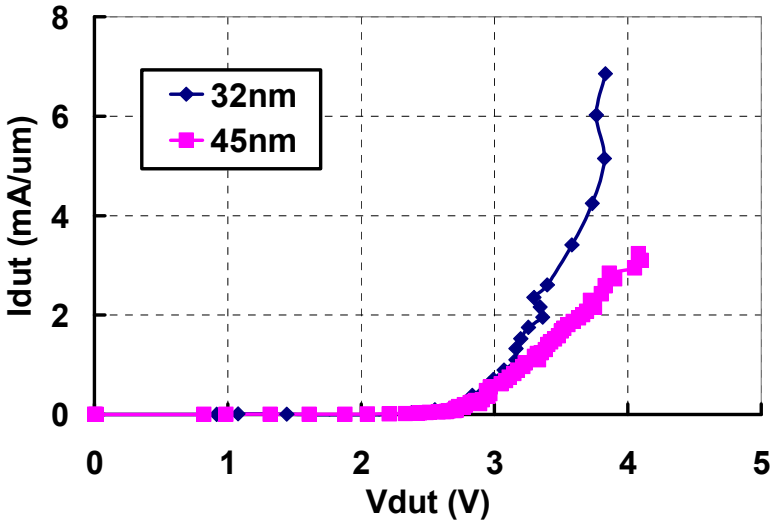



Fig. 2.3: Measured GGNMOS under 1 ns VF-TLP ($t_r$ = 100 ps) for 32 nm ($L_g$ = 40 nm) and 45 nm ($L_g$ = 44 nm) technologies thin gate I/O devices. Data points are shown up to the $I_{t2}$ breakdown point (defined as the level where the DC leakage current increases by 10 times).

## 2.2 Stacked Output Driver Design and Characterization

In order to expand the ESD design window [8] by increasing both the driver's $V_{t1}$ and breakdown voltage ($V_{t2}$), stacked [12-17] (also known as cascode) output drivers are considered in high-$V_{dd}$ domains in I/Os [18]. As scaling continues, implementing them even in low $V_{dd}$ domains seems to be inevitable. However, there are several challenges to be address in this area. First, devices with shared diffusion are not very effective in improving $V_{t1}$ and $V_{t2}$ [15]. In some cases, they can even cause worse ESD robustness than the single MOSFETs. Tradeoffs between shared and separated diffusion [12,13] merit careful investigation. Second, in recent studies [15,16], most devices are investigated without pre-drivers (inverters), power rail, ESD diodes or power clamp devices. Studies with circuits close to the ones used in

real I/O applications are required. Third, most previous work focuses on HBM-domain experiments [12-17]. Studies are needed for the charged device model (CDM) which is becoming the dominant failure mechanism. Solutions are needed to improve $V_{t1}$ and $V_{t2}$. In this section, the ESD robustness of stacked drivers is investigated with pre-drivers both in situations similar to the local clamping and implemented in coordination with ESD protection and clamping circuitry for the rail-based clamping. Both shared and separated diffusions are experimentally used with the very-fast transmission line pulsing (VF-TLP) technique to emulate the CDM conditions. Experimental results show that the pre-driver connection and the main driver's top-to-bottom device ratio have a large impact on ESD robustness. It has been discovered that by grounding the pre-driver inputs, the stacked driver's $V_{t2}$ is increased by twice, hence most of the ESD current flows into the power-rail, increasing the overall failure current ($I_{t2}$) by 8 times. A trigger circuit is proposed for coupling the pre-driver inputs to the desired level during ESD. This section also demonstrates that separated diffusion stacked drivers are preferred in order to improve $V_{t1}$ by more than 1 V. Shared diffusion-stacked drivers with body contact yield the lowest $V_{t1}$. Simulation results reveal the devices that are subject to the largest stress during ESD.

### 2.2.1 Stacked Driver Test Structures for Both Rail Based and Local Clamping Protection Schemes

Implementation of pre-drivers, ESD diodes and power clamps make this study different from previous work such as in [15,16]. Fig. 2.4 shows the structure of a stacked output driver and pre-drivers in the I/O circuit, together with ESD protection devices and the power clamp, all of which are included in the 130 nm bulk test structures. This structure closely emulates the rail-based clamping design. Similar to the real I/O, the power buses have a voltage drop under ESD which can raise the supply voltage of the pre-driver inverters. In a real circuit, In1 and In2 terminals are

connected to the signal lines before the pre-drivers. With carefully designed pre-drivers, the experiments provide realistic estimates of the HBM and CDM protection levels for real I/O circuits.

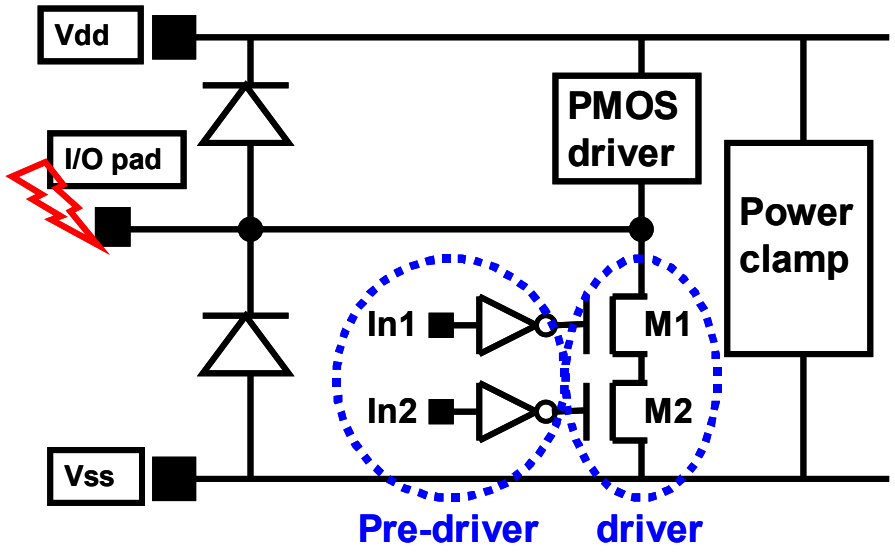



Fig. 2.4: Output driver with pre-drivers (both are circled), ESD protection diodes and power clamp in I/O architecture.

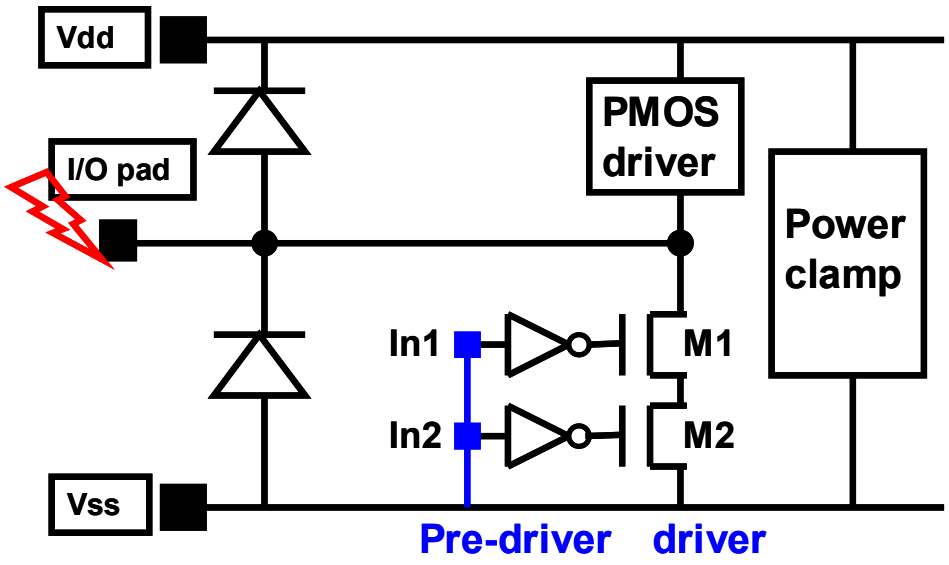



Fig. 2.5: Output driver with pre-drivers, ESD protection diodes and power clamp in I/O architecture; In1 and In2 are both grounded (the "0, 0" input connection case).

In order to test all the useful In1 and In2 connection combinations, namely "0, 0", "0, $V_{dd}$", "$V_{dd}$, 0", "$V_{dd}$, $V_{dd}$", and "floating, floating", the In1 and In2 terminals are connected to either $V_{dd}$ or ground internally using on-chip interconnect. Each connection pair is realized by a set of test structures. An example of the "0, 0" connection is shown in Fig. 2.5. Under pad-to-$V_{ss}$ ESD, the non-grounded pre-driver input transient voltage and M1, M2 gate voltages are coupled much higher than the DC levels, because the $V_{dd}$ is pulled up through the pad-to-$V_{dd}$ forward-biased ESD diode, and voltage builds up on the power clamp and interconnect.

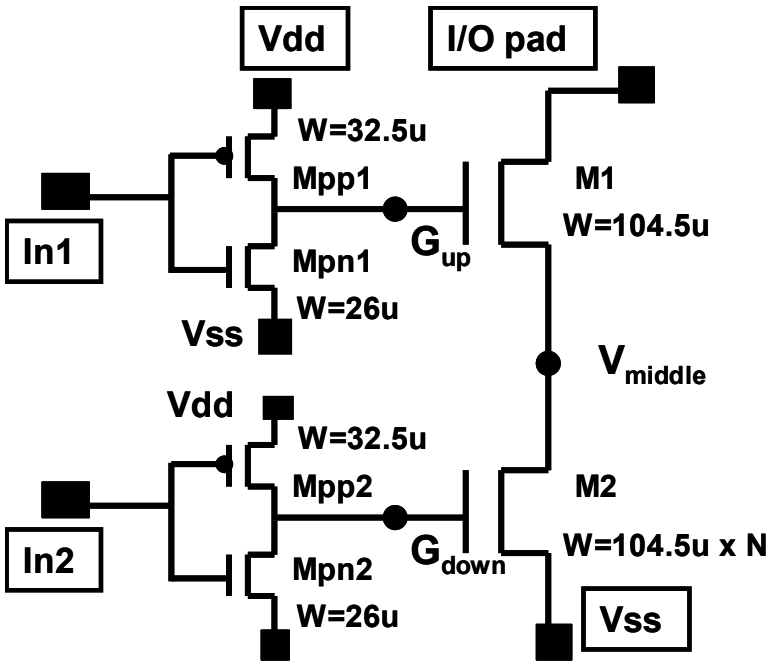



Fig. 2.6: Stacked driver and pre-driver sizing. Drivers with different M2 sizes (N = 1, 2, 10) are built, separated diffusion for all devices.

Fig. 2.6 shows the structure used for the 5-pad stacked driver investigation in 45 nm SOI technology (results presented in the upcoming sub-section). In this structure, while pre-drivers are present, the dual diodes are not added in order to emulate the situation of the local clamping scheme. Also, the pre-driver and driver sizing details are the same for both the structures in Fig. 2.5 (130 nm bulk) and Fig. 2.6 (45 nm SOI). All the MOSFET's are fully-silicided and are multi-finger. Each of the pre-

driver MOSFET's has 10 fingers, while the stacked driver NMOSFET's have 11 fingers each.

Fig. 2.7 shows the simplified layout of both the separated and shared diffusion drivers. While a layout-based estimate yields that for the same effective width, the shared diffusion driver can save area by about 30%, however, the parasitic path underneath the channel degrades the trigger voltage. More details will be discussed in later sections.

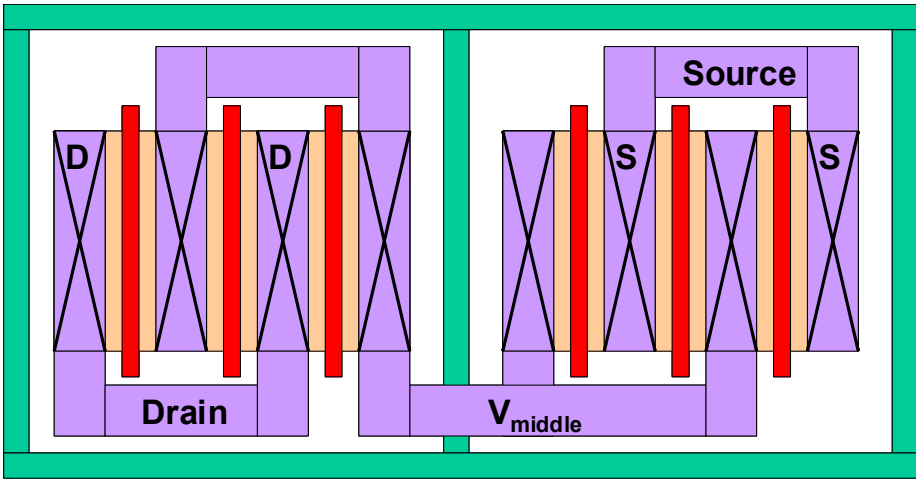



Fig. 2.7 (a): Separated diffusion stacked MOSFET structure layout.

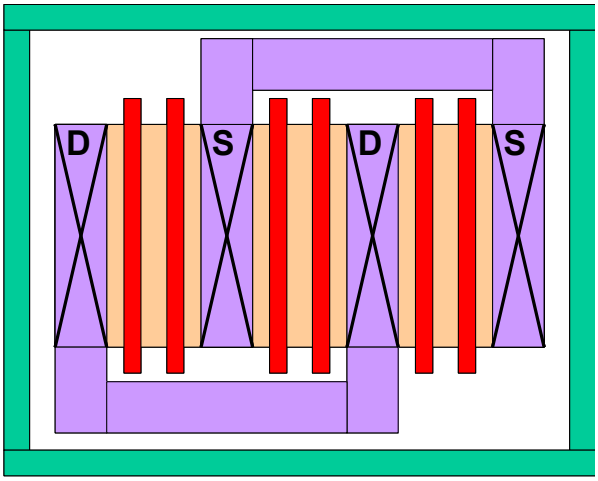



Fig. 2.7 (b): Shared diffusion stacked structure layout.

### 2.2.2 Results for Stacked Drivers in Rail-based Clamping Scheme

In this section, very fast transmission line pulsing (VF-TLP) [3] results are shown to emulate the charged device model (CDM) events. TLP [2] is used to emulate the human body model (HBM) discharge. Unless noted otherwise, the pulse width of the VF-TLP is 1 ns, with a 100 ps rise time; the pulse width of the TLP is 100 ns.

Fig. 2.8 shows the VF-TLP I-V characteristics of the 130 nm I/O circuit (Fig. 2.4) with separated diffusion stacked drivers (Fig. 2.7 (a)). The pre-driver inputs (In1, In2) are connected on-die using interconnect. Significant improvement is achieved in the case when both In1 and In2 are connected to ground (namely "0,0"). The breakdown does not occur until $V_{pad}$ reaches 13 V ($V_{t2}$), twice higher than in other connection cases. The failure current level is about 8 times higher. Most of the current flows into the upper ESD diode, power bus and power clamp. In this connection, the gate terminals of M1 and M2 ($G_{up}$ and $G_{down}$ as in Fig. 2.6) are both pulled to $V_{dd}$ which is at relatively high level because of the diode, power bus and power clamp's voltage build-up during ESD; thus both MOSFETs in the stack are turned on strongly, also contributing to a decreased $V_{t1}$, shortening the turn-on time. Therefore, in circuit implementations, it is desirable to keep the pre-driver inputs close to the ground level under ESD in order to achieve higher robustness.

To accomplish the optimal performance, a trigger circuit is proposed in Fig. 2.9. During normal operation, the gate of $M_{down}$ is connected to ground through the resistor R, turning it off. During ESD, $V_{dd}$ is pulled high due to the rail-based clamping. The resistor R and capacitor C are sized such that for the duration of the ESD transient, the gate of $M_{down}$ is kept high, thus the input voltage at the pre-drivers ($V_{in1}$, $V_{in2}$) is 0, satisfying the condition for maximum $I_{t2}$. The corresponding trigger circuit for the upper pre-driver can be designed similarly. Note that in the case where distortion is a concern for the drivers, buffer stages can be added between $M_{down}$ and the pre-driver.

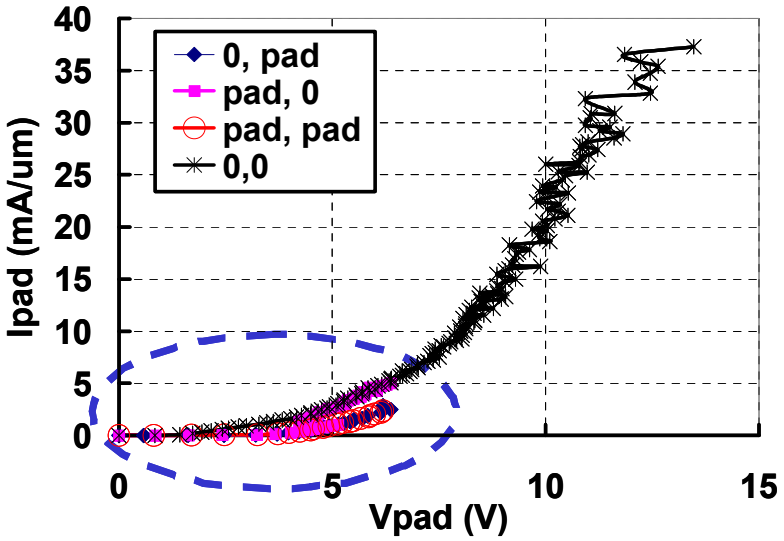



Fig. 2.8 (a): Measured 1ns VF-TLP ($t_r$ = 100 ps) I-V of the entire circuit in Fig. 2.4, for 130 nm bulk structures. N = 1. Pre-driver connections marked in the format "In1, In2". Top: All curves are shown up to $I_{t2}$.

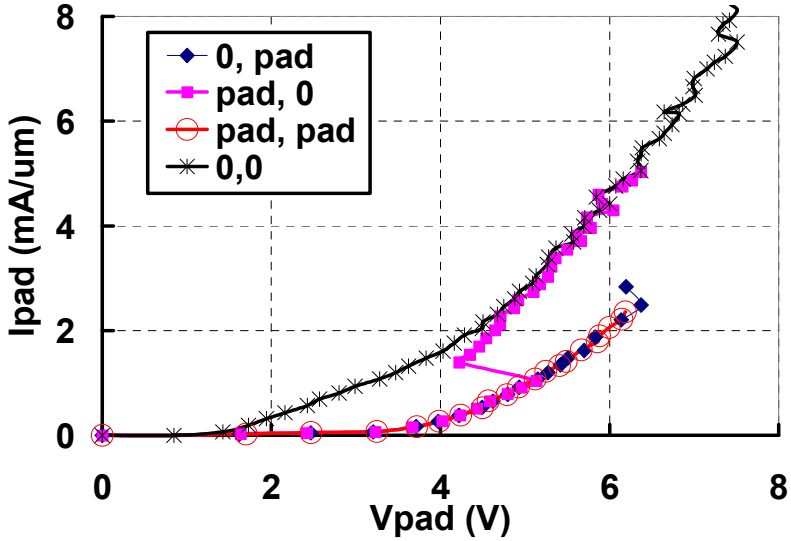



Fig. 2.8 (b): Zoomed version of the circled part of 2.8 (a); the "0,0" curve is cut short.

In the "pad, 0" case, $I_{t2}$ is increased by twice compared to the "pad, pad" and "0, pad" cases. This is because the voltage set-back from the snapback after 5 V. In this connection, M1's gate is 0, so channel is not formed under the gate. The current

mainly relies on the parasitic-BJT effect (LBJT) after the drain-to-body junction breakdown. However, sometimes in the circuit implementation, while $G_{up}$ is connected to the signal path and M1 is the switching component, M2 acts as a large biasing element in a current mirror. The voltage at $G_{down}$ is likely to be close to ground, because the larger device M2 has higher capacitance between $G_{down}$ to $V_{ss}$, thus it takes less voltage in the capacitor dividers from the I/O pad to $V_{ss}$. This case corresponds to the "0, pad" and "pad, pad" structures, having the lowest $I_{t2}$. Hence, the trigger circuit in Fig. 2.9 is especially useful in circuit implementations.

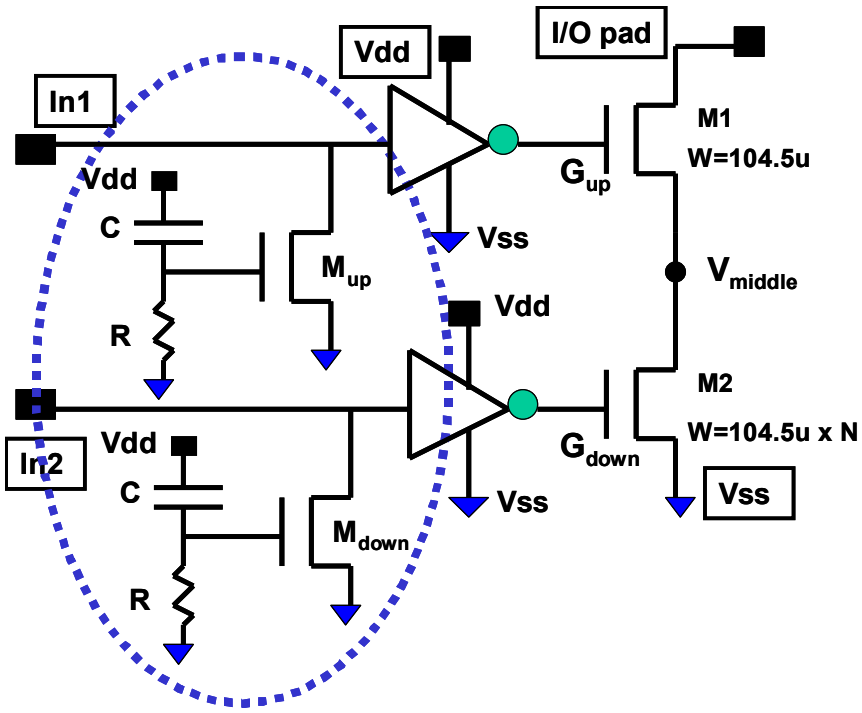



Fig. 2.9: Stacked output drivers and pre-drivers. Circled: proposed trigger circuit to achieve the best $V_{t2}$ and $I_{t2}$ (In1 = 0 and In2 = 0 during ESD).

Fig. 2.10 shows the 10 ns VF-TLP results. $I_{t2}$ reduction is not proportional to the pulse width compared to the 1 ns results. This is because most of the ESD current is shunted through the ESD diode and power clamp, exactly as their intended functionalities. The breakdown is caused by the voltage build-up along the ESD

path, which translates to high I/O pad voltage, stressing the stacked driver. Voltage build-up is the dominant cause of breakdown. So the goal of the stacked driver engineering is exactly to improve the breakdown voltage. With such improvement, the breakdown current is increased at the same time.

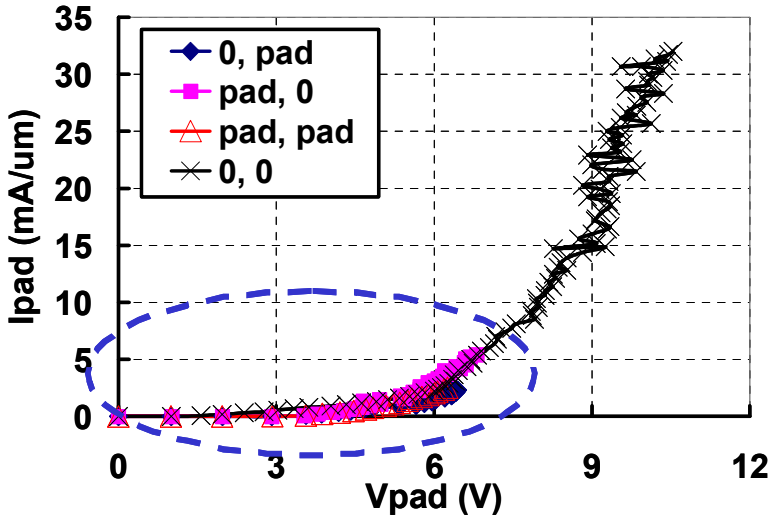



Fig. 2.10 (a): Measured 10 ns VF-TLP ($t_r$ = 100 ps) of the entire circuit in Fig. 2.4, for 130 nm bulk structures, N = 1. All curves are shown up to $I_{t2}$.

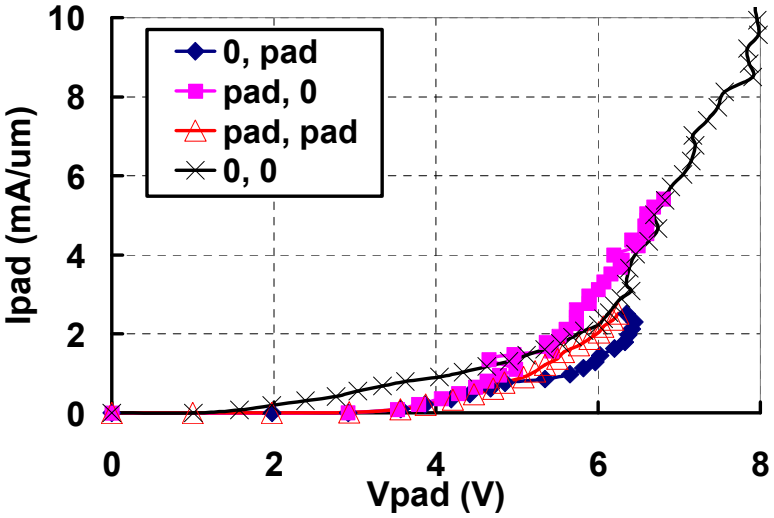



Fig. 2.10 (b): Zoomed version of the circled part of the (a) plot.

Fig. 2.11 shows that with a larger bottom MOS M2, $V_{t1}$ is decreased to around 4 V and $I_{t2}$ decreases as well. The reason is that larger M2 capacitance causes a lower voltage across M2 and a higher voltage across M1, hence breaks down M1 earlier.

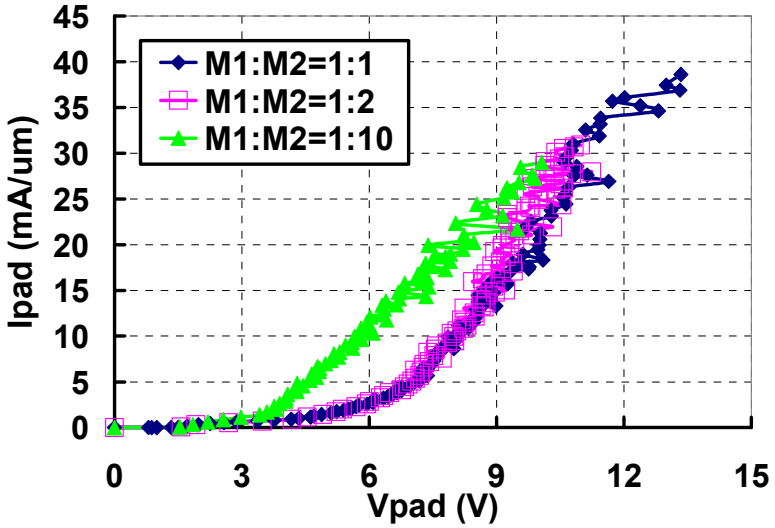



Fig. 2.11: Measured 1 ns VF-TLP (tr = 100 ps) for the stacked driver circuit of Fig. 2.4 with different M1:M2 sizing ratio. In1 and In2 are floating. Curves are shown up to the $I_{t2}$ breakdown points.

Fig. 2.12 shows the 100 ns TLP results for HBM emulation. The $I_{t2}$ of the TLP tests are summarized in Table 2.1. Note that comparing Figs. 2.8, 2.10 and 2.12, the I-V behaviors are consistent in that when stressed by longer pulse widths, $I_{t2}$ decreases. However, the (pad, 0) case converges to the (0, pad) and (pad, pad) cases in Fig. 2.12; the snapback effect which is evident under 1 ns pulse, becomes less prominent under 10 ns pulse, and almost disappears in the 100 ns case. This observation can be explained by the fact that longer pulses provide enough time for the device to enter a steady transient voltage state, thus the negative resistance period becomes negligible compared to the pulse duration.

Fig. 2.13 shows the transient voltage and current waveforms under VF-TLP right before the breakdown point. Both voltage and current for the (0,0) case are much higher than that of the (0,pad) case right before breakdown. These results

confirm that the "0, 0" connection can handle much higher $V_{t2}$ and $I_{t2}$ than the others. The voltage fluctuation around the average level is normal for such high voltages under VF-TLP tests.

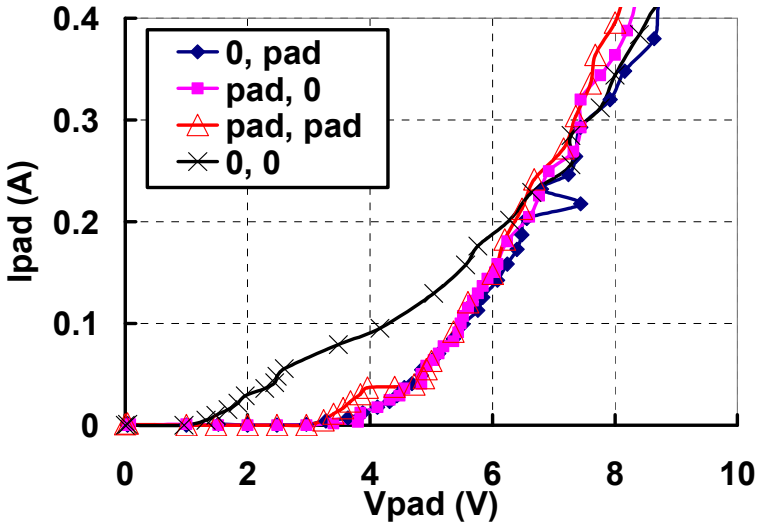



Fig. 2.12: Measured 100 ns TLP for the stacked driver circuit in Fig. 2.4. Curves are zoomed in and cut to focus on the turn-on points. $I_{t2}$ are summarized in Table 2.1.

Table 2.1: 130nm stacked driver circuit 100ns TLP $I_{t2}$ results

| In1, In2 connections (top : bottom size = 1:1) | 100 ns TLP It2 (A) | | Top:bottom size ratio (In1 and In2 floating) | 100 ns TLP It2 (A) |
|---|---|---|---|---|
| gnd, pad | 0.688 | | 1 to 1 | 1.78 |
| pad, gnd | 0.68 | | 1 to 2 | 1.62 |
| pad, pad | 0.52 | | 1 to 10 | 0.584 |
| gnd, gnd | 1.7 | | | |

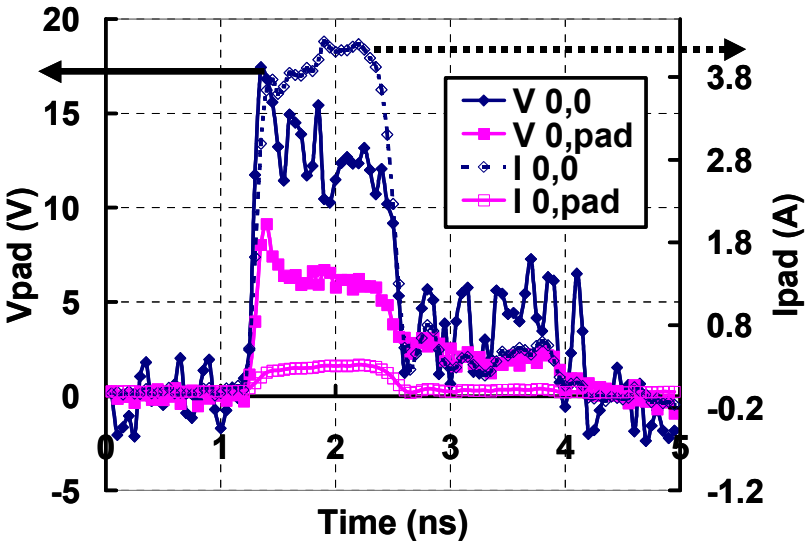



Fig. 2.13: Measured 1 ns VF-TLP ($t_r$ = 100 ps) transient voltage and current right before the breakdown point for (In1, In2) = (0,0) and (0,pad).

### 2.2.3 Results of Stacked Drivers for Local Clamping Scheme

The previous section provides a detailed investigation into the I/O ESD behavior for the rail-based clamping architecture, which is widely adopted in current technologies. However, because of technology scaling, the local clamping is becoming a promising option for advanced nodes [20]. The results in advanced SOI technologies are based on stacked drivers and pre-drivers without ESD clamping elements. The devices in this section are also fully-silicided MOSFET's.

Fig. 2.14 shows the VF-TLP I-V with all In1 and In2 connection combinations. Compared to the non-stacked GGMOS driver in the same plot, the $V_{t1}$ of all cases is improved by about twice. The $I_{t2}$ for each connection is clearly marked in the figure. For the two cases when In1 = 0, $G_{up}$ is pulled high. Thus, the formation of conduction channel facilitates the current shunting and improves robustness. To the contrary, for the cases when In1 = $V_{pad}$, the gate of the top MOS is pulled to ground, causing a very large stress across M1. Thus the breakdown is at much lower levels.

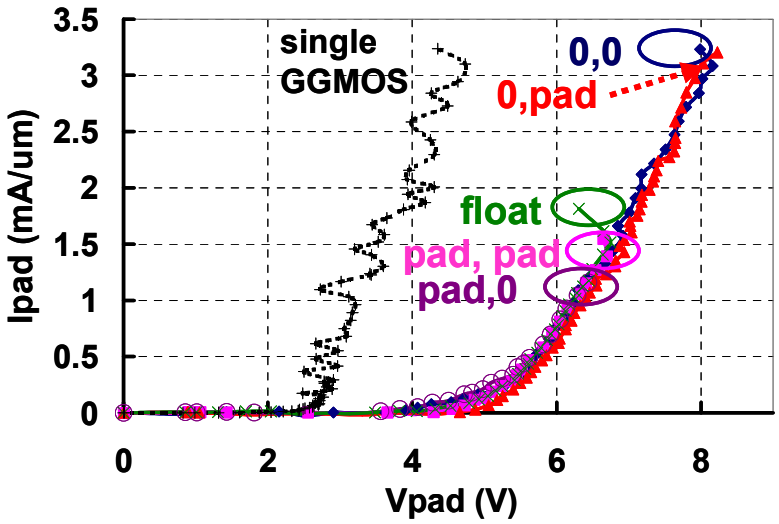



Fig. 2.14: Measured M1:M2=1:1 separated diffusion stacked driver in 45nm for different gate connections; $I_{t2}$ are circled, In1 and In2 connections are labeled with same color as line; 1 ns VF-TLP ($t_r$ = 100 ps) is used; the structures are drawn in Fig. 2.6; there is no ESD clamping elements.

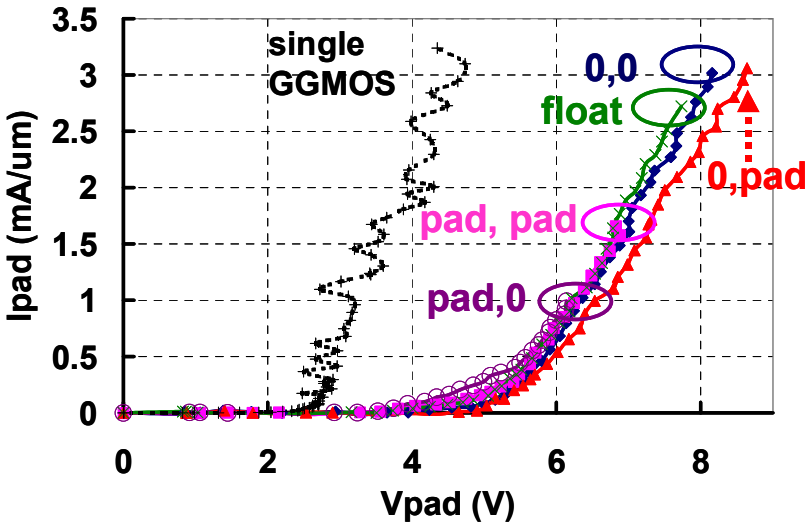



Fig. 2.15: Measured M1:M2 = 1:2 separated diffusion stacked driver in 45nm; 1 ns VF-TLP ($t_r$ = 100 ps); the structures are drawn in Fig. 2.6; there is no ESD protection elements.

The VF-TLP I-V results for drivers with a different top-to-bottom size ratio M1:M2 = 1:2 are shown in Fig. 2.15, demonstrating a consistent trend with the 1:1 case. An interesting result is for the floating-gate case, marked in green lines in Figs. 2.14 and 2.15. $V_{dd}$ is also floating in this circuit. $G_{up}$ and $G_{down}$ are weakly coupled to the driver. Different from the experiments in 130 nm structures where $V_{dd}$ is pulled up, in the current case the overall pad voltage causes the failure.

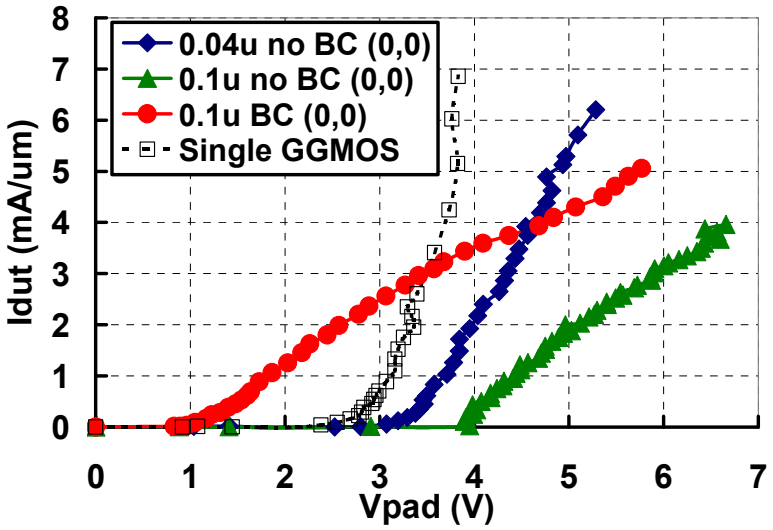



Fig. 2.16: Measured shared diffusion stacked driver in 32 nm technology but longer gate lengths than minimum, compared to single MOS. Curves are shown up to $I_{t2}$. "BC" means "Body Contact" (grounded). (0,0) means "In1, In2" connections are both grounded. 1 ns VF-TLP ($t_r$ = 100 ps).

The area-efficient shared-diffusion (Fig. 2.7 (b)) stacked drivers are also tested. The VF-TLP results are shown in Fig. 2.16 for 32 nm SOI devices. Note the gate lengths are longer than the minimum dimension, which is a common case for I/O devices. Both thin- and thick-gate devices and one with body contact are shown. The body contact (grounded) reduces $V_{t1}$, and $I_{t2}$ is slightly improved. Without body bias, the body potential in the thin silicon film is floating at a level between the drain voltage $V_d$ and 0, which reduces the reverse-bias across the drain-to-body junction, mitigating the effects of impact ionization. With a body bias pinned at 0, the larger

reverse-bias facilitates the impact ionization, reducing the $V_{t1}$. The results align well with previous work [16] in that for the shared diffusion devices, $V_{t1}$ is barely increased compared to the non-stack devices. This is because of the parasitic BJT structure between the drain of M1 and the source of M2, causing a direct current path. The increase of $V_{t1}$ in shared diffusion driver is much less than the separated diffusion driver; therefore, the latter is preferred.

### 2.2.4 Simulations

In order to mimic the discharge behavior under ESD, Spice-based [23] simulations are run to examine the nodal voltages. The schematic for the ESD tester is shown in Fig. 2.17. The cascode output driver's pad and $V_{ss}$ nodes are connected as the "DUT" terminals in the figure. Gsw represents the voltage-controlled resistors elements in Spice, used as the switches for ESD charging and discharging. The parasitic elements in an ESD tester are modeled using resistors, capacitors and an inductor. 2000 V HBM is discharged using the switches. The simulation results shown in Fig. 2.18 (a) to correlate with the critical elements causing the failures in Fig. 2.14. In the "pad, 0" case, and the "pad, pad" case, the voltage spikes are much higher than the other cases for the same ESD discharge voltage. This explains the lower failure levels for these two connections in Fig. 2.14. The (Pad, 0) case has the lowest $I_{t2}$ in both the measurement and the simulation. Fig. 2.18 (b) shows $V_{ds}$ of M1 in all input connection cases and $V_{gs}$ in the "pad, 0" case. The highlight of these results is that while $V_{ds}$ has a very high peak, the $V_{gs}$ remains low. Therefore, a large voltage $V_{gd}$ drops across the gate, causing the breakdown. The color-coding of this figure matches that of Fig. 2.18 (a). Again, the M1 of (pad, 0) sees the largest voltage stress.

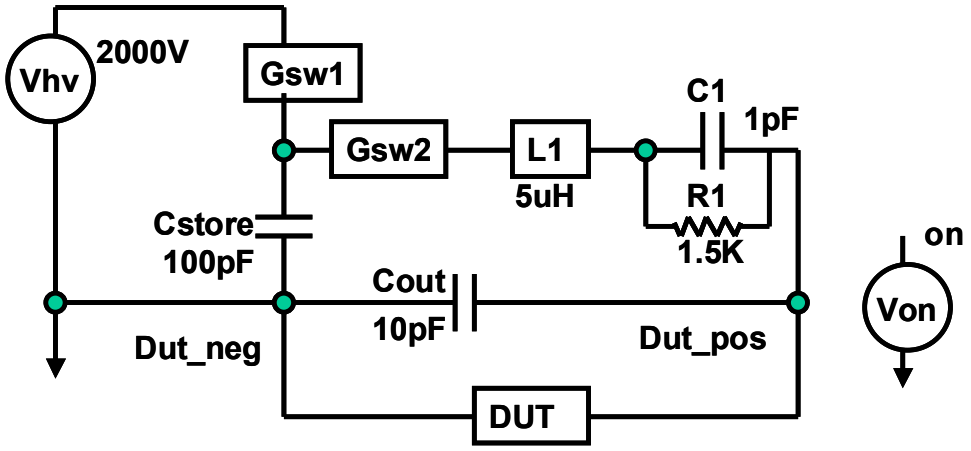



Fig. 2.17: HBM Simulator schematic in SPICE.

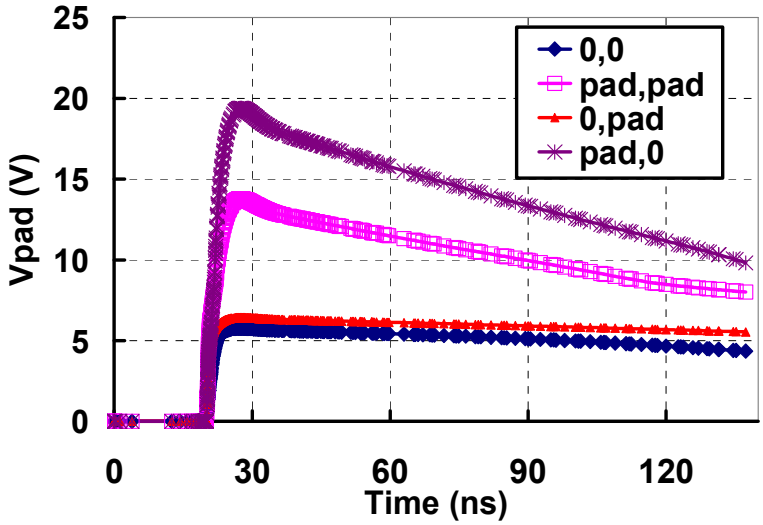



Fig. 2.18 (a): 100 ns HBM simulated in Spice: transient $V_{pad}$ of M1:M2=1:1 stacked driver with different gate connections; $V_{pad}$ is equivalent of the voltage from top MOS's drain to bottom MOS's source.

Comparing the measurement results in Figs. 2.14 and 2.15, the floating gate case, a larger bottom transistor M2 improves the $I_{t2}$ for these drivers. This is explained by the simulation results in Fig. 2.19, which verifies the reduction of $V_{peak}$ in drivers with larger M2 MOSFET.

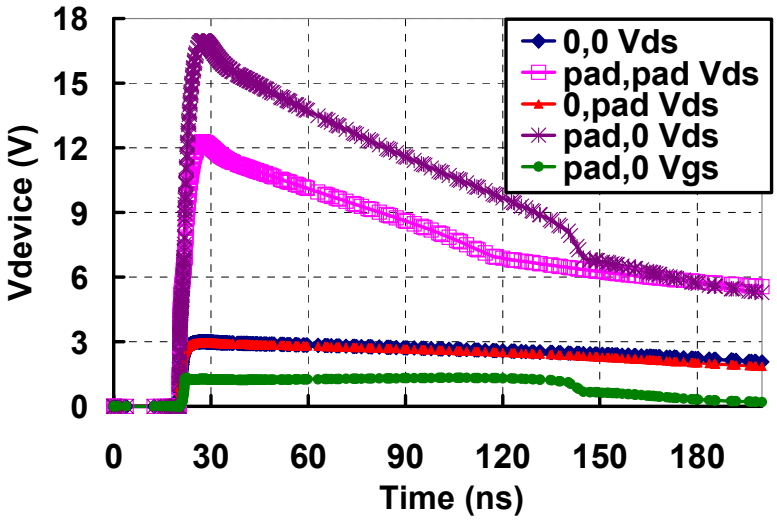



Fig. 2.18 (b): Simulated 100 ns HBM: transient voltage across M1 for M1:M2=1:1 stacked driver; the green curve is for $V_{gs}$ of M1; others are for $V_{ds}$ of M1.

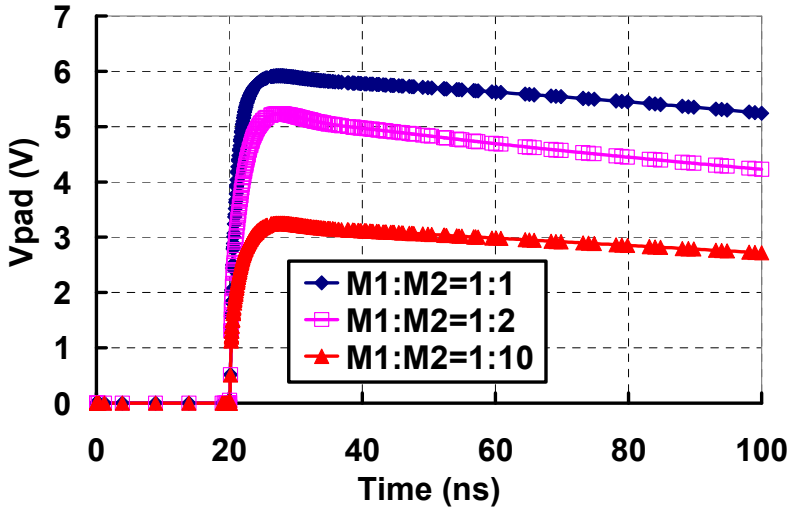



Fig. 2.19: 100 ns HBM simulated in Spice: transient behavior of different M1:M2 sizes with floating In1 and In2.

## 2.3 Chapter Summary

This chapter first investigates the breakdown levels of the widely used single MOS input and output drivers, showing an almost diminished window for ESD design. Circuit implementation issues for the stacked drivers are examined with pre-

drivers and associated ESD devices to imitate the rail-based ESD architecture. Also, pre-drivers and drivers in advanced technologies are investigated to predict the robustness in the local clamping ESD architecture. Experimental results show that the pre-driver connection and the top-to-bottom device ratio have large impact on ESD robustness. It is discovered that by grounding the pre-driver inputs, the stacked driver's $V_{t2}$ is increased by twice, hence most of the ESD current flows into the power-rail, increasing the overall I/O failure current ($I_{t2}$) by 8 times compared to other input connections. The proposed trigger circuit couples the pre-driver inputs close to the ground level to improve both $V_{t2}$ and $I_{t2}$. This work also demonstrates that in order to expand the ESD design window, separate diffusion regions are preferred in order to improve $V_{t1}$ by more than 1 V. The improvement achieved based on the careful investigation in this section helps alleviate the design window shrinkage. The solutions provide robust building blocks for the design methodology. The evaluation of I/O drivers defines clear protection targets for the subsequent sections on ESD device and methodology.

# Chapter 3

# ESD Protection Diodes for High-speed I/O Protection

This chapter focuses on electrical and ESD characterization, physical modeling, and design of ESD protection devices applicable for the rail-clamping scheme. Two types of devices, namely the gated diode and the bulk substrate diode (SUBDIO), are explored and improved in 45 nm silicon-on-insulator (SOI) technology. ESD protection capabilities are investigated using very fast transmission line pulse (VF-TLP) technique to predict the devices' performance in charged device model (CDM) ESD events. The characteristics under the human body model (HBM) test conditions are also summarized. Device capacitance, which is critical for high speed Input/Output (I/O) performance, is evaluated, and biasing schemes are proposed to reduce the parasitic capacitance during normal operating conditions. Technology computer aided design (TCAD) simulations are utilized to show the device physics and design tradeoffs.

## 3.1 Gated Diode and Substrate Diode Structures and Applications

Silicon-on-Insulator (SOI) technology [24-26] has major advantages in reducing the transistor's source and drain diffusion capacitance by the construction of a thick buried oxide (BOX) layer, making SOI a desirable option for very high-speed circuits. Despite the SOI's benefits in both performance and latchup reliability [27],

it has distinctive ESD challenges due to the presence of the BOX layer. First, many conventional ESD structures that utilize vertical junctions and relatively thicker bodies are no longer feasible. For instance, the vertical silicon-controlled-rectifier (SCR) [28,29] cannot be easily implemented as in bulk CMOS technologies, and the SOI GGMOS [30], built in a more limited active region in the thin silicon layer above the BOX, has a current handling capability below 10 mA/μm under VF-TLP tests [31]. To appreciably improve the current handling capabilities, ESD diodes have been developed and are widely used to as P-N junctions in the silicon layer [32]. These structures are generally implemented in the rail-based protection scheme as shown in Fig. 3.1.

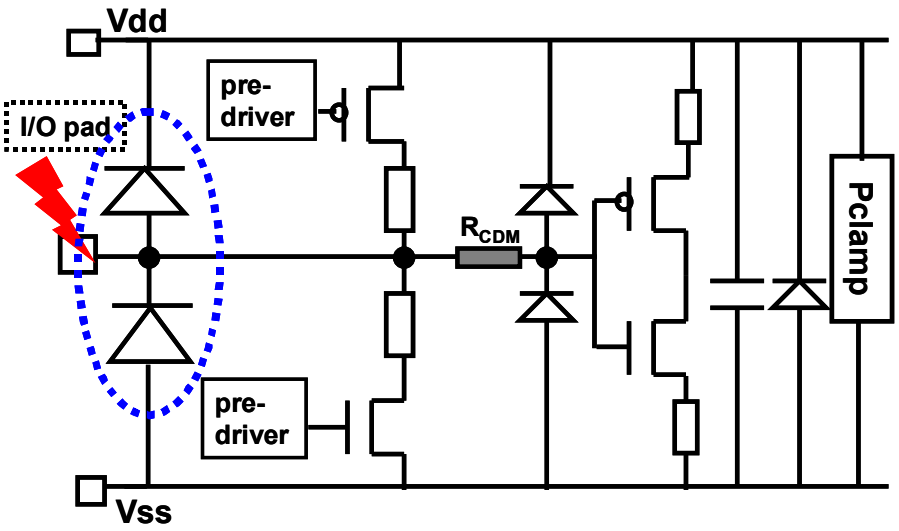



Fig. 3.1: Rail-clamping I/O with a pair of ESD diodes (circled) in place. These primary diodes shunt the majority of the ESD current. ESD at the pad is driven into one of the diodes and the power buses, power clamp, before flowing into the ground.

In this chapter, the SOI gated diode [32-34] and the SUBDIO (substrate diode) [32,35] are comprehensively investigated. Fig. 3.2 shows the cross sectional view of the gated diode structure. It is a P-I-N junction device doped in the silicon film above the BOX. The P+ diffusion region is connected as the anode and the N+ region acts as the cathode. There is no well contact for area reduction. The middle region can be

either an N-type well or a P-type well, with a normal poly gate constructed above the well. The purpose of the poly-defined gate is to serve as a blocking structure to separate the P+ anode and the N+ cathode, and to prevent electrical shorting caused by silicidation above the P/N junction region. Also, a biasing circuit can be connected to the gate to modulate carrier behavior and thereby change the device characteristics. An example of such biasing circuit is shown in Fig. 3.3. The main purpose of the circuit is to provide resistive paths which pull the gates of both ESD diodes to 0 V during normal operating conditions. It will be shown later that this reduces the overall capacitance of the diode. During ESD, however, the gate voltage values do not affect the diode's current shunting capability.

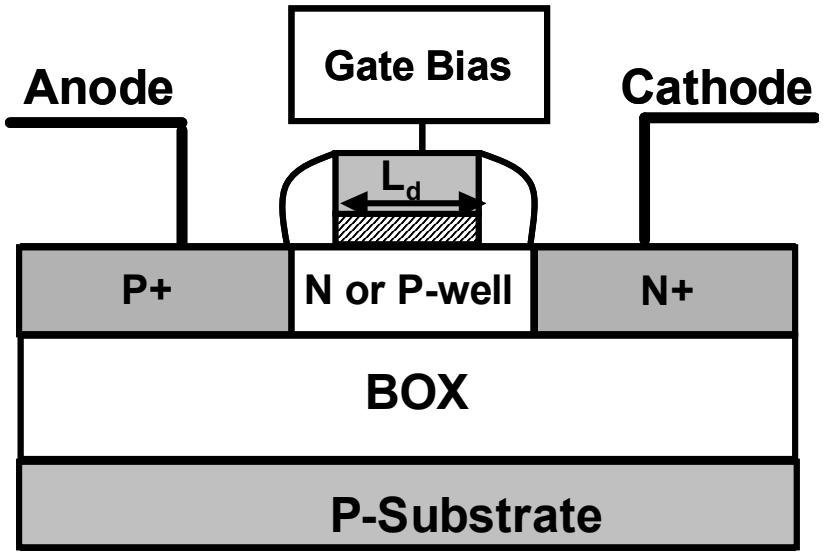



Fig. 3.2: SOI gated diode structure. The gate can be connected to ground or a biasing circuit. The well can be doped either N-type or P-type.

While the gated diode can be built in a generic SOI technology without extra process steps, in thermally constraint situations, the self-heating of the silicon film due to limited volume of the silicon region and lower thermal diffusivity of the BOX beneath the silicon [35] can pose challenges. The SOI diode has lower capacitance compared to the bulk counterpart, however, its current shunting capability is adversely affected by the increased heating. Previous work [36,37] has shown that

for devices in 65 nm technology under 100 ns transmission line pulsing (TLP) [2], the ESD diode in bulk technology has a normalized second breakdown current density ($I_{t2}$/W) of 16.67 mA/μm. However, the ESD diode in the same technology node but in SOI technology has an $I_{t2}$/W of 7.58 mA/μm, much lower than that of the bulk device. To alleviate the heat-accumulation problem, device option has been explored and the "under-the-BOX" substrate diode (SUBDIO) (Fig. 3.4) has been developed in SOI technology. With the construction of a bulk diode underneath the BOX layer, the heat accumulation is alleviated. Part of the BOX is etched to create via access to the substrate underneath, and high energy implantation is applied to create the diffusion regions.

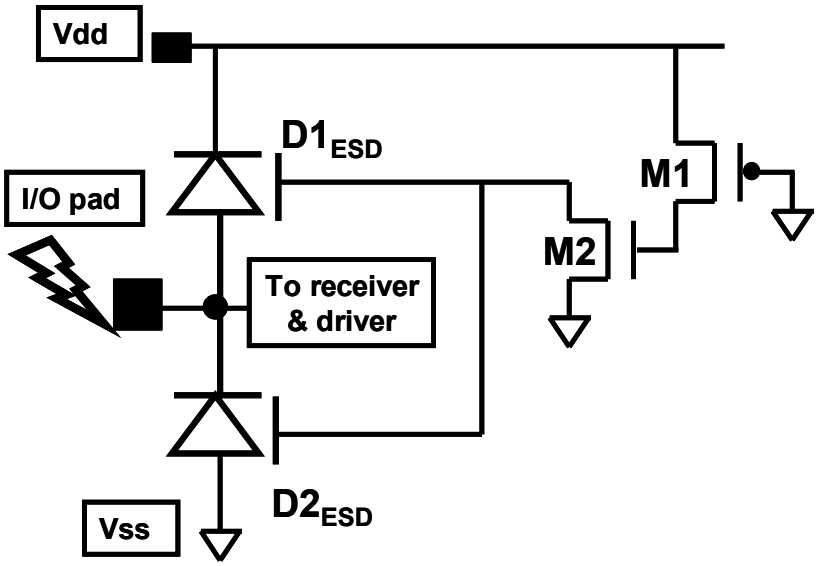



Fig. 3.3: Bias circuit for the gated diodes. During normal operation, both M1 and M2 are on to pull the gate of D1 and D2 to ground.

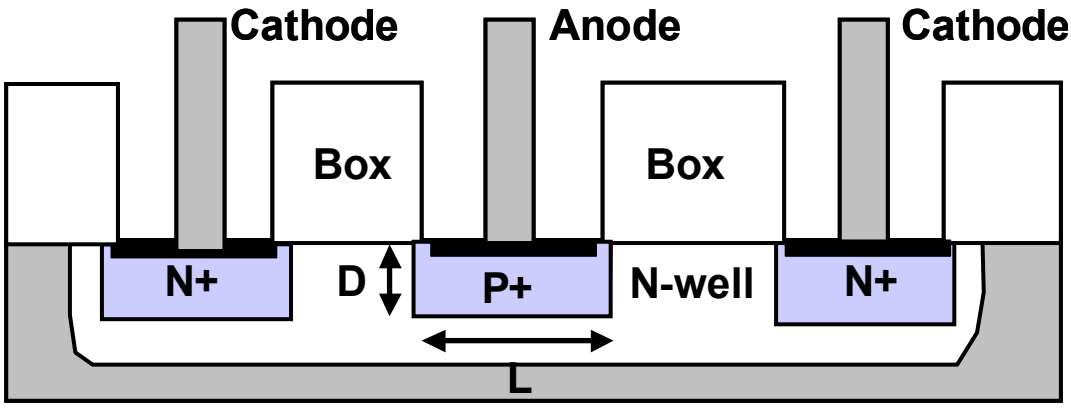



Fig. 3.4 (a): Side view of the active region of the substrate diode (SUBDIO), a structure constructed entirely in the substrate underneath the BOX.

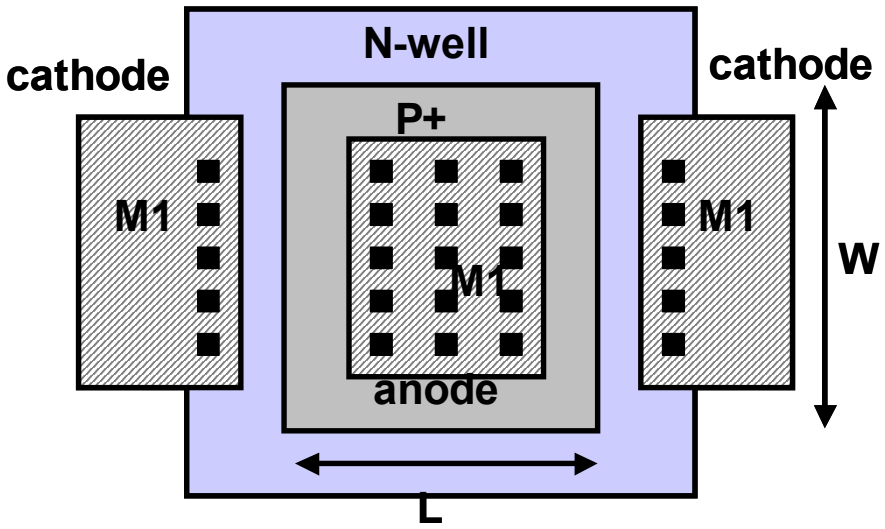



Fig. 3.4 (b): Top view of the substrate diode. Width (W) and length (L) are defined.

## 3.2 Gated Diode and Substrate Diode Characteristics

The very fast transmission line pulsing (VF-TLP) test is in conformance with the standard practice methodology [38,39], utilizing a 200 ps rise time, a 1 ns pulse width, and 20% to 80% time-averaging window on a VF-TLP system [22]. The DC leakage measurement is taken under 0.5 V forward bias after every VF-TLP pulse.

They are monitored in order to mark the breakdown of the ESD devices when an abrupt change happens.

### 3.2.1 VF-TLP I-V Characteristics

Fig. 3.5 contains both the VF-TLP I-V and leakage characteristics of the gated diode and the SUBDIO. The gate is left floating for the VF-TLP measurements on the gated device. However, gate coupling and biasing do not affect the breakdown levels. Pulse widths of 2 ns, 5 ns and 10 ns have also been experimentally confirmed and the results will be summarized later in this chapter. From the VF-TLP I-V characteristic, key parameters such as the second breakdown current ($I_{t2}$), turn-on voltage ($V_{on}$) and the dynamic resistance ($R_{on}$) can be determined for ESD and performance evaluation. $I_{t2}$ is defined by a VF-TLP current level at which the DC leakage current increases by ten times. All data points up to $I_{t2}$ are plotted.

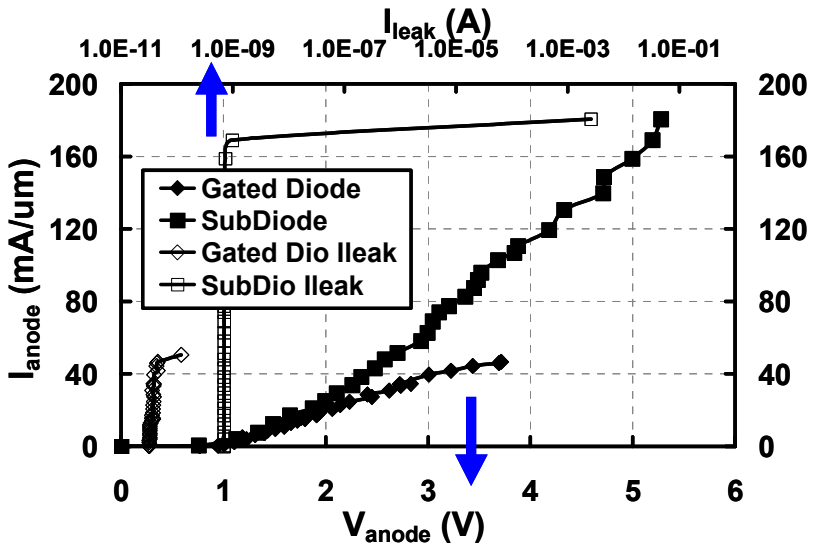



Fig. 3.5: Measured 1 ns VF-TLP I-V and post-ESD DC leakage characteristics of gated diode and SUBDIO. Solid points represent VF-TLP I-V (x-axis on the bottom of the figure); transparent points represent post-stress leakage current (x-axis on top of the figure). The I-V and leakage share the same Y-axis.

As shown in the 1 ns VF-TLP I-V characteristics in Fig. 3.5, the gated diode with a gate length of 0.1 μm has a turn-on voltage around 1 V, normalized $I_{t2}$ of about 50 mA/μm, and $R_{on}$ of approximately 60 Ω·μm. Longer pulse widths translate into higher discharge energies, if the same average voltage level is reached. Therefore, the second breakdown current level decreases for longer pulse widths for both devices, as shown in Fig. 3.6. Note that Fig. 3.6 shows the normalized current density in terms of mA/μm, such that devices can be compared for different sizes. By estimating the required device size for the given ESD protection level, the device area can be taken into account in the design optimization process. For instance, to shunt the ESD current of a 1 ns CDM event, e.g. 5 A, at least 111 μm is required for the gated diode. The 100 ns regular TLP results including the trigger voltage $V_{t1}$, $I_{t2}$, and on-resistance $R_{on}$ are summarized in Table 3.1. The TLP results are correlated with the human-body model (HBM) level [38], the other standard ESD test model. For the same 111 μm device size used in the previous example, $I_{t2}$ can reach about 1.11 A for the gated diode and 5.0 A for the SUBDIO, which translate into 1665 V and 7500 V in HBM.

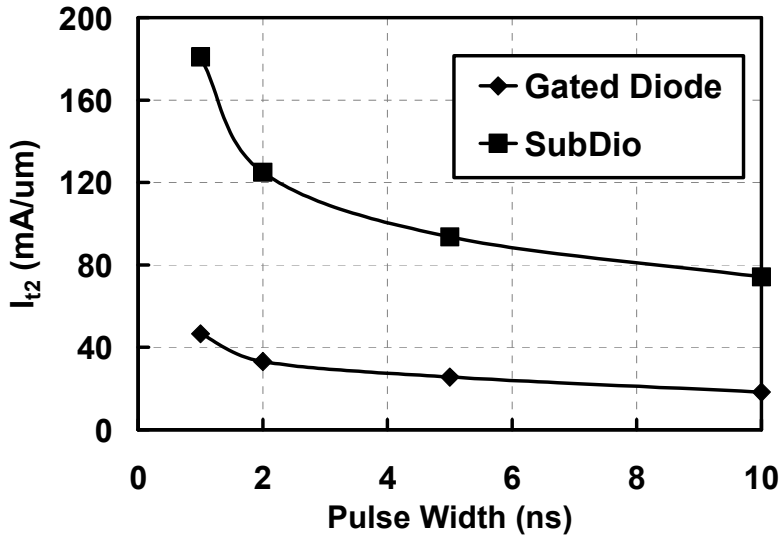



Fig. 3.6: Measured $I_{t2}$ taken from 1 ns, 2 ns, 5 ns and 10 ns VF-TLP I-V for the gated diode and SUBDIO.

Table 3.1: Measured 100 ns TLP (corresponds to HBM) ESD characteristics summary

| | $V_{t1}$ (V) | $I_{t2}$ (mA/um) | $R_{on}$ (Ohm*um) |
|---|---|---|---|
| **Gated Diode** | 0.9 | 10 | 130 |
| **Sub Diode** | 1 | 45 | 33 |

In ESD implementations, it is also important to prevent reverse-breakdown of the ESD devices. As shown in Fig. 3.1, both the upper and the lower diodes are under reverse bias during normal operations, thus their leakage needs to be minimized to reduce static power consumption. Furthermore, the lower diode can be stressed by high reverse bias from the pad, during the pad-to-$V_{ss}$ ESD. Hence, it's critical to ensure that the diodes can withstand high reverse voltage. The negative voltage VF-TLP I-V results are obtained and shown in Fig. 3.7. The reverse breakdown voltage is around 7 V for both devices, making them robust in both normal operating conditions (under about 1 V DC stress) and ESD events (in which case the $V_{ss}$-to-Pad ESD device can withstand higher stress voltage than the I/O devices [7]).

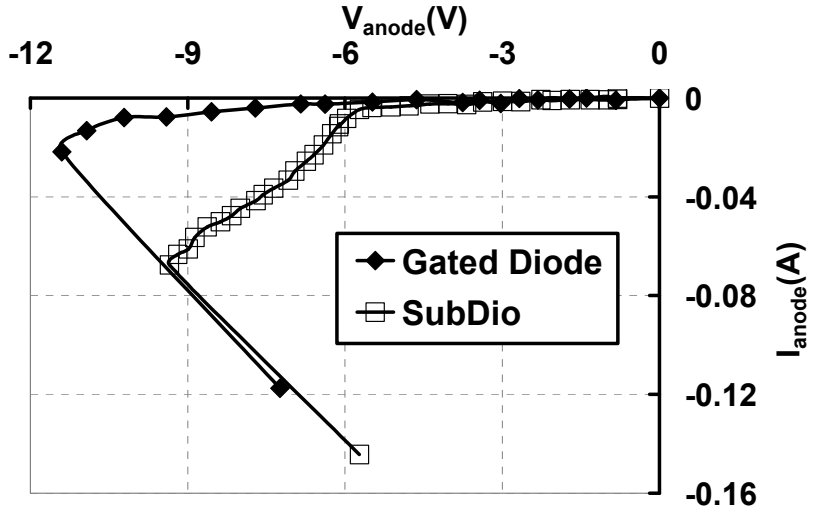



Fig. 3.7: Measured 1 ns VF-TLP reverse bias I-V characteristics of gated diode and substrate diode. All points up to the breakdown are plotted.

### 3.2.2 Capacitance Optimization for Gated Diode

Technology scaling [5-7] and the shrinkage of the ESD design window reduce the ESD device capacitance budget for high-speed I/O serial link data rates of above 20 Gbits/s to below 100 fF [9]. It is important to find ESD solutions that minimize the capacitive loading while achieving superior ESD robustness. However, simply reducing the size of the ESD devices is not an option because simultaneously, the current shunting capability is also weakened. A more appropriate method to evaluate the device's ESD efficiency is by using the figure-of-merit (FOM) $I_{t2}/C$, which normalizes the second breakdown current with respect to the capacitance per width. Therefore, for a given device structure, an efficient way to reduce the capacitance is to explore process and biasing options to modulate the C-V characteristics. Fig. 3.8 illustrates the gate-bias and cathode-bias dependence of the gated diode's cathode-to-anode capacitance, measured at 1 MHz. This is the capacitance seen from the I/O pad since the ESD diodes are connected back-to-back in reverse-bias at the pad. From published work on similar SOI technologies, capacitance variation is not significant below 30 GHz [36]. The results show that for the N-well diode, a negative gate bias has a greater effect in reducing the cathode-to-anode capacitance whereas a positive gate bias has lesser effect. For all the gate bias conditions measured, the largest capacitance is observed for the floating gate case (in which no gate bias is applied to assist the capacitance reduction). The physics of the bias dependence will be detailed in the following. Under the same gate bias, the capacitance decreases when the cathode voltage is increased, due to the extension of the depletion layer in the N-well.

It is noted that a higher overall capacitance of 1.5 fF/μm has been measured at the pad when the gate of the diode is directly connected to AC ground. This value is higher than the floating gate capacitance and the cathode-to-anode capacitances shown in Fig. 3.8, due to the contribution from the gate-to-cathode capacitance (about 1.2 fF/μm). However, such a connection does not represent the real circuit

implementation. Instead, a biasing circuit (Fig. 3.3) is constructed together with the diode at the high speed I/O, with a small MOSFET device (M3) connected to the gate of the diode, providing a resistive path to ground or a non-zero DC bias. The MOSFET introduces an additional R-C structure reducing the gate's contribution to the overall capacitance seen from the pad at high frequency (above 1 MHz). With a 5 KΩ external resistor connected to the diode's gate to mimic the MOSFET, the value of the measured total cathode capacitance at the pad becomes very close to the cathode-to-anode capacitance shown in Fig. 3.8. For instance, at 0 V cathode-to-anode bias and 0 V gate bias, the cathode capacitance is about 0.4 fF/μm; the capacitance is dominated by the cathode-to-anode junction capacitance. Therefore, the subsequent capacitance characterizations focus on the junction capacitance.

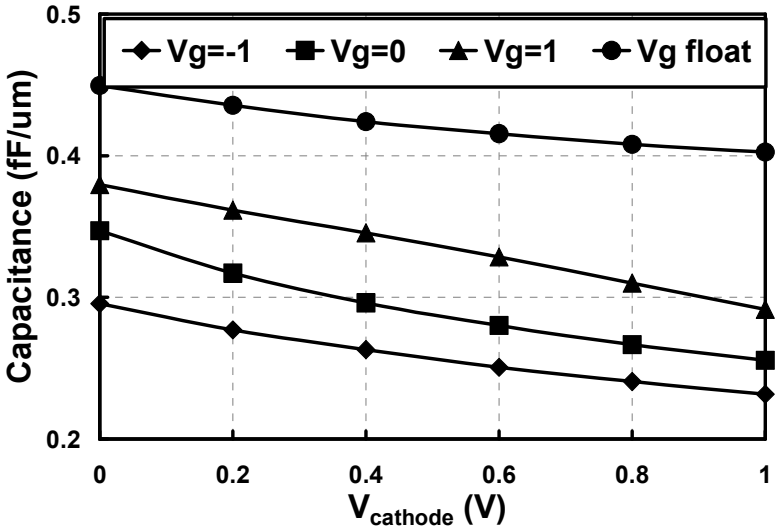



Fig. 3.8: Gated diode (P+/N/N+) capacitance versus cathode voltage for different gate biases. –1 V gate bias can minimize the capacitance. However, pulling the gate voltage to ground is more feasible on a regular IC.

The effect of gate biasing is verified using an estimated device structure with capacitance-voltage simulation. A detailed analysis of the TCAD simulation results explains the observed gate bias dependence on the cathode-to-anode capacitance. In Fig. 3.9, the carrier density (represented by the y-axis) is plotted along the SOI well

depth direction (represented by the x-axis), for different negative gate biases. As depicted in the figure, the depletion region extends further into the direction of the buried oxide (BOX) as the magnitude of the gate bias increases from 0 to 2 V. This depletion region expansion reduces the effective vertical junction area between the P+ diffusion and N-well, thus reducing the overall capacitance. On the other hand, as the magnitude of gate bias decreases, the depletion region width increases toward the 0 gate-bias case. If a positive gate bias is applied, an accumulation layer can be formed in the well.

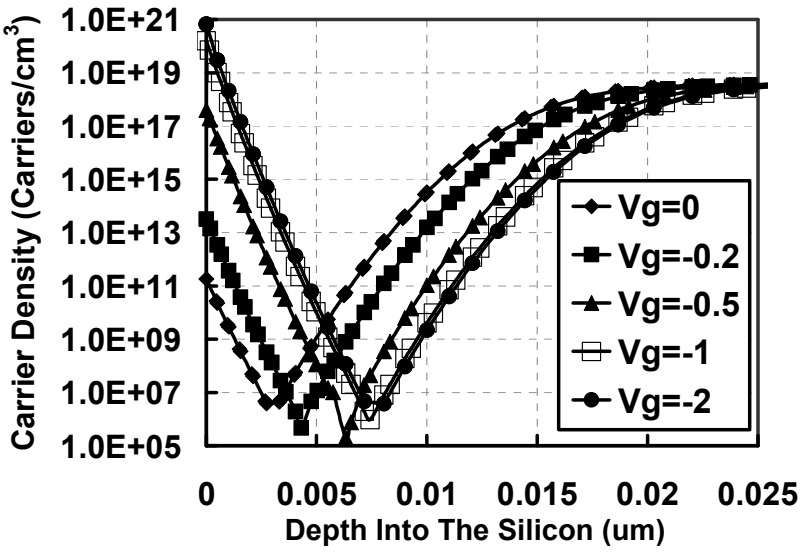



Fig. 3.9: Carrier density versus silicon position plot for the P+/N/N+ gated diode, extracted from TCAD results. The positive direction of the x-axis points toward the depth of the silicon film and the BOX. Lower carrier density at the channel (near x = 0) is in depletion condition, and higher carrier density implies inversion.

Furthermore, as noted in Fig. 3.9, under high negative gate bias, an inversion layer is formed underneath the gate oxide (the depth into the silicon is within 5 nm), causing a large inversion capacitance. This transition can be identified from the measurement results in Fig. 3.10, which plots the capacitance vs. the diode's gate bias for a fairly wide range of voltages. For this P+/N/N+ diode, the onset of inversion exists between –1.5 V to –1 V gate bias. The figure also shows the

comparison between high well-doping (HVT) of about $5 \cdot 10^{18}/cm^3$ and low well-doping (LVT) diodes of about $5 \cdot 10^{17}/cm^3$. Due to the lower doping concentration and longer depletion region, the LVT device achieves a 20% lower capacitance in the flat-curve region. Note that both HVT and LVT are standard options in generic SOI processes. Even though the exact doping levels can deviate, they should fall within the aforementioned HVT and LVT ranges, and the resulting device capacitances are different by only 20%.

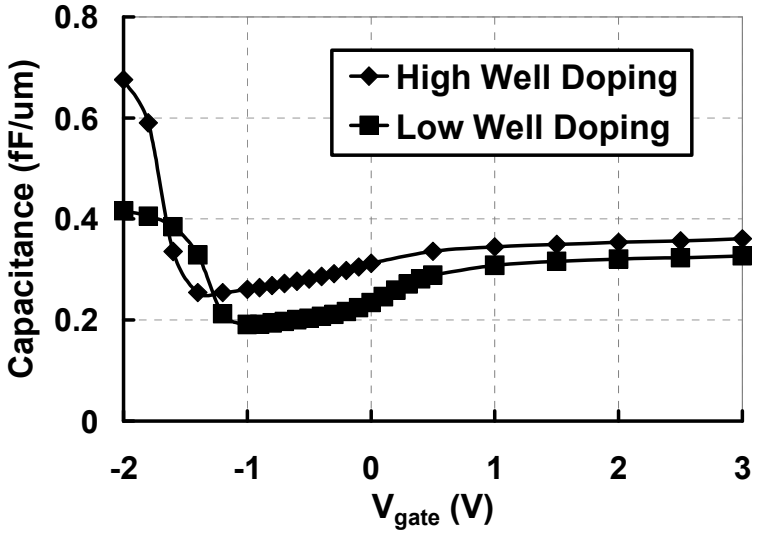



Fig. 3.10: Measured P+/N/N+ (solid lines) and P+/P/N+ (dashed lines) gated diodes' capacitance vs. gate bias. $V_{diode} = 0$ V.

For the P-well diode (P+/P/N+), similar but complementary results have been obtained and plotted in Fig. 3.11. Contrary to the N-well diode case, in which a negative voltage (around -1 V) is required to achieve minimum capacitance, the capacitance of the P-well diode can be reduced to its minimum level by applying a proper positive gate bias voltage. For instance, in this figure, for the high well doping case, the capacitance can be reduced to its minimum value at 0.7 V gate bias. For the low doping case, the capacitance of the diode can be minimized at a gate bias of 0.2 V. Furthermore, when 0 V gate bias is applied, the capacitance is only 5% higher

than the minimum achievable levels. The mechanism that causes the capacitance variation is similar to the N-well diode. Similar to the MOSFET case, the higher the substrate doping concentration, the higher the threshold voltage. But the turn-on voltage of the fabricated high well doping test diode is still below 1 V (within the functional range in digital circuits), causing concerns. The well doping can be increased further to boost the turn-on voltage; however, as predicted by the trend shown in Fig. 3.11, the resulting increase in capacitance limits the ESD design window. Process technology is generally not optimized for ESD protection devices and fine-tuning the doping level is difficult and costly. Therefore, the best solution is to use the biasing circuit presented in Fig. 3.3 to ensure that the gates of the diodes are always connected to 0 V, minimizing the capacitance and making the device applicable in any generic SOI technology.

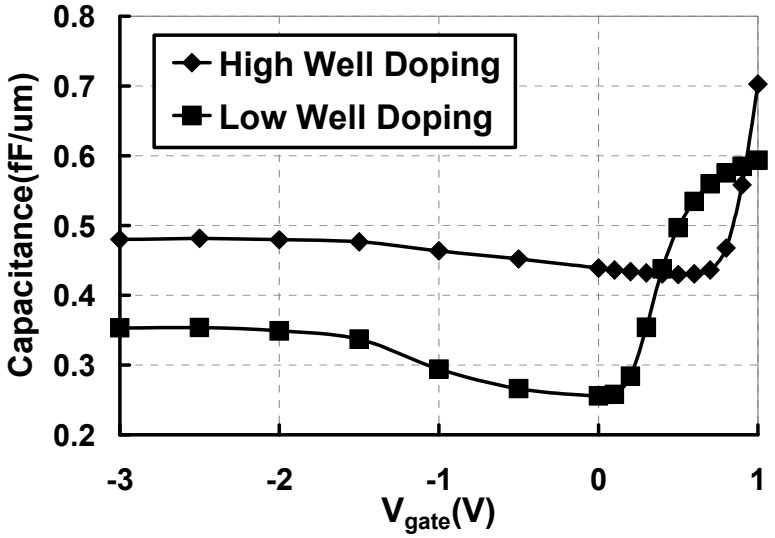



Fig. 3.11: Measured P+/N/N+ (solid lines) and P+/P/N+ (dashed lines) gated diodes' capacitance vs. gate bias. $V_{diode}$ = 0 V.

To explore the scaling effects, gated diodes with different gate lengths (which translates into the well dimension of the P-I-N) are experimentally studied. The reduction of the gate area can potentially reduce the gate capacitance. However, with

the presence of the trigger circuit, the gate capacitance does not contribute noticeably to the overall capacitance. These diodes are characterized with VF-TLP and the results are shown in Fig. 3.12, depicting very similar normalized $I_{t2}$ levels for all the devices. Moreover, shorter gate lengths reduce the on-resistance. Thus, it is more efficient to construct diodes with the smaller gate size to reduce both area and on resistance, making the gate stack's down-scaling an advantage to the gated diode. In fact, offering flexible gate dimensions is an important advantage of the gated diode compared to the relatively newer option—using the silicide-block mask to define the P/N junction of the diode (SB diode). The silicide-blocked diode does not have a gate to apply the bias for capacitance reduction. Moreover, the compactness of the SB diode is largely limited by the feature size of the silicide block mask, which is usually much longer than the poly gate dimension. The gated diode benefits from scaling with every new technology node.

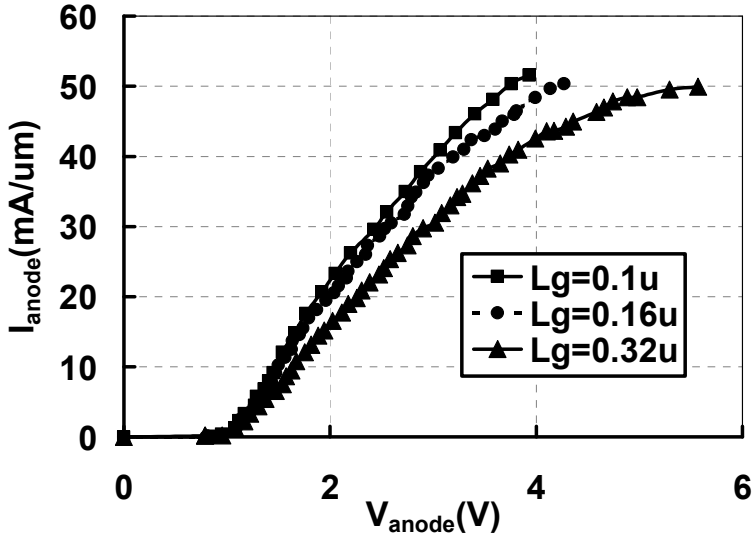



Fig. 3.12: Measured 1 ns VF-TLP I-V results for gated diode for different gate lengths.

### 3.2.3 SUBDIO Optimization

The substrate diode (SUBDIO) structure (Fig. 3.4) was demonstrated for the integration of ESD devices under the buried oxide region [35]. As shown in Fig. 3.5, the SUBDIO achieves significantly higher current shunting capability and second breakdown current level than the gated diode, mainly due to reduced self-heating. High-energy ion implantation is applied to create the well underneath the BOX. Despite the major advantage in providing a low resistance ESD device, the SUBDIO has a large bottom junction area, which adds extra capacitance. A careful investigation is carried out to characterize the I/V and capacitance of the SUBDIO structures for various dimensions.

In the actual layout, the SUBDIO is shaped into rectangles instead of stripes as shown in the top-view in Fig. 3.4 (b), such that the variation introduced by high energy doping does little to affect the overall dimension. The cross section of the active region is shown in Fig. 3.4 (a). To conform to the routing requirement, the cathode contacts are built on the left and right sides, while the anode is connected to the P+ region in the middle. The contact-connected sides contribute most to the current. However, both the P/N junctions along the perimeter and the large bottom plate contribute to the AC capacitance, and they are weighted by different coefficients.

There are three parameters that define the dimension of the SUBDIO's active region: width (W), length (L), and junction depth (D), as shown in Fig. 3.4. P/N junctions are present in five surfaces: the bottom plate junction defined by W and L, the two side junctions along the width direction defined by D and W, and the two side junctions along the length direction defined by D and L. The capacitance equation can be written as:

$$(W \cdot L \cdot a + 2\,W \cdot b + 2\,L \cdot c) \cdot N_{finger} = \text{Total Capacitance}$$

where a, b, c are capacitance coefficients and $N_{finger}$ is the total number of fingers of the device. Note that since the exact value of the junction depth D is a process-

dependent parameter and is usually not available, the coefficients b and c are used to include the scaling effect of both D and the capacitance factor. Measurements have been taken on devices with various dimensions. For a device with a total width of 300 μm (width/finger = 50 μm; 6 fingers) and L = 2 μm, the device capacitance is about 2 pF. More measurements are taken on two other types of SUBDIO. The first device has a total width of 1800 μm (width/finger = 12.5 μm; 144 fingers) and L = 2 μm. Its capacitance is 12.6 pF. The second device has a total width of 525 μm (width/finger = 2.92 μm; 180 fingers) and L = 0.5 μm. Its capacitance is 1.5 pF. By varying size and capacitance in the equation above and solving the resulting linear equations, the coefficients are identified: a = 2.75 fF/μm$^2$, b = 0.65 fF/μm and c = 0.65 fF/μm. The normalized current density for devices of both lengths is plotted in Fig. 3.13 to show their almost identical dynamic resistance. This indicates that the bottom plate and the plates defined by D and L do not contribute much to the current flow; the current mostly flows through the contact-connected left and right sides, which do not depend on L, as in Fig. 3.4 (b). This fact implies that the reduction of L can decrease the overall capacitance while not affecting a diode's current shunting capability. Fig. 3.14 shows the normalized capacitance values (measured at 1 MHz) of the initial design with L = 2 μm and the improved design with L = 0.5 μm. An overall capacitance of 3.6 fF/μm is obtained for the shorter length device, achieving a 57% reduction compared to the longer device.

Due to the substrate diode's reduced thermal accumulation compared to the other devices, it is especially useful in thermal-constraint applications. However, its high capacitance makes it less preferred as an ESD protection device for high-speed I/O. as previous works [36,37] have shown, for devices in 65 nm technology under TLP, the bulk diode has a capacitance-normalized second breakdown level ($I_{t2}$/C) of 26.3 mA/fF, while the SOI diode in the same technology node has an $I_{t2}$/C of 22.9 mA/fF. Not much benefit is achieved by using the bulk diode. Moreover, as shown in

this work, the 45 nm SUBDIO's $I_{t2}$/C under 1 ns VF-TLP is 50 mA/fF, much less than the SOI gated diode's $I_{t2}$/C of 156.7 mA/fF.

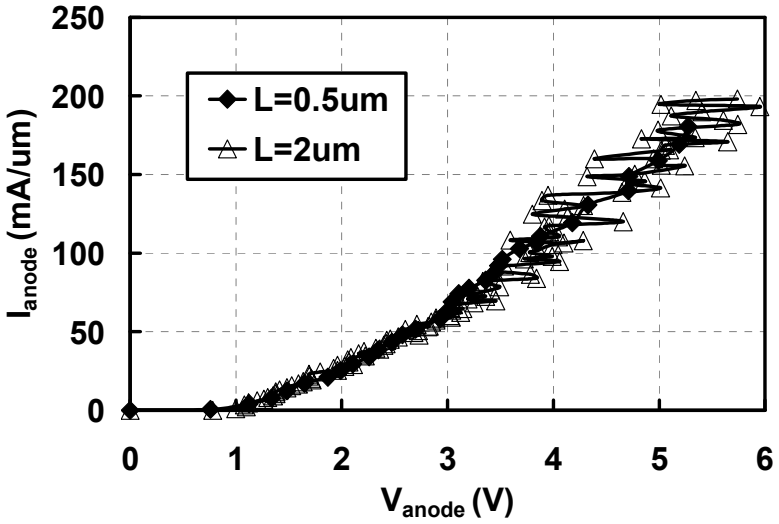



Fig. 3.13: Normalized substrate diodes 1 ns VF-TLP I-V measurement for long and short lengths.

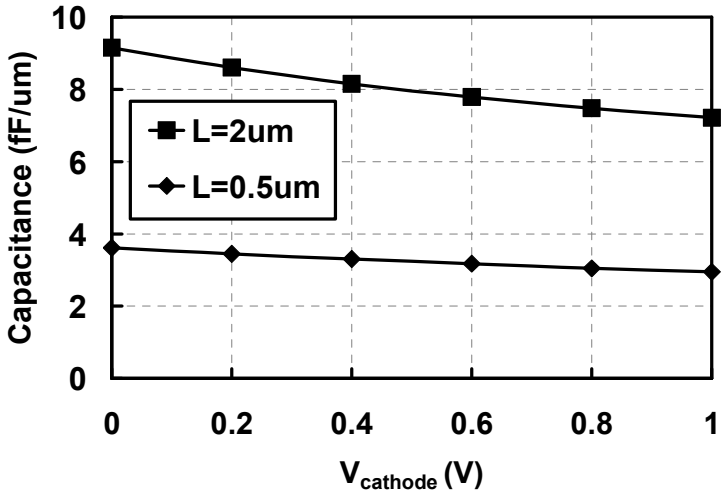



Fig. 3.14: Substrate diodes capacitance measurement for long and short lengths.

### 3.2.4 Figure-of-Merit

As mentioned earlier in this section, an important FOM to evaluate is the $I_{t2}/C$ which incorporates the information of both the device's current shunting capability and the capacitance per area. The geometrical factors are canceled in the calculation of the FOM. The FOM comparison for the two diode devices is presented in Fig. 3.15. It is noted that while the difference is about 4 times for 1 ns VF-TLP tests, the two curves show a smaller difference for experiments under longer pulsewidths. This is because the SUBDIO has less localized heating, hence its current performance improves relative to the thin film device. However, the focus of CDM ESD protection design is under the sub-10 ns. In this time regime, the gated diode is evidently more advantageous than the SUBDIO and therefore is the preferred option as rail-based ESD protection device for high-speed I/O.

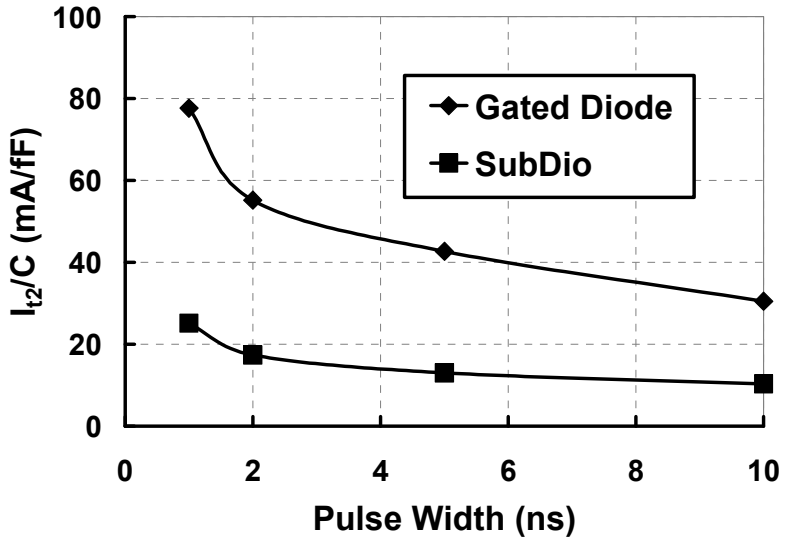



Fig. 3.15: Figure of merit comparison between the gated diode and the substrate diode.

## 3.3 Conclusion

This chapter presents the detailed electrical and ESD characteristics of the gated diode and substrate diode (SUBDIO), both of which can be implemented as the core building blocks for the rail-based clamping in SOI. It is shown that the overall capacitance of the gated diode is reduced by half with proper bias and implementation of biasing circuits. Both types of diodes are robust under forward and reverse bias ESD stress. While the SUBDIO is less thermally constrained and has much higher current shunting capabilities under both CDM and HBM, its excessive capacitance makes it less applicable in high-speed I/O applications. The gated diode shows much better FOM and can be constructed with very small feature size by using the poly gate mask in advanced technologies. Furthermore, the gated diode shows reduced on-resistance with shorter gate lengths, so it can directly benefit from technology scaling. The proposed gate biasing circuit minimizes the parasitic capacitance of the gated diodes and reduces the sensitivity of process parameters on performance, making it applicable and dependable in generic SOI process technologies. The SUBDIO requires special processing and has limited room for improvement with scaling. Therefore, it is not preferred unless in applications where excessive heating in the silicon film is prohibitive.

# Chapter 4

# ESD Devices for Pad-based Local Clamping I/O Protection in Advanced SOI Technologies

This chapter focuses on the electrical properties of protection devices and ESD characterization, physical modeling, and design of these devices for the local-clamping scheme. Two SCR-based devices, namely the field effect diode (FED) and the double-well field effect diode (DWFED), are presented in detail and improved in 45 nm silicon-on-insulator (SOI) technology. All the process steps are available in generic SOI technologies. ESD protection capabilities are investigated using very fast transmission line pulsing (VF-TLP) tests to evaluate the device's performance in charged device model (CDM) ESD events. The methods for reducing the turn-on time, a critical parameter for CDM protection, are explored in detail, and improvements are realized. Device capacitance, which is critical for high speed Input/Output (I/O) performance, is evaluated, and biasing schemes as well as device designs are proposed to reduce the parasitic capacitance during normal operating conditions. Technology computer aided design (TCAD) simulations are utilized to explain the device physics and evaluate design tradeoffs. This chapter first uses the DWFED as an example to highlight the advantages of local clamping compared to the diode-based rail clamping scheme which was introduced in previous chapters. Then, other local clamping device options such as the SOI SCR and FED are

explored and improved. Turn-on behaviors are compared in detail to identify suitable applications for each device. Applications in both ESD protection and power clamping are discussed. The proposed biasing circuit ensures the functionality of the devices in both normal operation and during ESD events, relaxing the geometrical requirements such that gates much longer than the minimum feature length can be used to construct robust and efficient ESD devices.

## 4.1 Double Well Field Effect Diode as Pad-based Local Clamping Device

The scaling of semiconductor technology unfavorably impacts on-chip ESD protection performance by decreasing I/O MOSFET's oxide breakdown voltage ($V_{BD}$) and parasitic bipolar junction trigger level (LBJT $V_{t1}$). The reduction of metal interconnect thickness increases its resistivity, causing high pad voltage during ESD. With ever-increasing I/O data-rate requirements, the capacitance budget is becoming more stringent. All these trends exacerbate the shrinkage of the ESD design window. On one hand, physics-based modeling [40-46] helps improve the device design process. On the other hand, architectural change need to be considered. The rail-based approach [10] presented in the previous chapter is becoming insufficient in the high-current CDM domain, owing to excessive voltage build-up along the long ESD current path involving resistive power buses, power-clamps [47-49], and the ESD diode. The dominance of sub-10 ns CDM failures [50] nowadays demands exploration of new design strategies and devices to avoid high voltage at the I/O pad. The local clamping [10] protection scheme (Fig. 4.1) is a promising option. By connecting an ESD device directly between the pad and $V_{ss}$, the protection circuit allows the ESD current to flow from the pad to ground without going through the $V_{dd}$ and $V_{ss}$ power buses (elements crossed out in Fig. 4.1) and the $V_{dd}$ to $V_{ss}$ power clamp. In this way, the discharge path resistance is considerably reduced and the pad voltage build-up is largely reduced. Note that in this scheme, the pad-to-$V_{dd}$

discharge still relies on rail-based clamping as the PMOS can generally tolerate higher ESD stress compared to NMOS [5]. The SCR-based SOI double-well field effect diode (DWFED) [20,51,52] (Fig. 4.2) has been developed and improved to fulfill the demand of local clamping devices in SOI. This device, featuring high current shunting capabilities, low capacitance, and higher-than-$V_{dd}$ trigger voltage, is a promising option.

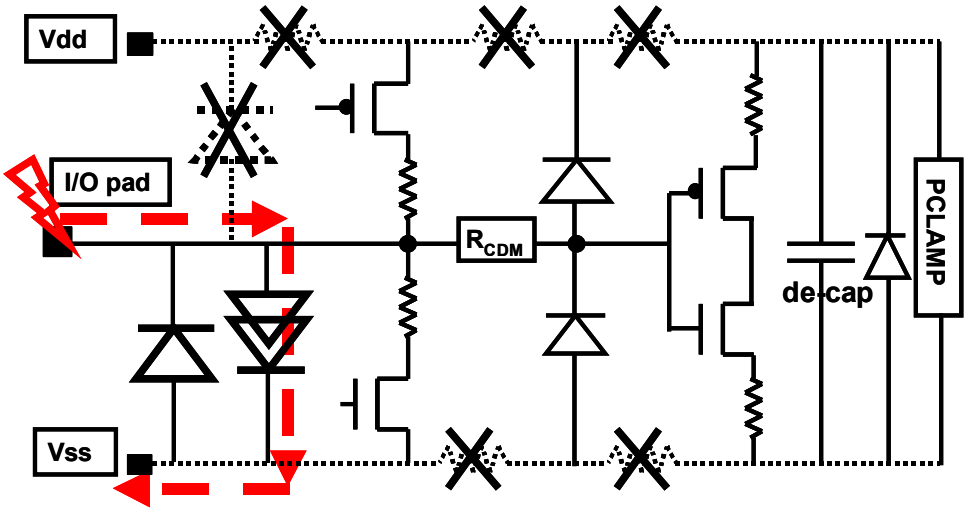



Fig. 4.1: I/O with the SCR-based local clamping device (drawn in double triangles) in place. Dashed red arrows represent the ESD current path. It shunts the majority of the ESD current into ground, without going through the resistive path along the power buses.

### 4.1.1 DWFED Device and Improved Device Structures

The DWFED structure is depicted in Fig. 4.2. The active region is entirely within the thin silicon film above the buried oxide (BOX) layer [53]. An N-well and a P-well are formed in the middle region and have the same well length. There is no well contact in order to reduce area. A poly-defined gate is constructed on top of the wells, allowing the formation of inversion in the wells by providing the appropriate gate bias whenever needed. A proposed biasing circuit is shown in Fig. 4.3. During normal operating conditions, $V_{dd}$ is high, so the inverter consisting of M1 and M2

pulls the voltage at the gate of the DWFED down to 0 V. During positive pad to $V_{ss}$ discharge, the $V_{dd}$ node becomes low due to the AC shorting of the decoupling capacitor (Fig. 4.1), turning on M1. Thus, the gate of the DWFED becomes coupled to the I/O pad, reducing the turn-on voltage. During pad-to-$V_{dd}$ discharge, the transistor M2 in the inverter pulls up the voltage at the gate of the DWFED, decreasing the DWFED's turn-on voltage. Note that in this discharge scenario, ESD current goes through the power buses and the power clamp, increasing the voltage across the PMOS gates. However, since PMOS gates are relatively more robust than the NMOS gates [5], this discharge path has not caused problems so far. $V_{dd}$-to-pad and $V_{ss}$-to-pad discharge relies on a diode connected in the opposite direction to that of the DWFED. The details of the turn-on behavior will be presented in the following sections.

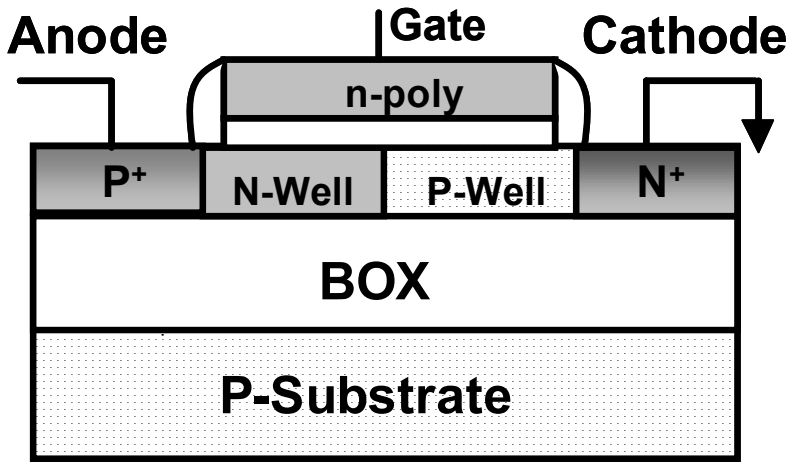



Fig. 4.2: DWFED connected between the I/O pad (to the anode) and $V_{ss}$ (to the cathode) in forward-biased connection.

To increase the turn-on voltage (thereby reducing leakage current and avoiding accidental false turn-on) of the DWFED, an extra processing step is applied to develop structures with higher turn-on voltage without affecting the device's ESD current shunting capability. For instance, an asymmetric DWFED is shown in Fig. 4.4. To fabricate this device, an anode-side silicide-blocking mask (available in

generic CMOS SOI technology) of 0.2 μm has been used to obstruct part of the P+ implantation next to the N-well, effectively extending the length of the N-well region while keeping the original poly gate length of 0.5 μm. This structure is named the Anode Silicide-Blocked DWFED (ASB-DWFED). Its superior characteristics will be compared with the original DWFED in later paragraphs.

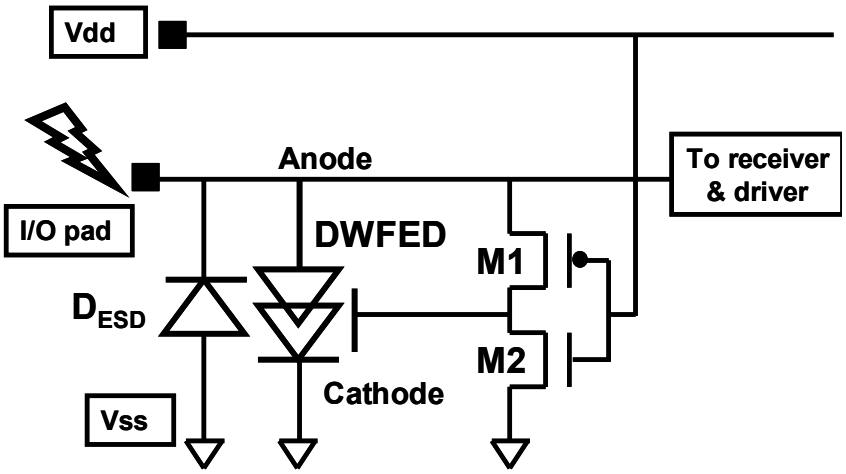



Fig. 4.3: Biasing circuit for the DWFED. The inverter (consisting of M1 and M2) ensures DWFED's gate at ground during normal operation and coupled high during ESD.

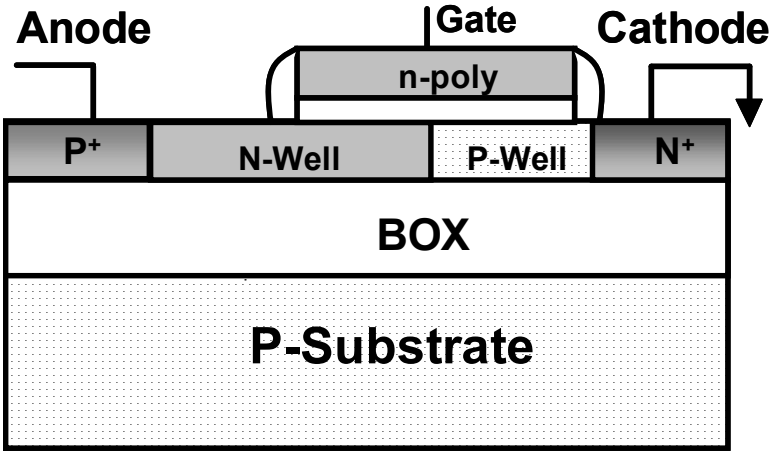



Fig. 4.4: ASB-DWFED ESD structure. Silicide block mask is used on the left side of the gate and above the N-well to block part of the P+ implant and extend the well length.

### 4.1.2 DWFED VF-TLP I-V Characteristics

Fig. 4.5 contains the VF-TLP I-V and leakage characteristics of the DWFED. The curves for the gated diode and SUBDIO detailed in last chapter are also plotted for comparison. Pulse widths of 2 ns, 5 ns and 10 ns have also been measured experimentally and the results will be summarized later in this chapter. From the VF-TLP I-V characteristics, key parameters such as the second breakdown current ($I_{t2}$), turn-on voltage ($V_{on}$) and the dynamic resistance ($R_{on}$) can be determined for ESD-performance evaluation. All data points up to $I_{t2}$ are plotted.

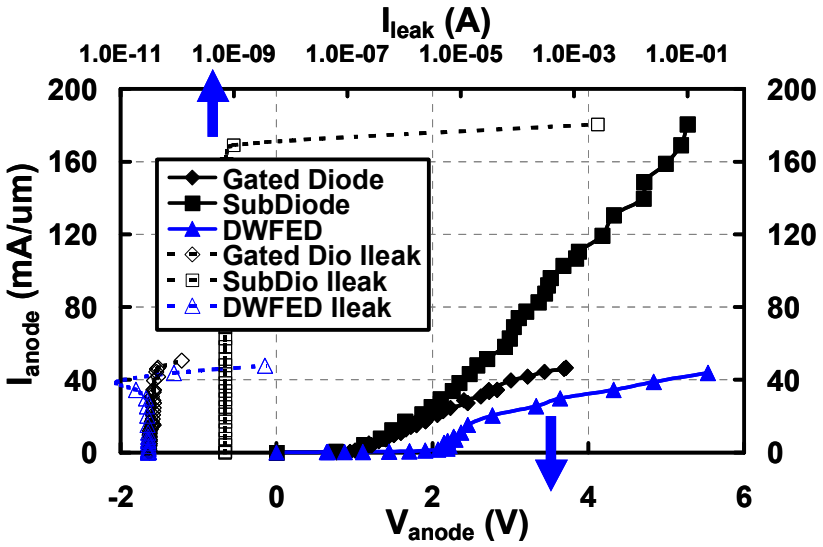



Fig. 4.5: Measured 1 ns VF-TLP I-V and post-ESD DC leakage characteristics of DWFED, gated diode and SUBDIO. Solid points represent VF-TLP I-V (x-axis on the bottom of the figure); transparent points represent post-stress leakage current (x-axis on top of the figure). The I-V and leakage share the same Y-axis.

As shown in the 1 ns VF-TLP I-V characteristics in Fig. 4.5, the DWFED has a turn-on voltage around 1 V, normalized $I_{t2}$ of about 44 mA/μm, and $R_{on}$ of approximately 80 Ω·μm. The 100 ns regular TLP results including the trigger voltage $V_{t1}$, $I_{t2}$, and on-resistance $R_{on}$ are summarized in Table 4.1. The TLP results are correlated with the human-body model (HBM) level [9], the other major ESD standard test level.

Table 4.1: Measured 100 ns TLP (corresponds to HBM) ESD characteristics summary

| | $V_{t1}$ (V) | $I_{t2}$ (mA/um) | $R_{on}$ (Ohm*um) |
|---|---|---|---|
| **Gated Diode** | 0.9 | 10 | 130 |
| **Sub Diode** | 1 | 45 | 33 |
| **DWFED** | 1 | 12 | 167 |

With a P-N-P-N structure doped underneath the gate, the DWFED device takes advantage of the SCR-like structure and behavior. The triggering mechanism of this device is illustrated in three steps in Figs. 4.6-4.8 for the case of negative gate bias. Current density distribution in the silicon film is obtained from TCAD device simulations [54,55]. When a gate bias of –0.2 V and a low anode bias of 0.4 V are applied, despite the formation of the inversion region underneath the gate in the N-well, the device is in the forward-blocking mode. A very small amount of current flows near the surface as shown in Fig. 4.6. The twin-well under the gate causes symmetric behavior with respect to the gate bias: for a positive gate bias, the inversion layer forms in the P-well region; while for a negative gate bias, the inversion layer forms in the N-well region. In both cases, little current flows in the channel because under low anode bias, the current is mostly due to generation and recombination.

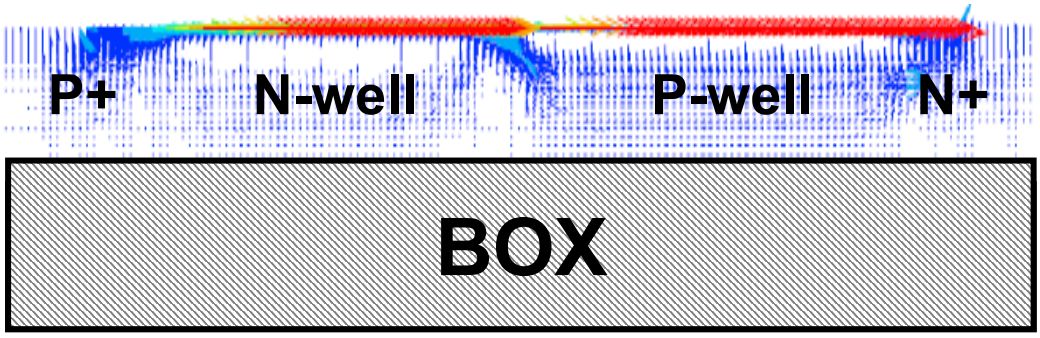



Fig. 4.6: Current density plot for symmetric DWFED under anode bias voltages $V_a$ = 0.4 V. Gate is biased at $V_g$ = -0.2 V to cause inversion in the N-well.

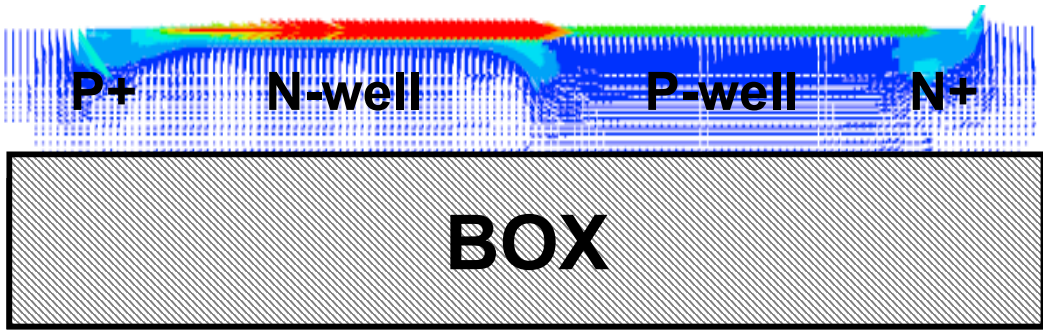



Fig. 4.7: Current density plot for DWFED under anode bias voltages $V_a$ = 0.6 V. More and more carriers are injected into the P-well through the channel in N-well.

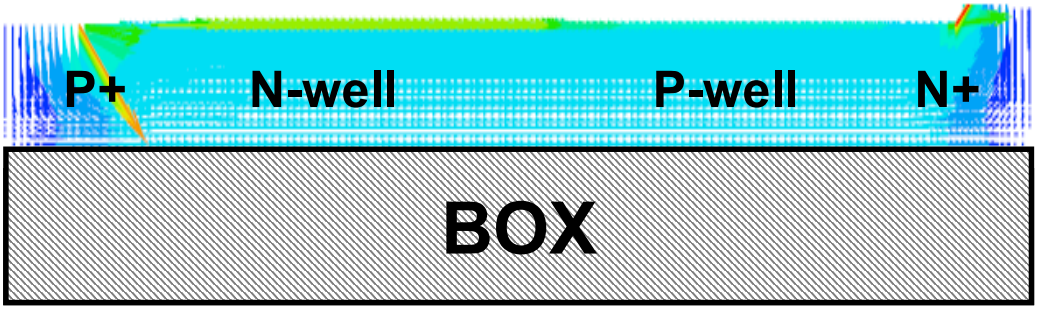



Fig. 4.8: Current density plot for DWFED under anode bias voltages $V_a$ = 1 V. At this point, the anode voltage is high enough to cause the turn-on of the P-N-P-N structure.

However, as the anode bias increases to 0.6 V (Fig. 4.7) while keeping the same gate bias, the inversion layer forms across the entire film near the surface, connecting the P+ region at the anode and the P-well. Increasingly, carriers travel through the channel and contribute to the current in the P-well region. As the anode bias continues to increase to 1 V (Fig. 4.8), the hole injection into the P-well region is large enough to trigger the lateral bipolar junction transistor (LBJT) effect in the N-P-N (formed by the N-well, P-well, and N+ regions), leading to regenerative feedback and reduced resistance. Similar to an SCR device behavior, significant current flows across the entire well region. The strong current-carrying capability enables the device to shunt high ESD current.

Table 4.2: DC leakage current comparison, unit: A/μm. Forward bias is applied to ASB-DWFED to simulate the real situation of local-clamping.

| $V_{DUT}$ | Reverse at -1V | Forward at 0.33V | Forward at 0.5V | Forward at 1V |
|---|---|---|---|---|
| **Gated Diode** | 4.33E-12 | 4.00E-11 | 8.00E-11 | |
| **Sub Diode** | 6.40E-13 | 1.20E-10 | 3.14E-09 | |
| **ASBDWFED** | | | | 4.12E-10 |

In addition to the ESD capability, low leakage levels are required for the DWFED to be implemented in pad-based local clamping protection, since the device is constantly under forward bias. The leakage current levels of the three devices are summarized in Table 4.2. When implemented as power-rail-based ESD devices, the gated diode and the SUBDIO are reverse-biased during normal operating condition. Consequently, very low leakage current flows through the devices, as expected. As shown in Fig. 4.5, the turn-on voltages of the gated diode and the SUBDIO under forward-bias are around 1 V, within the normal $V_{ss}$ to $V_{dd}$ range. Therefore, despite the occasional use in pad-based local clamping for low-swing circuit [56], a single P/N-based diode is generally not adequate for local clamping in I/O circuitry where larger voltage swing is expected. During ESD events, high levels of current can be shunted directly from the pad to the anode of the DWFED and then the ESD surge flows out of the cathode, without going through the resistive $V_{dd}$ and $V_{ss}$ buses. Under normal operating conditions, the ESD device is frequently under forward-biased. Leakage current has to be minimized to reduce power consumption. Thanks to the aforementioned forward-blocking functionality, the DWFED's leakage current can be controlled to a very low level.

However, the work in [51] illustrates a limitation of the original DWFED. The device's turn-on voltage can only be as high as 1 V, above which the current significantly increases. The I/O voltage can reach above this level, causing false-triggering and making the DWFED an unreliable device for local clamping. To

overcome this shortcoming, the ASB-DWFED, shown in Fig. 4.4, is developed. In this device, it becomes more difficult to form the p-channel in the extended N-well region, due to weaker gate control. To clearly explain this point, electric potential, carrier and current density plots are shown in Fig. 4.9, 4.10, and 4.11 under low gate bias and 1 V anode bias. The silicide-blocked region is exposed outside the poly gate and oxide. With low gate bias, no inversion is formed in this region. Thus, the P-N-P-N structure is still present in the silicon film even when the anode voltage reaches 1 V. As a result, the device is in the forward-blocking mode and an insignificant amount of current flows. This effect is verified by the current density simulation results (Fig. 4.11) and direct current (DC) I-V measurement (Fig. 4.12). In Fig. 4.12, the 0 V gate bias DC I-V measurement for the original (with no silicide block) DWFED is plotted in a dashed line for comparison. Results show that the new DWFED maintains a very low leakage current level even for anode voltages higher than $V_{dd}$, reducing the overall power consumption and making it suitable for pad-based local clamping.

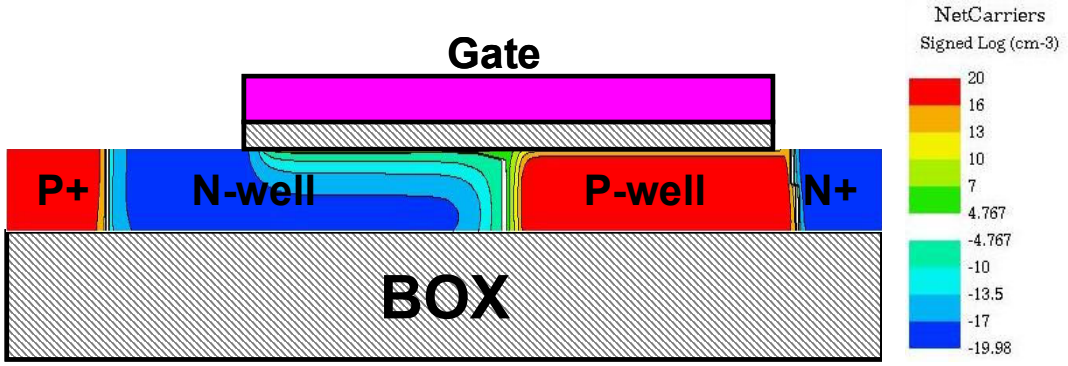



Fig. 4.9: Carrier density plot for the ASB-DWFED under $V_a$ = 1 V, $V_g$ = -0.2 V.

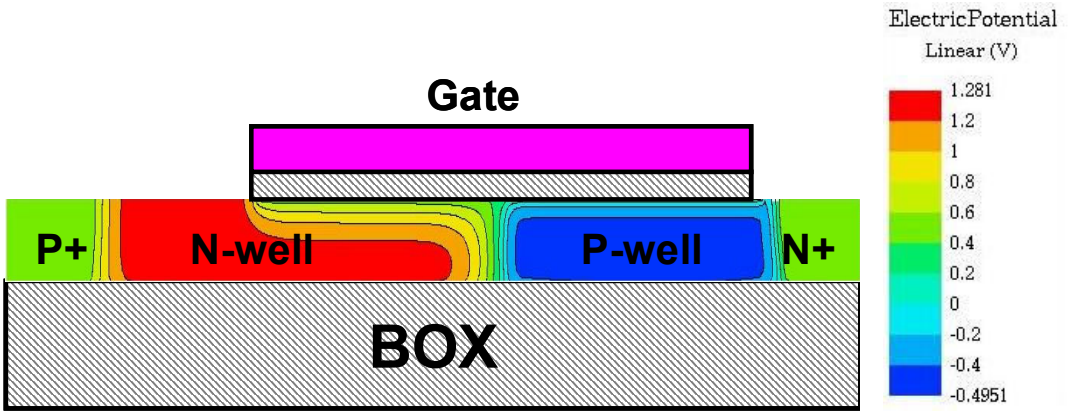



Fig. 4.10: Electric potential plot for the ASB-DWFED under $V_a$ = 1 V, $V_g$ = -0.2V.

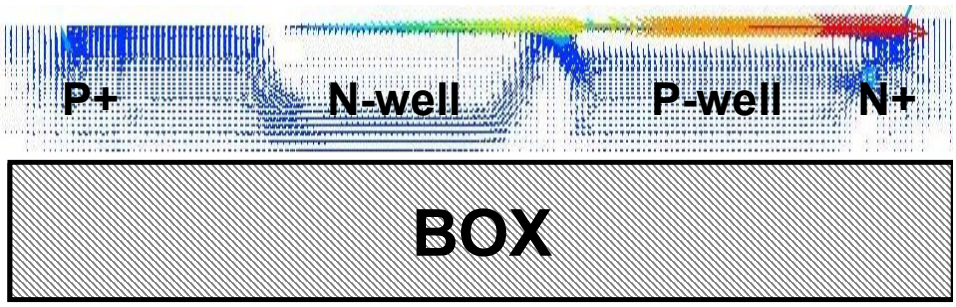



Fig. 4.11: Current density plot of the ASB-DWFED under $V_a$ = 1 V, $V_g$ = -0.2 V. Insignificant amount of current flows.

The VF-TLP I-V characteristics shown in Fig. 4.5 demonstrate a slightly lower current-shunting capability of the DWFED compared to the gated diode. This is mainly due to the higher resistance caused by longer gate lengths and extended body length used in the fabrication process to maintain an adequate turn-on voltage. The transient behavior of the DWFED will be investigated in detail in the next section.

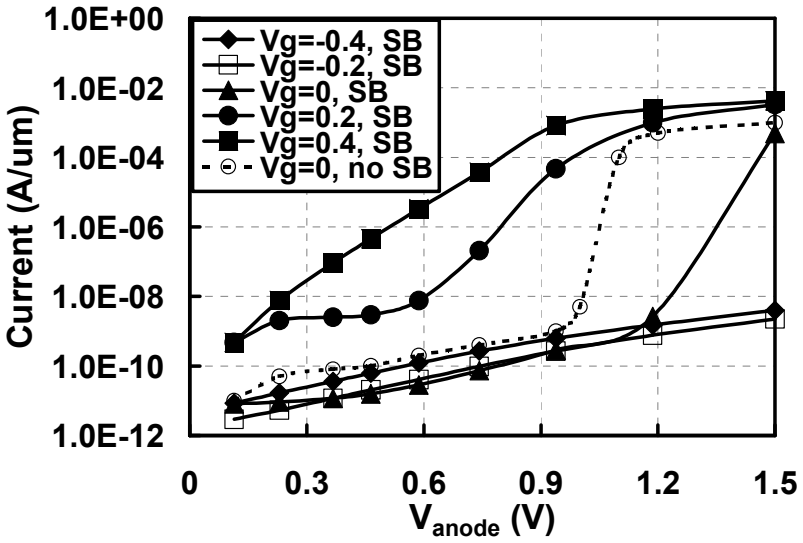



Fig. 4.12: Measured ASB-DWFED DC I-V characteristics for gate voltages of -0.4 V, -0.2 V, 0 V, 0.2 V, and 0.4 V; and regular DWFED (no SB) at 0 V gate voltage.

### 4.1.3 DWFED Capacitance Characteristics

Technology scaling and the shrinkage of the ESD design window reduces the ESD device capacitance budget for high-speed I/O serial link data rates of above 20 Gbits/s to below 100 fF [9]. The appropriate method to evaluate the device's ESD efficiency is by using the figure-of-merit (FOM) $I_{t2}/C$, which normalizes the second breakdown current with respect to the capacitance per width. After examining the I-V characteristics and breakdown levels in last section, this section delves into the characterization and reduction of parasitic capacitance.

The capacitance of both the DWFED and ASB-DWFED has been measured. With an inherent three-junction-in-series structure in the DWFED formed by the two lateral P/N junctions and the middle N/P junction, the overall capacitance is expected to be less than that of a single-junction diode, when no inversion layer is formed in either of the two wells underneath the gate. As depicted in Fig. 4.13, in which cathode capacitances (measured at 1 MHz) are plotted against cathode voltage for

gate biases at 0 V, for the original DWFED and ASB-DWFED. The capacitance of these two devices differs by an insignificant amount of about 5%.

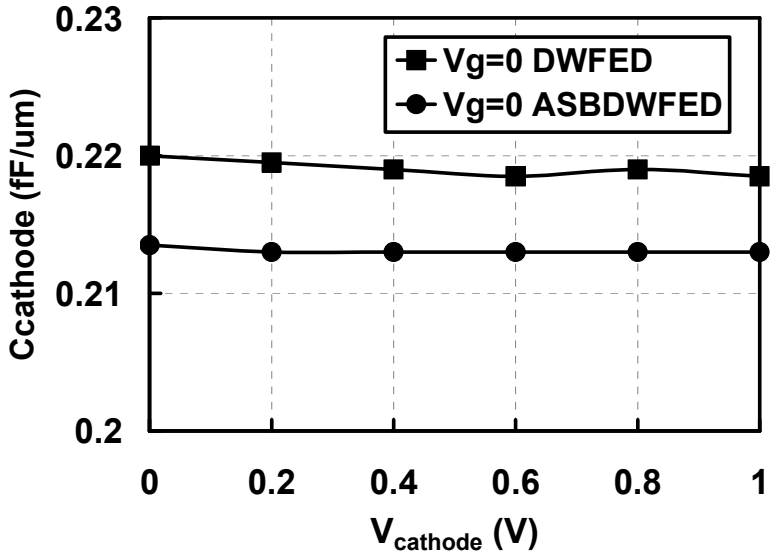



Fig. 4.13: Regular DWFED vs. ASB-DWFED cathode capacitance ($C_c$) measurement comparison. $V_g$ is biased at 0 V and $V_{cathode}$ varies from 0 to 1 V.

In Fig. 4.14, the total capacitance results measured at the anode are plotted against anode voltage for gate biases at 0 V. These results highlight the major advantage of the ASB-DWFED. The DWFED's leakage current increases with higher anode voltage, as depicted in the DC I-V characteristics (Fig. 4.12). A leaky path from the anode to cathode yields significantly higher capacitance measurement results, because the three aforementioned series junctions are collapsed into a single junction due to carrier injection. While the capacitance of the DWFED increases considerably as the anode voltage increases, the capacitance of the ASB-DWFED is almost constant over a wide voltage range. It is at a low level around 0.23 fF/μm even at $V_a$ = 1 V. The stable resistance value makes the ASB-DWFED a preferred option for local clamping ESD applications. The flat curve implies that circuit's linearity is not affected by the ESD device. From these results, it is concluded that stable capacitance is ensured as long as the leakage and turn-on of the device is

controlled. With the biasing circuit shown in Fig. 4.3, the ASB-DWFED can be reliably implemented as a local clamping device.

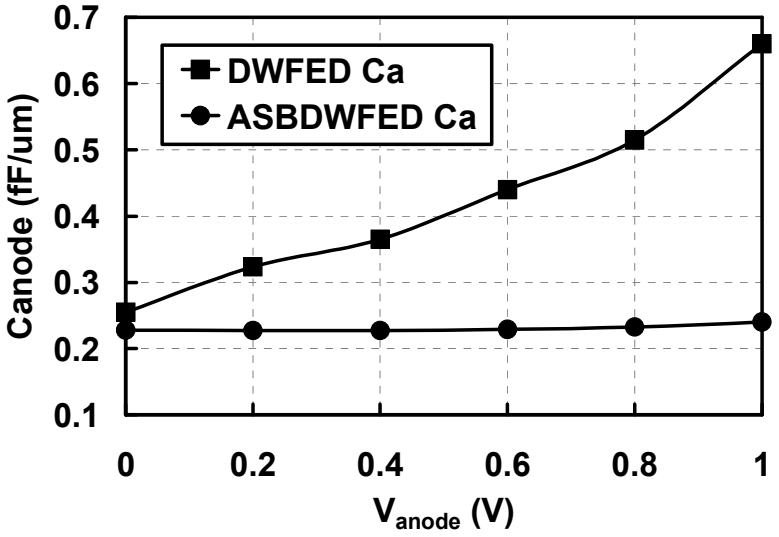



Fig. 4.14: Regular DWFED vs. ASB-DWFED anode capacitance ($C_a$) measurement comparison. $V_g$ is biased at 0 V and $V_{anode}$ varies from 0 to 1 V.

### 4.1.4 Figure-of-Merit Comparison

A comparison of the VF-TLP characteristics of the DWFED and ASB-DWFED is summarized in Table 4.3. Note that the $I_{t2}$ and $R_{on}$ are about the same for these two devices, despite the different well lengths. Therefore, the device's ESD performance should vary little with scaling of dimensions. Table 4.4 compares the critical characteristics of the gated diode, substrate diode and ASB-DWFED in terms of their second breakdown current, minimum achievable capacitance, dynamic resistance and other figure-of-merits. The total ESD path resistance is also summarized in this table. Table 4.4 includes a commonly used device level figure-of-merit, $I_{t2}/C$. The FOM comparison for the three devices is presented in Fig. 4.15. While the ASB-DWFED shows some benefit from this device level figure-of-merit comparison, its overall advantages are more prominent when it is implemented in local clamping to

reduce the clamping voltage between the pad and the power bus and expand the ESD design window. A comparison between rail-based clamping and local clamping will be presented in next chapter.

Table 4.3: Comparison between DWFED and ASB-DWFED.

| | DC $V_{t1}$ | 1ns $V_{t1}$ | $I_{t2}$ (mA/um) | $R_{on}$ (Ohm*um) | Cap (fF/um) $V_g$=0, $V_a$=0 | Cap (fF/um) $V_g$=0, $V_a$=1 |
|---|---|---|---|---|---|---|
| **DWFED** | 0.91 | 1.3 | 44 | 80 | 0.21 | 0.55 |
| **ASBDWFED** | 1.2 | 2 | 46 | 80 | 0.21 | 0.23 |

Table 4.4: Second breakdown current, minimum achievable capacitance, dynamic resistance and other Figure-of-Merit comparison. The $I_{t2}$ values are obtained under 1 ns VF-TLP pulses. "x2" implies that devices are constructed in pair but opposite directions to carry ESD current in both directions.

| Device | $I_{t2}$ (mA/um) | $C_{min}$ (fF/um) | $R_{on}$ (Ohm*um) | $I_{t2}/C_{min}$ | $R_{on}*C_{min}$ | ESD Path Rtot |
|---|---|---|---|---|---|---|
| **Gated Diode** | 47 | 0.3x2 | 60 | 78 | 36 | $R_{pad}+R_{ESD}+R_{Vdd}+R_{Vss}+R_{clamp}$ |
| **Sub Diode** | 180 | 3.6x2 | 22 | 25 | 158 | $R_{pad}+R_{ESD}+R_{Vdd}+R_{Vss}+R_{clamp}$ |
| **ASBDWFED** | 44 | 0.21+0.23 | 80 | 100 | 35.2 | $R_{pad}+R_{ESD}$ |

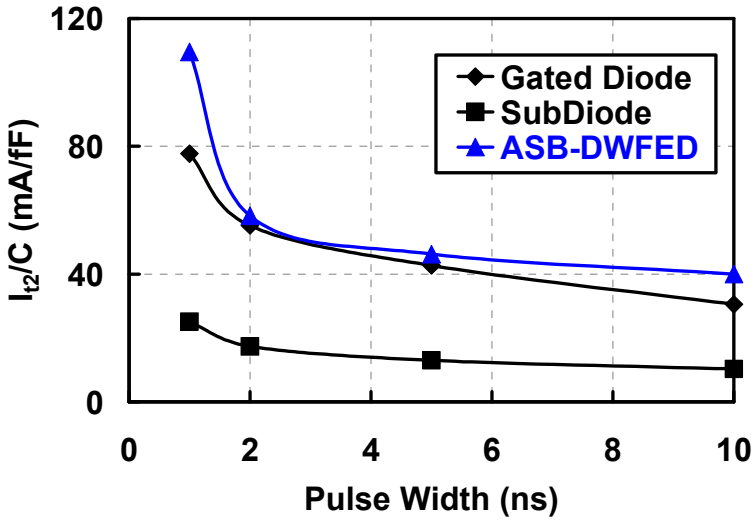



Fig. 4.15: Figure of merit comparison between the gated diode and the substrate diode.

The Table 4.2 presented earlier in this section includes leakage current comparison for diodes under 0.33 V and 0.5 V forward biases, which correspond to the three-diodes-in-series and two-diodes-in-series cases, respectively. Reverse bias leakage is also summarized. For the ASB-DWFED, only 1 V bias case is tested because it is not connected in series with other devices for local clamping. As shown in the table, the leakage current for all devices is lower than 5 nA/μm. Moreover, based on the 100 ns TLP characterization method [2], the required widths, total capacitance and clamping voltage for meeting 2KV HBM level are 120 μm, 72 fF, 2.5 V for the gated diode; 30 μm, 216 fF, 2.7 V for the SUBDIO; and 111 μm, 47 fF, 3 V for the ASB-DWFED.

In this investigation, the device behavior under positive, negative and 0 V gate biases have been characterized. In some of the results in Fig. 4.12, it has been shown that negative gate biases can optimize performance. However, this is not to say that improvement can only be achieved with negative biases. As shown in Figs. 4.13 and 4.14, even with 0 V bias the capacitance is significantly lowered and the turn-on

voltage is increased to above $V_{dd}$. Implementing the bias circuit to have 0 V bias under normal operating conditions is a reasonable solution in terms of practicality.

## 4.2 Improvement on Transient Effects for SCR-based ESD Devices

The previous section presents the DWFED and ASB-DWFED for local clamping ESD protection which offers architectural level benefits. In the past, silicon-controlled rectifiers (SCR) have also been considered for local clamping ESD applications [28]. A key requirement for local clamping devices is that the turn-on voltage needs to be above the $V_{ss}$ to $V_{dd}$ range, in order to avoid accidental turn-on and minimize leakage current during normal operation. Meanwhile, the turn-on voltage ($V_{on}$) should not be high enough to damage the I/O devices. Low capacitance and resistance are required to minimize parasitic loading. Furthermore, an important CDM-specific requirement is that the device should turn on faster than the CDM event to shunt current before the excessive charge accumulation raises the pad voltage. However, the conventional SCR suffers from high turn-on voltage and slow turn-on speed which causes problems in sub 10-ns CDM protection especially in deeply scaled technologies. In this section, the ASB-DWFED (for brevity, the ASB-DWFED is simply called "DWFED" in this section since only this type of DWFED is examined) and the field-effect diode (FED) are characterized and improved to address the challenges of SCR devices. They are fabricated and characterized in 45 nm silicon-on-insulator (SOI) technology and are experimentally shown to be suitable for pad-based local clamping under normal supply voltage ($V_{dd}$) range (below 1 V). ESD protection capabilities are investigated using VF-TLP and transient waveforms are fully analyzed. The FED's advantages in improving transient turn-on behavior and reducing DC leakage current are discovered. Gate bias helps improve the turn-on speed of the DWFED. Comparisons between FED, DWFED and SCR devices are shown. Technology CAD (TCAD) simulations are used to interpret the turn-on behavior and guide design improvement. The improved devices enable the implementation of local clamping and power clamping.

### 4.2.1 SCR, DWFED and FED Structures

A conventional SOI SCR device [29,57-59] is illustrated in Fig. 4.16. The active silicon film region is above the BOX. P+ defines the anode and N+ defines the cathode. A silicide-block (SB) mask is used to define the N-well (NW) and P-well (PW) in the middle. Body contacts can be connected to the wells when needed. The P-N-P-N structure serves as a current-blocking structure in normal operating conditions, and as an SCR during ESD-triggered turn-on. However, the turn-on speed is largely limited by two time constants [60]. First, the base-transit time of the NW and PW, which serve as the bases of the P-N-P bipolar junction transistor (BJT) and the N-P-N BJT. Second, the charge storage time in the wells.

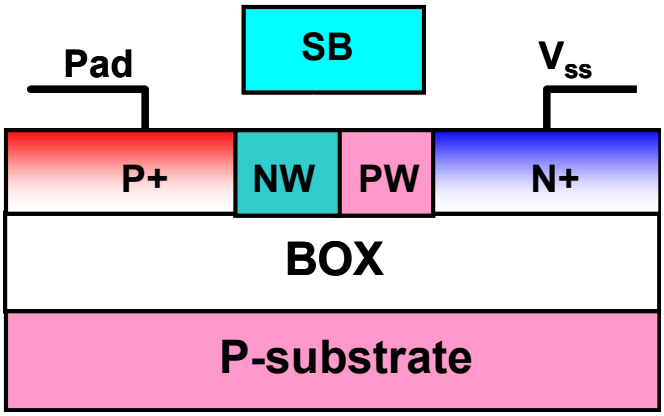



Fig. 4.16: Conventional SCR in SOI. Silicide block (SB) is used to prevent silicidation on the surface and define the n-well (NW) and p-well (PW).

To overcome the turn-on limitations of the SCR, improved devices such as the DWFED [52] and the field-effect diode (FED) (Fig. 4.4) have been developed [61,62] based on [63,64]. These devices combine the features of P-N-P-N SCR to block leakage current during normal operating conditions, and the forward-biased P-N junction diode to shut off the high current rapidly during the ESD event.

The structure and functionalities of the DWFED, first introduced in the previous section, are shown in Fig. 4.17 and recapitulated to highlight the similarities and differences with the FED in this section. The inverter's gate is connected to $V_{dd}$, and

the output is connected to the gate of the DWFED. During the normal operating conditions (Fig. 4.17 (b)), the inverter's NMOS is on, pulling the DWFED's gate voltage to ground. The DWFED preserves its intrinsic P-N-P-N structure, reducing leakage current. This is similar to an SCR's off mode. However, during an ESD event (Fig. 4.17 (c)), the $V_{dd}$ is pulled to ground by the de-coupling capacitance (Fig. 4.1) between $V_{dd}$ and ground, turning on the PMOS in the inverter. The DWFED's gate is now pulled to a high level, creating an inversion layer in the P-well (for positive ESD at the pad). This inversion layer connects the NW and N+ regions, collapsing the junctions between them. The device degenerates to a P-N diode between P+ and NW, and the turn-on speed is not limited by the base transit time or charge storage build-up.

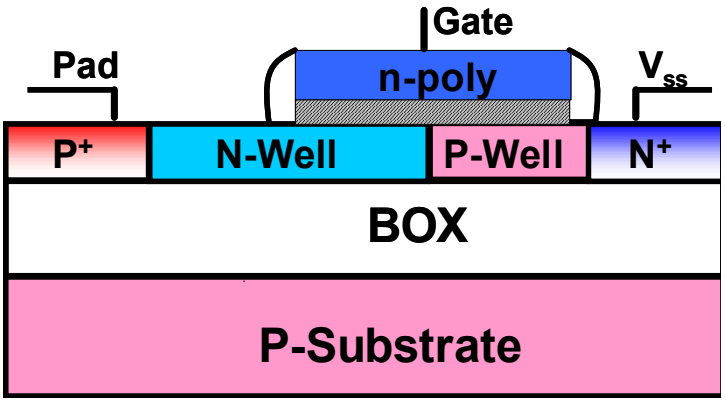



Fig. 4.17 (a): DWFED structure. (For abbreviation, the "DWFED" structures in this section are all ASB-DWFED introduced in the previous section.)

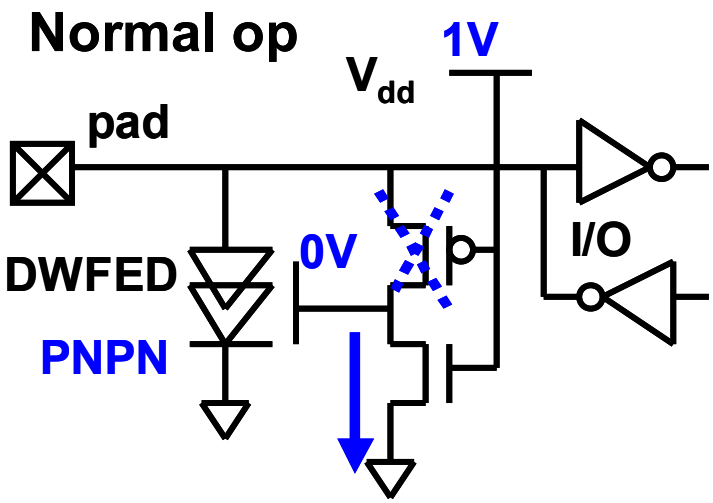



Fig. 4.17 (b): DWFED structure and biasing circuit behavior under normal operating conditions. The NMOS pulls DWFED's gate voltage to ground.

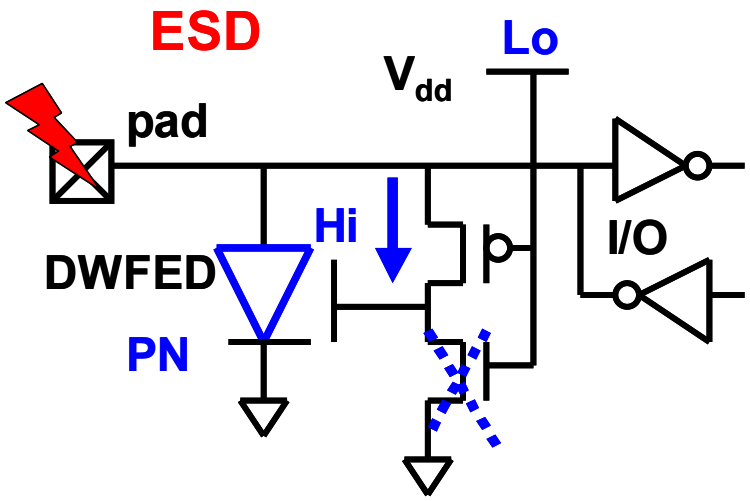



Fig. 4.17 (c): DWFED structure and biasing circuit behavior under ESD conditions. The PMOS pulls DWFED's gate voltage to high level.

The FED (Fig. 4.18) is built with two separate controlling gates on top of the SOI diode. Different from the DWFED, the FED is intrinsically a P-I-N diode, except the "intrinsic" region is a lowly doped well region. Fig. 4.18 (b) depicts that in normal operating conditions, $V_{dd}$ biases the gate and inverts the PW region underneath G1, forming a P-N-P-N structure in the silicon film, blocking the leakage current. In ESD

(Fig. 4.18 (c)), $V_{dd}$ is pulled to a low level by the decoupling capacitor (Fig. 4.1), converting the FED back to the intrinsic P-N diode state, which is capable of shunting high levels of current rapidly.

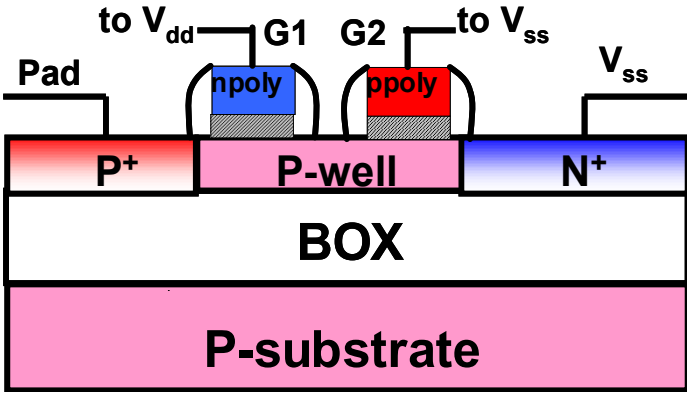



Fig. 4.18 (a): FED structure. Two gates are built above the P-well. There is only one P-type well.

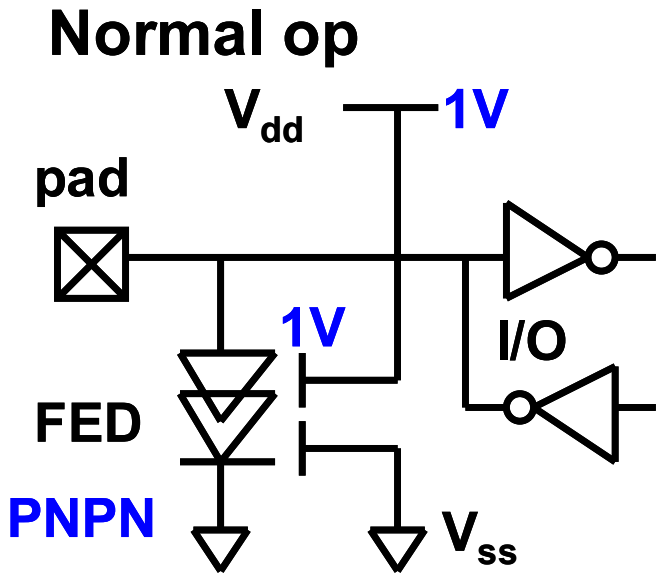



Fig. 4.18 (b): FED structure and biasing circuit behavior under normal operating conditions.

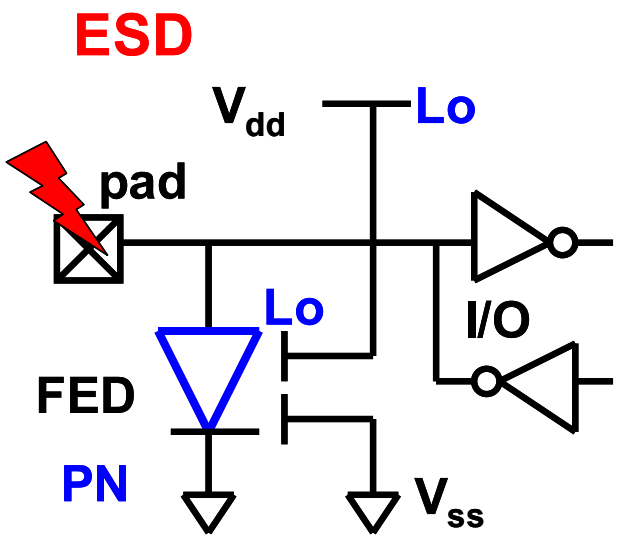



Fig. 4.18 (c): DWFED structure and biasing circuit behavior under ESD conditions. $V_{dd}$ is pulled to low level by the decoupling capacitor between $V_{dd}$ and $V_{ss}$.

However, the original FED's anode turn-on voltage ($V_{on}$) is below the supply voltage ($V_{dd}$) as shown in the I-V characteristics, which translates into high levels of leakage current in normal conditions, unless a high gate bias (> 2 V) is applied to maintain the P-N-P-N structure. Such gate bias is not readily available on-chip.

While the original FED structure (Fig. 4.18) works in applications where a bias voltage above 1 V is available, it is required to find solutions suitable for supply voltages near 1 V or below in high-performance integrated circuits. A limitation has been identified [61] in device design. If the P-well doping is not high enough, during normal operation, the high common-emitter gain of the N-inversion/P-well/N+ region induces lateral bipolar junction transistor (LBJT) effects, even at low anode voltages below $V_{dd}$, which results in unwanted turn-on and latch-up behavior when the device is expected to be in the forward-blocking mode. However, if the P-well (PW) doping is appreciably higher, a $V_{G1}$ higher than $V_{dd}$ is required to form the inversion in the PW in order to maintain the forward-blocking mode, making the device impractical. Therefore, the doping of the regions under G1 and G2 need to be controlled separately as suggested in the simulation study in [65]. An improved

"P+/P-/$HV_t$/N+" FED (I-FED) structure is created with the P-type High-$V_t$ ($HV_t$) doping under G2 to improve the performance and the structure is shown in Fig. 4.19. This device takes advantage of the increased doping level under G2 to reduce the common emitter gain of the parasitic N-inversion/P-well/N+ BJT, thus increases the anode turn-on voltage of the P-N-P-N structure to above 1 V. Also, this structure makes use of the low doping under G1 that results in the reduction in minimum gate voltage requirement (to < 1 V) for maintaining the inversion layer under G1. The characteristics will be detailed in the following sections.

All the devices in this work are fabricated using 45 nm SOI technology [26]. The gate length is 0.5 μm for each gate unless otherwise noted. For the DWFED (Fig. 4.3), a 0.2 μm silicide block is used to block part of the P+ implant, thereby extending the NW, creating an asymmetric device. An important fact about the three structures introduced in this section is that while the SCR, DWFED and FED differ in functionalities and structures, they share similarities in process steps. The primary structural difference lies in the number of gates and the number/types of wells. Since the SCR is a conventional device, the FED and DWFED can be implemented in any generic SOI process without special masks.

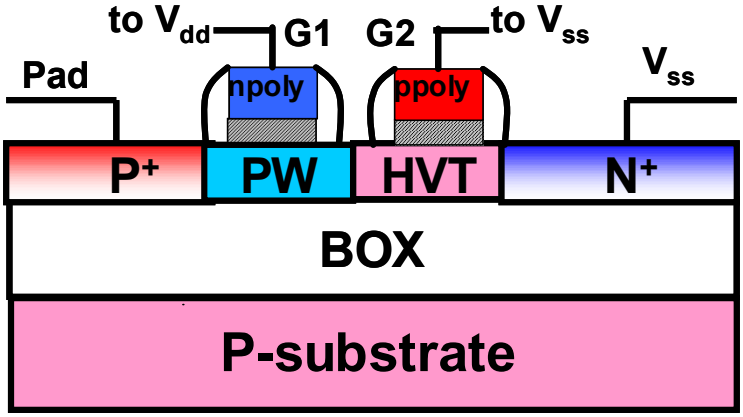



Fig. 4.19: Improved FED (I-FED) with High-$V_t$ P-type doping under G2 and P-doping (which forms P+/P-/$HV_t$/N+) under G1.

### 4.2.2 SCR vs. DWFED Transient Comparison

Since the SCR and DWFED share structural similarities in the silicon film region, and both of them can be regarded as SCR-based, the transient analysis of the next two sections starts with a comparison between the SCR and DWFED.

The SCR is stress-tested under VF-TLP, and the I-V around the turn-on is enlarged and presented in Fig. 4.20 for different pulse widths. The I-V plot shows that the longer pulse width cases show more evident snapback. In order to explain such behavior, full transient waveforms are analyzed in Fig. 4.21. Each of the three curves shows a voltage spike of 1.3 ns long, which means that the device is not turned on yet. The ESD charge accumulates, causing a sharp increase in voltage. The device turns on after 1.3 ns, as shown by the current waveforms in the same plot. However, the 1 ns pulse has already ended before the device turns on. Since the voltage values plotted by the VF-TLP tester in Fig. 4.20 is determined by the average of the voltage from 20% to 80% of the pulse duration, the 1 ns curve does not show any voltage set-back. Both the 2 ns and 10 ns stress are long enough for the device to enter the turn-on mode. For the 10 ns case, the average voltage value is taken in the stable plateau region, hence the snapback is fully captured in Fig. 4.20. However, if the I-V curves are the only characteristics considered, analysis would fail to take the spike into account, thus potentially overlooking an important hazard. Thus, it is best practice to analyze the transient waveforms when possible.

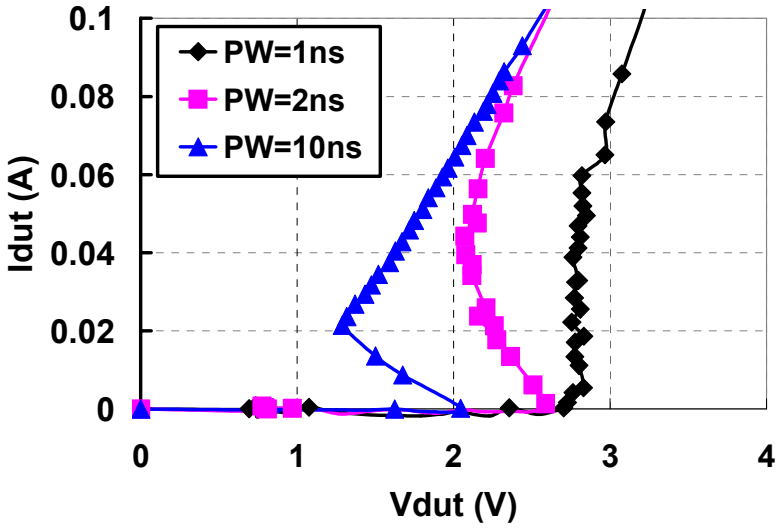



Fig. 4.20: Measured VF-TLP I-V curves of the SOI-SCR structure under different pulse widths.

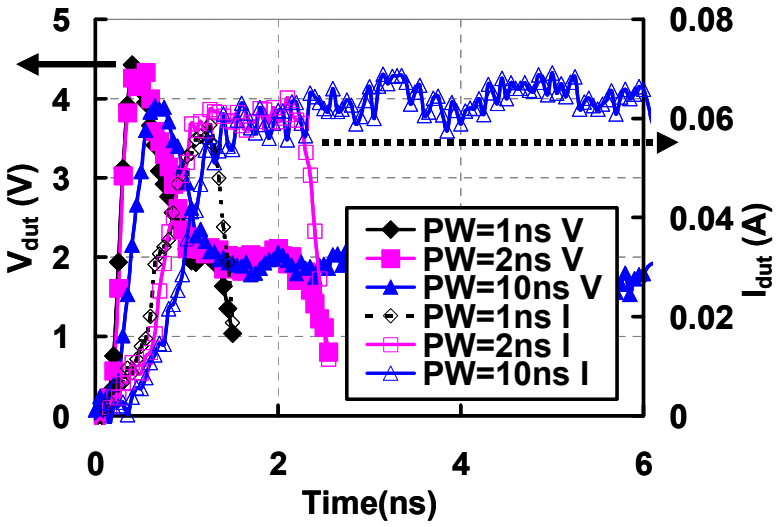



Fig. 4.21: Transient voltage and current waveforms of the SOI-SCR structure for different pulse widths.

The DWFED is stressed under VF-TLP, and the I-V around turn-on is enlarged and presented in Fig. 4.22 for different pulse widths. Snapback exists in all three cases. The reason can be explained by the shorter turn-on time of the DWFED. As

shown in Fig. 4.23, the DWFED turns on in about 0.5 ns, much faster than the SCR. Therefore, even for the 1 ns VF-TLP experiment, the device has enough time to turn on. And the voltage in Fig. 4.22 is calculated from the average voltage in the plateau region, which is much lower than the peak.

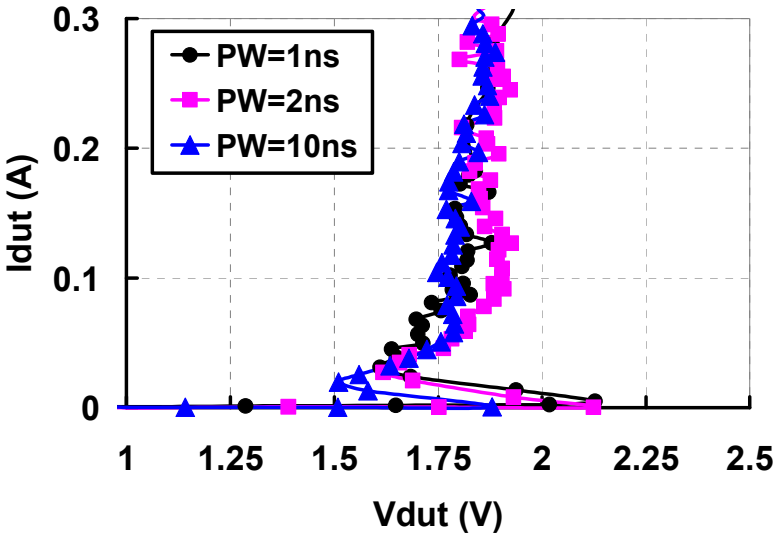



Fig. 4.22: Measured VF-TLP I-V curves of the DWFED under different pulse widths.

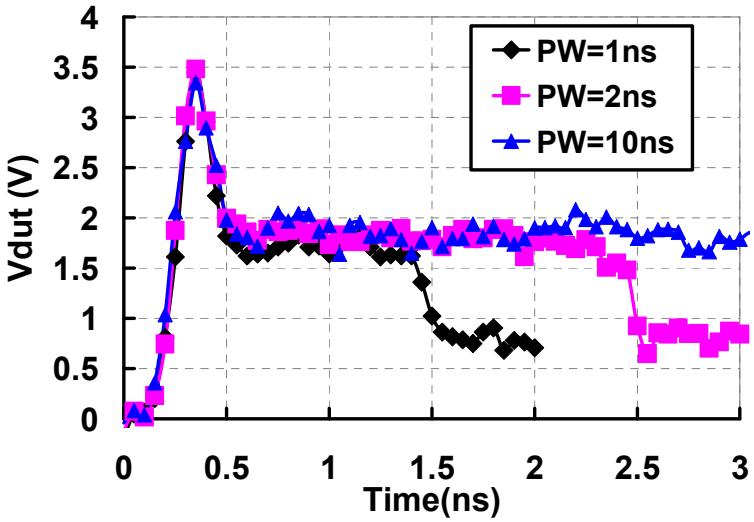



Fig. 4.23: Transient waveforms of the DWFED structure for different pulse widths.

Even though the DWFED turns on quickly, the voltage build-up may still jeopardize the I/O devices as the breakdown voltage has reached 3 V [5]. To explore the methods of improving the turn-on speed, bias is applied at the DWFED's gate to emulate the coupling. The VF-TLP I-V in Fig. 4.24 shows that a higher gate voltage can reduce the trigger voltage ($V_{t1}$). This is because the gate voltage helps to form an inversion in the PW, and the channel current of the N-P-N provides the base current of the P-N-P. The BJT current of the P-N-P provides the base current for the N-P-N in turn. This process is regenerative, and the turn-on is accelerated. Quickly, the P-N-P-N collapses into a diode-like structure. Voltage reduction is validated in the transient measurements shown in Fig. 4.25. The gate bias induced improvement can be achieved using the trigger circuit shown in Fig. 4.17.

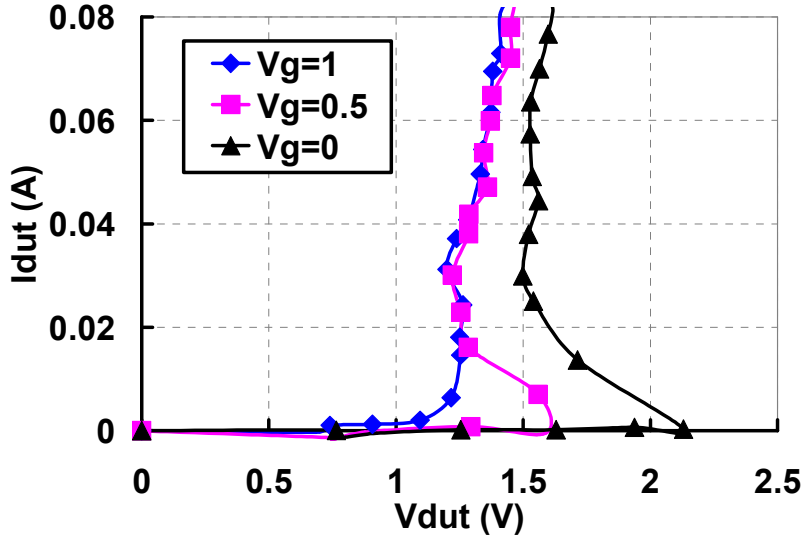



Fig. 4.24: Measured VF-TLP I-V curves of the DWFED under different gate bias, PW = 1ns.

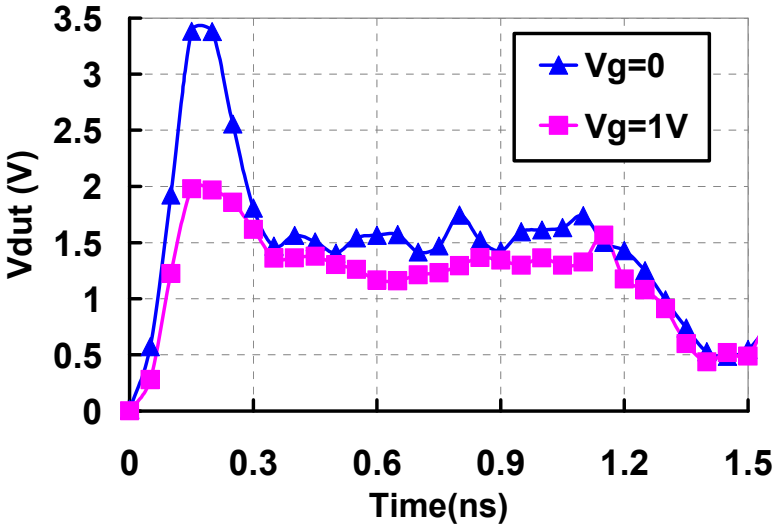



Fig. 4.25: Transient waveforms of the DWFED structure for different gate bias, PW = 1ns.

### 4.2.3 DWFED vs. FED Transient Characteristics

The previous sub-section shows the advantage of the DWFED over the SCR, especially in the transient domain. As illustrated in the previous section, the FED behaves like a diode under ESD conditions and as an SCR during normal operation. While the intrinsic structure in the silicon film underneath the gate is a P-N-P-N in a DWFED, for an FED, what's underneath the gates is essentially a P-I-N diode. In this section, a comparison between these two different devices is established to determine which configuration is the better candidate for I/O ESD protection.

During ESD events, with G1 coupled to a low voltage, the FED relies on the intrinsic P+/P-well/N+ diode under the two gates to shunt a large amount of current. Without a P-N-P-N structure, the trigger voltage $V_{t1}$ of the FED is lower than that of the DWFED, which relies on P-N-P-N turn-on (even with the trigger circuit, $V_{t1}$ is still higher than that of FED). Transient current waveforms are shown in Fig. 4.26 for a higher pulse voltage than used in the previous experiments. The FED turns on

more quickly than the DWFED and drives the injected ESD charges through the device to ground. The much higher current level of the FED prevents charge accumulation, reduces the peak voltage across the I/O devices, and shortens the duration of the high voltage spike. In highly scaled devices with thin gate oxide, the critical voltage above which the oxide is damaged has been steadily decreasing. Moreover, the stringent limitation set by the trigger voltage of the output driver has been identified. For thin gate oxide SOI output drivers, with a trigger voltage ($V_{t1}$) of about 3 V, the MOSFET can only handle an ESD current of 6.9 mA/μm under 1 ns VF-TLP stress. The FED's improved turn-on behavior and its high current carrying capability can potentially protect the I/O devices from being damaged by ESD events.

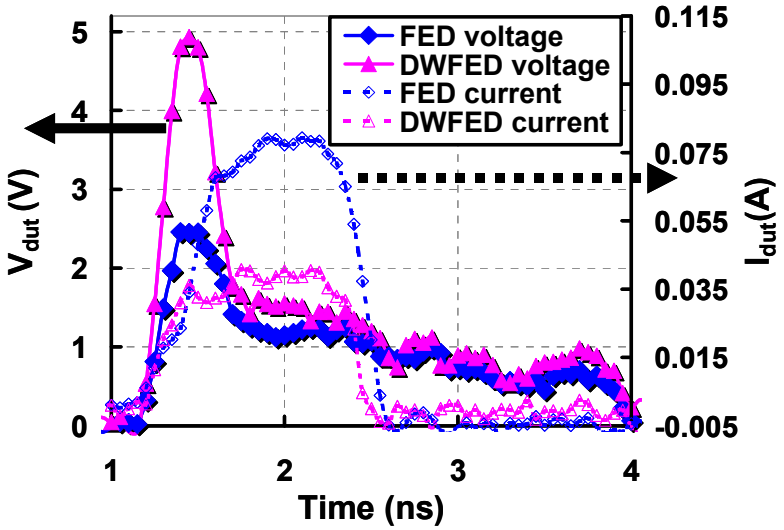



Fig. 4.26: Measured 1 ns VF-TLP transient waveform for P+/P-/$HV_t$/N+ FED and DWFED.

Further measurement results in Fig. 4.27 show that when higher VF-TLP pulse voltages are applied, both FED and DWFED enter the turn-on mode and are able to shunt high currents. This is because both the high voltage level and gate coupling improve the triggering behavior of the DWFED [52,62]. Therefore, the ESD charge can be fully discharged through the protection devices. As shown in Fig. 4.27,

without the charge accumulation problem, the discharge current waveforms for both devices are very similar. However, the FED still has a lower peak voltage, providing an advantage over the DWFED.

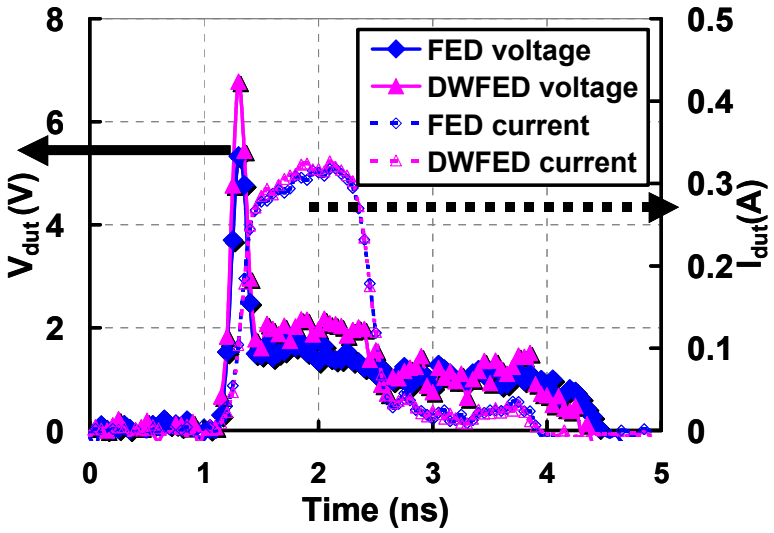



Fig. 4.27: Measured 1 ns VF-TLP transient current for higher current P+/P-/$HV_t$/N+ FED and DWFED.

### 4.2.4 DC I-V and C-V Characteristics

The previous sub-section shows that the FED has faster turn-on than the DWFED. In order to determine if the FED is the best device for pad-based local clamping, further investigation is needed. The DC I-V characteristics of the P+/P-/$HV_t$/N+ FED are shown in Fig. 4.28. As previously mentioned, the original P+/P-well/N+ FED (Fig. 4.18) suffers from high leakage current, which can only be reduced with higher-than-$V_{dd}$ gate voltage. Only with a gate bias above 2 V, can the anode turn-on voltage be increased to about 1 V (so it doesn't turn on during normal operation). The improved P+/P-/$HV_t$/N+ FED keeps the leakage current below 3 pA/μm at an anode voltage of 1 V (close to $V_{dd}$, the maximum level during normal operating conditions) even for a gate bias voltage as low as 0.8 V, which is well

within the voltage range that is readily available on-chip, making this device practical for the aforementioned pad-based local clamping approach (Fig. 4.1). Such a high anode turn-on voltage also provides enough safety margin to prevent accidental triggering of the ESD device. The DC I-V of the DWFED is also plotted in Fig. 4.28 for comparison. It has a lower turn-on voltage and higher leakage at $V_{anode}$ = 1 V. The lower leakage of the FED also reduces the static power consumption.

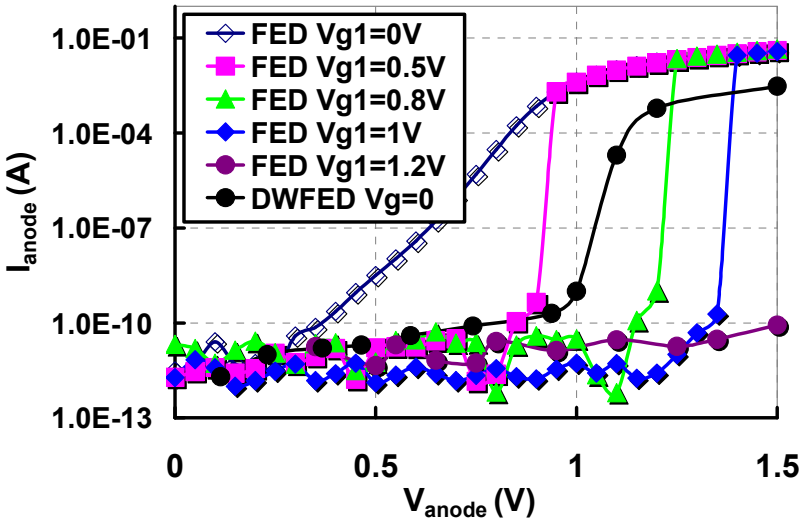



Fig. 4.28: Measured DC I-V of P+/P-/$HV_t$/N+ FED and DWFED structures under different gate biases.

As the ESD device capacitance budget for 20 Gb/sec high-speed I/O reduces to around 100 fF [9], it is important to find ESD device options that minimize the capacitive loading while achieving superior ESD robustness. Fig. 4.29 shows the measured capacitance characteristics of the SCR, FED and DWFED. During normal operating conditions, the FED's gate is connected to $V_{dd}$ to maintain the presence of P-N-P-N in the silicon film and thus reduces the capacitance by taking advantage of the structure of three-junctions-in-series. The FED has higher capacitance compared to the DWFED. Both devices have capacitances lower than 0.35 fF/μm, making them suitable for high-performance applications than the SCR.

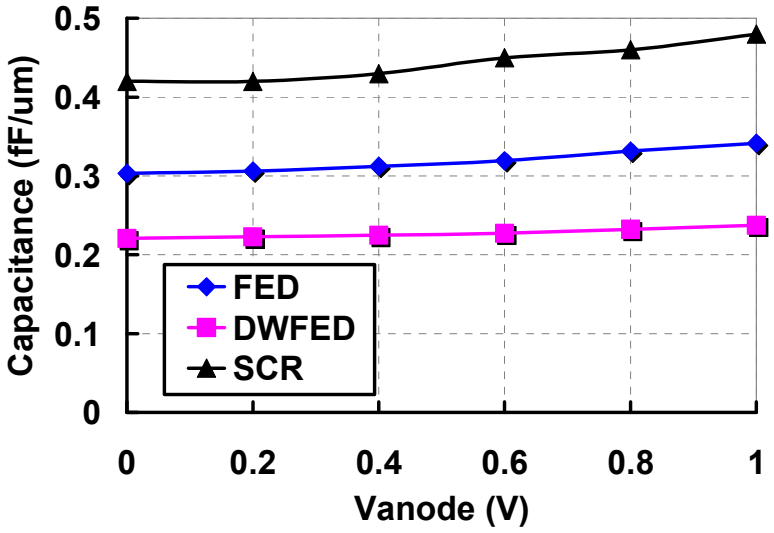



Fig. 4.29: Measured capacitance of SCR, DWFED and P+/P-/$HV_t$/N+ FED.

While the FED shows faster turn-on, its capacitance is about 35% higher than that of the DWFED. This extra capacitance can translate into a lower I/O speed for the same architecture. Therefore, while the FED is still a promising option for the local clamping device, compared to the DWFED, the results suggest that the FED is more suitable in power clamping application, where it provides a high current path between $V_{dd}$ to $V_{ss}$ discharge but the capacitance is not at all a concern. A suggested way to implementation the protection is shown in Fig. 4.30. A conventional way to implement the power clamp is to use a large MOSFET (BigFET) [48], which is sketched in dashed lines in Fig. 4.30. However, the current carrying capability per area of the channel-based BigFET is much smaller than that of the FED. Usually large dimensions above 2000 μm are required for a 10 A CDM protection level. By replacing the BigFET with an FED, only 300 μm device width is required for the same CDM level. Also, the very low leakage level of the FED (Fig. 4.28) translates into much reduced static power consumption. The ESD transient waveforms are qualitatively sketched at the nodes. As the ESD current flows in the power bus, it also shorts the capacitor and initiates a high input for the buffer chain. The chain

matches the delay of the power buses. The end of the buffer chain consists of an inverter, which pulls G1 of the FED down to a lower level, converting the FED back to a diode-like structure, which is capable of shunting high level of current rapidly.

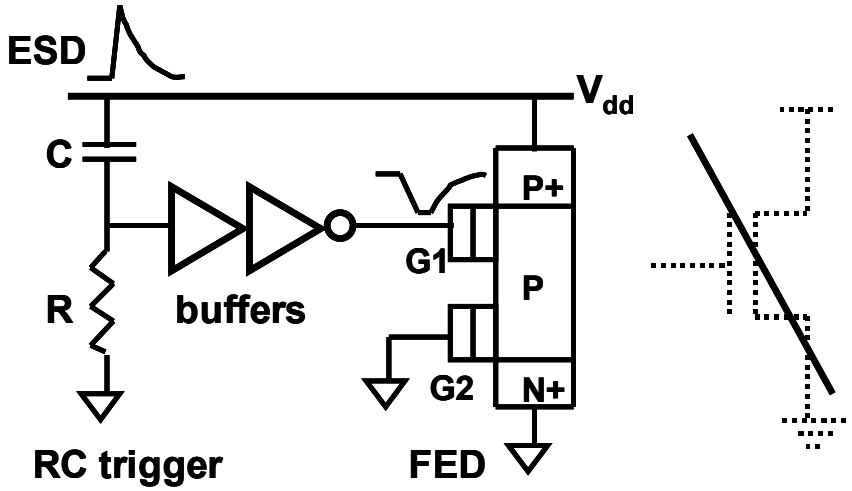



Fig. 4.30: Implementation of FED to replace the BigFET transistor as power clamp.

### 4.2.5 TCAD Simulations for FED

Understanding the physical details of turn-on behavior is key to enhancing the ESD performance of the field-effect-diode-based devices and to prevent unwanted turn-on or high leakage during normal operating conditions. TCAD simulations are illustrated by showing the current density plots in Fig. 4.31 to explain the details of the turn-on mechanism step-by-step.

Under 1 V G1 bias, the P-well region underneath G1 is inverted with the presence of a large amount of inversion electrons. With a P-N-P-N structure formed, the FED behaves like an SCR. When an anode bias of 1 V is applied, because of the formation of the inversion region underneath G1 in the P-well, the device is in the forward-blocking mode. Not enough carriers are injected into the base of the parasitic P-N-P BJT to reach the collector without being recombined. An

insignificant amount of current flows near the surface channel as shown in Fig. 4.31 (a) because the current is mostly due to generation and recombination.

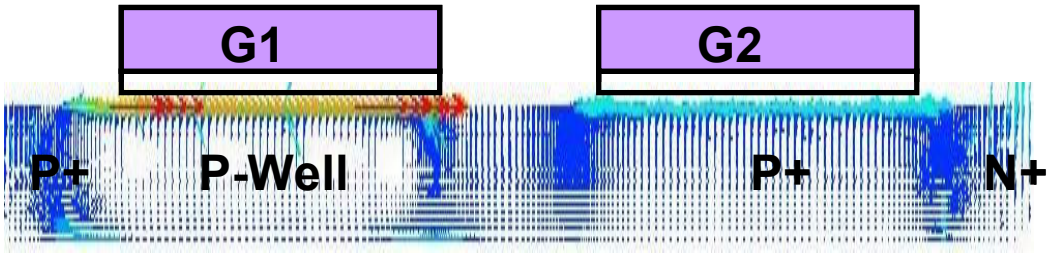



Fig. 4.31 (a): Current density simulation before the turn-on of the P-N-P-N in the Si film of P+/P-/$HV_t$/N+ FED. $V_{g1}$ = 1 V, $V_d$ = 1 V.

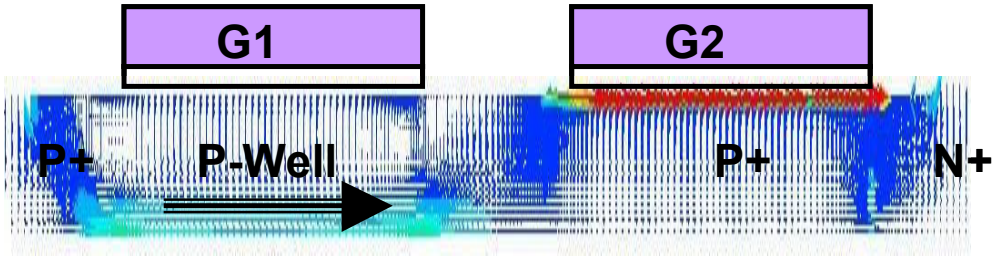



Fig. 4.31 (b): On the verge of the turn-on of the P-N-P-N in the Si film of FED. $V_{g1}$ = 1 V, $V_d$ = 1.3 V.

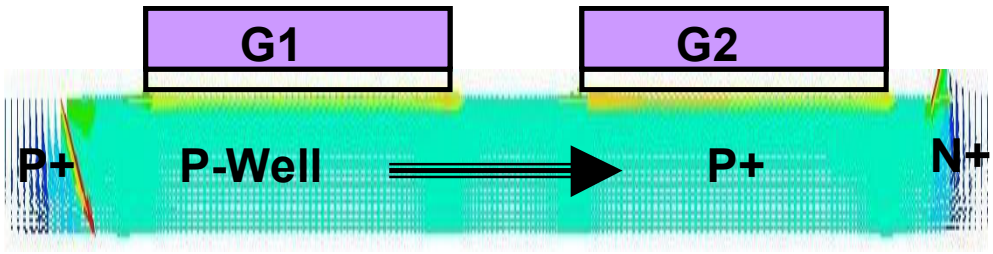



Fig. 4.31 (c): After the turn-on of the P-N-P-N in the Si film of FED. $V_{g1}$ = 1 V, $V_d$ = 1.4 V.

As the anode bias increases to 1.3 V (Fig. 4.31 (b)), progressively more carriers travel through the channel and contribute to the current in the P-well region. In the silicon film depth direction, the upper part of the PW is still strongly controlled by G1. However, the weakly controlled bottom part of the device starts to have an increased contribution of parasitic BJT (LBJT) current.

As the anode bias continues to increase (Fig. 4.31 (c)), the hole injection into the P-well region is significant enough to trigger the LBJT effect in the N-P-N (formed by the N-inversion, P-well, and N+ regions), leading to regenerative feedback and reduced resistance of the device. Similar to SCR device behavior [60], significant current flows across the entire well region. The strong current-carrying capability enables the device to shunt high ESD currents in the event of discharge. However, in normal operating conditions, constant gate bias is applied to help the device remain in the forward-blocking mode and prevent current from flowing. The current distribution is similar to Fig. 4.31 (a). In the FED design and optimization, the goal is to ensure that the current blocking mode is robust enough such that there is little current flowing during normal operation. In ESD, the FED relies on the diode mode to shunt current.

Fig. 4.32 reveals a limitation of the FED device by showing the carrier density under different anode biases on a log plot. Negative values show proliferation of electrons while positive values mean excess of holes. At high enough anode voltages, the inversion region in the P-well underneath G1 gets depleted of carriers, owing to the injection of the inversion electrons into the P+ anode region. When this happens, the holes injected from the P+ region across the inversion region (the base of the P+/N-inversion/P-well BJT) have lower probabilities of being recombined by electrons. Thus it becomes easier to start the regenerative process to turn on the FED. In order to circumvent the early depletion of the inversion region at low anode bias, device designs are tested to adjust the doping of the well segments under each gate.

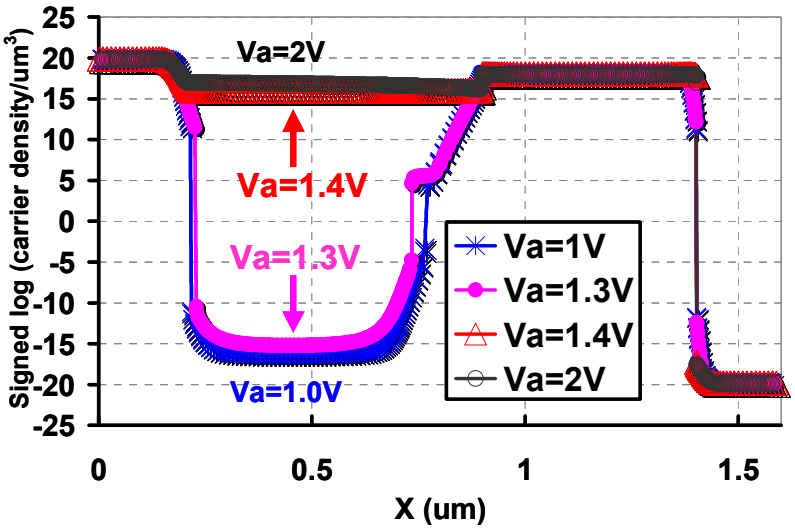



Fig. 4.32: Total carrier density in signed log plot for P+/P-/$HV_t$/N+. Inversion gets depleted for high anode voltage.

To explore the impact of doping profile on the anode turn-on voltage, various doping combinations have been simulated. Figs. 4.33 and 4.34 show the simulated I-V characteristics with different doping under G1 and G2. Lower doping under G1 helps reduce the gate voltage required to initiate the onset of inversion, thus the P-N-P-N structure (forward-blocking mode) in the silicon film is easier to form and sustain. For doping levels lower than $5 \cdot 10^{16}$, under 1 V gate bias, the leakage current is still negligible, even when the anode voltage is increased to above 1 V. Reducing the doping helps improve the anode turn-on voltage until the depletion limit is reached for the region underneath G1. Higher doping under G2 helps decrease the common-base gain of the N-inversion/P-well/N+ BJT, thus increases the anode turn-on voltage of the FED. This effect is shown in Fig. 4.34. For a region doping above $10^{18}$, the anode turn on voltage is higher than 1 V. The doping levels evaluated using these simulations are all within the normal available range for generic SOI technologies. Thus, there is enough design margin such that the device characteristics are not affected by scaling and process variations.

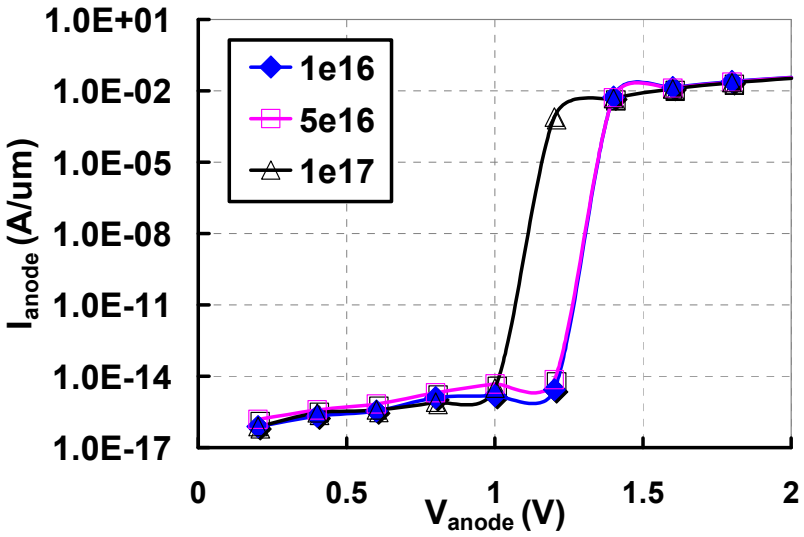



Fig. 4.33: Simulated DC I-V curves for P+/P-/$HV_t$/N+ FED with different P well doping, P-doping under G2 is $10^{18}$.

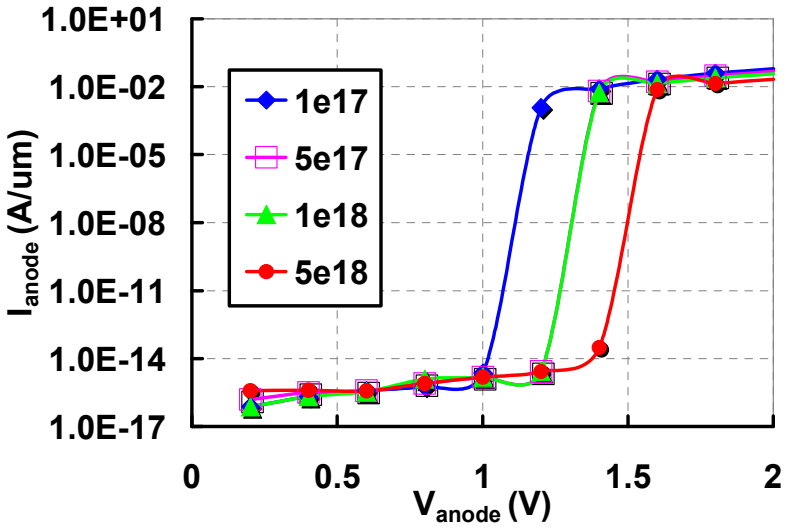



Fig. 4.34: Simulated DC I-V curves for P+/P-/$HV_t$/N+ FED with different P+ doping level under G2, well doping under G1 is $10^{16}$.

## 4.3 Conclusion

In this chapter, both the DWFED and the FED are investigated in great detail. First, the characteristics of the DWFED are compared with the I-V, leakage and C-V of the previously introduced rail-based clamping devices and DWFED is shown to have a higher FOM. The proposed biasing circuit ensures that the DWFED has device level benefits such as very low capacitance and SCR-like current shunting capabilities. Furthermore, DWFED enables local clamping which proves to have architectural benefits by letting the ESD current avoid the long and resistive buses. The robustness in both normal operating conditions and ESD, and high FOM makes DWFED a suitable option for local clamping of high-speed I/O.

Moreover, to address the CDM discharge challenge with SCR devices, the DWFED and the FED are investigated in detail under transient conditions in order to understand in detail the effects of charge storage (and recombination). The improved FED is shown to have faster turn-on behavior than the DWFED. Its trigger voltage is improved to the appropriate range above $V_{dd}$ to minimize leakage current. Because of its superior turn-on and low leakage performance, it is recommended to be applied for power clamp applications where capacitance is not a concern. DWFED has the lowest capacitance and turns on faster than the SCR, making it suitable for pad-based local clamping.

Both devices are modeled in TCAD and the turn-on physics are explained. Design tradeoffs are evaluated with different well doping levels. It is shown that the biasing circuit ensures the functionality and robustness of the DWFED. For FED, a wide range of doping is permitted to still guarantee adequate turn-on voltage. Therefore, both devices allow enough margin for technology scaling in future nodes. Furthermore, the structures are constructed with long gates and wells, making them less constrained by scaling effects. An important point is that in addition to fact that the DWFED and FED have major ESD protection benefits, their process similarities

to the conventional SCR makes implementation in generic SOI technologies feasible and no special (added) process steps are required.

# Chapter 5

# ESD Protection Design Methodology

The previous chapters have provided a detailed investigation into the essential building blocks for the I/O ESD protection schemes. Methods for improving I/O breakdown levels have been developed. The gated diode has been identified as the most suitable rail-based clamping device and the DWFED as a good choice for pad-based local clamping. In this chapter, all the building blocks become indispensable elements for the design methodology, which is presented with both the gated diode and the DWFED as the ESD devices. The workflow of the methodology starts from defining a CDM target and obtaining peak current levels, based on the correlation results. Both the rail-based and local clamping analyses are performed and results are incorporated. The devices are designed and optimized, based on the path voltage and current requirements. Tradeoffs are evaluated and parasitics are minimized in both schemes. The achievable high-speed I/O data rates are estimated. This methodology is more suitable for designing deeply scaled I/O compared to the low-C or plug-and-play methods. An abstraction of the methodology is presented in the format of pseudo-code, which can be translated into suitable programming hierarchy.

## 5.1 Choosing Between Rail Clamping and Local Clamping Schemes

Choosing between the rail-based clamping (Fig. 5.1) and pad-based local clamping approaches (Fig. 5.2) for protection takes us to the crux of the ESD design challenge. The choice determines the type of ESD devices to be used.

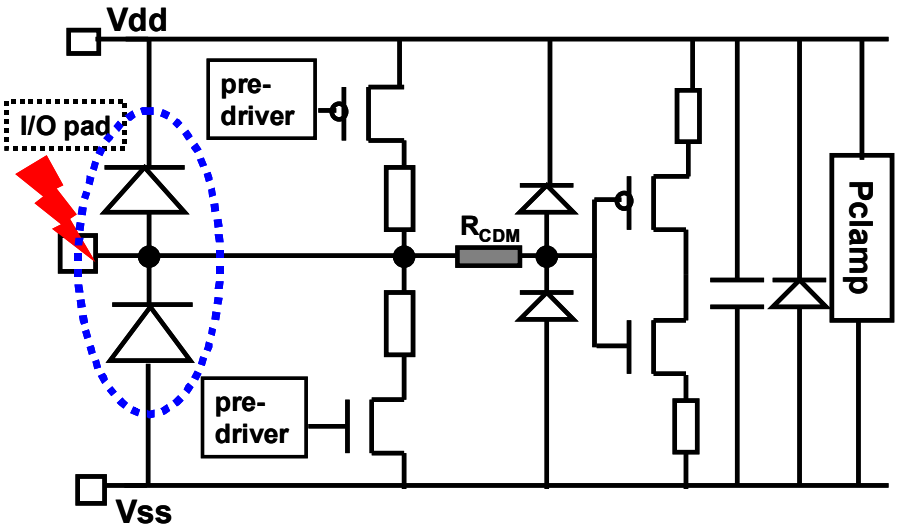



Fig. 5.1: Rail-based ESD scheme. Dashed circle marks the ESD diodes.

The P/N junction diode boasts high current shunting capability, low resistance and low structural complexity. Due to its low turn-on voltage (below 1 V), it is usually connected in reverse-bias and is used in the rail-based schemes (Fig. 5.1) to protect both the input and output drivers [66-68]. Under ESD conditions, one of the diodes is forward-biased to shunt the large transient currents between two adjacent pads or along the $V_{dd}$ or $V_{ss}$ power buses and power clamp.

However, this scheme becomes insufficient in the high-current CDM domain, owing to the excess voltage build-up along the long and resistive current paths [69,70], causing input driver oxide damage and the output driver's lateral bipolar junction (LBJT) effect. The dominance of CDM failures demands the exploration of other strategies and devices to circumvent the increasing voltage build-up. A pad-based local clamping protection scheme [10] is shown in Fig. 5.2. This protection circuit allows the ESD current to flow directly from the pad to ground, avoiding the power buses. The discharge path resistance is considerably reduced and the pad voltage build-up is minimized. However, the protection device's turn-on voltage must be controlled above the $V_{ss}$ to $V_{dd}$ range, to avoid turn-on during normal operating conditions and to reduce leakage currents.

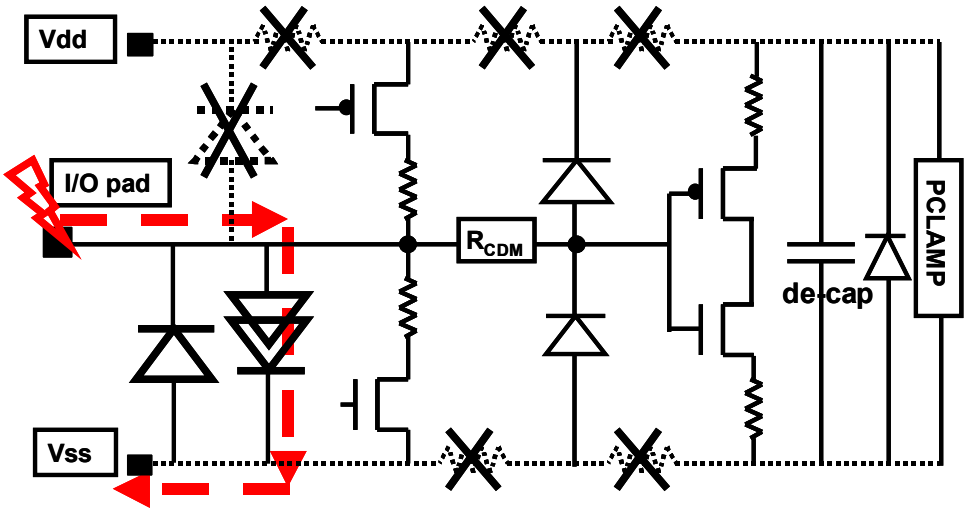



Fig. 5.2: Pad-based local clamping scheme. Need devices with high turn-on voltage. Dashed arrows represent the ESD current path.

The differences and similarities of the two schemes are summarized in Table 5.1. In addition to the device level differences, these two schemes also differ in focus of the design. The rail-based scheme uses diodes and their physics-based models are easier to establish. Hence, most of the design effort is on the biasing circuits and path-based optimization in order to minimize the voltage build-up along the paths. For the pad-based scheme, the discharge path is significantly shortened. However, the device needs to be optimized to achieve the best characteristics, for instance, fast turn-on, appropriate turn-on voltage, and low capacitance.

Table 5.1: Comparison between rail-based and local clamping strategies.

| | **Advantages** | **Disadvantages** |
|---|---|---|
| **Rail-based (dual diode)** | **Easy to design and model devices** | **IR drop due to power buses and ESD device (worse in more advanced nodes)** |
| **Local Clamping (SCR-based)** | **Much less IR drop by avoiding power buses, smaller devices needed, less parasitics** | **Need to design and optimize special SCR-based devices** |

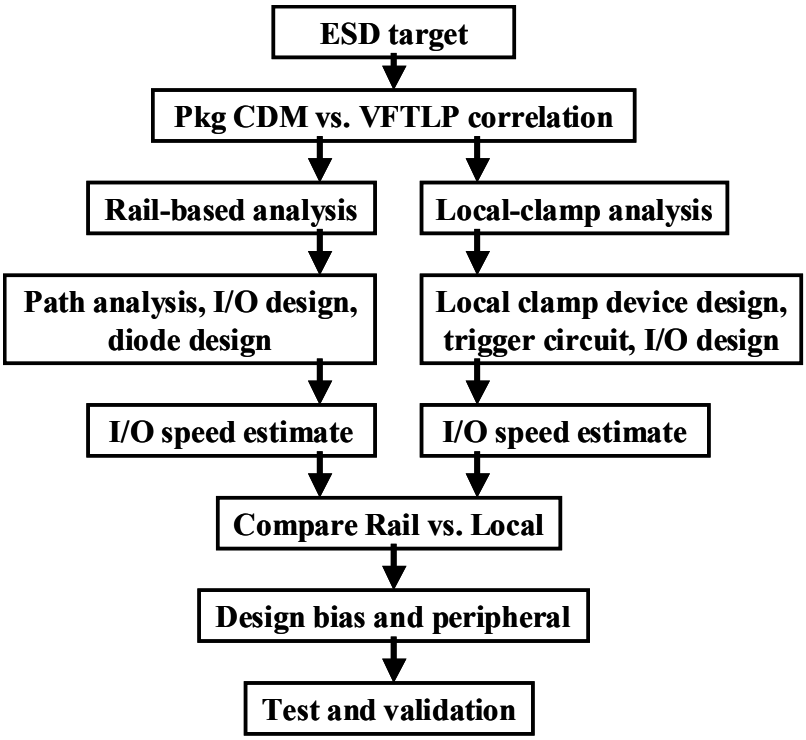



Fig. 5.3: Flowchart for the ESD-I/O design methodology.

To take all the foregoing analysis into consideration during the design process, a well-defined workflow needs to be followed. A methodology is developed to guide the design for different applications and reduce the turn-around time. The flowchart is shown in Fig. 5.3. The widely adopted low-C and plug-and-play approaches are becoming insufficient [71] in deeply scaled technologies where the design window is very small. The proposed methodology differs from those approaches in mainly two aspects. First, the methodology relies on a product level CDM voltage and VF-TLP failure current correlation as a starting point. The details of this part will be provided later in this chapter. Second, both rail-based and local clamping analyses are carried out simultaneously, and results are compared to identify the design with the optimal figure-of-merit and the lowest parasitic loading. With the extracted parasitic values, each design is estimated for its respective I/O data rate, given an I/O architecture [10]. As presented in previous chapters, some devices require associated biasing or

trigger circuits. Hence, these circuits are designed in the next step to achieve the best FOM. Finally, the design is translated into schematics, layout, and then fabricated. The chips are characterized.

## 5.2 Product Level CDM and Wafer Level VF-TLP Correlation

In SOI technology, experiments on 90 nm and 65 nm flip-chip packaged and unpackaged wafers establish correlation between the CDM failure voltage levels and maximum failure VF-TLP current. In Figure 5.4, each data point corresponds to a voltage value on the X-axis. The value is the CDM failure voltage level obtained from the CDM tester for a certain I/O, on a packaged wafer product. Equivalently, this level also represents the maximum CDM passing level. Usually, customers request a specific CDM passing level to ensure the product's ESD-robustness. On the y-axis, the same data point corresponds to a failure current level (normalized by package area). This current level is obtained from well-calibrated in-lab VF-TLP test on an unpackaged wafer. The VF-TLP test closely emulates the CDM discharge behavior, however, it is much easier to carry out and costs much less than the field CDM tests. These two levels together define a data point on the figure. For instance, one of the test chips in Package 8 fails at 250 V under the CDM test; in VF-TLP tests, the area-normalized failure current turns out to be 0.06 A/mm$^2$; the corresponding point is then plotted in the figure. All other data points are plotted similarly.

The plot shows that the data points fall on trendlines with similar slopes, establishing a correlation between the CDM voltage levels and the VF-TLP current levels. A possible explanation is shown in Figs. 5.5 and 5.6, derived from the analysis of the substrate structure of both bulk and SOI wafers. For a given CDM event, the ESD charge residing in the substrate is discharged when one of the I/O pins touches the ground. In bulk devices, because the substrate and the diffusion regions are adjacent (Fig. 5.5 (a) and 5.6 (a)), discharge can happen directly across

the substrate (P)-to-N+ junction or the P+-to-substrate junction. However, the 2-pin-based VF-TLP test forces the current to go through the ESD device in the lateral direction from P+ to body to N+, bypassing the substrate. For this reason, the resulting discharge current paths are very different. The difference in current paths makes the 1-pin discharge CDM failure level very different from the 2-pin VF-TLP levels in bulk technology wafers, especially in the case shown in Fig. 5.6 (a). The difference in path voltage buildup is especially evident when the supply buses are resistive. However, in SOI technology, the buried oxide (BOX) serves as an insulating layer to separate the active diffusion region and the substrate of the wafer (as shown in Figs. 5.5 (b) and 5.6 (b)). The ESD discharge has to rely on the substrate contacts and the die seal (Fig. 5.5 (b) and Fig. 5.6 (b)), which are connected to the $V_{ss}$ buses and ground plane. Thus, the CDM and VF-TLP discharge paths are very similar in SOI wafers; both currents have to go through the ESD device and the interconnects. Therefore, the correlation is established as shown in Fig. 5.4.

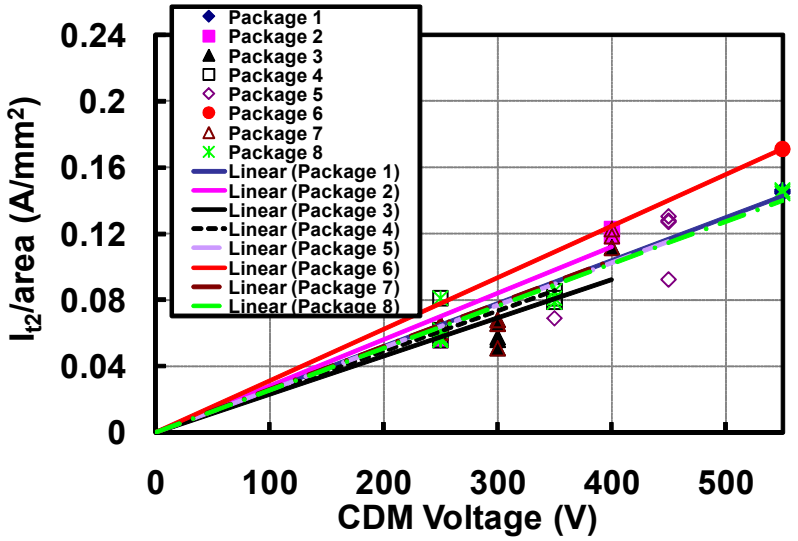
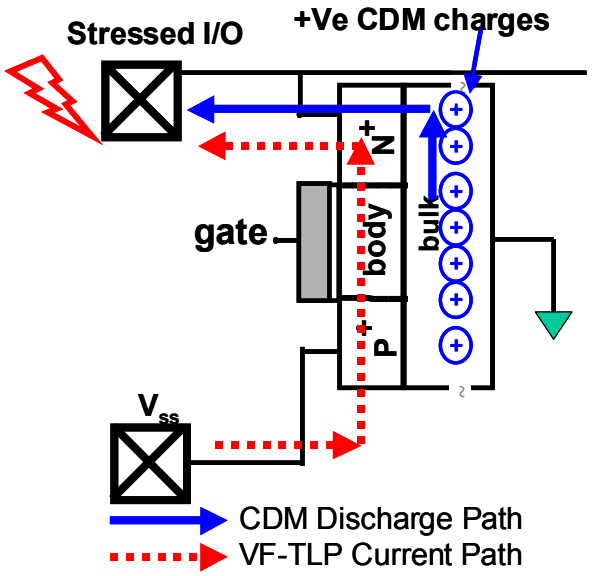
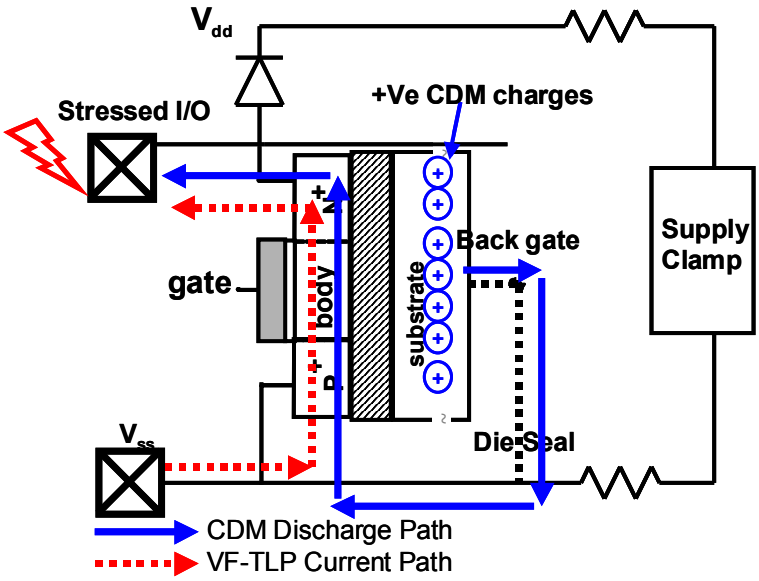



Fig. 5.4: Package CDM failure voltage vs. wafer level I/O failure-current-per-package-area correlation. The lines are linear trendlines. 8 types of test package are measured.

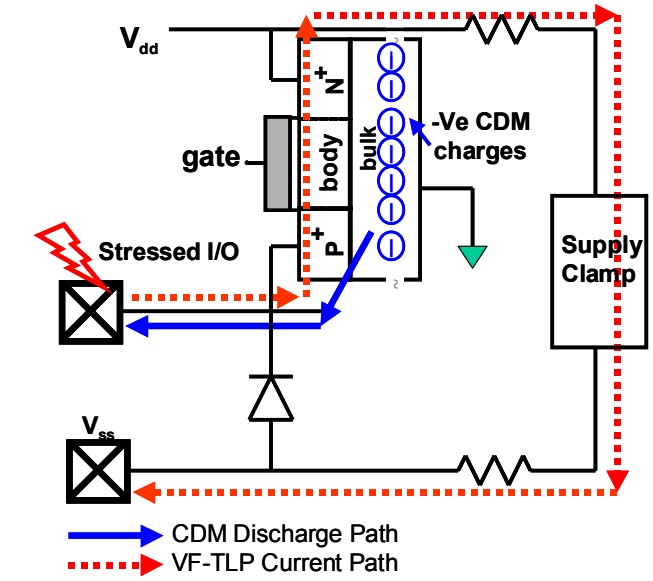



(a)

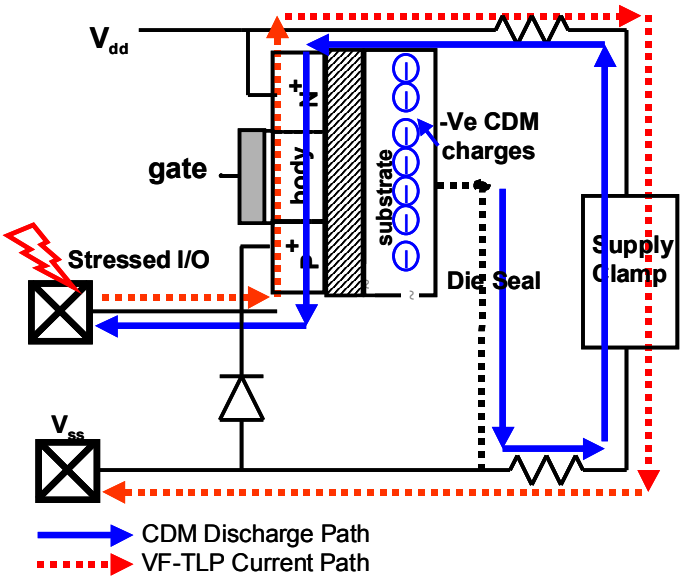



(b)

Fig. 5.5: Positive CDM and negative VF-TLP ESD discharge current paths. (a): discharge in bulk technology wafer. (b): in SOI wafer.




(a)




(b)

Fig. 5.6: Negative CDM/positive VF-TLP ESD discharge current paths. (a): discharge in bulk technology wafer. (b): in SOI wafer.

## 5.3 Path Analysis and Device Sizing

The CDM and VF-TLP correlation in the previous section prepares the first step in the ESD design methodology. Given a CDM protection target, the CDM—VF-TLP correlation figure serves as a database. It is examined to identify the failure current requirement—the minimum allowable current handling level $I_{min}$ (e.g. 5 A) for a particular CDM voltage level (e.g. 250 V). With this key parameter obtained, a careful path analysis takes the design to the next step.

The oxide breakdown and LBJT trigger voltage levels are determined, along with $V_{crit}$, of the current technology based on test structure characterizations. For instance, in the 32 nm silicon-on-insulator (SOI) technology node, the LBJT trigger voltage of an output MOSFET driver is generally lower than the oxide breakdown, (e.g. around 3 V [5]), hence the limiting constraint is the LBJT. These parameter values are stored in the database for the designers to check. Next in the methodology, both the rail-based and local clamping devices and paths are analyzed and evaluated.

If the dual-diode, rail-based ESD protection scheme is adopted, then the following condition should be met [6]:

$$I_{min} \cdot (R_{wire} + R_{clamp} + R_{ESD}) + V_{on\_ESD} + V_{on\_Clamp} \leq V_{crit} \quad (1)$$

Here, $R_{wire}$ and $R_{clamp}$ are wire and power clamp resistance, respectively. $V_{on\_ESD}$ and $V_{on\_Clamp}$ are the turn-on voltages of the ESD device and the power clamp. The distributed nature of the power clamp also needs to be taken into account [7,21]. The $I_{min} \cdot R_{ESD}$ term can equivalently be written as:

$$(I_{min}/W) \cdot [\Delta V/\Delta(I/W)]$$

where $I_{min}/W$ is the current density, and $\Delta V/\Delta(I/W)$ is the effective resistivity extracted from the derivative of the I-V characteristics, determined from the I-V curve of the diode.

The boundary condition is the equality to $V_{crit}$. In this equation, since $I_{min}$ is known, the optimal width of the gated diode W is the only unknown and can be obtained; the width of the substrate diode can be determined similarly. For the high

$V_{on}$ silicon-controlled rectifier (SCR)-based protection, however, the local clamping method shows a major advantage, manifested in the expression of its pad voltage:

$$V_{crit} = V_{pad} = V_{on\_ESD} + I_{min} \cdot (R_{ESD} + R_{wire}) \quad (2)$$

Compared to the rail-based derivation, a larger $I_{min} \cdot R_{ESD}$ value or higher $V_{on\_ESD}$ can be tolerated, because of the absence of power clamp resistance and reduction in wire resistance. Subsequently, the optimal width can be calculated for each device (e.g., 600 μm for 45 nm SOI gated diode, and 267 μm for double-well field effect diode (DWFED)).

For these devices, sufficient current can be shunted while no extra capacitance is added. Despite its comparable VF-TLP characteristics with the gated diode, the SCR-based DWFED requires a smaller device width.

Multiplying the optimal widths by the normalized capacitance per area values on the capacitance vs. voltage bias results, a fair comparison of the capacitance among all of the potential ESD devices can be obtained. The gated diode adds a capacitance of 360 fF (for 250V CDM protection level) to the I/O. DWFED, utilizing the local clamping scheme, only contributes 118 fF parasitic capacitance.

The DWFED is identified as a device with the lowest zero bias capacitance. However, as shown previously [20], the gated devices may achieve still lower capacitance with certain applied gate biases. Therefore, the next step in this design flow is to design biasing circuitry [20] for the DWFED to ensure that the gate is connected to ground during ESD. Following this method, an adequate current shunting capability is guaranteed and no extra area is added, thus the capacitance is minimized within the allowable current budget.

Fig. 5.7 shows the relationship between high-speed I/O data rates and capacitance budget [9]. As the demand on the data rates increase to above 10 Gb/sec, a capacitive loading of less than 200 fF is required. The ESD design window continues to shrink. The breakdown current density, capacitance and resistance are the key design parameters to be considered in the design methodology. From the

total parasitics calculation given in previous paragraphs, the DWFED can meet the capacitance budget while the gated diode cannot.

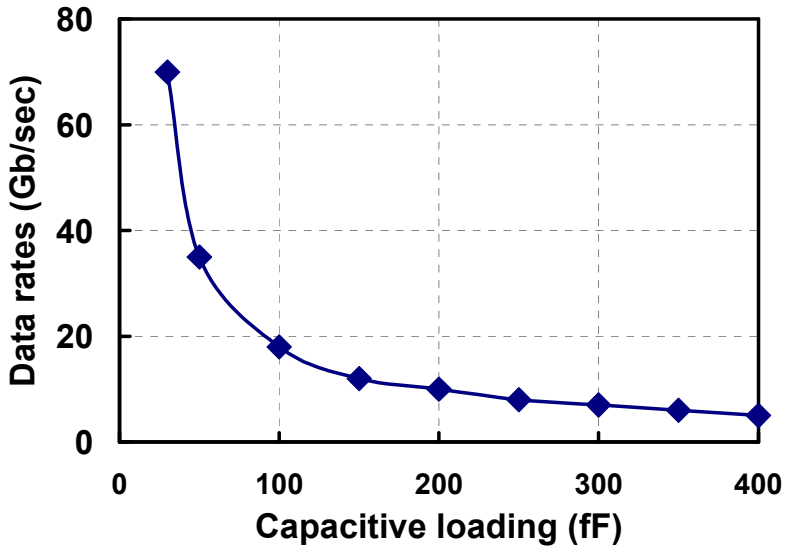



Fig. 5.7: Impact of capacitance loading [adopted from Industry Council on ESD Target Levels white paper, 9, Fig. 25].

## 5.4 A Codified Abstraction of Methodology

To put the design methodology into useful format for CAD designers' reference, a set of pseudo-codes are presented in this section to describe the design flow.

ESD-I/O Co-design Methodology in pseudo-code Format:

```
#include <libraries.h>
// Constants but defined as a var: negotiation with customer may be needed later
double V_CDM_target=250; % Customer request target level

// Variable definitions
double V_CDM_present, I_peak;
double* CDM_vs_VFTLP_correlation; // A pointer to correlation database
double V_ESD_rail_clamp, R_on_rail_clamp, C_total_rail_clamp,
Datarate_rail_clamp;
```

```
double V_ESD_local_clamp, R_on_local_clamp, C_total_local_clamp,
        Datarate_local_clamp;
int clamping_option;

// Structure (database) definitions
typedef struct {… abbreviated
} device_rail_clampT
deviceRailClampT device_rail_clamp;

typedef struct {… abbreviated
} I_O_architectureT
I_O_architectureT I_O_architecture;

typedef struct {… abbreviated
} device_local_clampT
device_local_clampT device_local_clamp;

typedef struct {… abbreviated
} parametersT
parametersT parameters;

typedef struct {… abbreviated
} IO_designT
IO_designT IO_design;


// Main function
main()
{
while(V_CDM_present < V_CDM_target)
{
        I_peak = obtain_I_peak(CDM_vs_VFTLP_correlation); //Look up
correlation

        // For rail-based, focus on path-based optimization;
        V_ESD_rail_clamp = calculate_V_ESD(I_peak, device_rail_clamp);
        R_on_rail_clamp = obtain_R_on(V_ESD_rail_clamp, device_rail_clamp);
        C_total_rail_clamp = obtain_C_total(R_on_rail_clamp, device_rail_clamp);
        Datarate_rail_clamp = estimate_datarate(C_total_rail_clamp,
I_O_architecture);

        // For local clamping, focus on SCR-based device level.
```

```
        V_ESD_local_clamp = obtain_V_ESD (I_peak, device_local_clamp);
        R_on_local_clamp = obtain_R_on(V_ESD_local_clamp,
device_local_clamp);
        C_total_local_clamp = obtain_C_total(R_on_local_clamp,
device_local_clamp);
        Datarate_local_clamp = estimate_datarate(C_total_local_clamp,
                                    I_O_architecture);

        if(Datarate_local_clamp > Datarate_rail_clamp) {
                Use_Local_Clamp(device_local_clamp);
                clamping_option = 1;
        } else {
                Use_Rail_Clamp(device_rail_clamp);
                clamping_option = 0;
        }

        //Spice and TCAD simulations. Note, "parameters" is a structure.
        parameters = IR_Simulation(clamping_option, I_O_architecture);

        // Use the parameters to create an IO_design database, which is also a
        structure.
        IO_design = Codesign(clamping_option, I_O_architecture, parameters);

        // Simulate with the co-designed I/O, a virtual ESD test
        I_peak_present = ESD_Simulation(I_O_design);

        // Virtual CDM test
        V_CDM_present = CDM_Simulation(I_peak_present);
}
EncodeSchematic();   //Translate the design into Schematic in Cadence
IncorporateLayoutLVS();       //Translate into layout or incorporate layout and LVS
check
FinalizeDesign();
}
```

## 5.5 Summary

This chapter presents an ESD design methodology in detail, taking into account design window parameters and details of the device options available. A CDM—VF-TLP correlation is established such that product level reliability figures can be

translated into circuit level numbers. The methodology analyzes both the rail-based and local clamping schemes and evaluates the tradeoffs. An example with 250 V CDM protection target shows that the DWFED achieves lower parasitic loading, meeting the 200 fF capacitance budget for high-speed I/O. An example of the design flow of the methodology is shown in a pseudo-code format, thereby allowing EDA/TCAD experts to consider options for future implementation in industrial tools. With this workflow, all the important results from this work, including the CDM-VF-TLP correlation, I-V, C-V, leakage, transient characterization, optimization, device design and improvements, TCAD modeling, biasing circuit design and I/O device improvements, are put into a useful format and may directly aid in future ESD-I/O design strategies.

# Chapter 6

# Conclusion

In this thesis, it has been shown that with the scaling of device technologies, package technologies and circuit performance, the ESD design window is diminishing. Therefore, the low-C and plug-and-play methods are no longer sufficient in deeply scaled technologies. Full understanding of every element in the I/O and ESD becomes more critical. Moreover, topological change in the I/O-ESD architecture is required. This work presents improvements of the I/O robustness and a methodology to consider design trade-offs. Local clamping devices are shown to be advantageous.

## 1.1 Summary of the Thesis

This thesis starts with a thorough introduction to the current ESD protection design challenges and design window shrinkage with technology scaling. It is identified that the local clamping scheme can potentially be very advantageous because it has architectural benefits on the global level. However, more sophisticated device designs are required.

The breakdown levels of the single MOSFET input and output drivers are examined in detail, showing a diminished design space for ESD protection with breakdown voltages below 4 V. To address this challenge, cascode or stacked drivers are designed to gain improvements. Circuit implementation issues for the stacked drivers are investigated with realistic design of pre-drivers and associated ESD diodes to imitate the rail-based ESD architecture. Also, pre-drivers and drivers in

advanced SOI technologies are investigated to predict their robustness in the local clamping ESD architecture. Experimental results show that the pre-driver connection and the top-to-bottom device ratio have a large impact on ESD robustness. It is discovered that by grounding the pre-driver's inputs, the stacked driver's $V_{t2}$ is increased by twice, hence most of the ESD current flows into the power-rail, increasing the overall I/O failure current ($I_{t2}$) by 8 times compared to other input connections. The proposed trigger circuit couples the pre-driver inputs close to the ground level to improve both $V_{t2}$ and $I_{t2}$. This work also demonstrates that in order to expand the ESD design window, separated diffusion regions are preferred in order to improve $V_{t1}$ by more than 1 V. The improvements achieved based on the careful investigation in this section can help alleviate the design window shrinkage. These solutions provide robust building blocks for the design methodology. The evaluation of I/O drivers defines clear protection targets for the subsequent sections on ESD device and methodology.

Then, the commonly used rail-based clamping scheme is investigated in detail. The electrical and ESD characterization of the gated diode and substrate diode are evaluated, both of which can be implemented as the core building blocks for the rail-based clamping in SOI. It is shown that the overall capacitance of the gated diode is reduced by half with the proper implementation of biasing. Both types of diodes are robust under forward and reverse bias ESD pulses. While the SUBDIO is less thermally constrained and has much higher current shunting capability under both CDM and HBM ESD, its excessive capacitance makes it less applicable in high-speed I/O applications. The gated diode shows a much better FOM with a 50 fF/μm $I_{t2}$, and can be constructed with very small feature size by using the poly gate mask in advanced technologies. Furthermore, the gated diode shows reduced on-resistance with shorter gate lengths, so it can directly benefit from technology scaling. The proposed gate biasing circuit minimizes the parasitic capacitance of the gated diodes to about 0.3 fF/μm and reduces the sensitivity of process parameters on performance,

making it applicable and dependable in generic SOI process technologies. The SUBDIO requires special process and has limited room for improvement with scaling. Therefore, it is not preferred unless used in applications where heating in the silicon film causes serious problems.

The local clamping scheme is fully examined in this thesis. Both the DWFED and the FED are investigated in great detail. First, the characteristics of the DWFED are compared with the I-V, leakage and C-V of the previously introduced rail-based clamping devices, and the DWFED is shown to have higher FOM. The proposed biasing circuit ensures that the improved DWFED has device level benefits such as very low capacitance of 0.22 fF/μm and SCR-like current shunting capability. Furthermore, the DWFED enables local clamping which proves to have architectural benefits by letting the ESD current avoid the long and resistive buses. The robustness in both normal operating conditions and ESD, and the high FOM make DWFED a suitable option for being applied in the local clamping of high-speed I/O. Moreover, to address the CDM discharge challenge of the SCR, the DWFED and the FED are investigated in detail in the transient-time domain. The improved FED is shown to have faster turn-on behavior than the DWFED. Its trigger voltage is improved to the appropriate range above $V_{dd}$ to minimize leakage current in normal operating conditions. Because of its superior turn-on and low leakage performance, the FED is recommended to be applied in power clamping applications where capacitance is not a concern. The DWFED has the lowest capacitance of 0.22 fF/μm and turns on faster than the SCR, making it suitable for the pad-based local clamping. Both devices are modeled using TCAD and the turn-on physics are explained. Design tradeoffs are evaluated with different well doping levels. It is shown that the biasing circuit ensures the functionality and robustness of the DWFED. For the FED, a wide range of doping is permitted while still ensuring adequate turn-on voltages. Therefore, both devices allow enough margin for technology scaling in future nodes. Furthermore, the structures are constructed with long gates and wells, making them less

constrained by scaling effects. An important point is that while the DWFED and FED have more benefits, their processes are similar to the conventional SCR, making them implementable in generic SOI technologies without special process requirements.

Finally, an ESD design methodology is developed and presented in detail. A CDM—VF-TLP correlation is established such that the product level reliability figures can be translated into circuit level numbers. The methodology analyzes both the rail-based and local clamping schemes and evaluates the tradeoffs. An example with 250 V CDM target shows that the DWFED achieves lower parasitic loading, meeting the 200 fF capacitance budget for high-speed I/O. A schematic implementation of the methodology is shown in a pseudo-code format. With this workflow, all the important results from this work, including the CDM-VF-TLP correlation, I-V, C-V, leakage, transient characterization, optimization, device design and improvements, TCAD modeling, biasing circuit design and I/O device improvements, are put into a useful format which can directly aid the ESD-I/O design implementation in more robust, industrial frameworks.

## 1.2 Recommendations for future directions

The continued scaling trend further reduces the ESD design window. For technologies beyond 32 nm, a very high speed I/O above 20 Gb/s may not offer a design window opening in the rail-based scheme. Thus, local clamping may become the only viable option. Scaling also has important implications on the gate stack and drain/source contacts. The ESD impact on advanced high-K metal gate, metal source/drain materials merits careful investigation to determine the breakdown levels [68]. Other device technologies such as the FinFET, nano-devices, and advanced fully-depleted SOI [72-78] need to be further explored for the breakdown voltage and current levels. Some technologies have already been identified to have unique breakdown states [77]. The ESD protection devices need to be modified to

accommodate the new technologies. The proposed local clamping takes time for industry wide acceptance. Validation needs to be carried out across a variety of technologies and applications. It has been discovered that as the systems become more complicated, CDM ESD can cause previously undiscovered damage [46]. This issue worsens as both front-end and back-end complexity increases. Inductive coupling can cause sub 1 ns discharge into the core devices [52]. Therefore, such events need to be addressed. So far, at least two ESD devices are required for the most efficient protection. Future technologies may offer opportunities to develop one-device-for-all protection to further reduce the capacitive loading and area penalty. Furthermore, architectural and topological options need to be further explored. For instance, the T-coil based clamping techniques, suitable for high speed I/O implementation, is beneficial in both digital I/O [79-81] and RF [82] domains. Testing techniques [83,84] more accurately emulating real HBM, CDM and CDM-induced coupling events are needed for future characterization, especially on the system level.

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