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Hierarchical Process Simulation for Nano-Electronics

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ABSTRACT

The challenges of computational electronics are considered from the perspective of process simulation. Essential limitations for device scaling posed from a technology point of view are discussed along with many new research opportunities. The key areas considered include: bulk processing, interconnect technology and software engineering for computational electronics.
Key Words: hierarchy, technology CAD, interconnects, parallel computing

INTRODUCTION

Over the period of more than two decades the field of process simulation for integrated circuits has become established as an essential enabling technology. Over this same period the critical dimensions for devices have steadily moved from the regime of 10 μm to well below 1.0 μm and the most recent device research is pushing the limits of 0.1 μm. With dielectric layers below 10 nm and junction depths below 100 nm, it is safe to say that we have entered the era of nano-electronics. Yet in spite of the very impressive progress in technology development and the use of process simulation as an integral part of the design process, there are major limitations in the physical models that are currently used in design---there are still abundant opportunities to push the "technology envelop." At the same time, the economics of IC technology development mandate cost-effective utilization of facilities.

The challenges in microelectronic innovation have shifted over the last decade from that of defining new intrinsic device structures towards achieving integration of heterogeneous technologies that are compatible with core silicon submicron technology. The silicon technology base provides not only abundant digital processing but also substrate versatility through equipment infrastructure and the growing use of micro-machining as a key enabling technology. In some cases there are attempts to tightly integrate advanced heterojunction devices (i.e. SiGe HBTs) using mainstream CMOS technology [1]. Alternatives that use silicon substrates as "glue" technology represent ongoing experimentation moving towards the regime of truly heterogeneous technology. In the broader domain of interconnect technologies--which has come to be the pacing factor in VLSI design and manufacturing--there are new levels of material complexity being used to advance the state-of-the-art. The distinctions between active device design and passive interconnections have become blurred as the equipment used for back-end silicon processing has more and more in common with that of the compound materials community.

To illustrate the range of issues facing VLSI technologists, Figure 1 shows a hierarchical taxonomy of design issues. At the highest level the circuit design issues begin with use of extracted (or simulated) models for devices and interconnects, leading to actual layout and then

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verification of the resulting structures. At the next lower levels of device and process design, there is a well-established hierarchy of CAD tools and methodology for creating virtual wafers, virtual equipment for process simulation, and virtual instruments for characterization. In fact, such a methodology for both digital and analog characterization of technology based on IC layout is becoming increasingly powerful at the cell levels of design [2][3]. In the bottom level of the hierarchy shown in Figure 1, the atomic-scale considerations are indicated including both device transport and process physics. In contrast to the higher level electronic (ECAD) and technology (TCAD) areas of design aids, the atomic level is still immature and the means to interface such data with the higher level tools is a topic central to the discussion presented here.

Figure 2 shows in more detail some of the CAD tools that are typical across this hierarchy as well as issues that reflect on information content and physical scale. As one moves deeper in the knowledge hierarchy, the scale of the respective models move from that of a continuum representation with scales of mm and μm to the atomic-scale nm domain. Having defined this very broad perspective of computational and physical modeling, we now turn specifically to the process modeling issues at the macro-, mesoscopic and atomic levels. By means of specific examples, the requirements for tools at these levels in the coming era of nano-electronics are presented. The next two sections consider first intrinsic devices and then interconnect structures. In the final section, many of the software issues are presented, including the needs to support technology versatility and code reusability.

INTRINSIC DEVICES

The scaling of silicon devices and especially MOS technology is fundamental to the ongoing growth of integrated systems. Memory density and speed are now key pacing factors in overall system performance. Dynamic, static and programmable memory each provide key system leverage and have quite different technology scaling parameters that affect their development. For example, dynamic memory is the most demanding in terms of technology---deep trenched devices are one example that clearly illustrates this trend. Static memory is much closer to the mainstream of technology for logic with the exception of load and sensing devices which often exploit devices other than bulk MOS. In the arena of programmable devices there is still many alternatives ranging from ferroelectric (FE) structures at one extreme to the well-established double-poly flash memory technology at the other.

For all the device structures mentioned above, there is an abundance of technology scaling issues that involve etching, deposition, oxidation and diffusion for silicon and polysilicon materials; these are also the areas where process simulator developments have been most productive. Fundamental to MOS technology, the patterning of polysilicon structures to form the gates and self-aligned contacts presents challenges in the area of deposition and etching. This includes both algorithmic issues for moving boundaries and the surface chemistry necessary to achieve anisotropic etching [4]. The kinetics of forming ultra-thin layers and their resulting electrical and interface properties continue to be a key process step where predictive models are needed. While there has been recent progress in both the metrology and modeling of submicron LOCOS structures [5][6], the full understanding of the defect structures and interface effects is still a fertile area for research. Figure 3 shows a comparison of experimental measurements and simulations of surface topography for a 0.8 μm x 0.8 μm nitride layer that has been locally oxidized around the edges. Note that there are changes in local height at the corners resulting from the 3D oxidant diffusion and surface reaction that can be represented using a quasi-3D model [5].

The use of selective etching of silicon to create both trenches and pillars is becoming of

increased importance since the relatively fixed die area motivates interest to pack still more devices along vertical edges, thereby fully utilizing the third dimension of the wafer. A pillar device is such an example where a vertical MOS was used as a Flash EPROM [7]. Current flows vertically along the pillar sidewalls and floating gate regions completely encircle each pillar. Process and device simulations were used extensively to explore the many trade-offs resulting from the etching process. The scaling of vertical nano-structures has many other challenges both in fabrication and electrical behaviors. Figure 4 shows the final shape of a 20 nm silicon cylinder that has been oxidized in a dry oxidizing ambient. The boundary of the gridded region shows the oxide shape and the cylinder has now become square as a result of the orientation and stress dependences of the oxide growth. Such nano-scale process physics must be fully characterized if advanced nano-devices are to be reliably manufactured. It is also useful to consider the still more aggressive requirements that will be imposed as quantum capacitance effects [8] are considered for use in memory systems.

A promising way to achieve predictive TCAD models that track technology evolution, including advanced levels of control needed for nano-structures, is through deeper understanding of the atomic-scale mechanisms. For example, the formation, activation and interface properties of point defects are key to device scaling. These atomic-level studies also create interdisciplinary research opportunities across the fields of electrical engineering, material science, solid state physics and physical chemistry. As a specific example, the energy and charge density for a SiO_2 defect in silica can be obtained from Density Functional Theory (DFT) calculations (see Fig. 5) [9]. Extraction of physical parameters and determination of macroscopic dynamics from the atomic-level calculations consist of an important part of knowledge hierarchy in Fig. 2.

INTERCONNECT STRUCTURES

The scaling of interconnects for ICs has become the pacing factor in determining performance and functional density for both signal processing and computer system architectures. As clock frequencies move towards 300 MHz and beyond, the issues of cross-talk, signal integrity, and functional behavior of logic have become more complex. Since the dynamic power of IC chips is controlled by clock speed and total capacitance, there is intense effort from the technology perspective to realize lower dielectric constant materials. Interconnection resistance and inductance are also important parameters at higher clock frequencies; the role of the skin effect has helped to promote the used of more advanced metallization as well. Figure 6a shows the functional and structural complexity of interconnection structures used for advanced memory systems. Looking at the interconnect cross-section shown in Figure 6b, it is clear that both the metal and dielectric layers are structurally complex. In addition to requirements for control of etching and deposition of these layers, there is growing use of chemical and mechanical polishing (CMP) as a planarization technique [10].

Issues of interconnections at the process and device levels are fundamentally quite different from that of intrinsic devices. It is essential to realize that the deposited layers involve grained microstructure for the conducting layers (metals, silicides and polysilicon) as well as amorphous materials for the dielectric interlayers. These structures change with processing and as a result of bias stress under electrical operation. During the fabrication process there are chemical reactions and stress-related changes due to the thermal cycles used; ductile behavior of both the metal and dielectric layers is observed. The electrical behavior of interconnects can be considered from several perspectives. The increased density of interconnects results in growing concern with signal cross-talk which affects functional behavior at the chip and cell levels. At the meso- and micro-

scopic levels, there are a range of surface and interface effects that all impact electrical behavior. In some cases, these effects have been considered from the perspective of novel transport and storage phenomena (i.e. “telegraph” and “single charge” devices). The study of such quantized effects will certainly contribute to improved physical understanding and hopefully also contribute to the mainstream modeling needs for VLSI interconnects.

SOFTWARE ENGINEERING FOR COMPUTATIONAL ELECTRONICS

The above sections have considered the evolution in intrinsic devices and interconnects with emphasis on examples that illustrate the challenges in process modeling. These challenges come not only from the growing complexity of the IC fabrication processes; there are also important software engineering problems that need to be considered. These software issues are considered from the perspective that the tools must support new and constantly changing problems of modeling advanced technologies. This section focuses primarily on developing scalable and configurable software for process modeling that can support an hierarchical approach.

The evolution of present 2D simulators such as SUPREM and SPEEDIE has demonstrated two important lessons. First, the definition of structures and how to model their geometric and structural changes are quite complex, especially owing to physics at surfaces and moving boundaries. Second, the possible equations representing the physics and the resulting numerical requirements are also becoming more complex. Hence, a key challenge in realizing simulators for process modeling of nano-structures is the need to create flexible and reliable software.

In an effort to create a versatile and scalable process simulation environment, a deeply layered and object-oriented code called ALAMODE has been developed [11]. The software hierarchy supports features which relate to structure definition, specification of PDEs and the overall solution of these equations have all been implemented in a very flexible framework. However, the structural definition of complex geometries with sub-domains (i.e. grain boundaries or other atomic-scale attributes) requires new methods and tools especially as new atomic-level tools are used in hierarchical modeling. There is clearly a need to abstract this information into the appropriate form for use in higher level models. The specification of PDE-based models and their consistent implementation in simulation tools is also of growing concern. Recent experiments with ALAMODE have used tcl (tool control language) as a formal means to both specify and implement the needed information within the simulator. An example of what typical tcl-scripting is like for coupled diffusion equations is shown in [11]. Finally, the solution of complex sets of PDEs over large numbers of computational grid represents a grand challenge set of problems; the use of parallel computers is becoming essential. There are already examples where such parallel computing have been applied in the device analysis domain [12]. Similar efforts are necessary and even more essential in the process modeling area where computational complexity is several orders of magnitude higher than for device analysis [13].

CONCLUSIONS

This paper has outlined the scope of hierarchical TCAD with emphasis on the many challenges in the area of process modeling, especially as we move into an era of nanoelectronics. Many motivating examples in device design show the opportunities for synergism with design concepts and even technology from the fields of computational electronics and compound semiconductor fabrication. In addition, there are many new software challenges to be faced in the nano-electronics era. A key question is how to exploit hierarchy and the growing need to create flexible tools.

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REFERENCES

[1] D. L. Harame et al, "A 200 mm SiGe-HBT Technology for Wireless and Mixed-Signal Applications," IEDM, Tech. Digest pp. 437-440, Dec. 11-14, 1994.

[2] K. Wang et al, "Layout-based Extraction of IC Electrical Behavior Models," IEDM 1994 Tech. Digest, Dec. 11-14, 1994, pp. 209-212.

[3] R. W. Dutton, B. Troyanovsky, Z. Yu, E. C. Kan, T. Chen, and T. Arnborg, "TCAD for Analog Circuit Applications: Virtual Devices and Instruments," to be presented at ISSCC'96, Feb. 1996.

[4] Z. Hsiau, E. C. Kan, J. P. McVittie, and R. W. Dutton, "Physical Etching/Deposition Simulation with Collision-Free Boundary Motion," to be presented at IEDM, Dec. 1995.

[5] H. Park et al, "Quasi-3D Modeling of Sub-Micron LOCOS Structures," to appear in IEEE Journal on Semiconductor Manufacturing, Nov. 1995.

[6] P. Smeys, P. B. Griffin, and K. C. Saraswat, "An Improved Calibration Methodology for Modeling Advanced Isolation Technologies," SISDEP'95 Tech. Digest, Sept. 6-8, 1995, pp. 42-45.

[7] H. Pein and J. D. Plummer, "Performance of the 3-D Sidewall Flash EPROM Cell," IEDM Tech. Digest, pp. 11-14, Dec. 5-8, 1993.

[8] K. Hess and L. F. Register, "Modeling Nano-Structure Devices," SISDEP Tech. Digest, pp. 9-16, Sept. 7-9, 1993.

[9] Dmol User Guide, version 2.3.5. San Diego: Biosym Technologies, 1993.

[10] G. Bronner et al., "A Fully Planarized 0.25 μm CMOS Technology for 256 Mbit DRAM and Beyond," 1995 VLSI Symposium Tech. Digest, pp. 15-16, June 6-8, 1995.

[11] D. Yergeau, E. C. Kan, M. Gander, and R. W. Dutton, "ALAMODE: A Layered Architecture for Model Development," SISDEP 1995 Tech. Digest, Sept. 6-8, 1995, pp. 66-69.

[12] B. P. Herndon, N. R. Aluru, A. Raefsky, R. Goossens, K. Law, and R. W. Dutton, "A Methodology for Parallelizing PDE Solvers: Application to Semiconductor Device Simulation," 7th SIAM Conf. on Parallel Processing and Scientific Computing Tech. Digest, Feb. 1995.

[13] R. W. Dutton and M. R. Pinto, "The Use of Computer Aids in IC Technology Evolution," Proceedings of IEEE, Vol. 74, No. 12, Dec., 1986, pp. 1730-40.

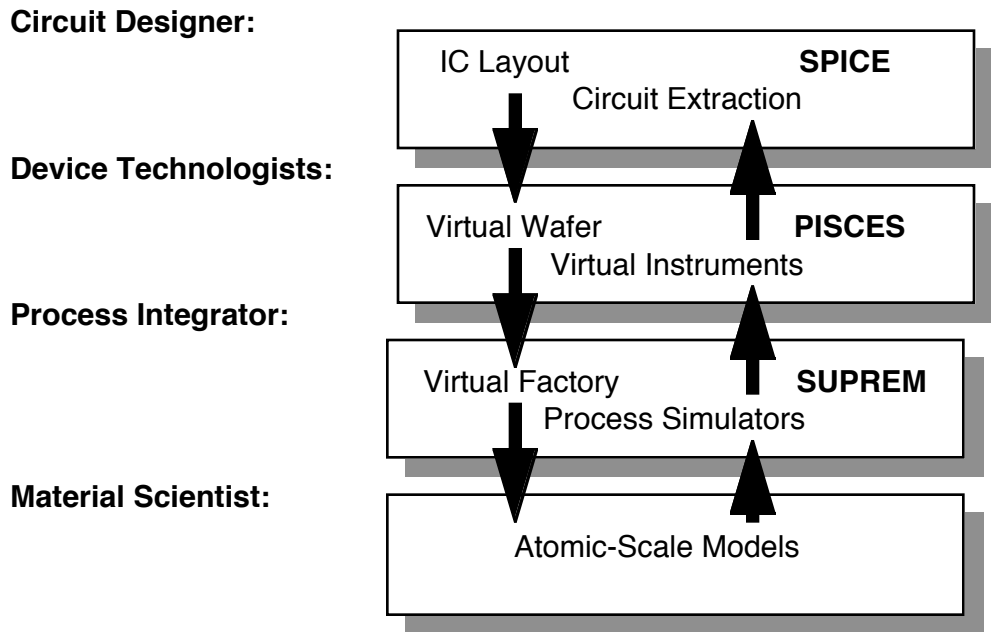


Figure 1: Hierarchical Taxonomy of Circuit, Device and Technology Design Issues.

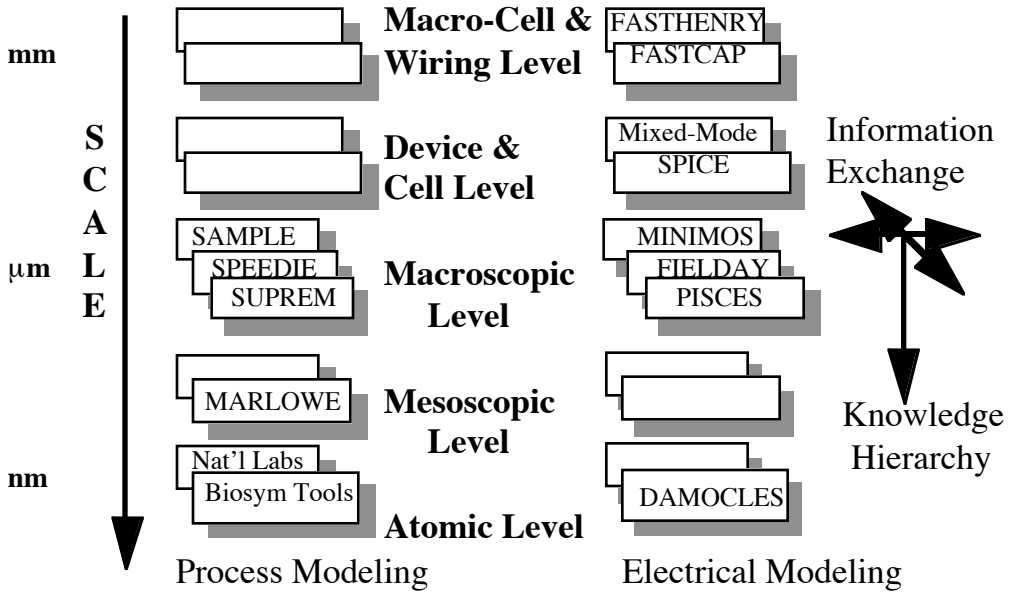
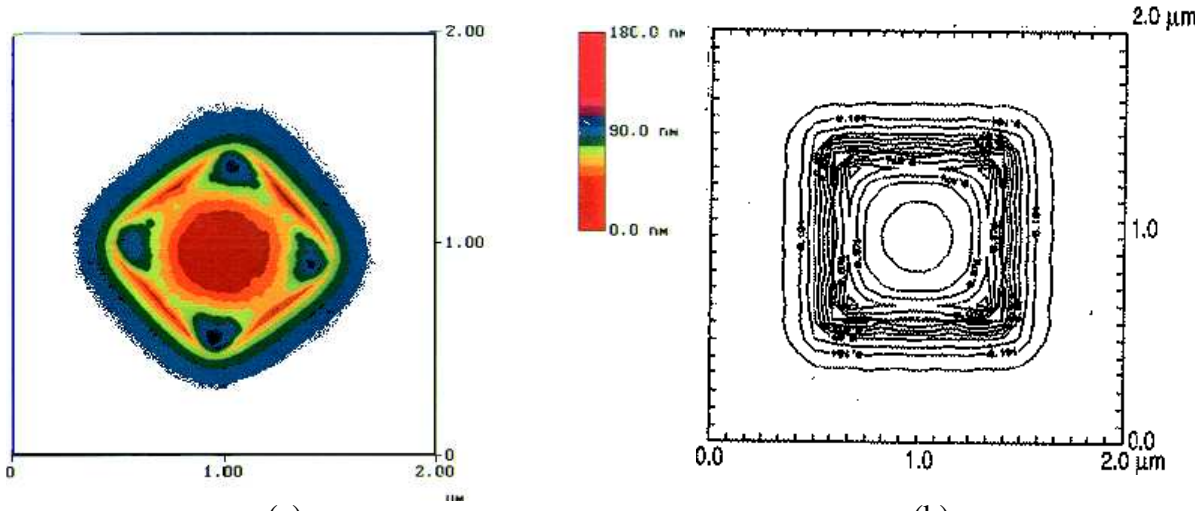


Figure 2: Expanded view of hierarchy and domain perspective: typical tools that populate the levels; scale of computational complexity including both domain size and duration of virtual events.



(a) (b)

Figure 3: Measured and simulated topography for 0.8 µm nitride mask layer [6] after local oxidation: (a) AFM measurements of topography, (b) simulation of surface shape.

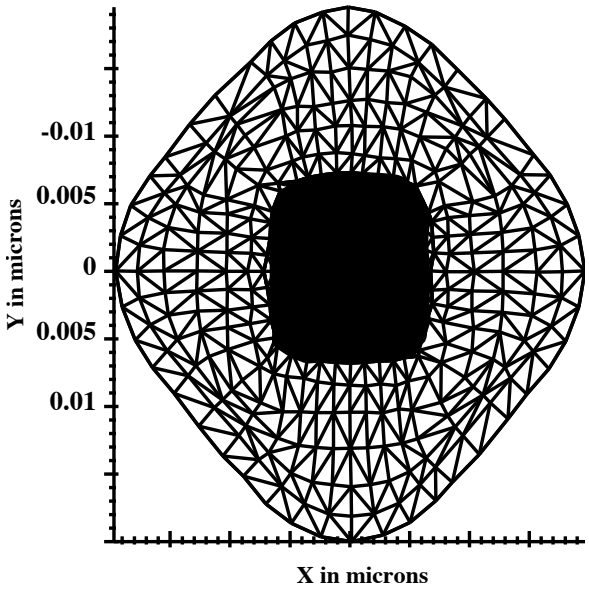


Figure 4: Simulated results for oxide growth (shown as grid structure) on a 20 nm silicon pillar which show effects of orientation and stress on final (rectangular) shape of the pillar.

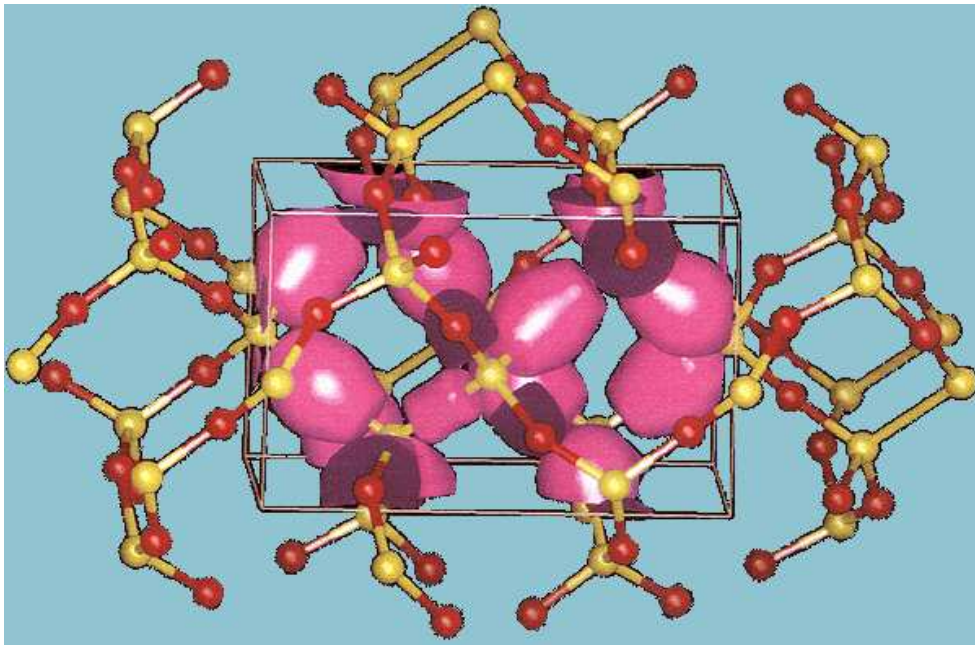
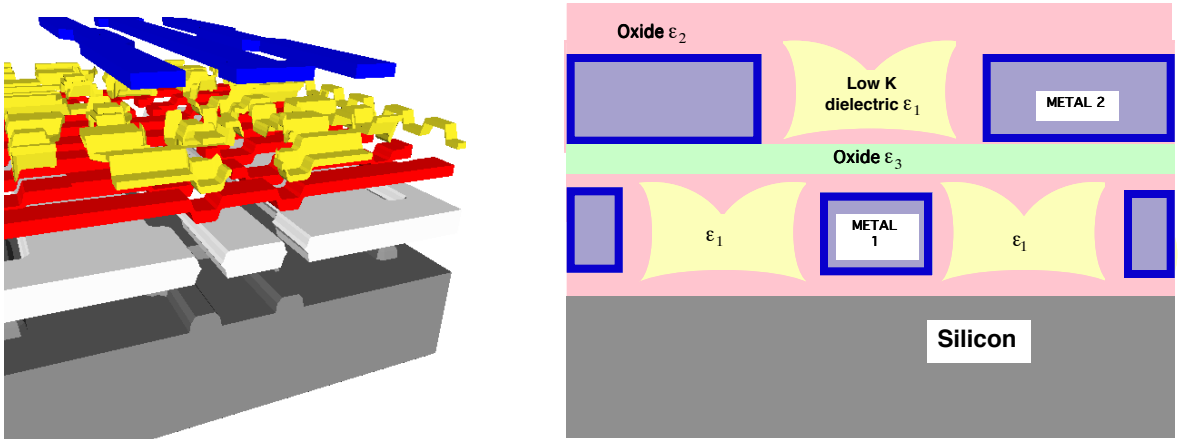


Figure 5: Charge density of a silicon dimer conformation for the oxygen defect in silica. Computational results obtained using ab initio calculations done with the DMol program, and graphical displays from Insight II molecular modeling system [9].



(a) (b)

Figure 6: Interconnections viewed from two perspectives: (a) a virtual wafer representation of three-dimensional interconnections in a high-density static memory [2] and (b) cross-sectional view of typical metal and dielectric effects in a deep submicron technology