Layout-based Extraction of IC Electrical Behavior Models

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Abstract

Behavior of IC structures is modeled using a heterogeneous set of tools and derived physical representations. A unified 3D information model is demonstrated with special emphasis on application of solid geometry modeling techniques. Examples used in this presentation include modeling of SRAM technology and interconnect structures that include packaging considerations as well. Issues of mixed level simulations are considered based on circuit and thermal constraints on IC structures.

Introduction

There are a growing number of technology and circuit design problems where the interactions between layout constraints and the underlying technology base create situations that require detailed TCAD analysis. This demonstration shows progress in supporting mask-to-behavior modeling. It involves the integration and demonstration of standard interfaces and tools--GDS2, ACIS (solid modeling) [1], PISCES and SPICE--as well as evolving standards and prototype tools such as SWR (Semiconductor Wafer Representation) [2] and VIP3D, Stanford's "3D Virtual Process" application. The focus of the demonstration will be on extracting IC cell behavior, primarily using two SRAM examples, based on layout input and tools that fully exploit the 3D nature of the problem. The goals of this work are two-fold: 1) to extend simulation capabilities in support of fully 3D considerations and 2) to revolutionize tool inter-operability through the use of a consistent information model--a major challenge facing both users and developers of TCAD. Traditionally, simulation of IC processes and circuit designs have been done using one- and two-dimensional models. The integration of simulators, where devices and circuits are connected, has been especially difficult due to the lack of common representations and means to extract the needed subsets of the data. For example, circuit extractions rely on 2D layout information (i.e. X-Y plane) whereas device simulators deal with 2D cross-sections (i.e. Y-Z plane). By means of the fully 3D geometry and gridding tools used in this work, along with the utilities that derive consistent subsets of the data, both classes of simulation tools can be supported and extended into the 3D domain. Moreover, through use of 3D solid modeling capabilities, a central and universally accessible information model is developed which serves to integrate tools and assure greater data consistency.

Summary of Results

The following discussion and set of examples give a summary of typical demonstration results to be exhibited. The intent is to walk the potential user through a design process going from layout through various stages of behavioral modeling. Fig. 1 (see final page) shows an architectural overview of information flow through this design process.

A. Extraction of Geometry from IC Layout

Simulation flow begins with the construction of devices based in part on mask information from an IC layout tool. The Cadence tool is used in creating the data and passed through a standardized interface with GDS2. In Fig. 2, a 6 transistor SRAM cell has been created with VIP3D, a tool which uses this mask information in conjuction with technology parame-

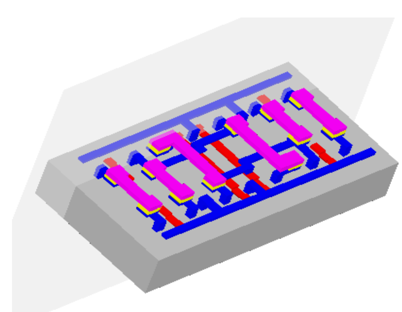

Fig. 2: Model of six transistor SRAM, created using VIP3D based on solid geometry manipulations. Cut-plane (2D) is used as part of mixed-mode analysis (see Fig. 5).

ters such as layer thicknesses as well as 2D simulation results to build up 3D geometries describing the structures created on a wafer. The SWR interface to solid-modeling is used by applications such as VIP3D to create, modify and maintain this wafer state data. In this way, VIP3D performs wafer processing and provides the user with a way to describe devices in 3D.

A more complex SRAM geometry based on a commercial cell design is shown in Fig. 3a, which was produced in collaboration with Cypress Semiconductor using the same basic methodology and solid modeling. Creation of this cell involved sweeping of arbitrary cross-sections along mask edges and resolution of step coverage during conformal deposition. The layer thicknesses and the bird's beak profile for the field oxide are based on either process simulation or measurement. Fig. 3b shows a 4X4 array assembled from these cells indicating the more complete configuration of second layer metal which will affect interconnect capacitances.

B. Deriving 2D Cross-Sections from Solid Geometry

Based on such 3D device models, both 2D and 3D device simulation can be run. One major advantage for having a single 3D device information model is the consistency of the data model, which ensures that simulation tasks can be performed in a unified manner. With the specification of a 2D cut plane,

(a)

(b)

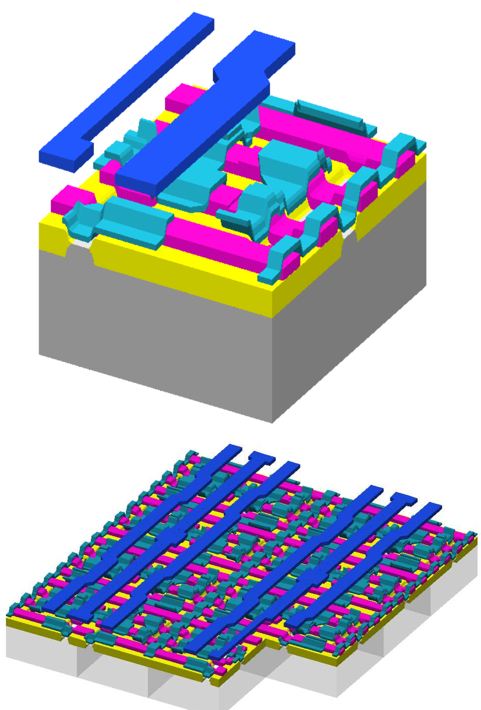

Fig. 3: Commercial SRAM modeled using solid geometry approach: (a) 6T cell and (b) array of cells.

such as the one shown in Fig. 2, the system can extract device geometry information through attributes which include various physical properties such as: material type, analytical or simulated doping distributions. In this way, 2D subsets of the complete 3D model can be obtained.

C. Gridding of 2D Surfaces and 3D Volumes for Simulation

In addition to geometrical cross-sectioning, various mesh services are also provided, including 2D cross section mesh, 2D surface mesh and 3D volume mesh. The mesh generation engines are based on quadtree(2D) and octree(3D) techniques with two major improvements: level control functions for controlling the mesh density and delta-zone (and warping) functions for optimizing the mesh quality along non-planar boundaries. To generate 2D surface mesh, the system first extracts all external boundary faces and then performs 2D mesh generation on each of these faces.

D. Lumped Parameter Extraction of Interconnect Parameters

One area in which 2D surface meshing of 3D volumes can be particularly useful is in parasitic analysis of devices and interconnect structures, which is a very important step in the design verification process. Traditional IC parasitic extraction is based only on the 2D layout artwork and is not well-suited to capture true parasitic behavior of devices when non-ideal planarizations and process variations are considered. For interconnect modeling, 2D electrical field analysis is proving insufficient in accounting for increasing fringe effects caused by shrinking interconnect size and closer line pitch. In Fig. 4 we see a surface mesh of the 3D interconnect structure of the SRAM cell in Fig. 2. By using this surface-meshed structure and the 3D capacitance extraction application FASTCAP from MIT [3], parasitic extraction for 3D models can be achieved.

E. Mixed-Mode Simulation for Extraction of Electrical Behavior

Cross sections and volumes of VIP3D results can also be used in mixed-mode simulations to obtain circuit performance as

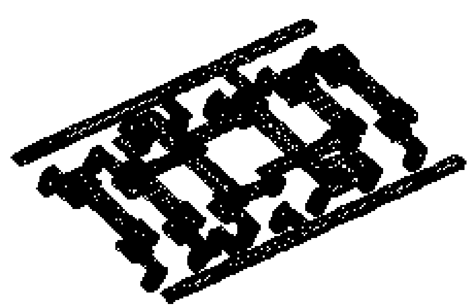

Fig. 4: Surface meshing of poly and metal layers for SRAM (see Fig. 1).

shown in Fig. 1. In this work a generalized interface between the Berkeley SPICE tool and numerical device simulators such as Stanford's PISCES (or IBM's FIELDAY) are demonstrated. This interface allows a designer to examine the circuit performance of a new device for which a SPICE analytic model does not exist or may be insufficient. Such inadequate models include those for short channel MOSFET's, GaAs MESFET's, and optoelectronic LED structures. In addition, more complex effects such as self heating and photon generation can be simulated by the numerical device and hence, examined in the circuit operation. The emphasis in this particular demonstration will be on illustrating the ability to quickly select cross-sections and merge device and circuit levels of abstraction into a unified simulation environment.

F. Examples using SRAM Technologies

In order to illustrate the utility of the overall system, the SRAM of Fig. 2 is used as a cell-based design where performance is of major interest to the designer. In this example, two aspects of the cell are examined. Fig. 5a shows the circuit diagram with the basic cell and control circuitry. The shaded

(a)

(b)

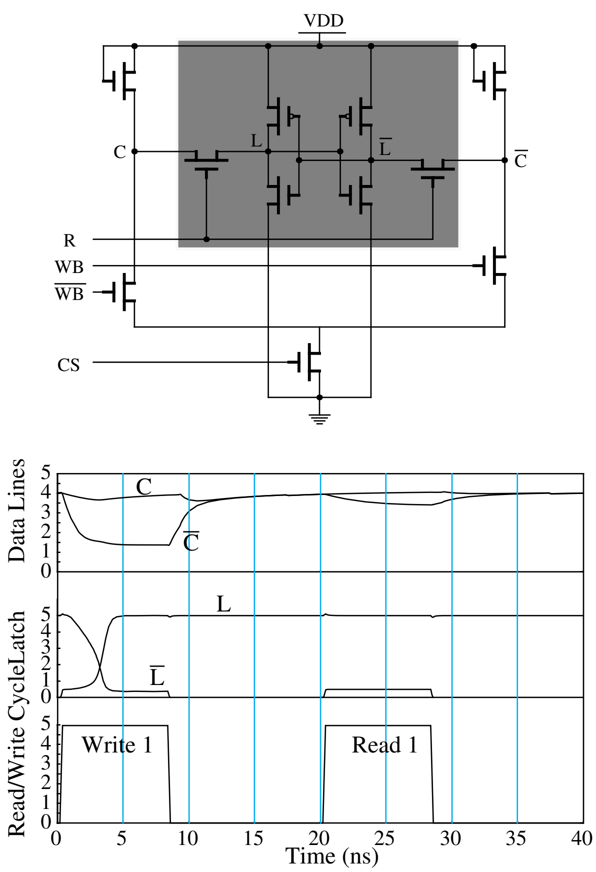

Fig. 5: Mixed-mode analysis of SRAM cell: (a) circuit schematic where shaded region represents device level modeling; (b) output waveforms based on coupled circuit- (SPICE) and device- (PISCES) level analysis.

region is simulated with PISCES numerical devices while the other control transistors are simulated with analytic circuit models. In addition, parasitics may be included for the line interconnects, as calculated with FASTCAP. Fig. 5b shows the transient behavior of the circuit for a write/read cycle. The major concern is how quickly C and C (bar) come back together once the pass transistors are turned off.

The more complex SRAM of Fig. 3 shows a cell where the tight design rules at the cell level can produce both manufacturability and circuit performance challenges. Presently the examples to be demonstrated for this commercial SRAM focus primarily on the geometric specification and parameterization issues rather than on the simulations. Nonetheless, by utilizing mixed-mode capabilities demonstrated above, the design can be examined for potential problems at both levels which can then be directly linked to the layout data. In addition, perturbations on the layout can be used to fix layout or performance related problems that may become uncovered.

Conclusion

An integrated system for 3D device and circuit characterization based on layout and process information is presented. Use of a geometrical wafer representation provides a consistent and effective means of manipulating 3D IC models. By means of sectioning and gridding tools, flexibility in moving from 3D wafer-level analysis to 2D and 3D interconnect-, device- and circuit-level simulation has been demonstrated. The supporting services allow designers to characterize circuit behavior of IC's directly from a layout tool. All of these capabilities will be demonstrated primarily using the two SRAM cell examples discussed above.

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