ACCURATE C-V CHARACTERIZATION OF QUARTER-MICRON MOS DEVICES USING QUANTUM MECHANICAL CORRECTIONS AND AC SIMULATION

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Abstract – *Extensive study of C-V characteristics of MOS structures (both capacitors and MOSFETs) with quarter micron feature size (gate oxide thickness of* $30 \sim 80\,\mathring{A}$ *and gate length of* $0.18 \sim 0.35\,\mu m$*) leads to the following progress in device modeling and simulation: 1) A generalized bandgap broadening model for quantum mechanical (QM) corrections applicable to both accumulation and inversion layers; 2) A relaxation numerical algorithm for ac device simulation allowing such nonlocal effects as QM be included; and 3) A calibration methodology for determining the doping profile accurately in the substrate using both TED (transient enhanced diffusion) and QM models. In this paper the modeling and algorithmic aspects of the study are discussed and simulation results are compared with the measured data using MOS devices where the doping profile has been calibrated using the methodology detailed elsewhere [1]. The excellent agreement between simulation and measurement results justified the modeling approach used.*

INTRODUCTION

Recent experiments and simulation with improved physical models and numerical techniques confirm that quantum mechanical (QM) effects are significant for MOS device characteristics even with gate oxide thickness, t_{ox}, at 80 Å range (corresponding gate length, L_g, of $0.35\,\mu$m).

The departure of two key MOS device parameters – threshold voltage (higher) and gate capacitance (lower) – from the classical prediction based on the physically measured gate oxide thickness has been attributed to the following two phenomena in the surface region of the MOS structure due to QM effects. First, the change of the shape of the channel carrier distribution – the peak is away from the Si-SiO_2 interface. Second, the transition of the band structure in the surface potential well from continuum band to discrete (i.e., quantized) levels. The net effect in terms of the device electrical behavior is to render a thicker effective gate oxide thickness than an actual one. van Dort [2] has quantified the fundamentals of this physical picture and proposed a simple *bandgap broadening* model which correlates the intrinsic carrier concentration in the channel region to the surface transverse electric field. This simplistic model has been verified using a more sophisticated three subband model [3] in the inversion region. So far, however, little attempt has been made to apply the model to the entire MOS operation region (i.e. from accumulation through flatband and depletion to the inversion regions). And the analysis was limited to MOS capacitors (two-terminal, passive devices) due to lack of ability to perform small signal *ac* simulation for multi-terminal, active devices, mainly MOSFETs.

In this paper, a generalized bandgap broadening model, applicable to the entire MOS operation region, to account for QM effects is proposed. A physically meaningful factor is introduced to allow good fitting of experimental data in a broad range of MOS structures – $p-$ and $n-$substrate MOS capacitors and FETs – and extraction of active poly-gate doping level. An efficient, relaxation based algorithm has been developed for the small signal *ac* analysis in the device simulation when non-local effects such as QM and universal mobility models have to be included. The model and the simulator (PISCES) have been extensively calibrated using MOS structures with the gate oxide thickness ranging between 30 and 80 Å and gate length from 0.18 to 0.35 μm. With the doping profile simulated using an improved TED model, very good agreement between device simulation and measurement has been achieved.

MODEL FORMULATION

The energy bandgap in the channel region is augmented by the following amount which is driven by the magnitude of the surface transverse electric field, $|\mathcal{E}_n|$.

$$\Delta E_g(z) = \kappa \frac{13}{9} \beta \left(\frac{\epsilon_{Si}}{4qkT} \right)^{1/3} |\mathcal{E}_n|^{2/3} g(z) \quad (1)$$

$$g(z) = \frac{2e^{-(z/\lambda)^2}}{1+e^{-2(z/\lambda)^2}} \quad (2)$$

where z is the coordinate in the normal direction to the Si-SiO$_2$ interface towards the substrate. $g(z)$ is a transition function which peaks at the interface ($z = 0$) and decays to zero when $z >> \lambda$. The characteristic length, λ, is usually around 300Å. $\beta = 4.1 \times 10^{-8}$ eV·cm and all other parameters have the conventional meaning [2]. The use of the magnitude of $\mathcal{E}_n$ allows the model be applied to both accumulation and inversion regions and different type of MOS ($p-$ or $n-$type) structures. To compensate for the approximation made during the model formation which is based on only the ground level in the quantum well, a coefficient, κ, equal or larger than one is introduced as a fitting parameter. It has been found that for $p-$substrates (i.e. nMOS) $\kappa = 1.75$ and for $n-$substrates (pMOS) $\kappa = 1$ generally gives good fit.

NUMERICAL ALGORITHM

For MOS capacitors, the quasi-static *dc* analysis can be used to compute the capacitance. For MOSFETs, however, to find the cross-capacitances such as the gate-source and gate-substrate capacitances, small signal *ac* analysis must be used. Because of the nonlocal nature of the bandgap broadening model – the intrinsic carrier concentration in the channel region depends on the surface potential which may not be on the neighboring nodes – the *ac* analysis capability in conventional device simulators can no longer be applied since the Jacobian matrix used in the *dc* analysis during Newton-Raphson iteration has to be modified. Even worse is the fact that due to the addition of random off-diagonal terms, the original band structure of Jacobian matrix is lost, which introduces lots of fillings during LU decomposition. To simplify the code modification and to maintain the numerical efficiency of the sparse matrix solver, we have developed a relaxation-based, iterative scheme to resolve a general category of problems complicated by the perturbation resulting from non-local effects. The exact Jacobian, J, in *ac* simulation is partitioned into a *dc* part, the main one, i.e., J_0, and a perturbation part, J_{QM} in the QM correction case. The iteration process for solving the linear equation of $Jx = b$ thus becomes:

$$J = J_0 + J_{QM} \quad (3)$$

$$J_0 x^{i+1} = b - J_{QM} x^i \quad (4)$$

where x generally represents the perturbation in the basic semiconductor variables such as potential and carrier concentrations and b is the stimulus. $i = 0, 1, \ldots$ with $x^0 = J_0^{-1} b$. This relaxation scheme can easily be implemented in the existing code and our test shows that it works very efficiently in this application. In fact, as can be seen from the following table, after two iterations the capacitance thus computed is within the 0.1% range of the exact value. The perturbation terms in the Jacobian can either be computed using rigorous differentiation or by a difference method which can be quickly implemented at the expense of computational cost.

iter #	C_g (pF)	relative err (%)
0	7.8722	8.9
1	7.1726	0.76
2	7.2347	0.10
quasi-static	7.2272 pF	

Table 1: Computation of the gate capacitance for a MOS capacitor with $t_{ox} = 31$Å and area of $100 \times 100\,\mu\text{m}^2$ at bias of $V_g = 2$V (inversion region for $p-$substrate). Both the relaxation *ac* scheme and the quasi-static approach of a difference in integrated gate charge (considered to be exact) are used. It can be seen that after 2 iterations, the error is reduced from 9% (without Jacobian correction) to 0.1%.

CALIBRATION and RESULTS

The above physical model and relaxation algorithm have been implemented in Stanford's PISCES and the program has been extensively tested using both MOS capacitors and MOSFETs fabricated in HP Labs. A key issue in the simulation is the calibration of the doping profile. The variation of the substrate bias in the C-V measurement of MOS structures is explored to reveal (i.e. probe) the doping profile at different depths and an improved TED model [1] helps accurately determine the doping distribution near Si-SiO_2 interface and source/drain region. The extraction procedure of the model parameters (κ and poly-gate doping N_p) is as follows: First, κ is determined by curve fitting in the accumulation region where the poly-gate depletion does not exist. Then N_p is extracted in the inversion region as a fitting parameter.

This modeling approach has been justified by the excellent agreement between the simulation and measured C-V data on a variety of devices and different bias. Figure 2 shows the simulation results for large area ($100 \times 100\,\mu m^2$) MOS capacitors with $t_{ox} = 30$ and 79 Å, respectively. Without QM correction the simulated gate capacitance can be off as much as 15% compared to the measured data. Moreover, the fitting parameter remains rather insensitive to the gate oxide thickness – in both cases, $\kappa = 1.75$, and the extracted poly-gate doping concentration of $3 \times 10^{19}\,cm^{-3}$, in compliance with the process specification.

In Figure 1, the simulated doping profiles are compared using the improved TED model and the default one in SUPREM 4. It can be seen that the new model predicts higher channel doping (boron) at the Si-SiO_2 interface, which gives a better fit to the threshold voltage. Figures 3-4 show the C-V simulation of $0.35\,\mu m$ MOSFET at zero substrate bias and $V_{bs} = -9.4\,V$ using small signal *ac* analysis. The fitting of all cross-capacitances at vastly different substrate bias is generally good, indicating that both the doping profile and simulation approach are correct.

CONCLUSIONS

It has been noted that the fitting of C-V characteristics in the flatband region, where QM effects do not play role, is not satisfactory. The exact cause is still under investigation and a multi-dimensional QM correction scheme is being developed. Nonetheless, from this study it can be concluded that with the improved QM corrections model and *ac* analysis capability, the electrical characteristics of MOS structures with quarter micron feature size can be predicted with confidence based on physically measurable parameters.

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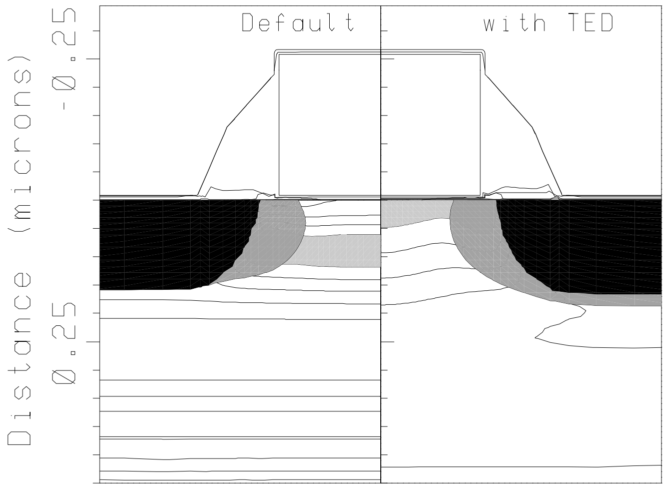
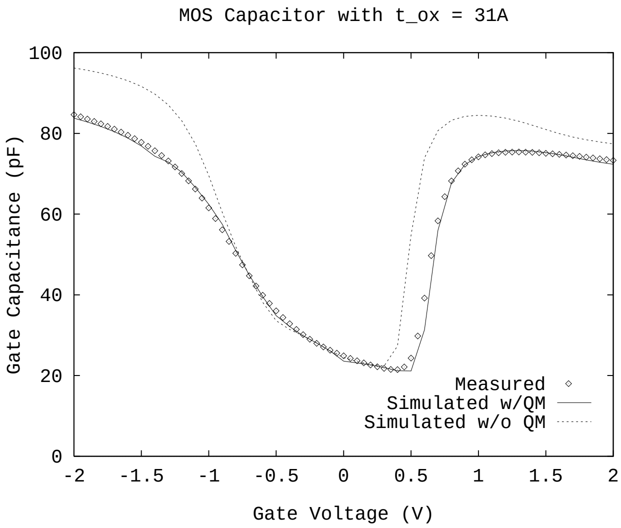


Figure 1: Device structure and doping contour plot for a MOSFET with channel length of $0.35\,\mu m$ and $t_{ox} = 79$Å. The doping profile is obtained from an improved TED model and has been calibrated using C-V measured data.



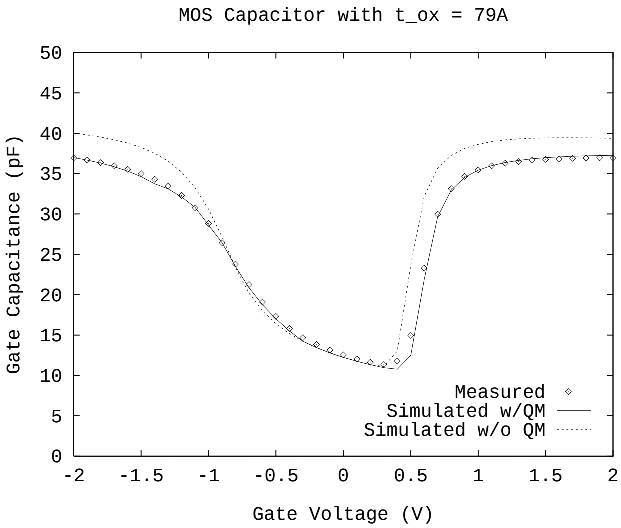


Figure 2: Measured (symbols) and simulated (lines) gate capacitance (C_g) for large area ($100 \times 100\,\mu\mathrm{m}^2$) capacitors, with gate oxide thickness, t_{ox}, of 31 and 79 Å, respectively. The accumulation region is well fitted using QM corrections based on the physical oxide thickness, and κ remains 1.75 for different t_{ox}. The fitting to the depletion region allows the active polysilicon doping to be extracted ($3 \times 10^{19}\,\mathrm{cm}^{-3}$ for both cases). For comparison, simulated C_g without using QM corrections are also shown and the error can be as large as 15%.

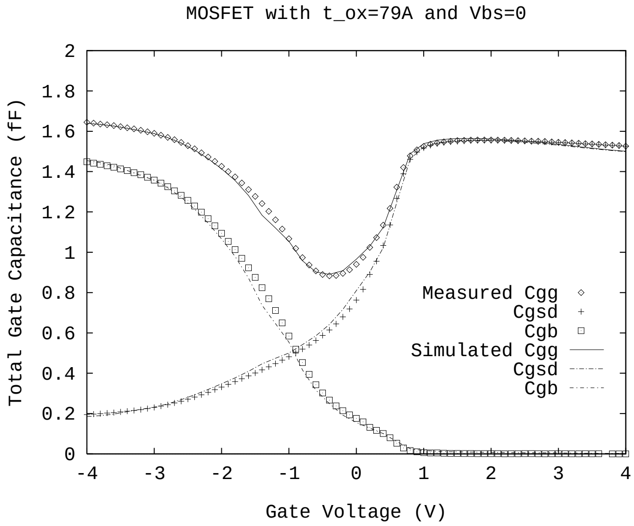


Figure 3: C-V simulation of MOSFET for all cross capacitances. The agreement between simulation and measurement for $V_{bs} = 0$ is excellent in the accumulation and inversion regions and is reasonably good in the depletion and flatband regions.

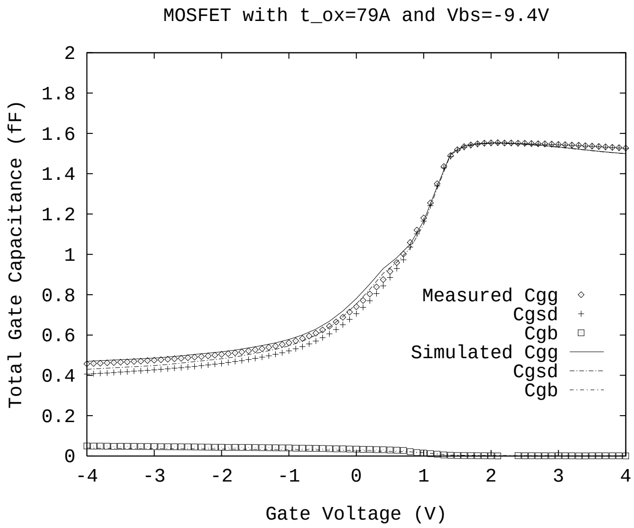


Figure 4: C-V simulation for $V_{bs} = -9.4\,\mathrm{V}$. The flatband region is beyond the plot range ($< -4\,\mathrm{V}$). The discrepancy between the measured and simulated data when the device is out of the inversion region is the indication of the potential deficiency of the current model and needs to be further improved.