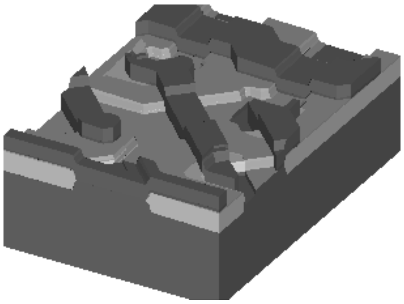

Figure 1: Previous results using solid modeling for wafer structures.

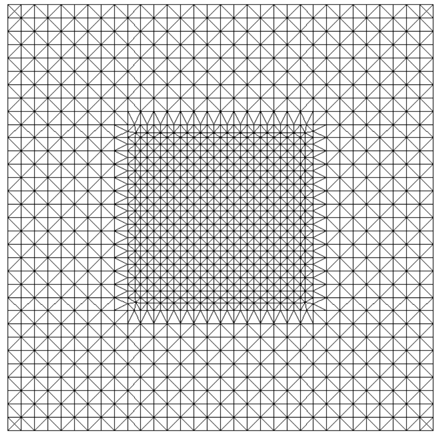

Figure 2: Quad-tree grid of mask area generated by Forest.

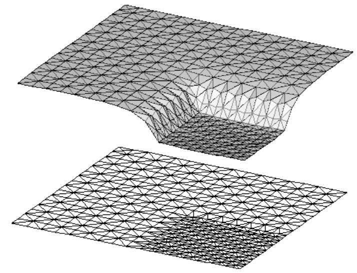

Figure 3: Corner section of Forest grid and one of the resulting LOCOS surfaces.

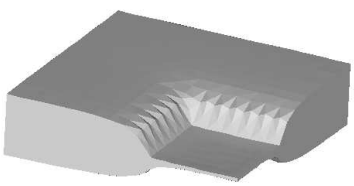

Figure 4(a): Finished corner section solid.

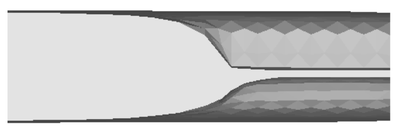

Figure 4(b): Side-view of corner section solid.

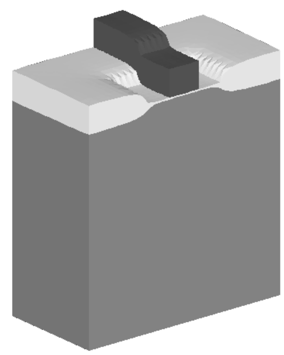

Figure 5: Deposited gate showing further processing on the LOCOS solid.

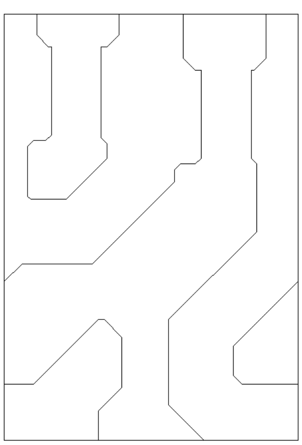

Figure 6: Active region layout for a single 4T static RAM cell.

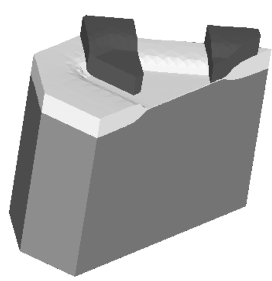

Figure 7: One active region of the cell and the deposited poly gate layer.

Figure 8: Another active region of the cell and the deposited poly gate layer.

3D Solid Modeling of IC Structures Using Simulated Surface Topography

Kenneth Wang, Hwasik Park, Zhiping Yu, Edwin Kan and Robert W. Dutton
CISX 332, Stanford University, Stanford, CA 94305, USA
Phone: (415) 723-1950, Fax: (415) 725-7731, Email: wang@gloworm.stanford.edu

INTRODUCTION:

The importance of 3D effects in semiconductor processes and devices is growing as structures are scaled into the deep submicron regime. In order to perform 3D analysis, however, designers need to accurately specify the structure to be simulated. A virtual integrated process modeling tool, based on a set of techniques which enable the construction of 3D device structures, is presented with emphasis on a new technique to build 3D LOCOS geometries. Examples illustrate how this technique is used to construct both a test structure as well as an actual memory cell design.

VIRTUAL INTEGRATED PROCESSING:

The objective of virtual integrated processing (VIP) is to produce realistic 3D wafer structures without incurring the cost of fully 3D process simulations. To achieve this goal, a solid modeling tool is used to manipulate 3D geometries. Using this tool, layout information (i.e. mask polygons) is combined with 1D process parameters, such as layer thickness or lateral step coverage, and 2D profiles, such as a simulated bird's beak shape [1]. The integration of these different types of data has resulted in structures such as the static RAM cell shown in Figure 1 [2].

INCORPORATING 3D SURFACES:

Limitations of using 1D parameters or 2D profiles in creating 3D structures are apparent from the above example. For example, 3D LOCOS structures generated in this way do not show the effects of enhanced oxidant diffusion at mask corners. A new capability to integrate simulated 3D surfaces has been used with solid models to generate more accurate wafer structures.

A quasi-3D LOCOS modeling algorithm [3] is used. The algorithm uses a combination of parameterized 2D analytic bird's beak shape equations and a fully 3D oxidant diffusion simulation based on the boundary element method to model corner effects in local oxidation. 2D and 3D simulations are combined in order to reduce computational cost. This heterogeneous approach reduces overall complexity which mirrors the goal of VIP as a means for rapid prototyping.

Results for a simple square mask region start with a quad-tree grid of the mask generated by Forest [4]. The grid shown in Figure 2 is used to convert the element-based results of the LOCOS simulation into nodal values. These results are in the form of two height values: z_{sur} for the oxide surface, and z_{int} for the Si-SiO_2 interface. For each of z_{sur} and z_{int}, a triangular face of the LOCOS boundary is created in 3-space based on each grid element and its nodal values. In addition, the boundary of the grid domain is traversed to create sidewall faces. These faces are joined together using the solid modeler. Figure 3 shows a section of the original quad-tree grid and the resulting surface corresponding to the z_{sur} values. The final 3D solid for this section is shown in Figure 4. This solid is fully compatible with the VIP framework, and further processing can be done as illustrated by the deposited gate structure shown in Figure 5.

OTHER EXAMPLES:

These methods have also been applied to a commercial static RAM design. Figure 6 shows the active region layout for a single 4T cell. Simulations of the local oxidation in this cell are done on each individual mask polygon, and Figures 7 and 8 show the resulting LOCOS geometries for two of those active areas. The polysilicon gate layer on top of the oxide is also shown.

CONCLUSIONS AND FURTHER WORK:

A new technique is demonstrated which allows incorporation of 3D simulation results in virtual wafer structures. This capability allows more realistic 3D device specification by enabling users to utilize 3D surface topographies. Gridded 3D geometries, which are obtained using CAMINO [5] with these structures, support fully 3D device simulation. Geometries with these flexible capabilities serve as a natural means for integrating many different representations, including traditional boundary representations, volume mesh and level-set surfaces. Finally, using solid models as a common ground for comparison, validation of models is possible.

ACKNOWLEDGEMENTS:

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