# C–V and Gate Tunneling Current Characterization of Ultra-Thin Gate Oxide MOS ($t_{ox}$=1.3–1.8 nm)

**Chang-Hoon Choi, Jung-Suk Goo, Tae-Young Oh, Zhiping Yu, and Robert W. Dutton**

Center for Integrated Systems, Stanford University, Stanford, CA 94305-4075, USA

**Amr Bayoumi, Min Cao, Paul Vande Voorde, and Dieter Vook**

ULSI Lab, HP Labs, HP Co., Palo Alto, CA 94303, USA

## I. INTRODUCTION

Direct tunneling of ultra-thin gate oxides results in exponential increases in gate leakage current [1]. Moreover, the loss of inversion charge due to the quantization of carriers is now significant. Hence, more physically accurate models are urgently needed. In this paper, an equivalent circuit approach considering the gate tunneling current as well as other QM effects is presented to characterize these phenomena for the gate oxide thicknesses ranging 1.3–1.8 nm.

## II. CAPACITANCE SIMULATION

An empirical, hybrid model for the QM correction in MOS structures has been implemented in a 2D device simulator, which combines both the van Dort and Hansch models [2]. The advantages of this model are as follows: i) elimination of the discontinuity at flatband that occurs in the van Dort model, ii) single set of parameters for different technologies. The hybrid model applies the improved van Dort model for the entire bias range (from accumulation to inversion region) while incorporating the Hansch model for electrons only. The simulation agrees with the measurement very well across six generations of CMOS technology (from 0.35 to 0.1 um) with only the active poly doping concentration as an adjustable parameter.

Fig. 1 shows the comparison between experimentally measured and simulated nMOS C–V data for an oxide thickness of 2.0 nm and area of $100\mu$m $\times$ $100\mu$m. For this analysis, the substrate doping profile is obtained using process simulation that includes TED (transient enhanced diffusion) effects.

## III. GATE TUNNELING CURRENT EFFECTS

Ultra-thin gate oxides ranging between 1.3–1.8 nm were grown in $N_2O$, using rapid thermal oxidation (RTO) in the temperature range of 900–950°C. Fig. 2 shows C–V curves of the $n^+-$poly/$SiO_2$/$p-$Si MOS capacitors for oxide thicknesses of 1.3, 1.5, and 1.8 nm, respectively. The capacitor area is $100\mu$m $\times$ $100\mu$m, and the small signal frequency is 100 kHz. It should be noted that sharp transitions are observed in the capacitance both in the inversion and accumulation regions. This is caused by the gate tunneling current through the oxide.

In this work the tunneling current is calculated using a 1D Green's function simulator, NEMO [3]. Because the multiple-scattering effects become extremely important, the WKB approximation is no longer satisfied for the thinner $SiO_2$ layers.

Fig. 3 shows the measured and simulated gate current for three gate oxide thicknesses.

## IV. C-V MODELING USING A CIRCUIT APPROACH

In order to model the capacitance for gate oxide thicknesses ranging from 1.3–1.8 nm, an equivalent circuit is introduced, as shown in Fig. 4. First, in order to consider the channel resistance, the silicon surface region is divided into small rectangular segments perpendicularly to the channel-current flow, as in Fig. 4 (a). $R_{ch}$ represents the channel resistance for each segment; this channel resistance also varies as a function of gate bias. $R_g$ represents a distributed resistance in the polysilicon gate, and the measured sheet resistance of the polysilicon is 5 $\Omega/\Box$, which is much smaller than the channel resistance ($R_{ch} \simeq$ 1.5 K$\Omega/\Box$). Next, the tunneling current is modeled using a nonlinear, voltage-controlled current source ($i = f(V_g)$) as in Fig. 4 (b). Also, the gate capacitance without the gate tunneling effect is modeled using a nonlinear, voltage-controlled capacitance ($C = f(V_g)$). SPICE ac small-signal analysis is then performed to find input admittance ($Y_{in} = G + j\omega C$) of the circuit at a given frequency of 100 kHz.

Finally, the gate tunneling effect on the C–V data is obtained by taking the imaginary component of $Y_{in}$ as a function of gate bias. Fig. 5 compares the modeling with the measurements as a function of gate bias for oxide thicknesses of 1.3, 1.5 and 1.8 nm, respectively, when the number of RC segments is 20. Once it exceeds five, the number of RC segments makes little difference in terms of the final capacitance. Additionally, the extracted average channel resistance values are 2.5 K and 1.1 K $\Omega/\Box$ in the inversion and accumulation regions, respectively.

## V. CHANNEL LENGTH DEPENDENCE OF GATE CURRENT

Gate tunneling current with respect to the drain bias ($V_d > 0$V) can be modeled using the equivalent circuit, as shown in Fig. 6. Here, the channel length dependence of $I_{gate}$ can be estimated by considering the short channel effects, i.e. drain-induced barrier lowering, due to the distributed channel resistance. As a result, the simulated gate tunneling current decreases as the drain bias increases since the potential difference between the gate and the channel surface becomes smaller, as shown in Fig. 7 (a). Fig. 7 (b) shows the simulated gate-channel dependence of $I_{gate}$; $I_{gate}$ decreases in inversely proportion to $L_g^{1.5}$, which is comparable to the experiments by Momose et al [4][5], where the slopes were 1.5 and 1.8, respectively.

## VI. SUMMARY

The C-V characteristics of ultra-thin MOS capacitor ranging 1.3–1.8 nm are modeled using a distributed RC network including QM corrected capacitance model and numerically calculated gate tunneling. This combined numerical/lumped model maintains excellent (and physical) accuracy compared to experiments, including gate tunneling current with respect to drain bias and channel length.

**References**

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