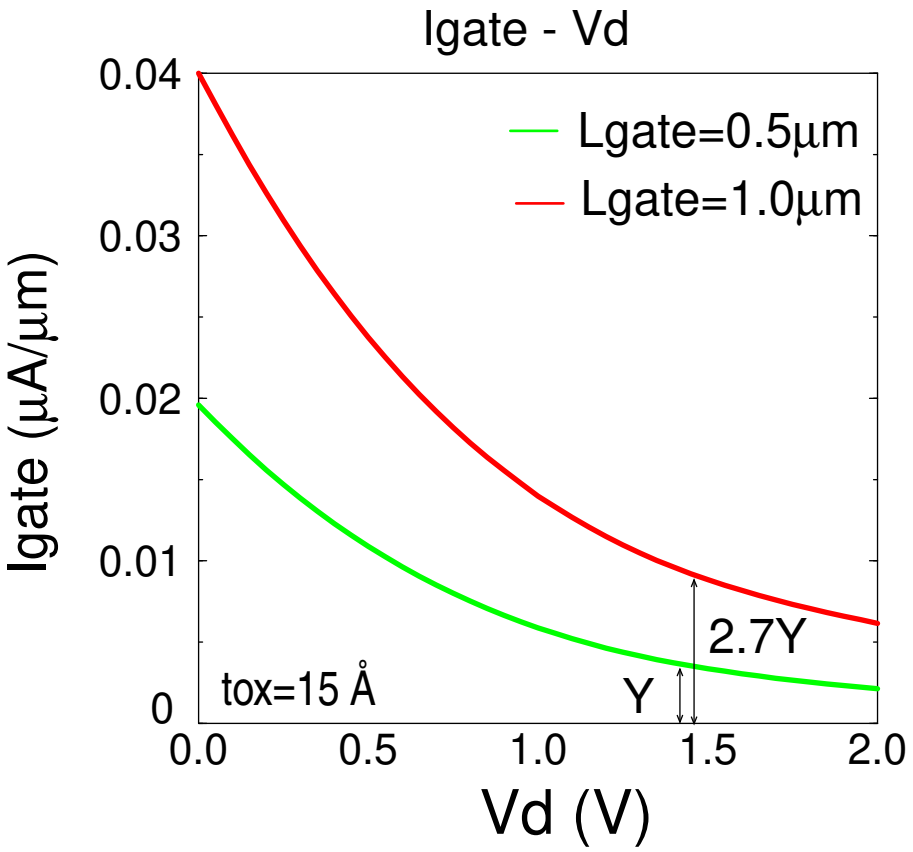
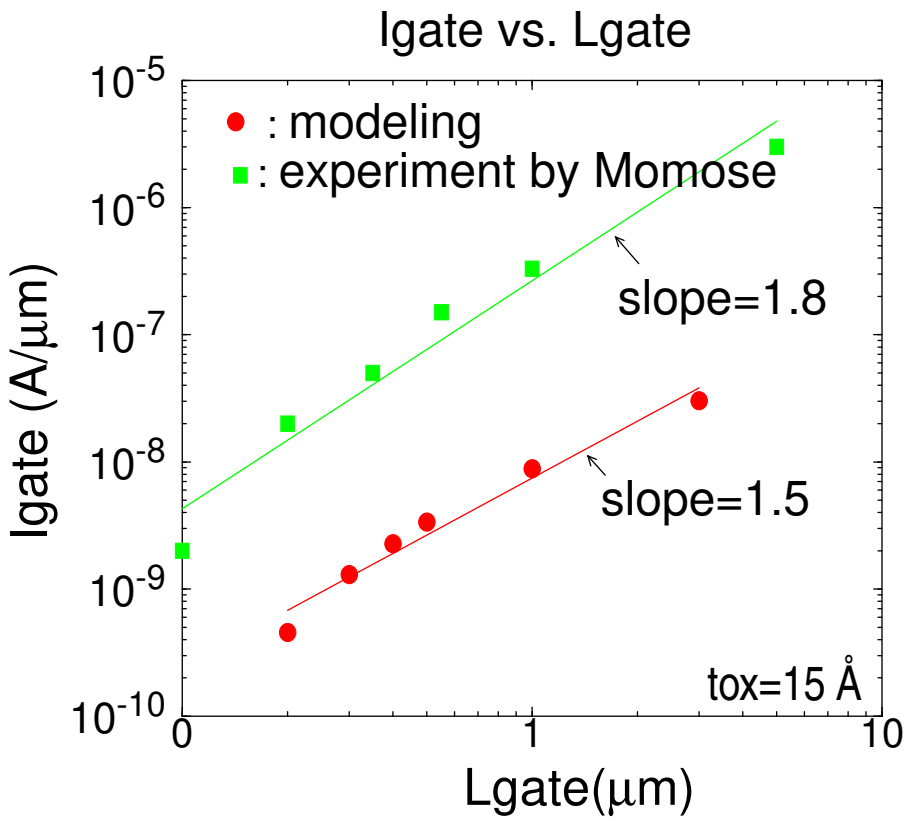
Conclusions

- Empirical, hybrid QM correction model implemented in device simulator
- Tunneling current is calculated from Green's function solver
- RC circuit approach including QM correction capacitance and gate tunneling current
- Network analysis results match well with the measured C-V for tox=13 - 18 Å

Igate modeling on MOS transistors : Result (II)

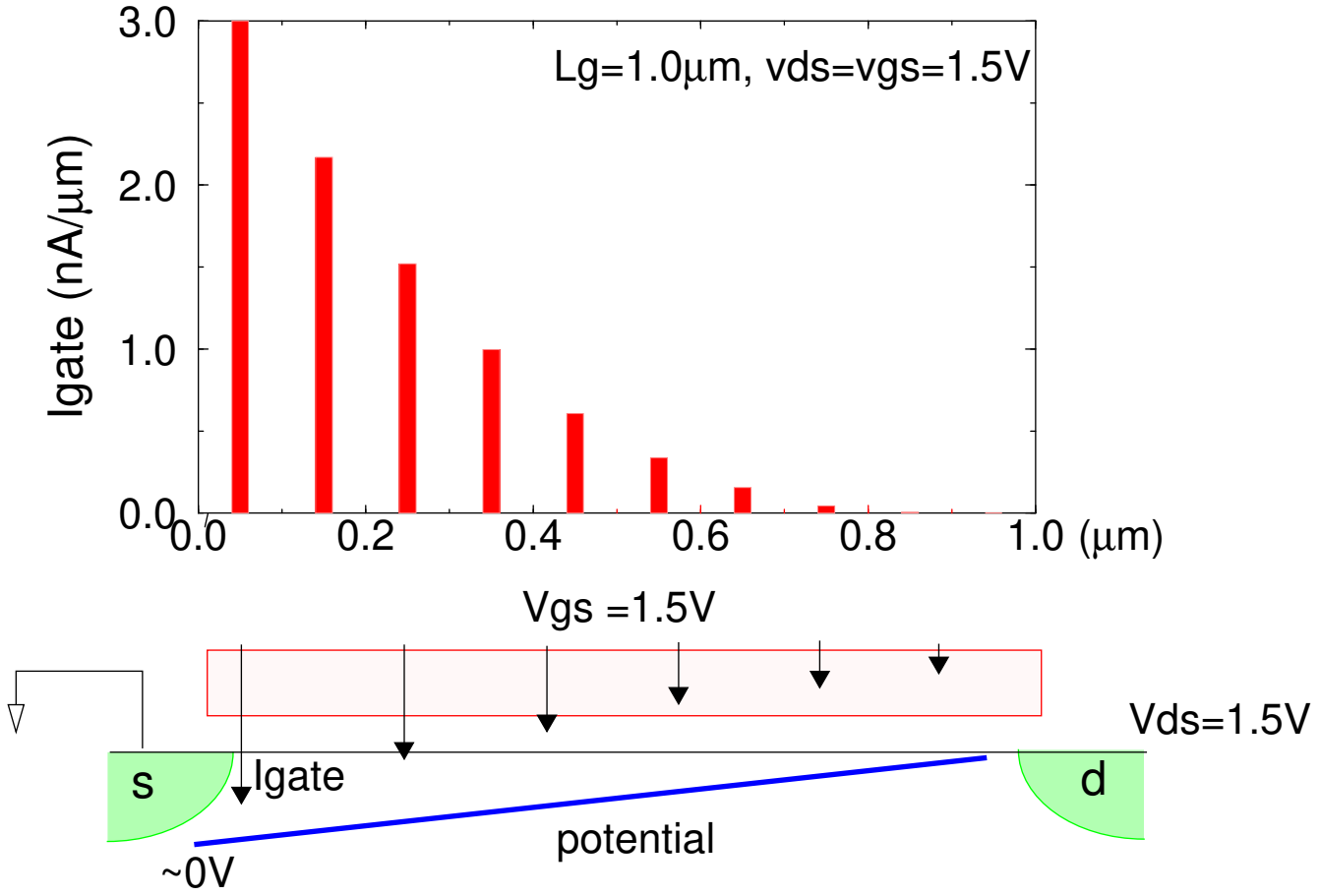
- Igate vs. Vds : Igate lower as Vds higher
- Igate vs. gate length : Igate decreases in proportion to $1/Lg^{1.5}$





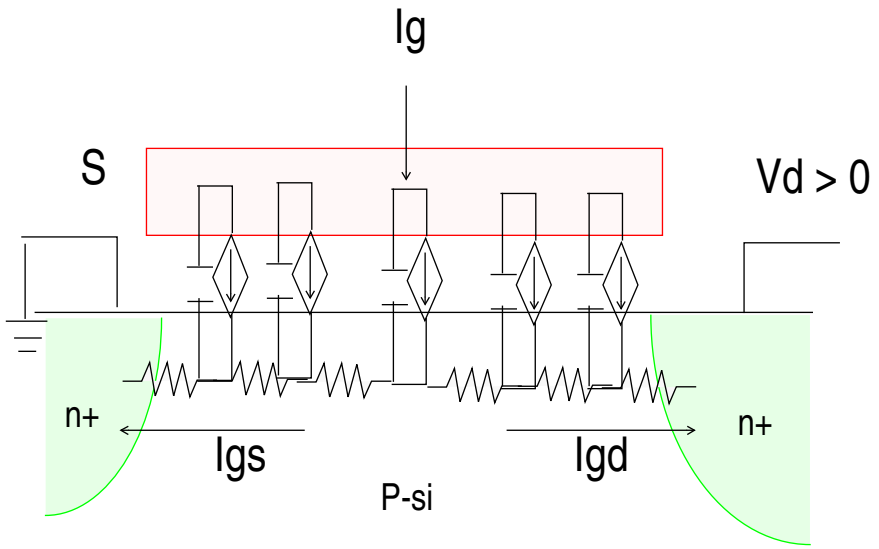
Igate modeling on MOS transistors : Result (I)

- Igate along the channel direction for Vds >0 - position dependent

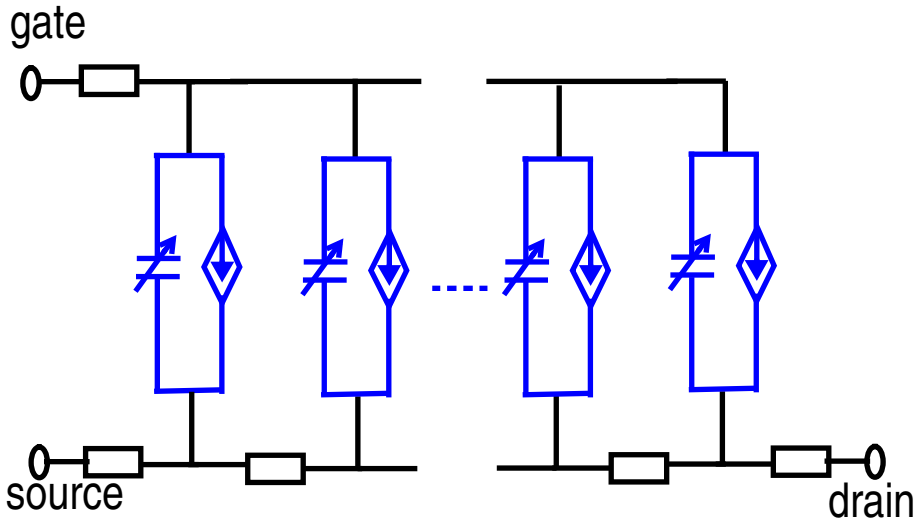


Igate modeling on MOS transistors

- Channel potential modeled by R_{ch}
- Different I_{gate} along channel directions for Vds > 0



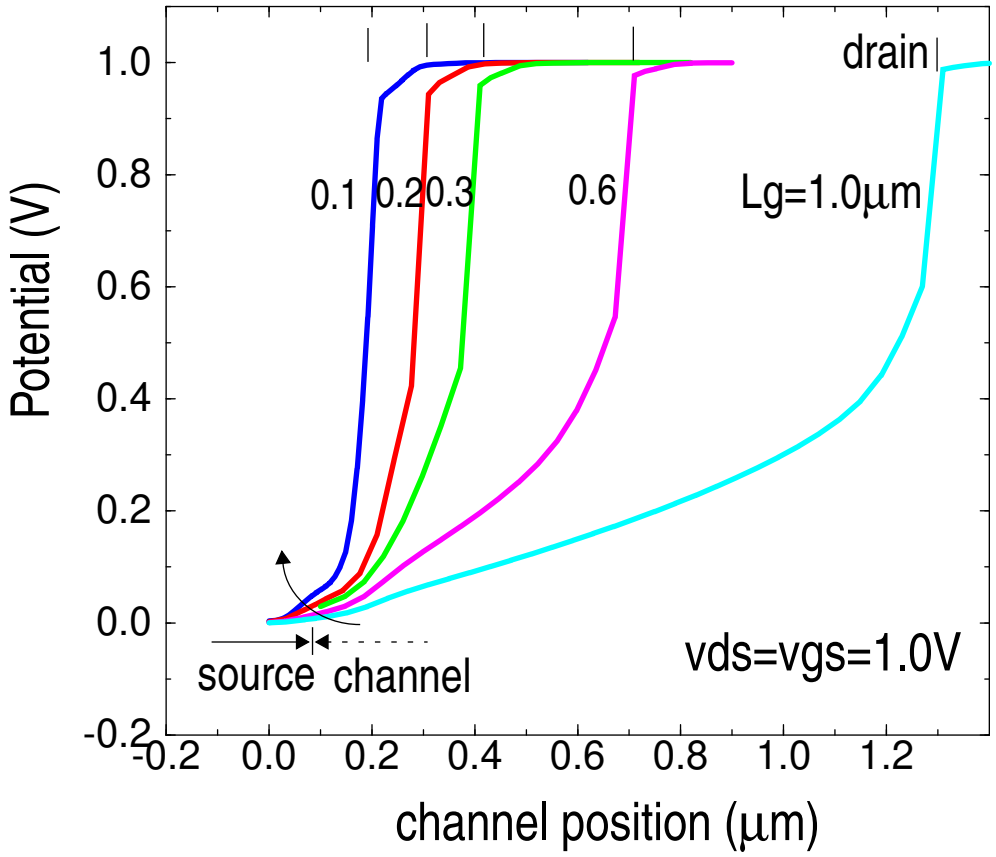
Ig = Igs + Igd



Equivalent circuit for Vds > 0

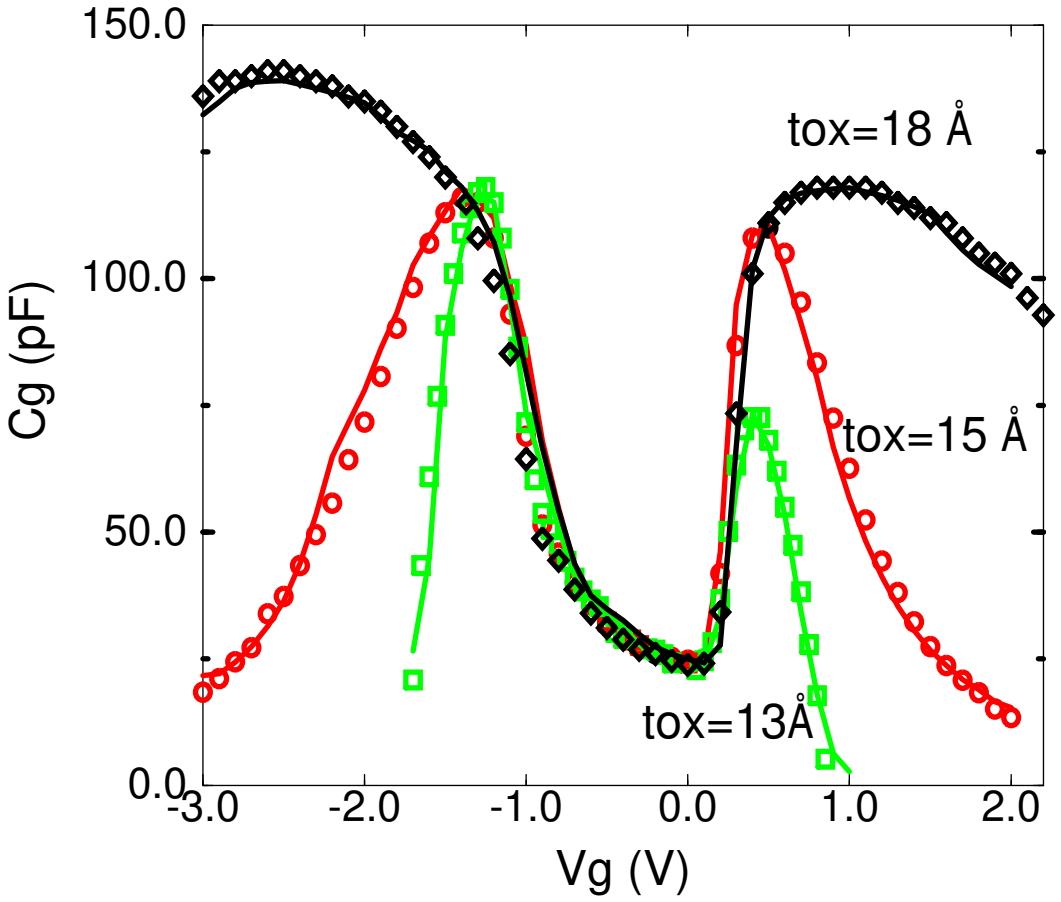
Gate current on MOS Transistors

- Drain bias effect, channel length dependence (DIBL)
- Potential at source increases as Lgate is shorter - lower I_{gate}



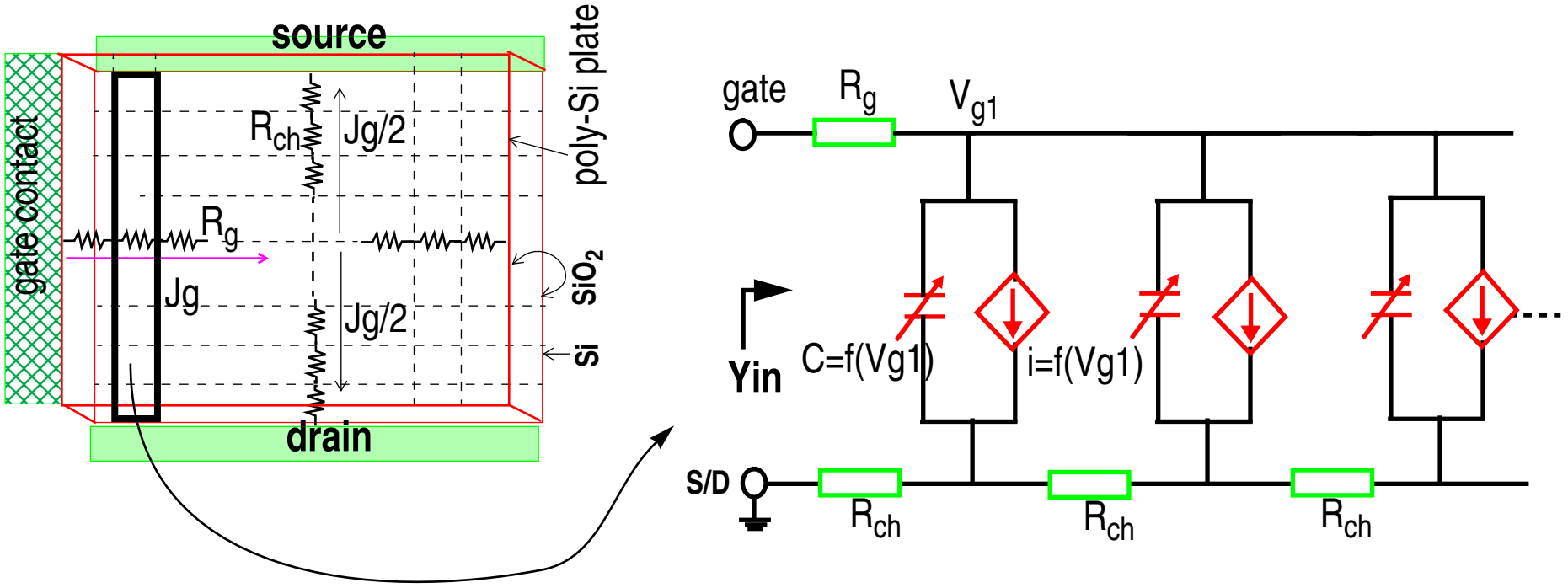
Equivalent RC circuit approach : results

- Good agreement between measured Cg and the imaginary part of Y_{in}
- R_{ch} ranges 1.1 K - 2.5 K Ω/sq. in accumulation and inversion region



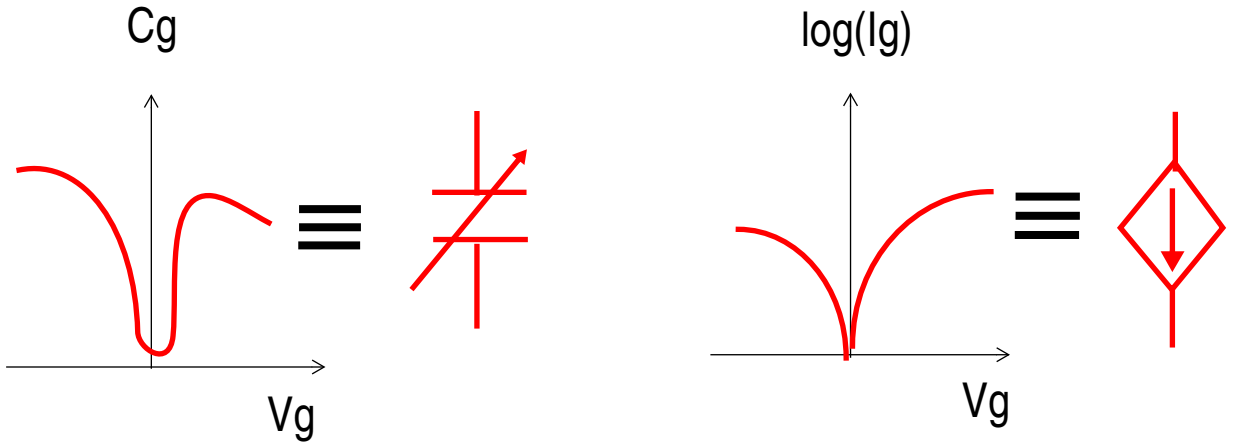
Equivalent RC circuit approach : application

- 20 RC ladder circuit, Rg= 5 Ω/sq., frequency=100 K Hz
- SPICE ac small-signal analysis to find input admittance ($Y_{in}=G + j\omega C$)



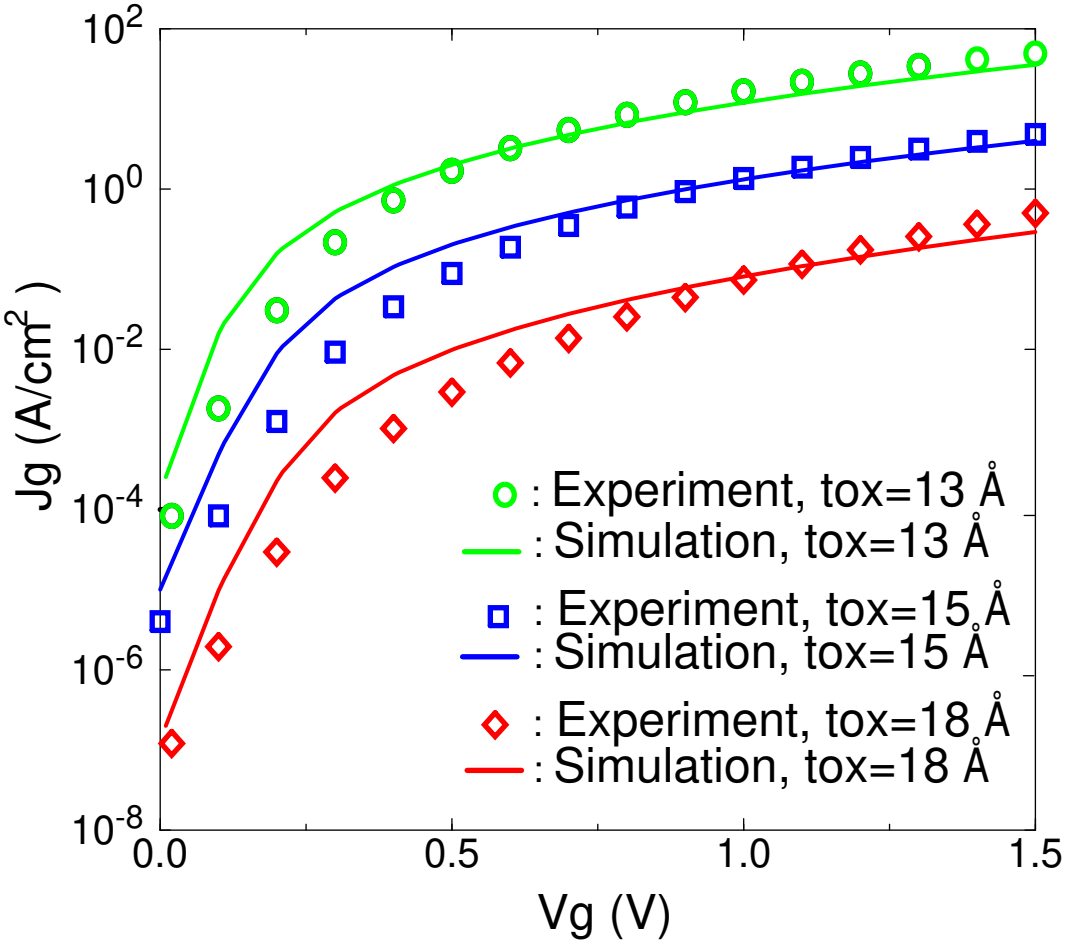
Equivalent RC circuit approach

- Equivalent RC ladder circuit model for NMOS capacitor with tox=13-18 Å
- Voltage dependent Capacitor for QM corrected capacitance model + Voltage dependent Current source for gate tunneling current effect (1D table data)
- Distributed RC modeling for poly-gate and channel resistance (Rg, Rch)



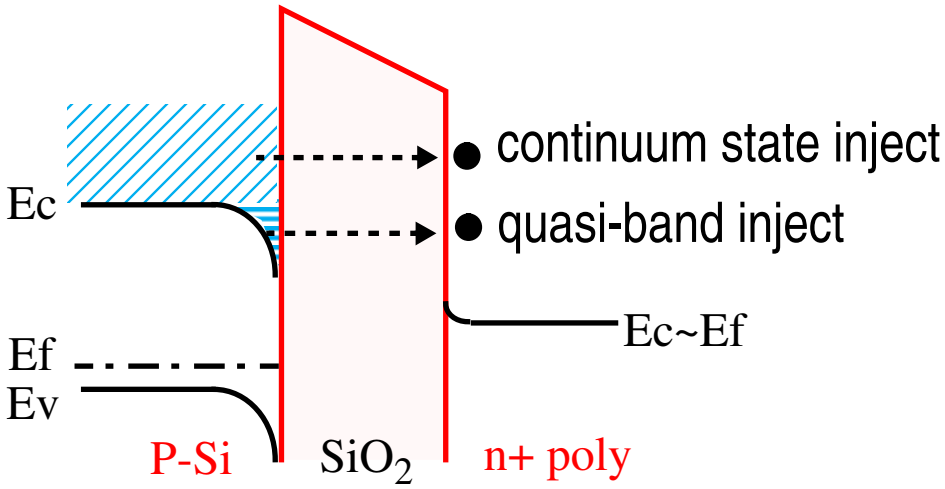
Gate Tunneling Current : application

- Gate tunneling current for NMOS capacitors, tox=13, 15 and 18 Å



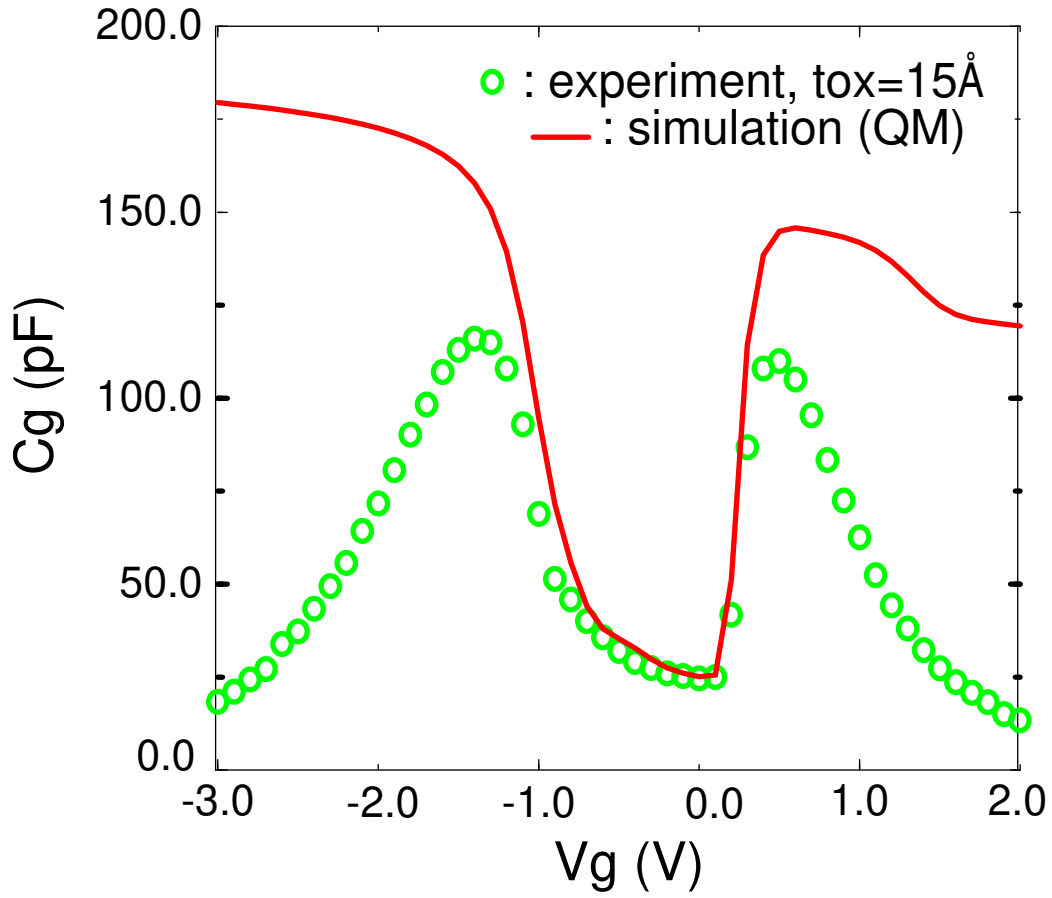
Gate Tunneling Current

- Tunneling current calculation using a 1D Green's Function simulator, NEMO
- Electrons in inversion layer are treated quantum mechanically
- Multi-scattering effect, injection from quasi-bound/continuum states and carrier density calculation



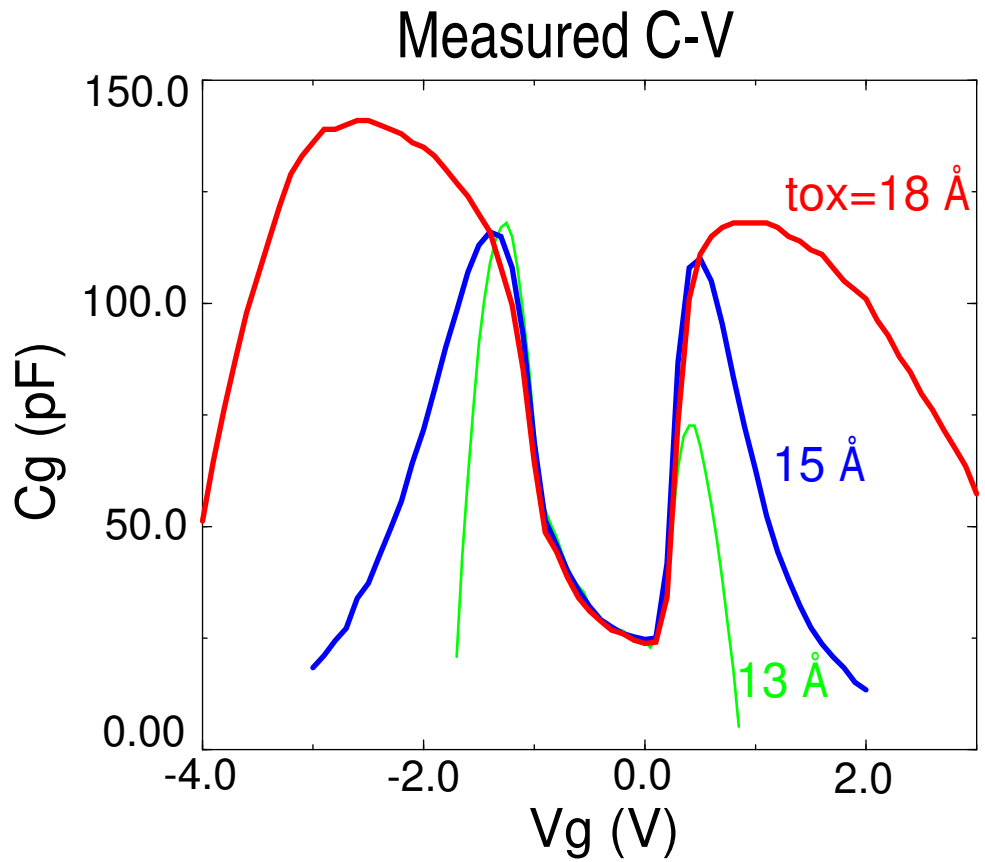
Need of tunneling current model

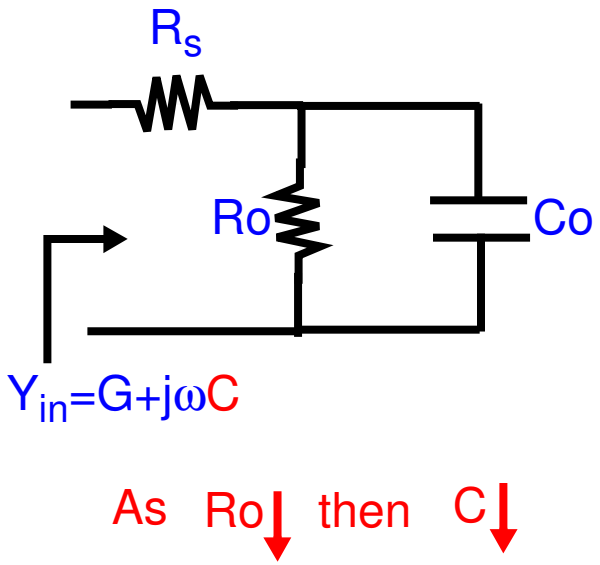
- QM correction only cannot predict C-V characteristics for tox =15 Å
- Need a gate tunneling current and resistance (R_s) model



New C-V behavior for tox < 20Å

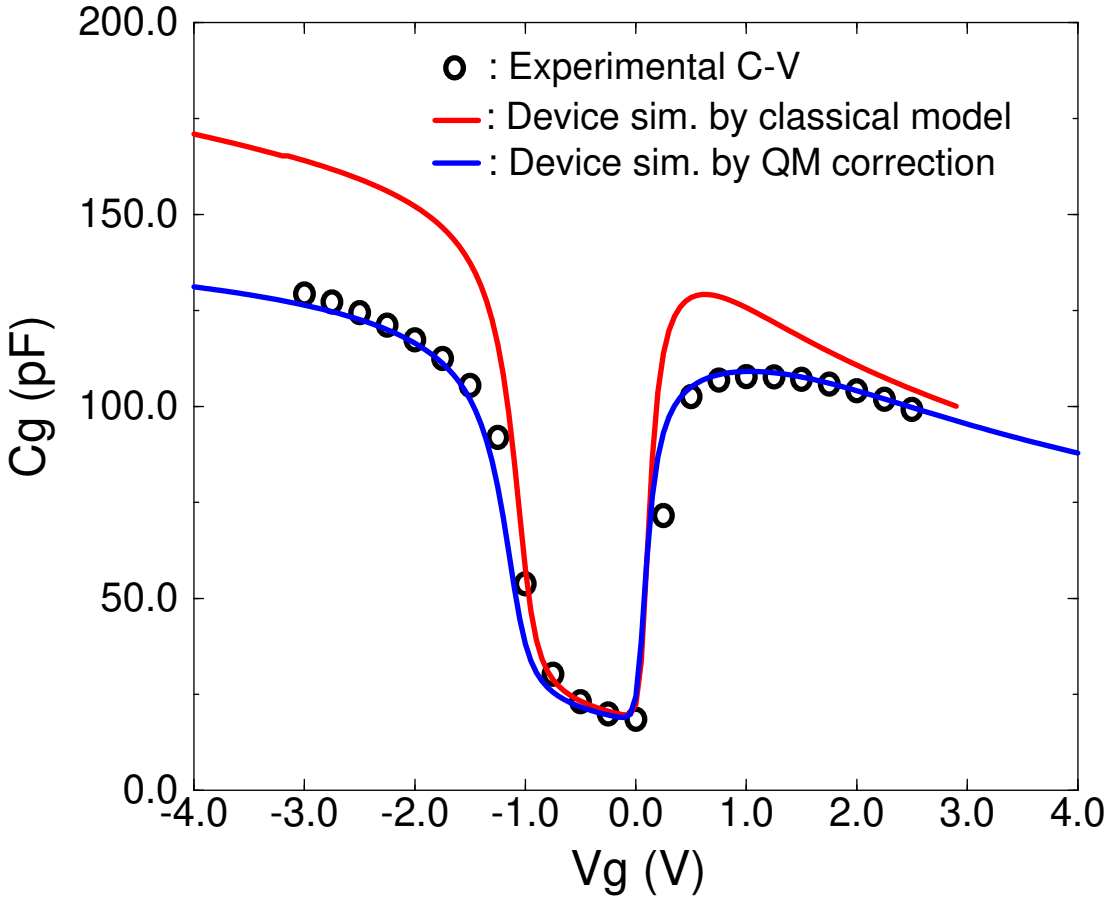
- Large gate leakage current by direct tunneling across two plates
- Sharp decrease of gate capacitance in accumulation / inversion regions due to I_{gate} and poly-gate/substrate resistance (R_s)





Capacitance Simulation by QM corrections

- NMOS capacitor with tox = 21 Å, area=100 μm x 100 μm
- Device simulation including poly-Si depletion & TED effects



QM Corrections

- Shift of carrier distribution

$$N_C(z) = N_C[1 - e^{-(z+z_0)^2/\lambda_{th}^2}]$$

N_C:the normal density of conduction band states

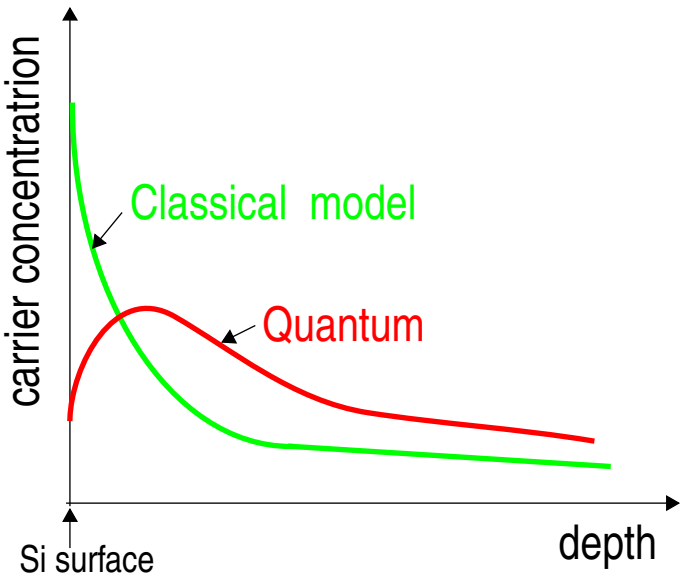
λ_{th} : thermal wavelength

- Bandgap broadening effect

$$\Delta E_g(z) = \frac{\kappa\beta}{2k_BT} \frac{F_S^2}{ae^{-(F_S/\sigma)^2} + F_S^{4/3}} \left[\frac{2e^{(z/L)^2}}{1 + e^{-2(z/L)^2}}\right]$$

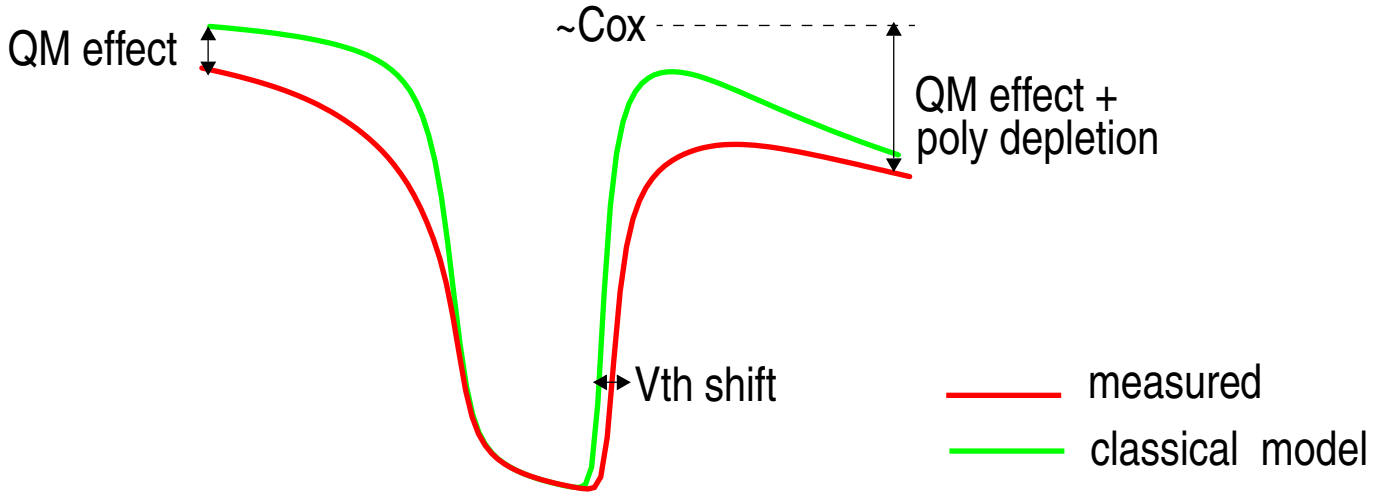
F_S : electric field

β, κ, a and σ are adjustable parameters



QM effects in C-V

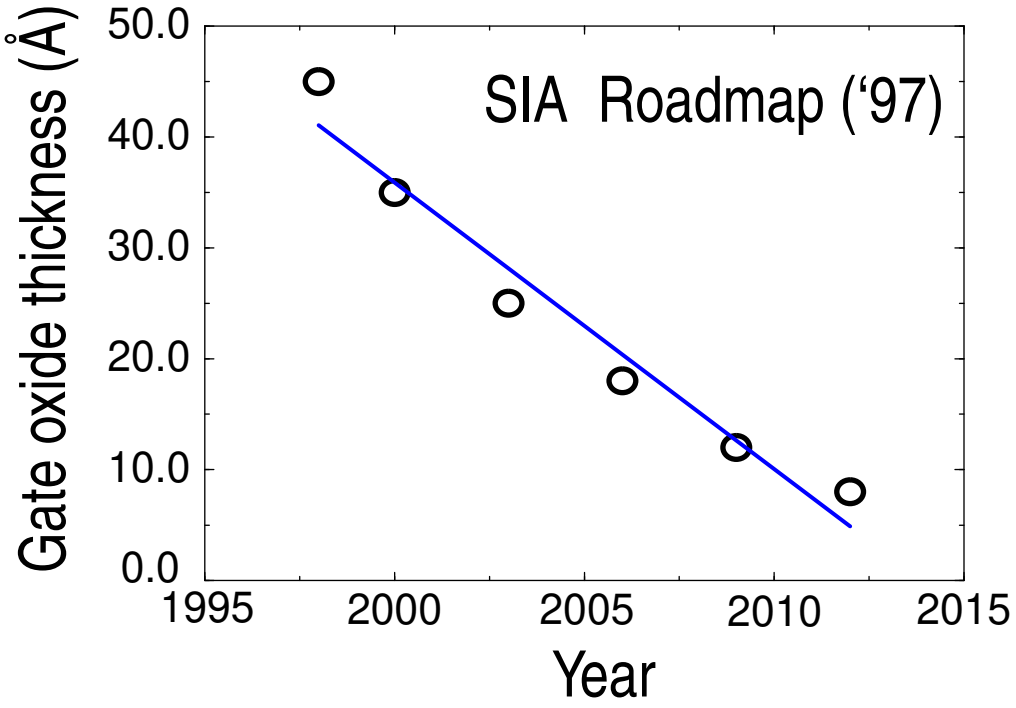
- QM effects : Shift of the carrier distribution from Si-SiO_2 surface
- Empirical and hybrid QM corrections implemented in 2D device simulator
- Modified van Dort model + Hansch model
- Evaluation of electron concentration by bandgap broadening mechanism



QM effects on ultrathin gate C-V

Motivation

- Modern CMOS with Lg=0.1μm requires tox < 30Å (Lg/tox=const.)
- Quantum Mechanical (QM) effects : loss of inversion charge, reduced gate capacitance and transconductance
- Direct tunneling - increase of gate leakage current and power dissipation
- Needs of characterization of thin gate MOS for the choice of design parameters



C-V and Gate Tunneling Current Characterization of Ultra-Thin Gate Oxide MOS (t_{ox} =1.3-1.8 nm)

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Zhiping Yu, and Robert W. Dutton

Center for Integrated Systems, Stanford University

Amr Bayoumi, Min Cao, Paul V. Voorde, and Dieter Vook

ULSI Lab, HP Labs, HP Co.