An Accurate and Efficient High Frequency Noise Simulation Technique for Deep Submicron MOSFETs

Jung-Suk Goo, *Student Member, IEEE*, Chang-Hoon Choi, *Student Member, IEEE*, François Danneville, *Member, IEEE*, Eiji Morifuji, *Member, IEEE*, Hisayo Sasaki Momose, *Senior Member, IEEE*, Zhiping Yu, *Senior Member, IEEE*, Hiroshi Iwai, *Fellow, IEEE*, Thomas H. Lee, *Member, IEEE*, and Robert W. Dutton, *Fellow, IEEE*

***Abstract*—Based on an active transmission line concept and two-dimensional (2-D) device simulations, an accurate and computationally efficient simulation technique for high frequency noise performance of MOSFETs is demonstrated. Using a Langevin stochastic source term model and small-signal equivalent circuit of the MOSFET, three intrinsic noise parameters (γ, δ, and c) for the drain noise and induced gate noise are calculated. Validity and error analysis for the simulation are discussed by comparing the simulation results with theoretical results as well as measured data.**

***Index Terms*—MOSFETs, semiconductor device modeling, semiconductor device noise, simulation.**

I. Introduction

THE IMPORTANCE of CMOS technology is increasing in radio frequency (RF) design applications owing to the promise of integrating electronic systems on a single silicon chip. Recent work has demonstrated the viability of CMOS low noise amplifiers (LNAs) [1] and mixers [2]; RF designs are increasingly taking advantage of CMOS technology.

Several studies have claimed that the fundamental noise performance of CMOS amplifiers would be limited by the noise sources of thermal origin, such as the excessive drain noise in the saturation region [3], [4] and the induced gate noise [1], [5] at radio frequencies. While complete broad band characterization and accurate modeling of the MOSFET noise are indispensable for future RF circuit designs, the noise behavior in short channel MOSFETs is not well understood.

Simulation of MOSFET noise can play an important role in realizing optimal CMOS RF circuit design by providing *a priori* noise performance metrics of devices and underlying technology issues. A very popular technique in device noise simulation is the *impedance field method* (IFM) [6] with *Langevin stochastic noise source*. Even though the IFM was theoretically extended up to three dimensions [7], [8], its practical application has been limited to one-dimensional (1-D) devices [9]. The 1-D simulation conveys simple and insightful results at reasonable computational cost; unfortunately, its accuracy is limited. Recently an alternative technique, using a 1-D Boltzmann transport equation, has been proposed to improve model accuracy for short channel MOSFETs [10]. Nevertheless, the primary weakness involves incorporation of two-dimensional (2-D) dependencies. This problem is particularly acute for state-of-the-art MOSFET technologies because of various second-order effects caused by complex processing such as new drain structures, gate overlap effects, nonuniform doping profiles in the substrate, etc. Hence, in conjunction with process simulation, the capability to exploit multidimensional device simulations to extract physical dependencies of noise is highly attractive.

Recently several studies have reported full 2-D noise simulation results implementing the IFM in a drift-diffusion (DD) based device simulator [11]–[13]. However, the unsatisfactory agreement with experimental data implies that the noise modeling of deep submicron MOSFETs requires not only multidimensional features but also higher order transport models to capture essential dispersive nonequilibrium effects [9], [13]. The problem is that the expansion to higher order moments in 2-D noise simulation requires substantially increased cost both for implementation and simulation. For example, the hydrodynamic (HD) formulation involves at least four times larger matrices [11] and to date has not been used for 2-D noise analysis.

Fortunately, the nature of the MOSFET provides an important clue that reconciles the tough requirements of MOSFET noise simulation with limited computational resources. The primary issue in understanding noise performance of FETs is the knowledge of the small-signal behavior [14]. Based on Shockley's theory [15], van der Ziel and Ero [16] have proposed a modeling approach that considers the FET as an active, distributed, nonuniform transmission line. This approach has been refined by Klaassen [17] and has provided basic insight into the behavior of FETs. Such an approach is based on the fact that small-signal transport in MOSFETs is a linear process confined to the shallow inversion layer. A recent simulation result [13] has shown that the noise contribution from the substrate is negligibly small; empirically our results support the same conclusion. On the other hand, once coupled equations converge in multi-dimensional simulation, the solution at each node contains structural information of the whole along with the underlying physics. Namely, the 2-D solutions of the substrate are redundant in

Manuscript received March 28, 2000; revised July 5, 2000. This study was initiated by DARPA under Contract Army-DABT63-94-C-0055 and supported by SRC under Contract 98-SJ-116. The review of the paper was arranged by Editor J. N. Hollenhorst.

J.-S. Goo, C. H. Choi, Z. Yu, T. H. Lee, and R. W. Dutton are with the Center for Integrated Systems, Stanford University, Stanford, CA 94305-4075 USA.

F. Danneville is with the Institut d'Electronique et de Microélectronique du Nord, University of Lille, 59652 Villeneuve d'Ascq Cedex, France.

E. Morifuji and H. S. Momose are with the ULSI Device Engineering Laboratory, Toshiba Corporation, Kawasaki 210, Japan.

H. Iwai is with ULSI Device Engineering Laboratory, Toshiba Corporation, Kawasaki 210, Japan, and also with Tokyo Institute of Technology, Yokohama 226, Japan.

Publisher Item Identifier S 0018-9383(00)10408-3.

0018–9383/00$10.00 © 2000 IEEE

the noise simulation of MOSFETs. Thus the transmission line analogy can incorporate the required second-order effects in noise analysis if accurate local information for the inversion layer is provided by multi-dimensional device simulators.

This paper presents a mixed approach for MOSFET noise modeling that combines a 1-D active transmission line model with a 2-D device simulation. Since this approach utilizes only a limited number of local solutions imported from the device simulator, it imposes neither extra simulation time nor more complexity in implementation, regardless of the carrier transport model.

This paper is constructed as follows: Section II offers the basic concept of the IFM and Langevin stochastic noise source and introduces practical concerns related to the implementation such as the impedance field formulation and device segmentation error. Then Section III explains how the noise simulation is actually implemented using a commercial device simulator. Finally, Section IV demonstrates noise simulation results for MOSFETs as well as comparisons to measured data using an industrial technology.

II. Basic Theory for Noise Calculation

A. Impedance Field Method

From the microscopic point of view, noise is due to local random events of the carriers, which produce fluctuations of carrier velocity or in their number. These local fluctuations can be modeled by a *Langevin stochastic source term* superimposed on the dc current or bias voltage. The resulting fluctuations propagate to the electrodes and produce noise at the terminal electrodes. The propagation is called the *impedance field* [9]. Usually the local noise source is represented by a current source, otherwise the noise voltage sources across different sections are correlated [8]. Then, depending on termination of the electrodes, the impedance field is given either by an impedance Z or a dimensionless factor A [14]. Since the primary interest of this paper is current representations for the drain and gate noise, the respective two electrodes should be short-circuited for ac analysis and the impedance fields should become dimensionless factors.

The basic concept of the IFM [8] is illustrated in Fig. 1. The current source i_n is the local noise source; i_d and i_g are short-circuited currents induced by i_n at the drain and gate electrodes, respectively. The noisy segment of a MOSFET in Fig. 1(a) can be modeled as a noiseless segment with a Norton generator representing the local fluctuation as shown in Fig. 1(b). Again it can be reconfigured as Fig. 1(c). If the spectral density of a noisy segment is given by S_{i_n}, its subsequent noise power spectral density at two electrodes and their cross correlation coefficient are given by:

$$S_{i_d} = |\Delta A_d|^2 S_{i_n} \tag{1}$$

$$S_{i_g} = |\Delta A_g|^2 S_{i_n} \tag{2}$$

$$S_{i_g i_d} = \Delta A_g \Delta A_d^* S_{i_n} \tag{3}$$

where $*$ denotes a complex conjugate; and,

$$\Delta A_d \triangleq \frac{i_d}{i_n} = [A_d(x) - A_d(x+\Delta x)] \tag{4}$$

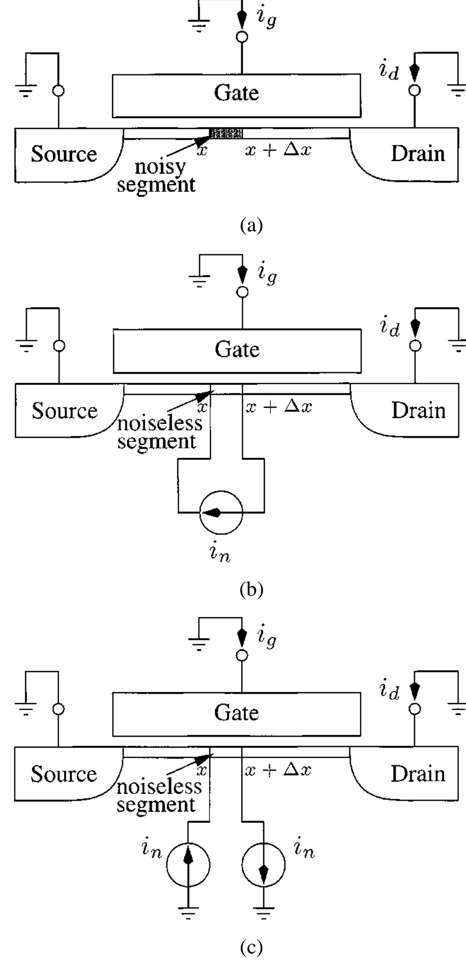


Fig. 1. Basic concept of the impedance field method. (a) Original device representation with a noisy segment. (b) Modified device representation based on the Langevin method. (c) Another modified device representation adopting the impedance field method.

$$\Delta A_g \triangleq \frac{i_g}{i_n} = [A_g(x) - A_g(x+\Delta x)] \tag{5}$$

Hence the total noise power spectral density and cross correlation coefficient for the entire MOSFET become simply the sum of the components for all segments.

B. Microscopic Noise Source

The dominant noise in MOSFETs is the velocity fluctuation noise and its local spectral density is given by [18]:

$$S_{i_n} = \frac{\overline{i_n^2}}{\Delta f} = 4q^2 n D_n \frac{\Delta y \Delta z}{\Delta x} = 4kT_n \frac{qn\mu_{\mathrm{ac}} \Delta y \Delta z}{\Delta x} \tag{6}$$

where

Δ	denotes a differential amount;
f	operating frequency;
q	electronic charge;
n	carrier density;
D_n	real part of the noise diffusion coefficient;
x	longitudinal dimension;
y	transverse dimension;
z	azimuthal dimension;

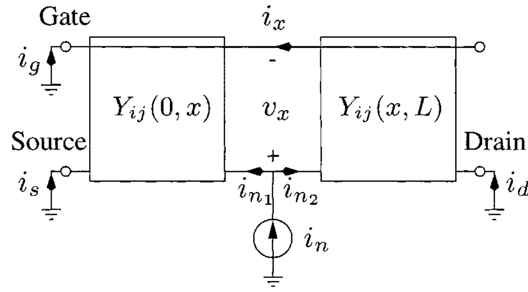


Fig. 2. Basic principle of the impedance field calculation. The MOSFET is divided into two subdevice blocks that are represented by two-port networks.

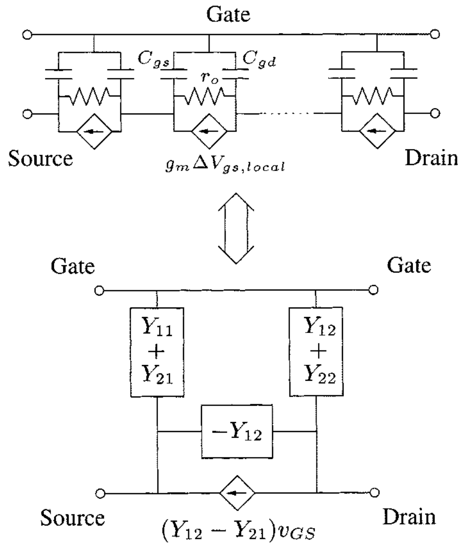


Fig. 3. Small-signal equivalent representation for a MOSFET at high frequency in a common-gate configuration.

- k Boltzmann's constant;
- T_n noise temperature;
- μ_{ac} ac mobility.

In comparison to the spreading diffusion coefficient (D_s), D_n has the same value at thermal equilibrium while its field ($\mathcal{E}$) or energy (E) dependancy is different in general. Although D_s may be used as an approximation of D_n [9], it would be questionable for MOSFETs beyond 0.1 μm where the ballistic transport assumes an important role.

C. Impedance Field Formulation

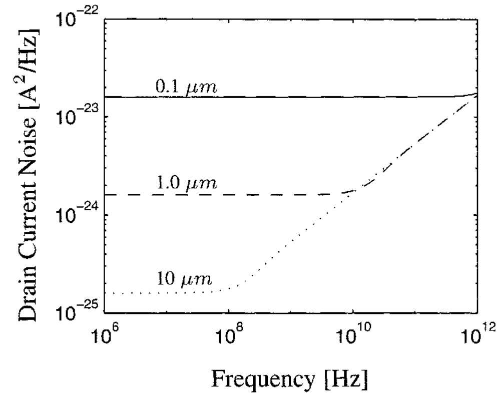
One of the key issues in our approach is how to formulate the dimensionless impedance field A. Fig. 2 shows a two-port network representing the MOSFET in a common-gate configuration and with a current source i_n added at x. Analysis for the given network gives (see the Appendix, Section A):

$$A_d(x) \triangleq \frac{i_d}{i_n} = \frac{Y_{21}(x, L)}{Y_{22}(0, x) + Y_{11}(x, L)} \tag{7}$$

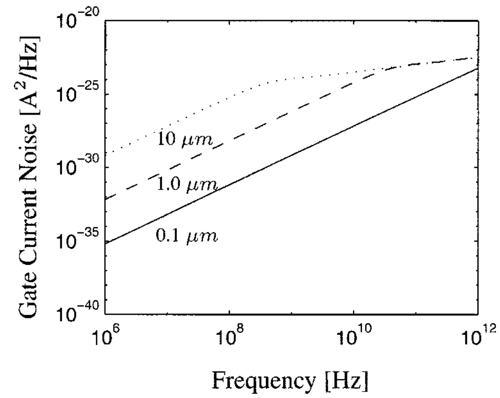
$$A_g(x) \triangleq \frac{i_g}{i_n} = -1 - \frac{Y_{12}(0, x) + Y_{21}(x, L)}{Y_{22}(0, x) + Y_{11}(x, L)}. \tag{8}$$

D. Network Analysis

To derive the network parameters Y_{ij}s at x, suppose a MOSFET is divided into n segments like Fig. 3. Each segment



(a)



(b)

Fig. 4. Frequency evolution of noise spectral power density terms for a uniform transmission line. (a) Drain current noise. (b) Gate current noise.

of the MOSFET can be represented by its localized small-signal circuit, which is commonly used in SPICE, where the following parameters are applicable.

- C_{gs} gate-to-source capacitance;
- C_{gd} gate-to-drain capacitance;
- r_o output resistance;
- g_m transconductance.

Then simple transformation (see Appendix, Section B) and matrix multiplication yield desired network parameters for the impedance field calculation.

E. Device Segmentation

An important question to be considered is how dense the segmentation should be. Although the MOSFET is a nonuniform transmission line under actual operating conditions, a uniform transmission line analysis can provide a crude idea about the segmentation issue. The MOSFET can be considered as a uniform transmission line only under zero drain bias. In such a case, we can derive the noise characteristic for an *assumption-free unsegmented* transmission line.

Fig. 4 shows the calculated noise power spectra for an *unsegmented* uniform transmission line (see Appendix, Section C). Contrasted to common circuit design assumptions [1], at very

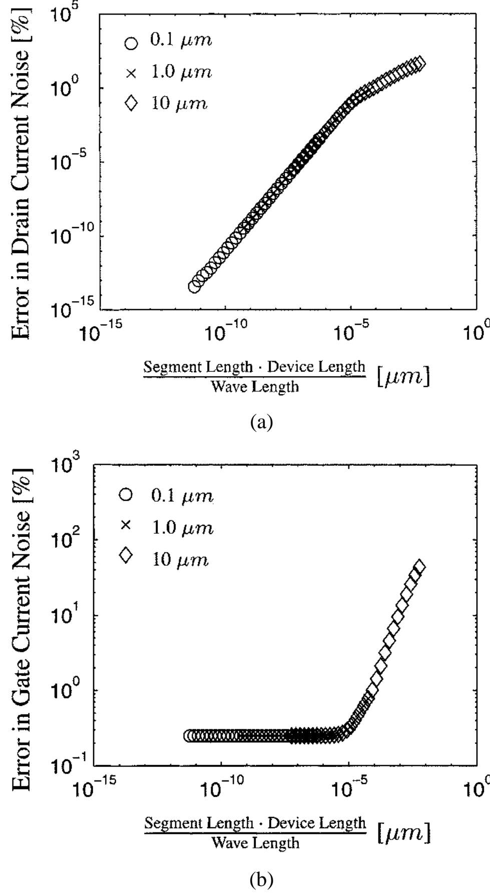


Fig. 5. Noise calculation error by segmentation for a uniform transmission line case. The MOSFETs are divided into 20 segments. (a) Error involved in drain current noise calculation. (b) Error involved in gate current noise calculation.

high frequencies, the drain noise has frequency dependence and the gate noise is not proportional to the square of the frequency. Obviously the correlation between drain noise and gate noise will also differ across this frequency range. Nevertheless, this would not be important in most practical situations because these changes take place in a range above the cutoff frequency (f_t).

To examine the segmentation limit, a segmented case has been compared with unsegmented results of Fig. 4. Fig. 5(a) and (b) respectively show the error in drain and gate noise calculation caused by segmentation for different sizes and frequencies. It is obvious that the smaller error is achieved by the denser segmentation and the smaller ratio of the device length to the wavelength. For example, to maintain an error of less than 1 percent, $(\Delta x L/\lambda)$ should be less than 10^{-5} μm, which corresponds to an upper frequency limit of 280 GHz for a 0.25 μm device divided into 20 segments. If the numbers of segment are 4 and 10, the lower limits of error are 6.2% and 1.0% respectively. Note that the number of segments imposes a lower limit on the error of gate noise calculation in Fig. 5(b) due to the distributed nature of the device. By comparing these indices to the average meshing distance of device simulators and the cutoff frequency of the 0.25 μm MOSFET (about 30 GHz in the actual operation region), we can conclude that the segmentation itself practically would not impose any limit.

III. Noise Simulator Implementation

A. Two-Dimensional Device Simulator

The proposed noise simulation method has been implemented as a postprocessor of MEDICI [19], a commercial 2-D numerical device simulator. MEDICI is in conjunction with TSUPREM4 [20], a commercial 2-D numerical process simulator, and equipped with field-dependent mobility models [21], [22]. The simulator also provides self-consistent solutions of carrier density, mobility, and carrier temperature based on the carrier-temperature-dependent mobility model, thermal diffusion current model, and carrier-temperature-based impact ionization model when the HD model [23] is selected.

B. Two-Dimensional to 1-D Transformation

The noise analysis of devices is based on ac sensitivity analysis. To take advantage of the 1-D transmission line analogy, we thus need to extract the 1-D ac equivalent circuit using 2-D solutions. Assuming local small-signal parameters are frequency independent, we mimicked the ac behavior using local perturbations of dc quantities acquired from three bias conditions: the desired bias ($[V_{DS}, V_{GS}]$) and two adjacent biases ($[V_{DS} + \Delta V_{DS}, V_{GS}]$ and $[V_{DS}, V_{GS} + \Delta V_{GS}]$). The same technique has been adopted in HELENA [25] and is known to be valid up to $2f_t$, which sets the applicable frequency limit of the proposed mixed approach.

The small-signal parameters associated with Fig. 3 are deduced as follows:

$$C_{gs} + C_{gd} = \frac{\Delta Q_{inv}}{\Delta V_{gs,\, local}} \tag{9}$$

$$r_o = \frac{\Delta V_{ds,\, local}}{\Delta I_{DS}} \tag{10}$$

$$g_m = \frac{\Delta I_{DS}}{\Delta V_{gs,\, local}} \tag{11}$$

where

Δ	denotes a differential quantity for different sets of bias;
Q_{inv}	sum of inversion charge in the channel;
$V_{gs,\, local}$	difference between the gate electrode potential and the local source potential;
$V_{ds,\, local}$	potential difference between the local drain potential and source potential;
I_{DS}	current at the drain electrode.

Note that changing V_{DS} affects not only $V_{ds,\, local}$ but also $V_{gs,\, local}$ and vice versa.

Fig. 6 illustrates how those local quantities are determined. The local potential has been obtained from the nodal quasi-Fermi level along the Si/SiO$_2$ interface; the inversion charge has been calculated by summing up the product of the nodal carrier density and its associated area along the y-direction. MEDICI uses the finite-box discretization method [24] with a triangular mesh structure. While MEDICI allows the irregular triangular mesh, only right-angled one was used in our implementation to simplify the summing up procedure for the inversion charge. The extracted 1-D small-signal equivalent circuit has been verified by comparing terminal characteristics of the

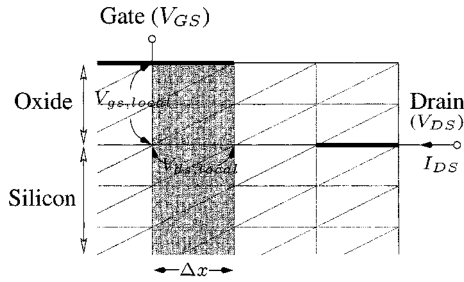


Fig. 6. Illustration for local quantity extraction from a 2-D device simulation result.

2-D device—capacitance, transconductance, and output resistance—to the first-order terms of Y_{ij}s deduced for the entire MOSFET as shown in Fig. 3.

C. Microscopic Noise Source Calculation

The local noise source has been approximated using the spreading diffusion coefficient. Since MEDICI implicitly assumes the Einstein relationship, the local noise spectrum can be obtained as follows:

$$S_{i_n} \approx 4kT_c \frac{qn\mu_{\mathrm{dc}}\Delta y \Delta z}{\Delta x} \tag{12}$$

$$\approx 4kT_c \frac{1}{R_{\mathrm{dc}}} = 4kT_c \frac{I_{DS}}{V_{ds,\,local}} \tag{13}$$

where

T_c carrier temperature;

μ_{dc} dc mobility;

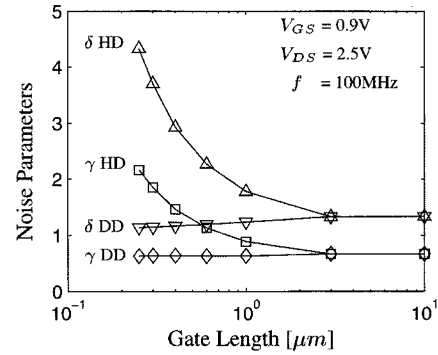
R_{dc} dc resistance of a segment.

We have assumed that a segment is a homogeneous resistor with the carrier temperature at the Si/SiO_2 interface since the inversion layer has only tens of angstroms in thickness and its temperature distribution is almost homogeneous. For a piece of silicon, this approximation successfully depicted the reported field dependence of diffusion coefficient [9]. For more precise simulation, D_n needs to be acquired through either Monte Carlo simulations [25] or experiments [9], as a function of the electric field or energy. Nevertheless, the above approximation causes a negligible error in the MOSFET noise calculation because, as to be discussed in Section IV, the actual contribution to the drain or gate noise is dominated by the source junction side where D_n is about the same to D_s.

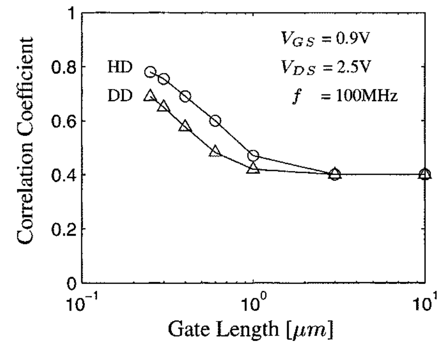
IV. Results

We have performed noise simulations of nMOSFETs from an industrial 0.25 μm CMOS process. No optimization was done except for the doping profile calibration process. The structure and doping of the device were directly imported from TSUPREM4 and all model parameters were kept at the default values in MEDICI simulations. Simulated dc characteristics showed good agreement with measured results for both the DD and HD transport models.

Using a classical noise theory as applied to circuit design, the white spectrum of drain current noise, blue spectrum of gate



(a)



(b)

Fig. 7. Gate length dependence of noise parameters comparing HD and DD model results. (a) γ and δ. (b) The imaginary part of c.

current noise, and their cross correlation coefficient are given by [26]

$$\overline{i_d^2} \triangleq 4kT\Delta f \gamma g_{d0} \tag{14}$$

$$\overline{i_g^2} \triangleq 4kT\Delta f \delta g_g \tag{15}$$

$$c \triangleq \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2}\,\overline{i_d^2}}} \tag{16}$$

where

γ and δ bias-dependent factors;

g_{d0} drain output conductance under zero drain bias;

g_g real part of the gate-to-source admittance; and

c cross correlation coefficient.

For long channel MOSFETs, γ satisfies the inequality $2/3 \leq \gamma \leq 1$. The value of 2/3 holds when the MOSFET is in the saturation region, and the value of one is valid when the drain bias is zero [18]. Also for long channel MOSFETs in saturation, δ and c are reportedly 4/3 and $j0.395$ [5]. As shown in Fig. 7(a) and (b), the long channel simulation results exhibit good agreement with the classical values, regardless of the transport model used in device simulation. Jindal [3] and Abidi [4] have reported increased values of γ in submicron nMOSFETs. As the channel length decreases, only the HD simulation results show gradual increases of γ and δ in Fig. 7(a). Both models yield increased correlation factor in Fig. 7(b) and it suggests that this would mitigate the impact of larger γ and δ on the noise figure. Some oscillatory behavior was observed in the bias dependence of HD results and may be caused by the numerical stability problem related to the HD model implemented in MEDICI.

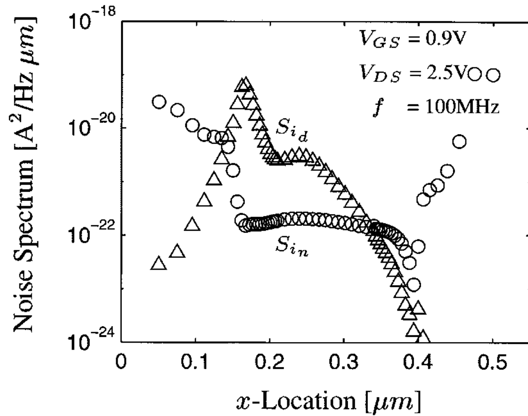


Fig. 8. Noise spectral density distribution of the local noise source (circles) and the its actual contribution to the drain noise (triangles) along the channel. The HD model was used.

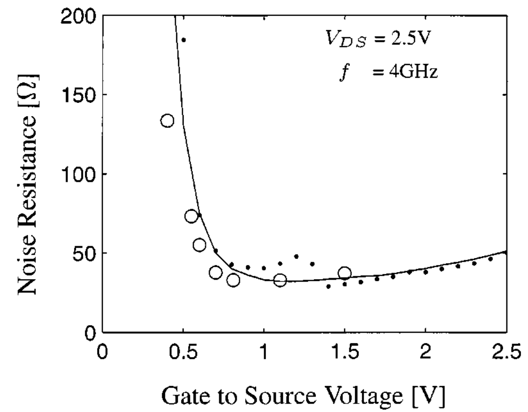


Fig. 9. Comparison of de-embedded measurement data (circles) to the simulated equivalent noise resistance (dots) for a 0.25 μm nMOSFET. Solid lines refer to smoothed simulation results of the HD model.

The HD simulation results in Fig. 8 compare the spectral density distribution of the local noise source with its actual contribution to the drain noise along the channel. Because the drain and gate noise are highly correlated, contributions to the gate noise show a similar distribution. The drain noise distribution justifies the approximated noise source given by (13) and also suggests that the increases of γ and δ in short channel MOSFETs are not due to carrier heating near the drain junction but due to the impedance field near the source junction. Namely, even if the local noise source is kept to the DD value, the HD impedance field still yields the same results. This contradicts recent MOSFET noise modeling approaches that have explained the behavior of γ and δ based on the hot carrier effects [27], [28]. Their primary problem is that voltage sources are used to represent the local fluctuations, assumed to be uncorrelated even though the local noise voltage sources are correlated, unlike the noise current sources [29], [30].

The approximated impedance field formulation suggests that the local ac resistance (r_o) is primarily responsible for the difference between two transport models in the impedance field. While the DD model determines the mobility based on the electric field, the HD model determines it based on the carrier energy whose changes in the device are not spatially synchronous with changes of the electric field. This phenomenon is called *nonlocal* nature of carrier transport and causes mobility deviating from the classical model. Unlike near the drain junction, the electric variation near the source junction is small enough that the HD model gives almost the same value of mobility but, due to the spatial nonlocal effect, the HD model exhibits a much smaller differential mobility and subsequently causes a higher local ac resistance and larger impedance field.

A 0.25 μm nMOSFET with $W = 200$ μm was measured using the ATN NP5B system [31] to examine the validity of the noise simulation. To compare the intrinsic part only, the pad loss [34] has been properly de-embedded by removing the parasitic components of the noise correlation admittance matrix from that of the total matrix as proposed by Morifuji *et al.* [35]. The de-embedding procedure is critical in performance measurements of intrinsic noise since the ac current path from the bonding pad, via the conductive substrate to the ground, causes a significant influence on measured $F_{\min}$, especially for silicon technology. Although the distributed resistance of the gate electrode [33] can cause increases in $F_{\min}$ and R_n, this contribution has been neglected because the gate electrode of the MOSFET was silicided and divided into 5 μm-width-fingers during layout. Finally the simulation results are transformed (see Appendix, Section D) from the noise power spectral density and their cross correlation coefficient based on the equivalent circuit in Fig. 3. The transformed intrinsic data for the DD model largely underestimates the noise performance, achieving less than half that of HD model in $F_{\min}$ and R_n. The HD case also shows some discrepancy in $F_{\min}$ and Y_{opt}, while R_n is in good agreement [36] as shown in Fig. 9. Since Y_{opt} is mainly determined by the small signal equivalent circuit of the MOSFET, which is verified using the current and capacitance of the device, a large discrepancy in Y_{opt} implies that the de-embedding procedure was not satisfactory. Large size MOSFETs inherently include *semi-intrinsic* components, also showing a dependence on the layout scheme employed. Because $F_{\min}$ is closely related to G_{opt}, correction of G_{opt} may improve agreement of simulated $F_{\min}$. In Fig. 10(a) and (b), an increase in G_{opt} by a factor of 1.7 is used in the transformation to fit model results with the measured G_{opt}; excellent agreement of $F_{\min}$ is then observed in both bias and frequency dependencies. The accuracy of intrinsic noise simulation is thus clearly satisfactory and it is possible to estimate circuit level noise performance, based on technology parameters contained in the simulation model.

V. Conclusion

An accurate and computationally efficient simulation technique for high frequency noise performance of deep submicron MOSFETs is proposed. This technique is based on an active transmission line concept but uses 2-D device simulation. The Langevin stochastic source term is introduced as a local noise source and the small-signal behavior of the MOSFET is represented by a cascaded two-port network characterized in a common gate configuration. Since the local static quantities required for noise calculation are imported from a 2-D numerical device simulator using advanced transport models, this technique is able to capture dispersive nonequilibrium effects and incorporate second-order effects caused by complex

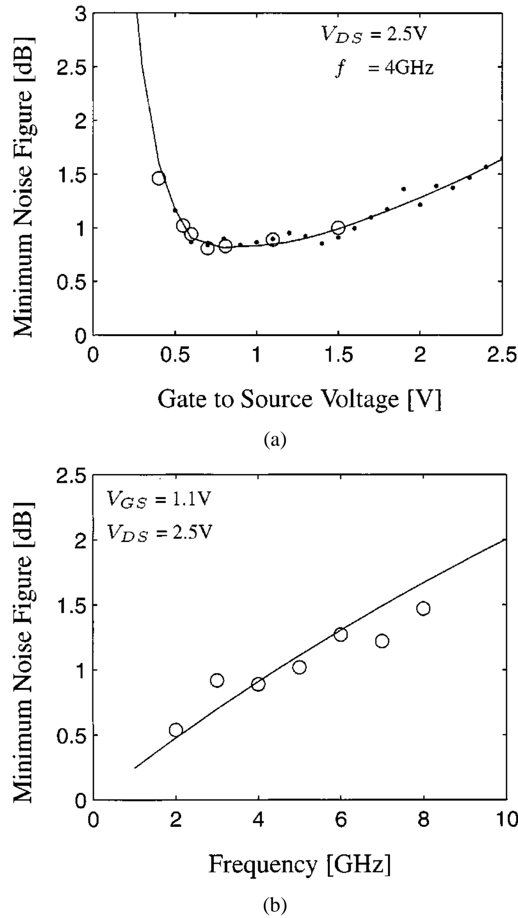


Fig. 10. Comparison of de-embedded measurement data (circles) to simulated minimum noise figures (dots) with correction for the loss due to G_{opt} for a 0.25 μm nMOSFET. Solid lines refer to smoothed simulation results of HD model. (a) Gate bias dependence. (b) Frequency dependence.

processing. Background of the proposed approach includes details of the impedance field formulation. Segmentation itself does not cause significant error in the noise calculations within a practical range of frequencies and meshing elements. The long channel noise simulation results are in good agreement with classical values; short channel results based on the HD model successfully describe the reported excess noise in short channel MOSFETs. The transformed simulation results of the HD model show excellent agreement with the de-embedded measurement data, both in bias and frequency dependencies, while the DD model largely underestimates the experimental results. This paper demonstrates and explains the importance of advanced (i.e., HD) transport models for 2-D noise analysis and also verifies the use of the model based on noise simulation results for deep submicron MOSFETs. The proposed simulation technique is accurate and fast enough for practical RF noise performance analysis of deep submicron MOSFETs.

APPENDIX

A. Impedance Field Formulation

As illustrated in Fig. 2, all electrodes are short-circuited to ground. The noise current i_n is divided into i_{n_1} and i_{n_2}, and subsequently induces v_x (voltage across the local node and gate node), i_x (current flows from the left to right blocks), and three short-circuited electrode currents (i_g, i_d, and i_s). Basic KCL conditions governing the network are

$$i_n = i_{n_1} + i_{n_2} \tag{17}$$

$$i_{n_1} + i_g + i_s + i_x = 0 \tag{18}$$

$$i_{n_2} + i_d - i_x = 0. \tag{19}$$

Simple two-port network analysis for the left block yields

$$v_x = \frac{i_{n_1}}{Y_{22}(0,\, x)} \tag{20}$$

$$i_s = Y_{12}(0,\, x) v_x \tag{21}$$

where the $Y_{ij}(0,\, x)$s are admittance parameters of the subdevice located between the source and equipotential line passing by x. Also, network analysis for the right block gives

$$v_x = \frac{i_{n_2}}{Y_{11}(x,\, L)} \tag{22}$$

$$i_d = Y_{21}(x,\, L) v_x \tag{23}$$

where $Y_{ij}(x,\, L)$s are admittance parameters of the subdevice located between the equipotential line passing by x and the drain. Then, combining (17)–(23) leads to impedance fields (7) and (8).

B. ABCD Matrix of the MOSFET

For a common-gate configuration

$$A = \frac{1 + j\omega r_o C_{gd}}{1 + g_m r_o} \tag{24}$$

$$B = \frac{r_o}{1 + g_m r_o} \tag{25}$$

$$C = -\frac{\omega^2 r_o C_{gs} C_{gd}}{1 + g_m r_o} + \frac{j\omega[C_{gs} + (1 + g_m r_o) C_{gd}]}{1 + g_m r_o} \tag{26}$$

$$D = \frac{1 + g_m r_o + j\omega r_o C_{gs}}{1 + g_m r_o} \tag{27}$$

where $j = \sqrt{-1}$ and $\omega = 2\pi f$.

C. Unsegmented MOSFET Noise Spectra

When L is the channel length, $R_{channel}$ is the channel resistance, and C_{OX} is the total oxide capacitance, the characteristic properties are

$$\gamma_p = (1 + j)\sqrt{\frac{\omega R_{channel} C_{OX}}{2L^2}} \triangleq \alpha + j\beta \tag{28}$$

$$Z_0 = (1 - j)\sqrt{\frac{R_{channel}}{\omega C_{OX}}} \tag{29}$$

where

γ_p propagation constant whose real and imaginary parts;
α and β attenuation constant and phase constant of the line, respectively;
Z_0 characteristic impedance of the line.

Then the required network parameters for the impedance field calculation are easily derived, as follows:

$$Y_{12}(0, x) = -\frac{1}{Z_0 \sinh \gamma_p x} \tag{30}$$

$$Y_{22}(0, x) = \frac{\cosh \gamma_p x}{Z_0 \sinh \gamma_p x} \tag{31}$$

$$Y_{11}(x, L) = \frac{\cosh \gamma_p (L-x)}{Z_0 \sinh \gamma_p (L-x)} \tag{32}$$

$$Y_{21}(x, L) = -\frac{1}{Z_0 \sinh \gamma_p (L-x)}. \tag{33}$$

Thus the terminal noise power spectral density terms and their cross correlation coefficient are

$$S_{i_d} = K_0 K_d \tag{34}$$

$$S_{i_g} = K_0 K_g \tag{35}$$

$$S_{i_g i_d} = K_0 K_{gd} \tag{36}$$

where

$$K_0 = 4kT_n \frac{L}{R_{channel}} \left| \frac{\gamma_p}{\sinh \gamma_p L} \right|^2 \tag{37}$$

$$K_d = \int_0^L |\cosh \gamma_p x|^2 \, dx = \frac{\alpha \sin 2\beta L + \beta \sinh 2\alpha L}{4\alpha\beta} \tag{38}$$

$$K_g = \int_0^L |\cosh \gamma_p x - \cosh \gamma_p (L-x)|^2 \, dx = \frac{(\cos \beta L - \cosh \alpha L)(\alpha \sin \beta L - \beta \sinh \alpha L)}{\alpha\beta} \tag{39}$$

$$K_{gd} = \int_0^L [\cosh \gamma_p x - \cosh \gamma_p (L-x)] \cosh \gamma_p^* x \, dx = \frac{(\cos \beta L - \cosh \alpha L)(\alpha \sin \beta L - \beta \sinh \alpha L)}{2\alpha\beta}. \tag{40}$$

D. Transformation of Noise Parameters

$$F_{\min} = 1 + 2R_n (G_{opt} + G_c) \tag{41}$$

$$R_n = |B|^2 \frac{\overline{i_d^2}}{4kT\Delta f} \tag{42}$$

$$G_{opt} = \sqrt{\frac{G_u}{R_n} + G_c^2} \tag{43}$$

$$B_{opt} = -B_c \tag{44}$$

where

$$Y_c = \frac{D}{B} + \frac{c}{B} \sqrt{\frac{\overline{i_g^2}}{\overline{i_d^2}}} \tag{45}$$

$$G_u = (1 - |c|^2) \frac{\overline{i_g^2}}{4kT\Delta f} \tag{46}$$

$$B = \frac{1}{Y_{21} + Y_{22}} \tag{47}$$

$$D = \frac{Y_{11} + Y_{12}}{Y_{21} + Y_{22}} + 1. \tag{48}$$

Note that $ABCD$ parameters are for a common source configuration while Y_{ij}s are for a common gate one.

ACKNOWLEDGMENT

The authors would like to thank Prof. M. Lundstrom and Prof. A. Abramo for helpful discussions concerning transport models. Special thanks go to Dr. M. Mierzwinski of Hewlett-Packard EEsof for promoting and mentoring this project.

REFERENCES

[1] D. K. Shaeffer and T. H. Lee, "A 1.5 V, 1.5 GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, p. 745, May 1997.
[2] A. N. Karanicolas, "A 2.7-V 900-MHz CMOS LNA and mixer," *IEEE J. Solid-State Circuits*, vol. 31, p. 1939, Dec. 1996.
[3] R. P. Jindal, "Hot-electron effects on channel thermal noise in fine-line NMOS field-effect transistors," *IEEE Trans. Electron Devices*, vol. 33, p. 1395, Sept. 1986.
[4] A. A. Abidi, "High-frequency noise measurements on FET's with small dimensions," *IEEE Trans. Electron Devices*, vol. 33, p. 1801, Nov. 1986.
[5] A. van der Ziel, *Solid State Physical Electronics*. Englewood Cliffs, NJ: Prentice-Hall, 1976.
[6] W. Shockley, J. A. Copeland, and R. P. James, "The impedance field method of noise calculation in active semiconductor devices," in *Quantum Theory of Atoms, Molecules and the Solid-State*. New York: Academic, 1966, p. 537.
[7] K. M. van Vliet, "General transport theory of noise in PN junction-like devices—I: Three-dimensional Green's function formulation," *Solid-State Electron.*, vol. 15, p. 1033, 1972.
[8] K. M. van Vliet, A. Friedmann, R. J. J. Zijlstra, A. Gisolf, and A. van der Ziel, "Noise in single injection diodes—I: A survey of methods," *J. Appl. Phys.*, vol. 46, no. 4, p. 1804, Apr. 1975.
[9] J.-P. Nougier, "Fluctuations and noise of hot carriers in semiconductor materials and devices," *IEEE Trans. Electron Devices*, vol. 41, p. 2034, Nov. 1994.
[10] L. M. Franca-Neto, E. Mao, and J. S. Harris Jr., "Low noise FET design for wireless communications," in *IEDM Tech. Dig.*, Dec. 1997, p. 305.
[11] F. Bonani, M. R. Pinto, R. K. Smith, and G. Ghione, "An efficient approach to multi-dimensional impedance field noise simulation of bipolar devices," in *Proc. 13th Int. Conf. Noise in Physical Systems and $1/f$ Noise*, Singapore, 1995, p. 379.
[12] F. Bonani, G. Ghione, M. R. Pinto, and R. K. Smith, "An efficient approach to noise analysis through multidimensional physics-based models," *IEEE Trans. Electron Devices*, vol. 45, p. 261, Jan. 1998.
[13] S. Donati *et al.*, "Physics-based RF noise modeling of submicron MOSFETs," in *IEDM Tech. Dig.*, Dec. 1998, p. 81.
[14] A. Cappy and W. Heinrich, "High-frequency FET noise performance: A new approach," *IEEE Trans. Electron Devices*, vol. 36, p. 403, Feb. 1989.
[15] W. Shockley, "A unipolar field effect transistor," *Proc. Inst. Radio Eng.*, vol. 40, no. 11, p. 1365, Nov. 1952.
[16] A. van der Ziel and J. W. Ero, "Small-signal, high-frequency theory of field-effect transistors," *IEEE Trans. Electron Devices*, vol. ED-11, p. 128, Apr. 1964.
[17] F. M. Klaassen, "High frequency noise of the junction field-effect transistor," *IEEE Trans. Electron Devices*, vol. ED-14, p. 368, July 1967.
[18] A. van der Ziel, *Noise in Solid State Devices and Circuits*. New York: Wiley, 1986, ch. 5.
[19] . Avant! Corp. [Online]http://www.avanticorp.com/Avant!/SolutionsProducts/Products/Item/1,1172,39,00.html
[20] . Avant! Corp. [Online]http://www.avanticorp.com/Avant!/SolutionsProducts/Products/Item/1,1172,38,00.html
[21] D. M. Caughey and R. E. Thomas, "Carrier mobilities in silicon empirically related to doping and field," *Proc. IEEE*, vol. 55, p. 2192, 1967.
[22] K. Yamaguchi, "A mobility model for carriers in the MOS inversion layer," *IEEE Trans. Electron Devices*, vol. ED-30, p. 658, June 1983.
[23] B. Meinerzhagen and W. L. Engl, "The influence of the thermal equilibrium approximation on the accuracy of classical two-dimensional numerical modeling of silicon submicrometer MOS transistors," *IEEE Trans. Electron Devices*, vol. 35, p. 689, May 1988.

[24] R. S. Varga, *Matrix Iterative Analysis*, 1st ed. Englewood Cliffs, NJ: Prentice-Hall, 1962.
[25] H. Happy *et al.*, “HELENA: A friendly software for calculating the DC, AC, and noise performance of HEMTs,” *Int. J. Microwave and Millimeter-Wave Computer-Aided Engineering*, vol. 3, p. 14, Jan. 1993.
[26] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 1st ed. New York: Cambridge Univ. Press, 1998, ch. 11.
[27] D. P. Triantis, A. N. Birbas, and D. Kondis, “Thermal noise modeling for short-channel MOSFET’s,” *IEEE Trans. Electron Devices*, vol. 43, p. 1950, Nov. 1996.
[28] C. H. Chen and M. J. Deen, “High frequency noise of MOSFET’s I modeling,” *Solid-State Electron.*, vol. 42, p. 2069, Nov. 1998.
[29] K. M. van Vliet, “Markov approach to density fluctuations due to transport and scattering—II: Applications,” *J. Math. Phys.*, vol. 12, p. 1998, Sept. 1971.
[30] K. K. Thornber, “Some consequences of spatial correlation on noise calculations,” *Solid-State Electron.*, vol. 17, p. 95, Jan. 1974.
[31] ATN Microwave, Inc.. [Online]http://www.atn-microwave.com/device/np.html
[32] H. Rothe and W. Dahlke, “Theory of noisy fourpoles,” *Proc. Inst. Radio Eng.*, vol. 44, p. 811, June 1956.
[33] R. P. Jindal, “Noise associated with distributed resistance of MOSFET gate structures in integrated circuits,” *IEEE Trans. Electron Devices*, vol. 31, p. 1505, Oct. 1984.
[34] C. E. Biber *et al.*, “Technology independent degradation of minimum noise figure due to pad parasitics,” in *IEEE MTT-S Int. Microwave Symp. Dig.*, Baltimore, MD, June 1998, p. 145.
[35] E. Morifuji *et al.*, “RF noise study of small gate width Si-MOSFET’s up to 8 GHz application for low power consumption,” in *Ext. Abs. Int. Conf. Solid State Devices and Materials*, Hiroshima, Japan, Aug. 1998, p. 80.
[36] J.-S. Goo *et al.*, “RF noise simulation for submicron MOSFET’s based on hydrodynamic model,” in *Proc. Symp. VLSI Technology*, Kyoto, Japan, Jun. 1999, p. 153.

Jung-Suk Goo (S’97) was born in Seoul, Korea, in 1966. He received the B.S. degree in electrical engineering from Yonsei University, Seoul, Korea, in 1988, and the M.S. degree in electrical engineering from Stanford University, Stanford, CA, in 1997. He is currently working toward the Ph.D. degree at Stanford University.

From 1988 to 1989, he was with GoldStar Semiconductor, Co., Korea, involved in EPROM and 4M DRAM projects. And then he was with LG Semicon, Co., Korea, until 1995. During this period, he was engaged in next generation DRAM development such as 64 M and 256 M, and also was involved in a Flash memory project. His primary research areas were DRAM process development, device evaluation, and reliability modeling, in particular the hot carrier effect. He has authored and co-authored approximately 20 journal and conference papers and holds six U.S. patents. His current research interests are CMOS low noise amplifier design and high-frequency MOSFET noise modeling.

Chang-Hoon Choi (S’97) received the B.S. and M.S. degrees in electronic engineering from Sogang University, Seoul, Korea, in 1988 and 1990, respectively. He is currently pursuing the Ph.D. degree in electrical engineering at Stanford University, Stanford, CA.

From January 1990 to May 1997, he was with Samsung Electronics Co., Ltd., Kyungki-Do, Korea, where he was engaged in modeling and simulation on the IC circuits, devices, and TCAD. His research interests include characterization, modeling, and simulation of processes/devices for future CMOS generations.

Mr. Choi is a member of the IEEE Electron Device Society and has served as a reviewer for IEEE TRANSACTIONS ON ELECTRON DEVICES. He is listed in *Who’s Who in the World*.

François Danneville (M’98) was born in Ham, France, on March 16, 1964. He received the Ph.D. degree from the Centre Hyperfréquences et Semiconducteurs, University of Lille, France, in 1991.

He is currently an Assistant Professor with the Institut d’Electronique et de Microélectronique du Nord (IEMN), University of Lille. His main research interests are concerned with noise modeling in devices under linear and nonlinear operation for applications in the centimeter- and millimeter-wave ranges. He has been invited as Visitor in Hewlett-Packard EEsof Division, Santa Rosa, CA, working on the investigation of improved CAD noise models of devices for linear and nonlinear circuit simulation.

Eiji Morifuji (M’98) was born in Aichi, Japan, on December 20, 1970. He received the B.E. and M.E. degrees in electrical engineering from University of Tokyo, Tokyo, Japan, in 1993 and 1995, respectively.

He joined Toshiba Corporation, Yokohama, Japan, in 1995, and he has been engaged in the research and development of advanced analog and logic devices at the company’s Microelectronics Engineering Laboratories, Kawasaki, Japan.

Mr. Morifuji is a member of IEEE Electron Devices Society and the Japanese Society of Applied Physics.

Hisayo Sasaki Momose (M’94–SM’00) was born in Gifu, Japan. She received the M.S. degree in Chemistry from Ochanomizu Women’s University, Tokyo, Japan in 1984.

In 1984, she joined the Semiconductor Device Engineering Laboratory of Toshiba Corporation in Kawasaki, Japan, where she engaged in the development of static RAM and CMOS/Bi-CMOS logic devices and the research of hot-carrier reliability of CMOS and BiCMOS devices. In 1989, she joined the ULSI Research Center of Toshiba Corporation, where she engaged in the development of logic and analog CMOS devices and researched small-geometry CMOS with nitrided oxide gate and 1.5 nm oxide gate. Since 2000, she has been with System LSI Research & Development Center, Toshiba Corporation, Yokohama, Japan. She is now working on the research and development of CMOS analog devices

Ms. Momose is a member of the Electrochemical Society and the Japan Society of Applied Physics.

Zhiping Yu (SM’90) received the B.S. degree from Tsinghua University, Beijing, China, in 1967, and the M.S. and Ph.D. degrees from Stanford University, Stanford, CA, in 1980, and 1985, respectively.

He is presently a Senior Research Scientist with the Department of Electrical Engineering, Stanford University, and also holds a full professorship in Tsinghua University. His research interests focus on IC process, device, and circuit simulation, and in particular, the numerical techniques and modeling of RF and heterostructure devices. He has been involved in efforts to develop a simulation package for optoelectronic devices and 3-D solid modeling for ICs. Besides the full time university research, he is a consultant to Hewlett-Packard Computer System and Technology Laboratory, developing advanced transport models for subquarter-micron CMOS technology, including quantum mechanical effects.

Dr. Yu is currently serving as the Associate Editor of IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN responsible for TCAD related field.

Hiroshi Iwai (F'97) was born in Tokyo, Japan, on April 25, 1949. He received the B.E. and Ph.D. degrees in electrical engineering from the University of Tokyo, in 1972 and 1992, respectively.

In 1973, he joined the Research and Development Center of Toshiba Corporation, Kawasaki, Japan, where he developed the first generation of Toshiba's NMOS LSI technology. From 1978 to 1980, he was also associated with NEC-Toshiba Information Systems, Inc., Kawasaki. From 1979 to 1989, he was with the Semiconductor Device Engineering Laboratory in the Semiconductor Group of Toshiba. In 1983 and 1984, he worked with Prof. R. W. Dutton at the Integrated Circuit Laboratory, Stanford University, Stanford, CA, as a Visiting Scholar, where he studied small-geometry effects of MOSFET capacitances. From 1989 to 1996, he was associated with the ULSI Research Laboratories in the Research and Development Center of Toshiba. From 1997 to March 1999, he was a Chief Specialist of Microelectronics Engineering Laboratories of Toshiba. Since April 1999, he has been a Professor in the Department of Advanced Applied Electronics, Interdisciplinary Graduate School of Science and Technology, Tokyo Institute of Technology, Nagatsuta, Yokohama, Japan. Since joining Toshiba, he has developed several generations of high density static RAMs, dynamic RAMs, and logic LSIs including CMOS, bipolar, and bi-CMOS devices. He has also been engaged in research on device physics, process technologies, and T-CAD related to small-geometry MOSFETs and high speed bipolar transistors. His research area covers wide range; isolation scaling analysis, deep ion-implanted channel doping technique, on-chip capacitance measurement technique, two-dimensional process and device simulation, small geometry MOSFET capacitance analysis, rapid thermal process, silicides technique, interconnects technique, nitrided oxide gate insulator technique, p+polysilicon gate MOSFETs, polysilicon emitter technique, BiCMOS process, hot carrier effects on small geometry MOS and bipolar transistors, bias temperature tests of MOSFETs, charge pumping measurement technique, mechanical stress analysis of trench isolation, Ti-, Ni, Co-silicide technique, 40-nm gate length MOSFETs and 1.5-nm thick direct tunneling gate oxide MOSFE's, RF CMOS technologies, and so on. He has authored and co-authored more than 200 papers. His current research interests are downsizing of CMOS, high K gate insulator, ultra-shallow junction, and RF silicon technologies for mobile telecommunication.

Dr. Iwai has served on many committees of conferences and as editor of many journals. He was elected member of the IEEE EDS AdCom, served as an editor of *IEEE EDS Newsletter*, a Guest Editor of IEEE TRANSACTIONS. ON ELECTRON DEVICES, and an editor of the Proceedings of ECS Symposium on ULSI Process Integration. His awards include Local Commendation for Invention from Japan Institute of Invention and Innovation (1990); Grand Prize of Nikkei BP Technology Awards (1994); IEEE EDS Paul Rappaport Award (1994); and the IEICE ES Electronics Award (1998). He is a member of Electrochemical Society, the Japan Society Applied Physics, the Institute of Electronics, Information and Communication Engineers of Japan, and the Institute of Electrical Engineers of Japan.

Thomas H. Lee (M'87) received the S.B., S.M., and Sc.D. degrees in electrical engineering, all from the Massachusetts Institute of Technology, Cambridge, in 1983, 1985, and 1990, respectively.

He joined Analog Devices in 1990, where he was primarily engaged in the design of high-speed clock recovery devices. In 1992, he joined Rambus Inc., Mountain View, CA where he developed high-speed analog circuitry for 500 megabyte/s CMOS DRAMs. He has also contributed to the development of PLLs in the StrongARM, Alpha, and K6/K7 microprocessors. Since 1994, he has been an Assistant Professor of Electrical Engineering at Stanford University, Stanford, CA, where his research focus has been on gigahertz-speed wireline and wireless integrated circuits built in conventional silicon technologies, particularly CMOS. He is the author of *The Design of CMOS Radio-Frequency Integrated Circuits* (Cambridge, U.K.: Cambridge University Press, 1998), and is a co-author of two additional books on RF circuit design. He is also a co-founder of Matrix Semiconductor. He holds 12 U.S. patents.

Dr. Lee has twice received the Best Paper Award at the International Solid-State Circuits Conference, and was co-author of a Best Student Paper at ISSCC. He recently won a Packard Foundation Fellowship. He is a Distinguished Lecturer of the IEEE Solid-State Circuits Society, and was recently named a Distinguished Microwave Lecturer.

Robert W. Dutton (S'67–M'70–SM'80–F'84) received the B.S., M.S., and Ph.D. degrees from the University of California, Berkeley, in 1966, 1967, and 1970, respectively.

He is Professor of Electrical Engineering at Stanford University and Director of Research in the Center for Integrated Systems. He has held Summer staff positions at Fairchild, Bell Telephone Laboratories, Hewlett-Packard, IBM Research, and Matsushita during 1967, 1973, 1975, 1977, and 1988, respectively. His research interests focus on IC process, device, and circuit technologies—especially the use of computer-aided designand parallel computational methods. He has published more than 200 journal articles and graduated more than four dozen doctorate students.

Dr. Dutton was Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN (1984–1986). He was a Guest Editor of the October 2000 special issue of IEEE TRANSACTIONS ON ELECTRON DEVICES on computational electronics. He was winner of the 1987 IEEE J. J. Ebers Award and the 1988 Guggenheim Fellowship to study in Japan. He was elected to the National Academy of Engineering in 1991, and was awarded the Jack A. Morton Award for 1996.