ESD Simulation to Find Correlation Between Junction Depth and Snapback Slope Using 0.35μm LDD MOSFETS

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Abstract

*This paper studies the correlation between junction depth and snapback slope of AMD's 0.35*μm *LDD nMOS using TMA's 2D device simulator Medici. By modifying the effective gate length and substrate doping next to the junctions to keep them the same for all junction depths and holding all the other parameters constant, the junction depths of the LDD and deep source/drain junctions are varied. As the junction depths (LDD and deep junction) are increased from 0.08*μ*m and 0.10*μ*m to 0.15*μ*m and 0.20*μ*m incrementally, the snapback slope also increases respectively. Further simulations and experiments are proposed to pinpoint the underlying mechanism.*

I. Introduction

Typically the design of ESD protection is a trial-and-error procedure in which several variations of a circuit are fabricated and tested on a simple pass/fail basis. This approach is not only costly and time consuming, but it also does not facilitate the evolution of protection circuits in future technologies. A better design methodology includes a more complex testing technique in order to provide a better understanding of the functionality of the various components making up the circuit. In addition to a sophisticated testing technique, proper modeling can aid the design of an optimum protection circuit, and help to predict the performance of similar circuits in future technologies. Two-dimensional numerical device simulation have made the modeling of ESD events possible [1]. For example, simulations of a MOSFET structure can be used to provide the understanding of the physics involved during snapback and second breakdown. Moreover, by varying process and layout parameters of the MOSFET, simulations will also reveal the dependences of critical device characteristics on these parameters, which can be adjusted for better ESD protection[1]. This paper examines the dependence between the junction depth (Xj) and snapback slope (1/R) using TMA's Medici.

II. Simulation Process

A MOSFET with the configuration shown in Fig. 1 is often used as a part of the ESD protection circuit. During ESD stress, as a large positive discharge pulse is applied to the drain of the grounded gate nMOS, the transistor goes into avalanche followed by snapback, which is a parasitic bipolar action. Once in snapback mode, the nMOS can be used to clamp voltages and discharge currents[2]. Fig. 2 shows a typical I-V curve for an nMOS with gate and source at 0V. The first breakdown voltage ($V_{t1,}$ also called the avalanche breakdown voltage) depends on the junction curvature and depth, and it should be designed to have the smallest breakdown voltage so that it will breakdown first to protect the internal circuitry from breaking down. Then the nMOS goes into snapback, which clamps the voltage at V_h. During snapback mode, it is important that V_h is lower than the power supply so that the nMOS can discharge large amounts of current away from the internal circuitry. As the current increases further, a second breakdown voltage occurs at V_{t2} and I_{t2}. The mechanism of the second breakdown has been the focus of much research, and it is hard to model because of its thermal feedback nature. In order to better control the snapback behavior, the relationship between the junction depth and snapback slope is investigated. A 2D LDD nMOS is constructed from 1D doping profile and Suprem4 output of AMD's 0.35μm LDD nMOS.

Since the junction depths of the LDD and deep junctions are the only parameters to be changed, it is important to keep the other parameters constant. Varying junction depths mainly change the effective gate length and the amount of the substrate doping next to the junctions, so these parameters are adjusted for each junction depth to maintain the same for all junction depths. The size of the gate mask is changed in order to keep the effective gate length the same. Different grids are generated to ensure the output does not change with grid density. TMA's 2D numerical simulator Medici is used to simulate the resulting snapback curves. Figure 4 plots out the snapback slope as the junction depth is increased from 0.08μm and 0.10μm to 0.15μm and 0.20μm respectively.

III. Results and Discussion

As shown in Figure 4, the snapback slope (1/R) does increase as the junction depths increases, providing a way of controlling snapback slope. This correlation can also be used to fit the simulated snapback slope to the experimental curve by changing the junction depth of the simulation deck.

However, this simulation result need to be verified further. More grids need to be generated to ensure that the results does not depend on grid density. Also, test structures needs to be fabricated to verify the simulation results. To generate the experimental I-V curves, Transmission Line Pulsing (TLP) method should be used to measure the test sructures[1]. If the correlation is verified experimentally, more simulations and experiments need to be conducted to explain this situation.

IV. Acknowledgments

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References

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2. A. Amerasekera, et. al., IEEE Transactions on Electron Devices, Vol. 38, No. 9, pp 2161-8, Sep. 1991.

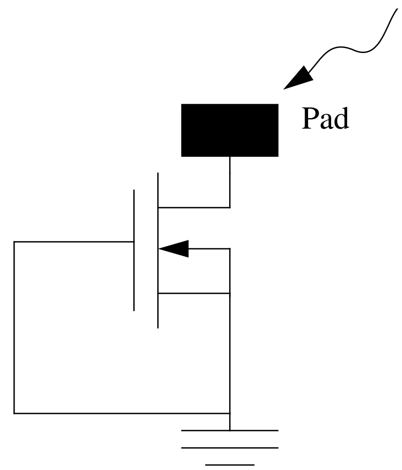

Figure 1. Schematic of nMOS as a protection circuit

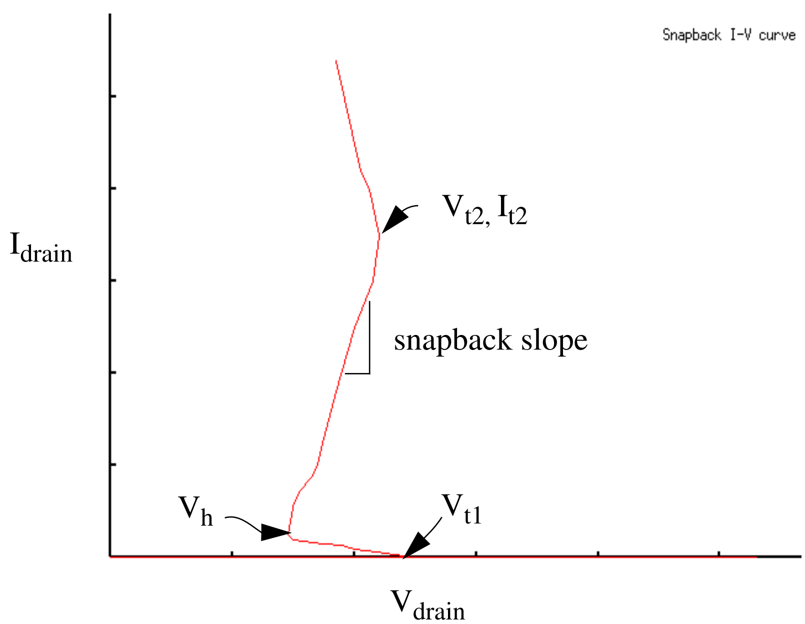

Figure 2. The I-V curve of the circuit in Fig. 1 under ESD
. stress (high drain voltage)

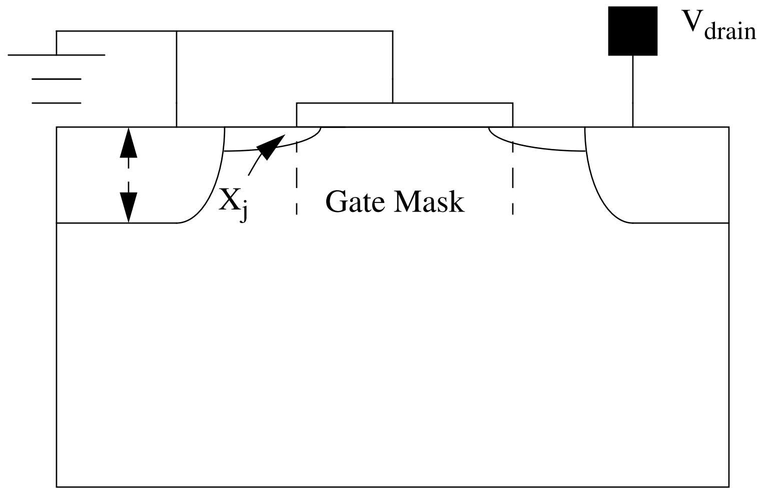

Figure 3. The cross section of the simulated LDD nMOS with varying junction depth gate mask to adjust for effective gate length

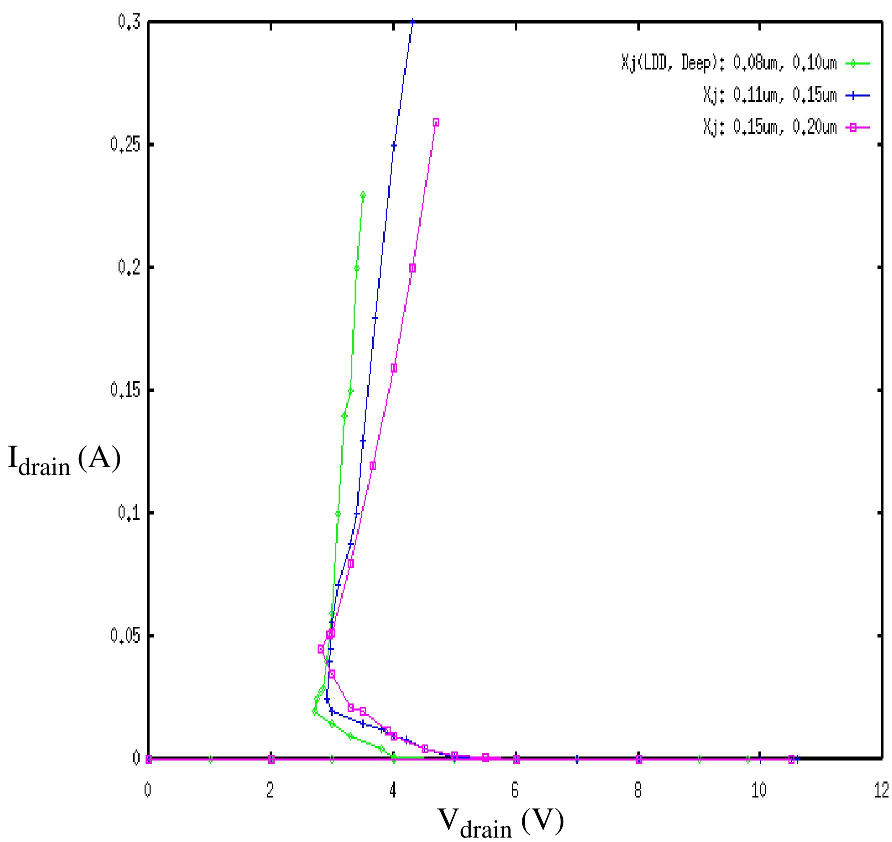

Figure 4. The plot of the snapback slopes corresponding to each junction depth