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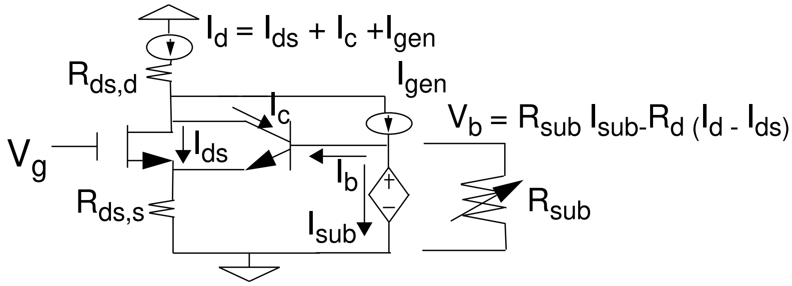

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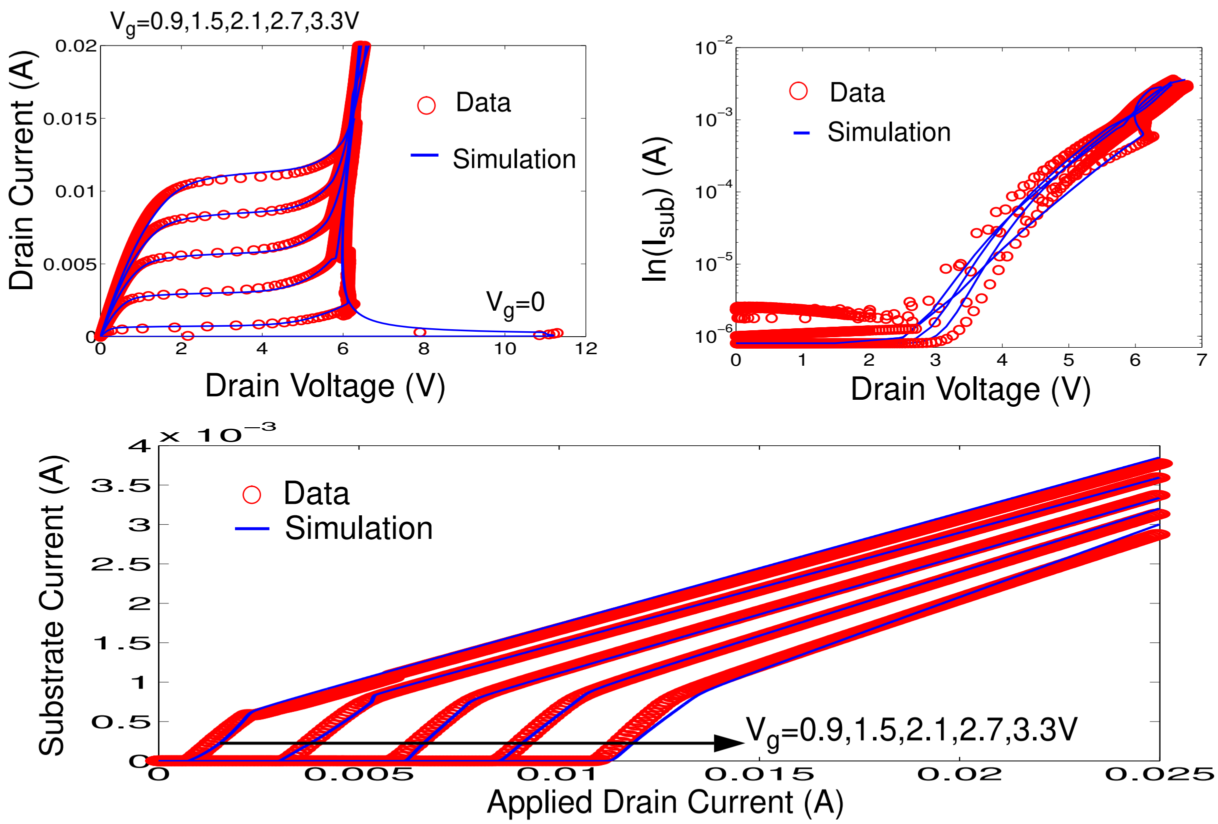

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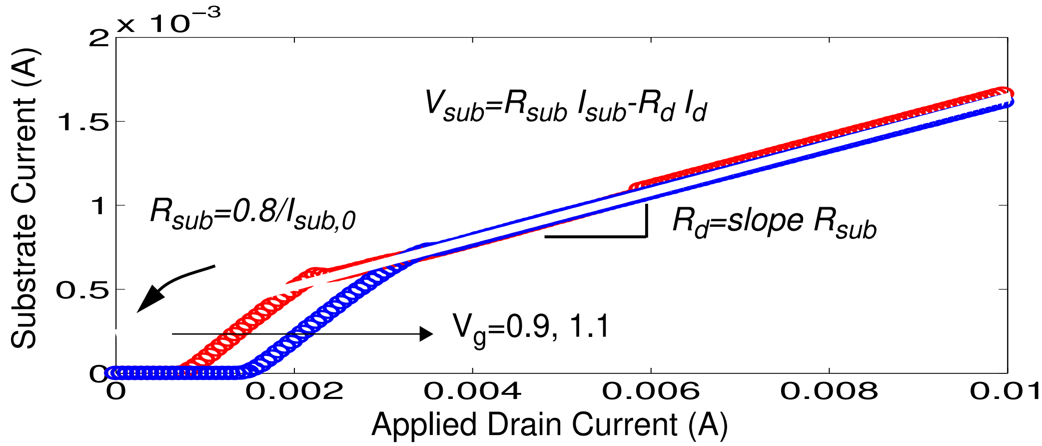

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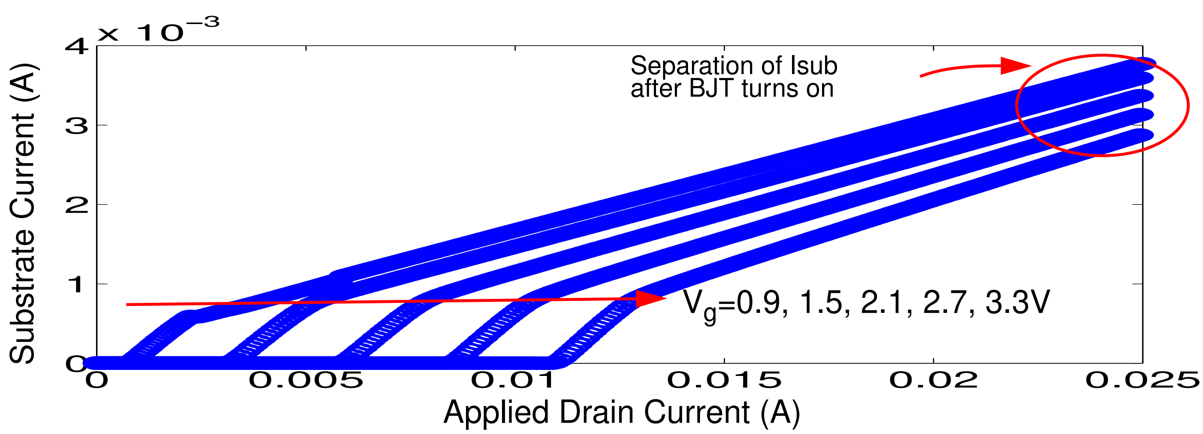

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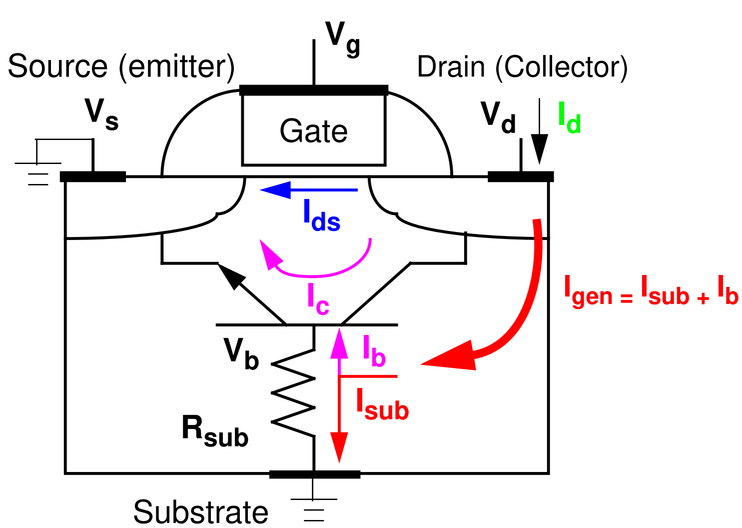

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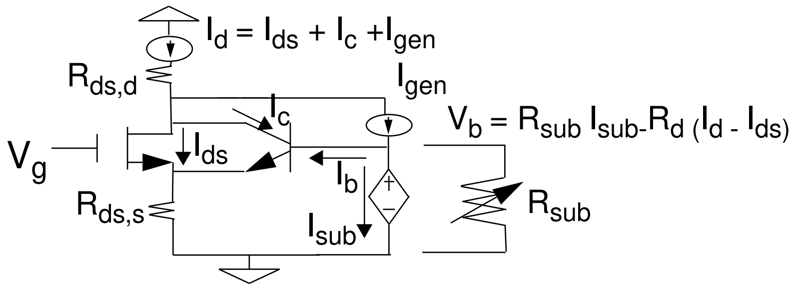

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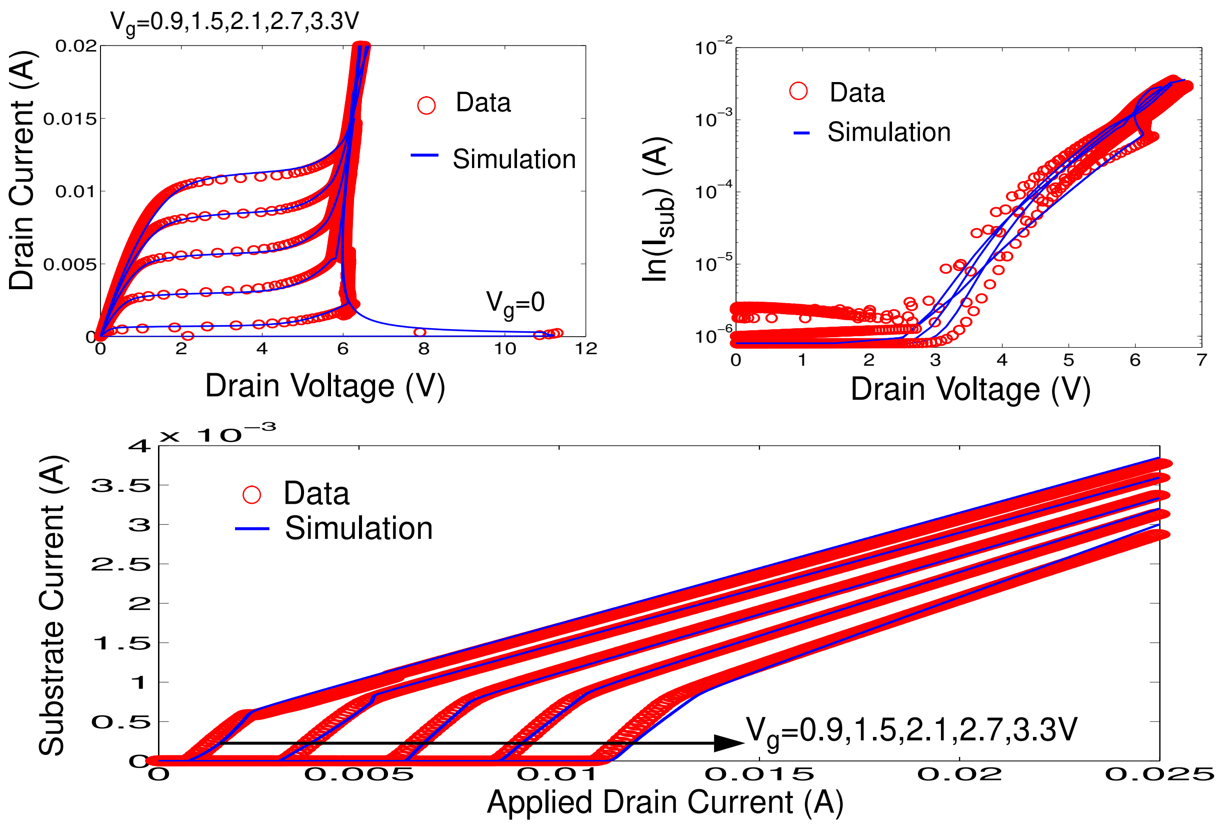

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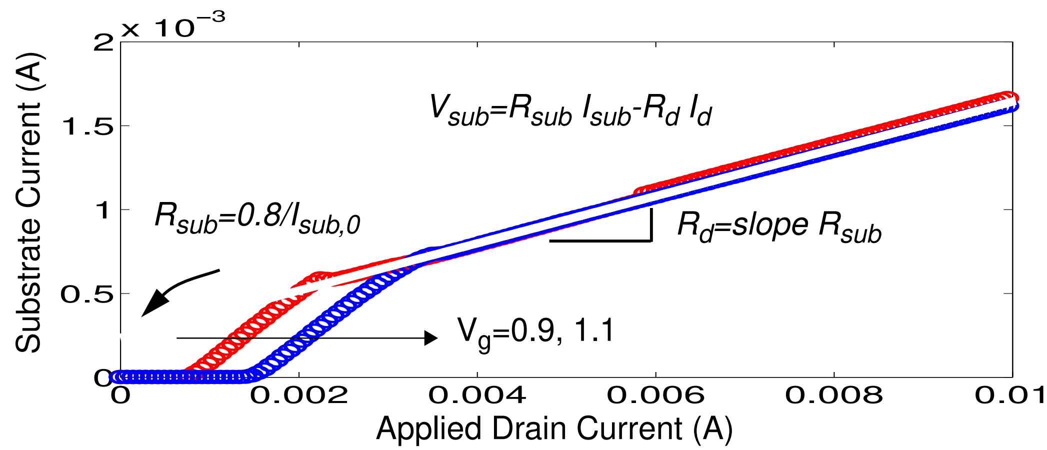

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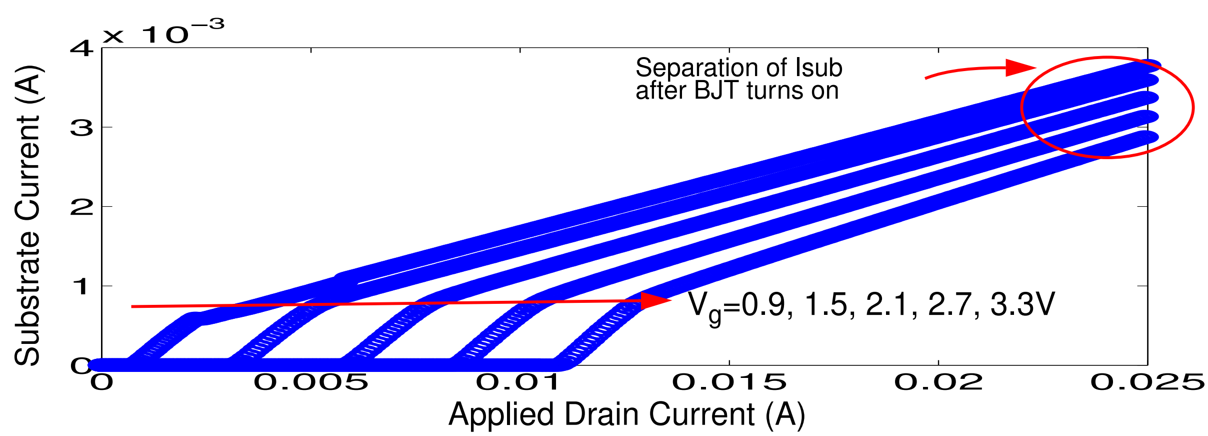

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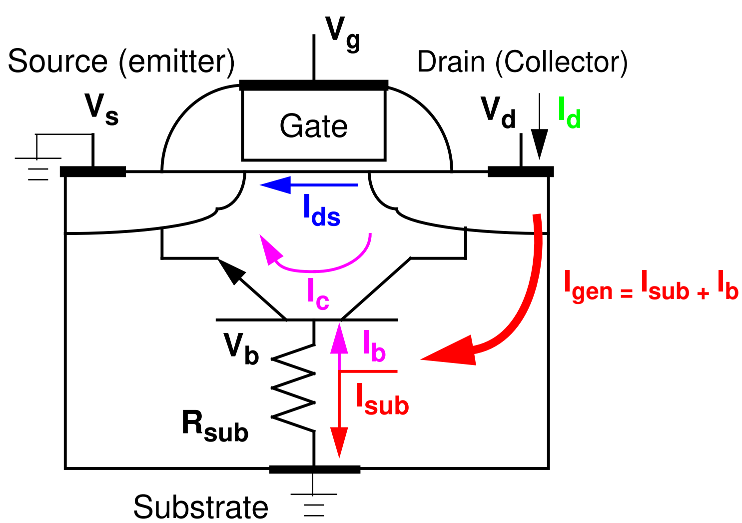

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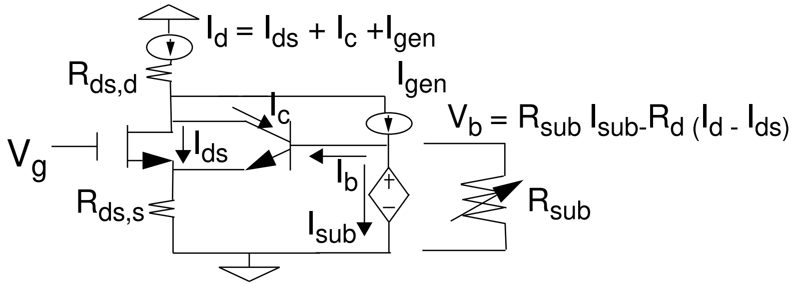

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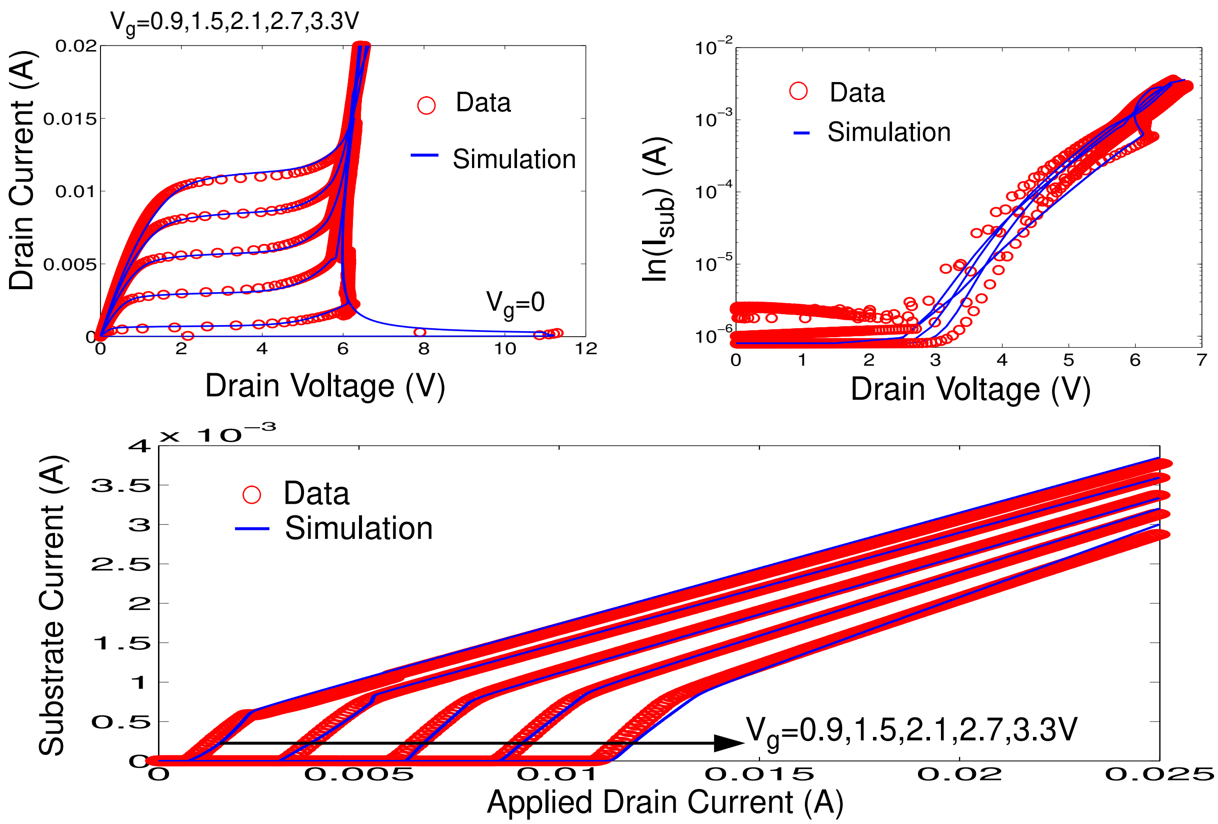

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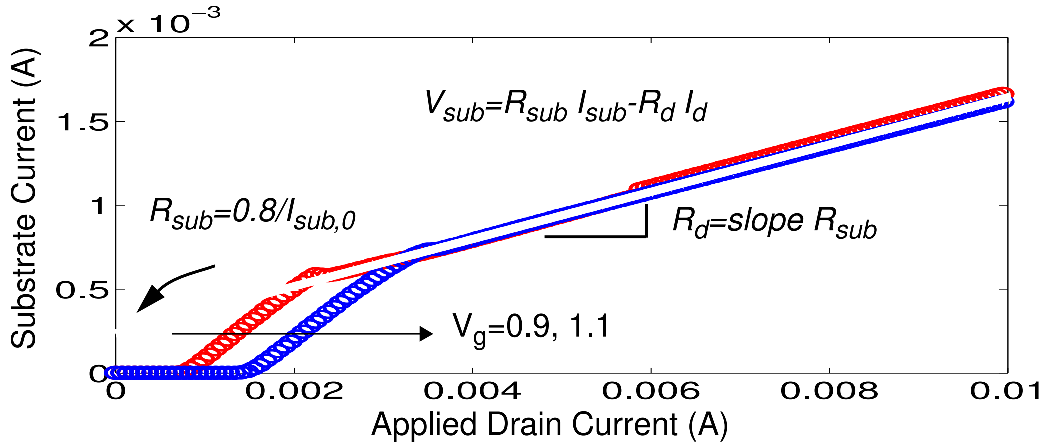

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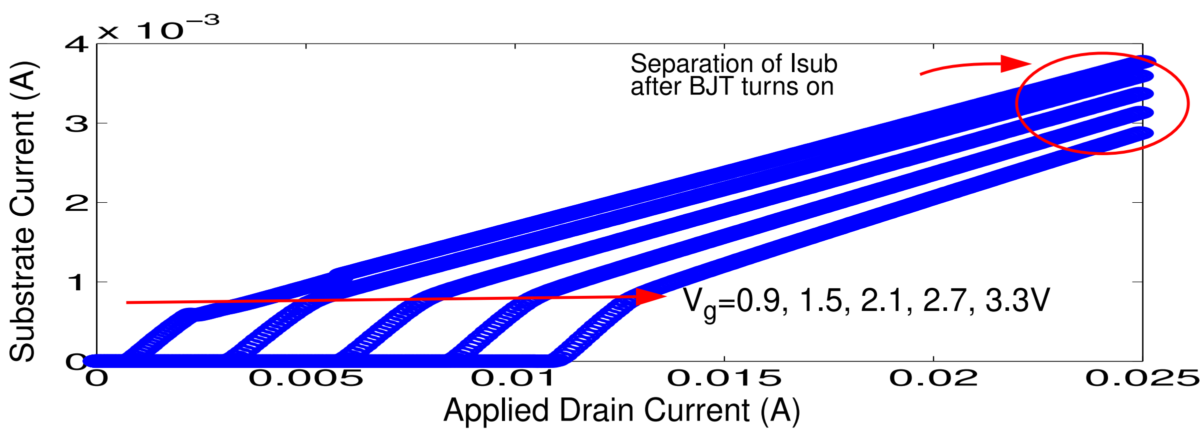

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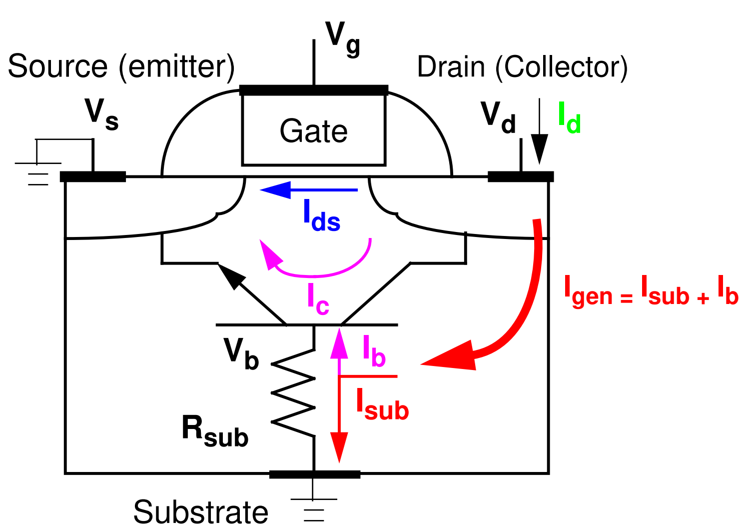

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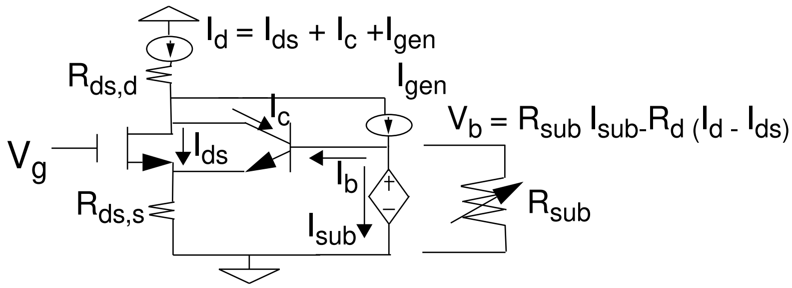

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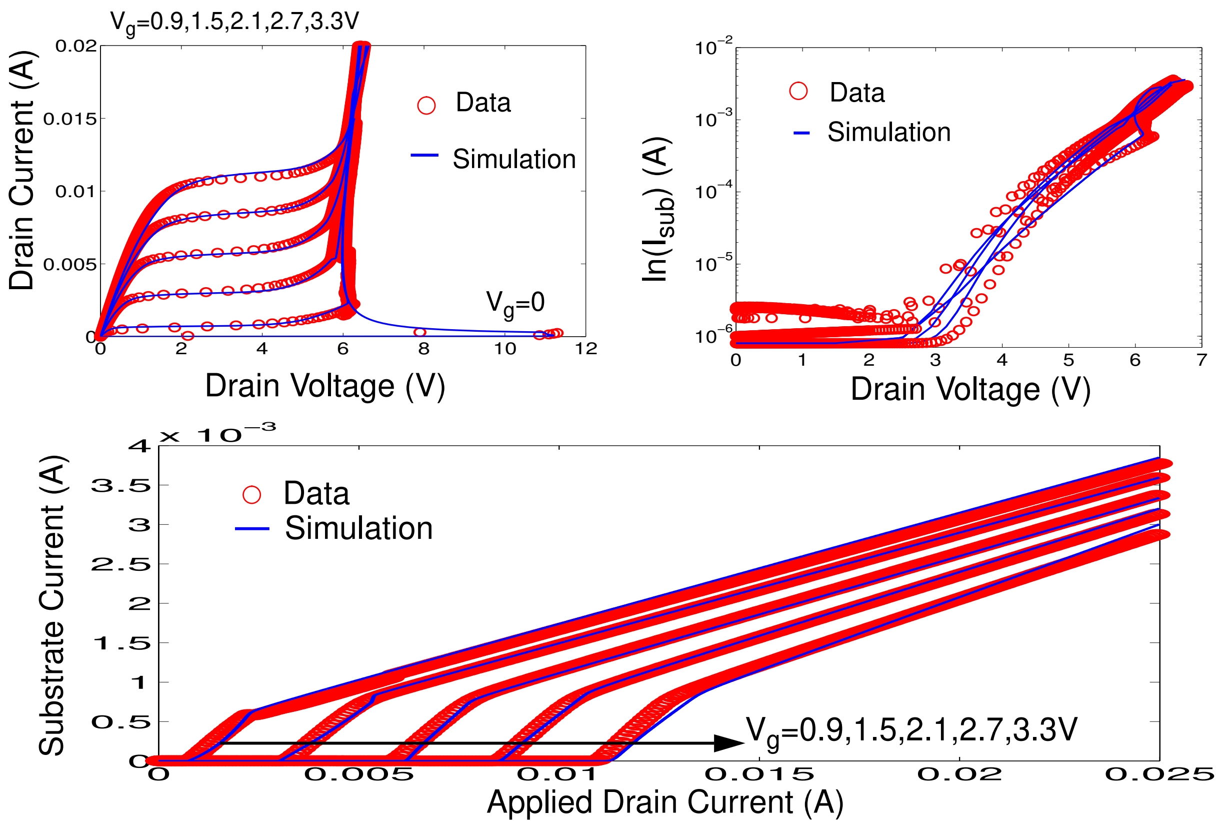

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To capture the separation of I_{sub} at different gate bias, the substrate resistance model is modified as:

$$V_b = R_{sub} \cdot I_{sub} - R_d \cdot (I_d - I_{ds}) \tag{5}$$

R_{sub} and R_d can be extracted from the Isub vs. Id curve at very low gate bias, slightly larger than V_t as shown in Fig. 2. The added I_{ds} parameter is the surface MOSFET current as shown in Fig. 4. For silicided devices the $R_d \cdot I_{ds}$ term is very small compared to $R_d \cdot I_d$ during the turn-on of the parasitic BJT, so it can be neglected and eq. (5) reduces to eq. (2). However, for non-silicided devices, the $R_d \cdot I_{ds}$ is significant and can be used to accurately describes the effect of large drain and source resistance on the intrinsic base voltage at low substrate current. Furthermore, the $R_d \cdot I_{ds}$ term allows a single substrate model to be used before as well as after the parasitic BJT action, whereas the previous model can only be used during the turn-on of the parasitic BJT.

Calibration and Results

The circuit model is shown in Fig. 4 was implemented in HSPICE to study a 20μ/0.35μ non-silicided NMOS ESD device. Comparison of HSPICE simulation results with measurements is shown in Fig. 5. There are good fits for both the snapback current/voltage and the separation of I_{sub} at different gate biases.

The calibration process begins by extracting M in eq. (4) before the snapback region, which is accomplished by following the methodology outlined in [4]. Next, R_{sub} and R_d are extracted from the I_{sub} vs. I_d curve at low gate bias. For this measured device, R_{sub} and R_d are extracted to be 3KΩ and 400Ω, respectively.

Conclusion

A circuit level substrate resistance model has been presented, and its useful application to the characterization of ESD-protection transistors has been demonstrated. Its continuity throughout breakdown and snapback regions makes it more robust and easy to implement than the previous substrate model. The impact of each model parameter on the IV curve was described, and the explanation of each relationship is consistent with experimental results. Finally, good agreement

(i.e. turn-on of the parasitic BJT). Hence, to maintain a constant base voltage, the substrate resistance must decrease. This reduction in R_{sub} has been attributed to the expansion of the substrate equipotential (i.e. base) region, which is in turn caused by the formation of the hole current due to impact ionization [2]. Therefore, the substrate resistance has to be modeled as a dynamic device. The standard approach is to model the reduction of the substrate resistance as a drain-current controlled voltage source [3]:

$$V_b = R_{sub} \cdot I_{sub} - R_d \cdot I_d \tag{2}$$

where R_{sub} and $R_{d,}$ a fitting parameter, can be extracted from the I_{sub} vs. I_d curves as shown in Fig. 2.

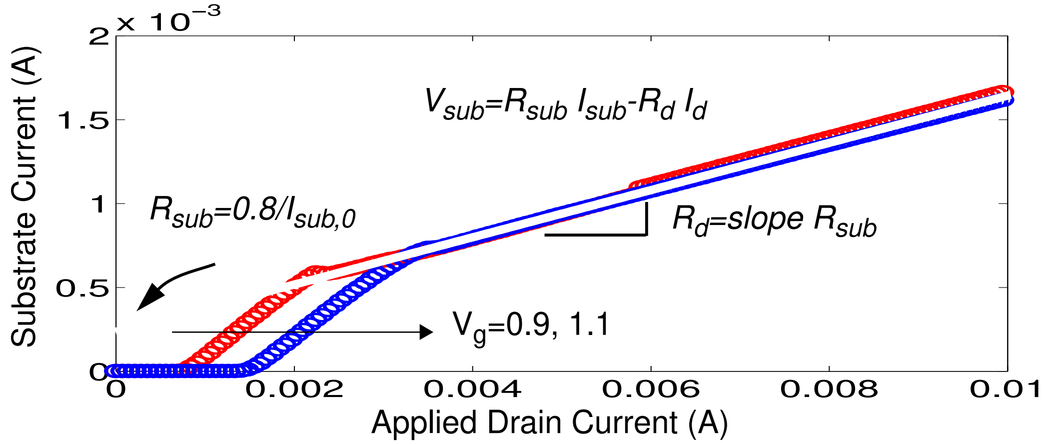

Fig. 2 The experimental I_{sub} vs. I_d curves for non-silicided 0.35μm LDD NMOS at low gate bias. The substrate current increases at higher drain current, showing the effect of decreasing substrate resistance.

However, the above expression of V_b does not model the separation of I_{sub} at different gate bias for non-silicided devices as shown in Fig. 3. In this case, as gate bias increases the y-intercept of the I_{sub} vs. I_d curve decreases to negative values, making the extracted R_{sub} parameter different and meaningless (negative R_{sub}) for each gate bias. Since many ESD protection structures are non-silicided transistors, improving the above substrate resistance model to account for the separation of I_{sub} curves would increase its usefulness and range of application.

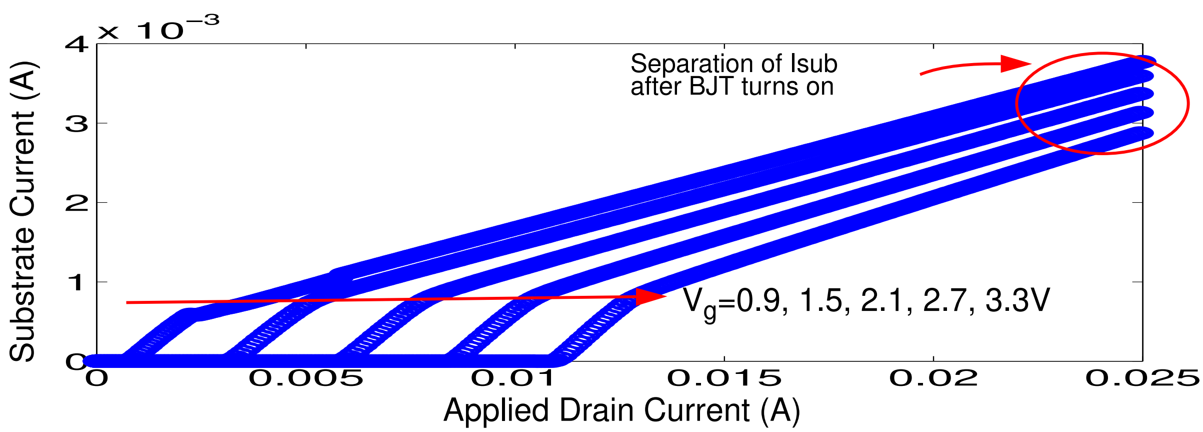

Fig. 3 Experimental data obtained from non-silicided 0.35μm LDD NMOS shows I_{sub} separation at different gate bias.

Substrate Resistance Model for Simulating MOSFET Breakdown in ESD Protection

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Abstract

This study presents a continuous substrate resistance model for circuit level simulation of MOS transistors under ESD stress. This model expands on previous work to take into account not only the intrinsic substrate resistance modulation effects but also the effect of gate bias on the substrate resistance which is pronounced in non-silicided devices. The substrate resistance modeling for non-silicided devices has not been captured before in the literature. The calibration process for the model is described, and the simulated results show excellent agreement with measured data.

Introduction

During ESD stress, current and voltage levels far exceed the level of normal circuit operation; therefore, the ability to model high current behavior is important to ESD protection circuit design. Compact modeling of MOS breakdown has been shown to be an efficient tool for ESD protection analysis and design [1]. A critical issue in this circuit analysis approach is the proper modeling of the substrate resistance, which affects both drain and substrate current.

Fig. 1 shows a cross-section of an NMOS transistor with various currents which are present during turn-on of the parasitic bipolar. The magnitude of the base voltage is determined by the substrate resistance (R_{sub}) and current (I_{sub}):

$$V_b = R_{sub} \cdot I_{sub} \tag{1}$$

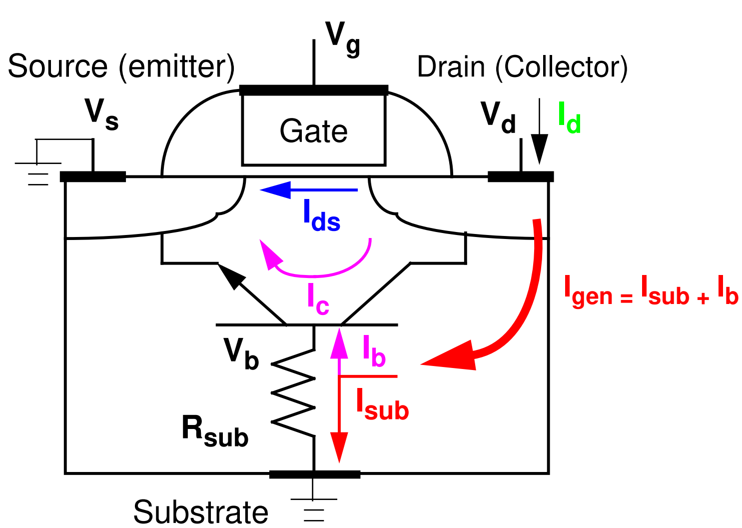

Fig. 1 The cross-sectional view of an NMOS transistor showing the currents after the parasitic BJT turns on.

Experimental evidence suggests that the substrate current continues to increase after snapback