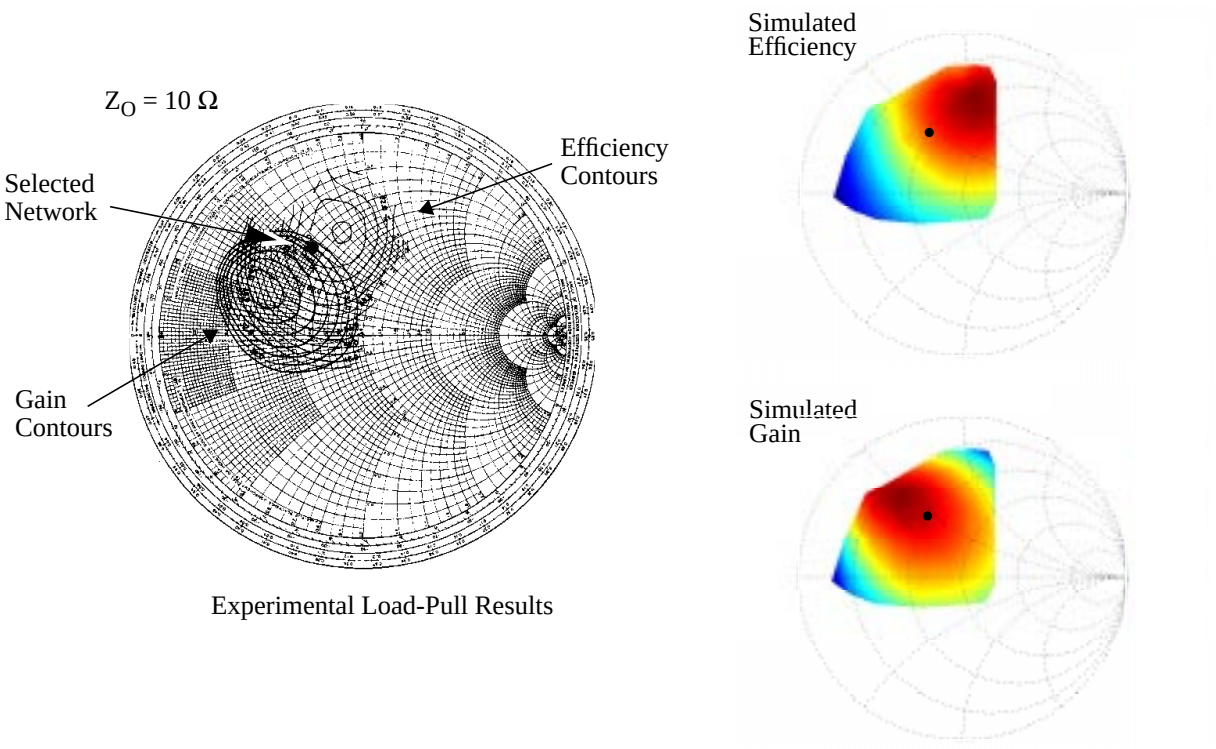

Figure 5: Comparison of experimental and simulated load-pull analysis. The darken point represents that matching network used in the earlier RF response.

V. Conclusion

Using PISCES2H-B, a methodology for modeling RF MOS devices is described. The model is verified with IV and CV characteristics and used in harmonic balance simulation. The simulation results are compared to experimental data to verify their accuracy. Once proven reliable, variations in the parasitics, device structure, and matching network are analyzed.

VI. Acknowledgments

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VII. References

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the matching networks are optimized for the real device and hence, may not be ideal for the simulated device albeit fairly close. Second, the device exhibits self-heating under high power operation. The net result is degradation at these higher power levels causing the gain to fall at a lower P_{out} than the simulated results.

With this verified model, effects due to changes in either parasitics or physical model can be analyzed. For example, consider a design of experiments (DOE) where the effect of the gate resistance, Faraday shield capacitance (C_{gs} (E)), and source package inductance (L_s) are allowed to vary within their physical limits. Fig. 4 shows the effect of these variations on efficiency. The first plot shows the primary affect caused by the change in the gate resistance. Secondary affects in the adjacent graph are shown for the source inductance and Faraday shield capacitance.

Gain and efficiency depend upon the matching networks that connect the signal source and load to the amplifier. One of the important design choice is to make sure that a good matching network allows for a smooth impedance transition from the input signal to the input impedance of the amplifier and then to the load impedance. The goal is to have the network transmit at the fundamental frequency without reflections or attentuation due to filtering and likewise have the network filter out higher order harmonics without reflections back into the amplifier.

To determine the optimum matching network, load-pull analysis is used to sweep across different network configurations over the range where one expects to find the optimum[4]. Fig. 5 shows experimental contour plots for gain and efficiency on a Smith chart which is used to represent the different reflection coefficients of the output matching network[5]. The characteristic impedance of 10Ω is used in the plot to make the results more clearly visible The darken point on the graphs indicates the matching network used to generate the earlier plot of gain and efficiency. The selection criteria for this point depend upon the application for the device. The alignment of the maxima and the shape of the contours demonstrate that the simulated results (Fig. 5) agree with the experimental data.

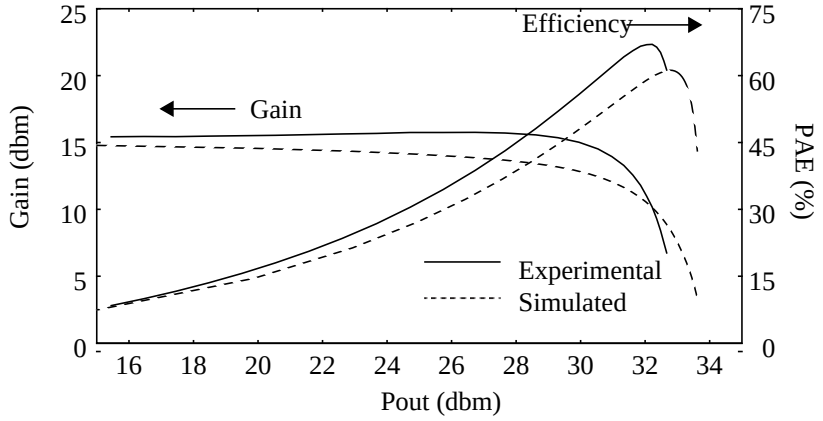

Figure 3: RF responses for gain and efficiency of a power amplifier.

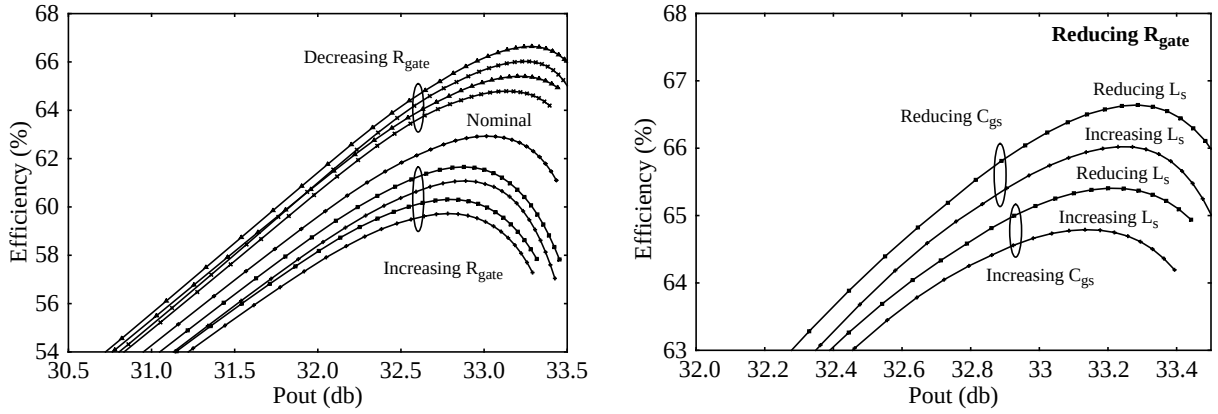

Figure 4: Effect of variations in the parasitic components on the efficiency.

electric field at the drain side of the device and optimizes R_{ds}(on), BV_{dss}, and C_{dg}. A metal field plate (i.e. Faraday shield) reduces the electric fields a the edge of the gate thereby increasing the breakdown voltage and reducing C_{dg}.

The model for the device is show in Fig. 1b. Only the intrinsic device is used in the PISCES device simulation while the rest of the device is modeled with linear circuit components. The components labeled with (E) represent the contribution from the electrode contacts. The components labeled with a (P) are those parasitics from the pad. In addition, not shown in the diagram are the parasitics from packaging such as inductances. Matching networks connect the amplifier to the source and 50 ohm load while a biasing network establishes the operating point for the device.

III. Modeling Tuning

The values for the parasitics are determine by analyzing the individual contributions in PISCES and then tuning the model to meet measured IV and CV characteristics. The electrode's capacitance are obtained in a PISCES simulation of the interconnect structure. To find the pad components, a 1 micron square section is simulated and then scaled to the area of the pads. Finally, for the source resistance, the sinker and substrate are simulated without the device present to a value for this resistance.

Fig. 2a shows the measured IV characteristics with the model's simulated results. The simulated IV characteristics are tuned to the measured characteristics by adjusting the doping profile of the intrinsic device. The profiles are tuned by adjusting parameters that determine how the one dimensional profiles are spread into two dimensions within their physically realizable limits. From the fitting of IV characteristics the extracted source resistance matches that of the simulated source resistance of the sinker structure.

Fig. 2b shows the standard CV plot for C_{gs}. Note that parasitic components add about 10% to the measured value of the capacitances. Like the source resistance, the CV characteristics are used to tune the external parasitics in addition to the intrinsic parasitics. This tuning should lead to parasitic component values that are equivalent to those determined from the independent simulation of the interconnect and pad structures.

IV. Harmonic Simulation

Given a model that agrees with measured characteristics, it is now possible to analyze its large signal sinusoidal response for a power amplifier incorporating this device. Fig. 3 shows the simulated and experimental power gain and efficiency for a single large signal sinusoidal input at 850Mhz. The gain rolls off at higher power levels because the device operates in g_m compression and the output power is limited by the saturation current. The efficiency is low for small P_{out} because the device drains more power in Class A operation. Efficiency increases until just after the gain starts to roll off. At this point, P_{in} approaches P_{out} resulting in very little power added to the input signal.

The simulated results approximate that of the experimental results. Errors come primarily from two sources. First the IV and CV characteristics are matched fairly well, but they are not exact. The primary impact of this difference is that

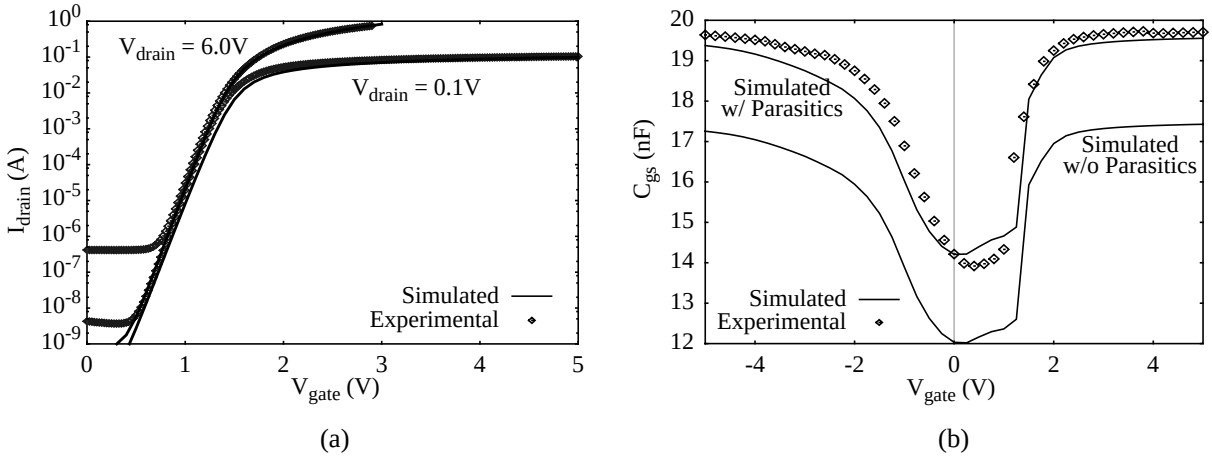

Figure 2: Comparison for one each of the simulated and measured (a) IV and (b) CV characteristics.

Modeling and Simulation of an RF LDMOS Device Using Harmonic Balance PISCES

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Abstract

This paper discusses the methodology and results for modeling and simulating RF MOS devices utilizing an harmonic balance (HB) device simulator. An equivalent circuit model is developed based upon the physical device structure and layout. This model is calibrated and compared to experimental IV and CV characteristics of LDMOS devices. Using the tuned model, harmonic balance simulations are shown to predicted measured experimental results. Perturbations to the device design can be reflected in the model and used to analyze the consequences of process and layout variations.

I. Introduction

In order to accelerate the design phase of new devices, simulation tools provide valuable insight into performance. For RF devices, Stanford and HP jointly developed an harmonic balance version of PISCES for analyzing a device in the frequency domain [1]. In addition, the PISCES simulator allows parasitics to be included through a set of boundary condition equations [2]. Using this simulator, RF LDMOS devices are modeled with the intrinsic device represented physically in PISCES and the extrinsic components and parasitics represented as linear circuit elements. This model is verified to match experimental measurements and then used to analyze the parasitic components and matching network.

II. Model Development

Fig. 1a shows the cross section of an LDMOS device [3]. A laterally diffused graded channel enhances RF performance, prevents punch-through, and increases the device transconductance. A P+ sinker connects source and substrate together to eliminate extra bond wires and provide for a back side contact. An N- LDD decreases the

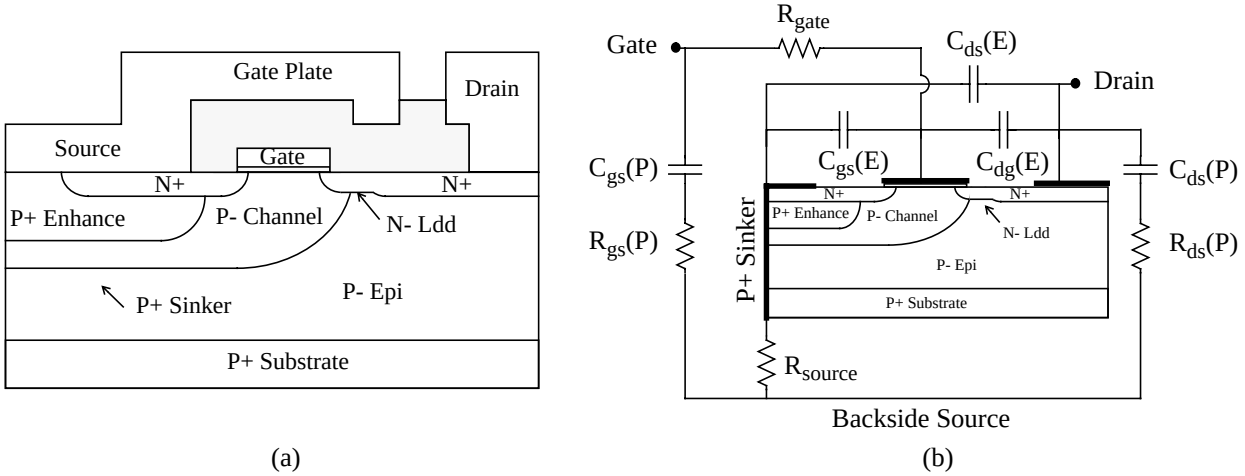

Figure 1: (a) RF LDMOS power device and (b) model showing parasitic components.