Characterization of RF Power BJT and Improvement of Thermal Stability with Nonlinear Base Ballasting

Jaejune Jang, *Student Member, IEEE,* Edwin C. Kan, *Member, IEEE,* Torkel Arnborg, *Senior Member, IEEE,* Ted Johansson, *Senior Member, IEEE,* and Robert W. Dutton, *Fellow, IEEE*

***Abstract*— A novel base ballasting scheme for interdigitated power RF bipolar transistors has demonstrated improved performance and thermal stability. The nonlinear ballast resistor in series with each base finger is implemented using a depletion-mode FET, which requires only minor modification in the fabrication process. Mixed-mode simulation, instead of analytical equations, is used for more accurate device characterization.**

***Index Terms*— Ballasting, parasitic characterization, power BJT.**

I. Introduction

THE positive feedback from inhomogeneous temperature distributions in interdigitated power bipolar transistors can cause thermal instability or gain collapse [1], [2]. Usually emitter ballast resistor is used for prevention, and its optimal value needs to be carefully chosen to ensure good instability protection without severe performance degradation [3]. The design of finger spacing is also a tradeoff in view of thermal management, since its reduction can increase thermal coupling between fingers and hence decrease the current hogging effect [4], [5], but this reduction will lead to inefficient head dissipation for the entire cell [5]. We propose to use a new nonlinear base ballasting scheme that is very effective in thermal instability protection with little performance penalty at normal operating conditions. Since the positive feedback from Joule heating can be nearly eliminated, the layout design can also be more aggressive toward handling total heat dissipation.

II. Power RF Device Modeling

Power RF devices pose significant challenges to modeling strategies, since both thermal and parasitic effects need to be accurately accounted for. For the power bipolar junction transistor (BJT) in this study (Fig. 1), mixed-mode device/circuit simulation which interfaces Stanford's device simulator PISCES and University of California at Berkeley's circuit simulator SPICE-3f2 has been demonstrated as an effective method to model the parasitic elements and to link the detailed doping profiles directly with circuit performance [6].

For devices which are fabricated on a monolithic substrate, the circuit often exhibits parasitic behavior due to elements that can be represented by a two-port network configuration as shown in Fig. 2. This T-like topology has been used successfully by many authors [8], [9]. For this network it is assumed that over the frequency range of concern (from 300 MHz to 3 GHz) the equivalent circuit composed of lumped RLC elements, can be described using general interconnect parasitics. In reality, at high frequencies the interconnect circuit parameters such as resistance may vary with frequency, due to skin and other distributive effects. For the frequency range considered here, however, frequency-independent modeling parameters are usually sufficient.

As shown in Fig. 3, construction of the two-port matrices from the inner shell to the outer one or vice versa is straightforward. The extracted parasitics of C_f, Z_e, Z_b, and Z_c are as below [6].

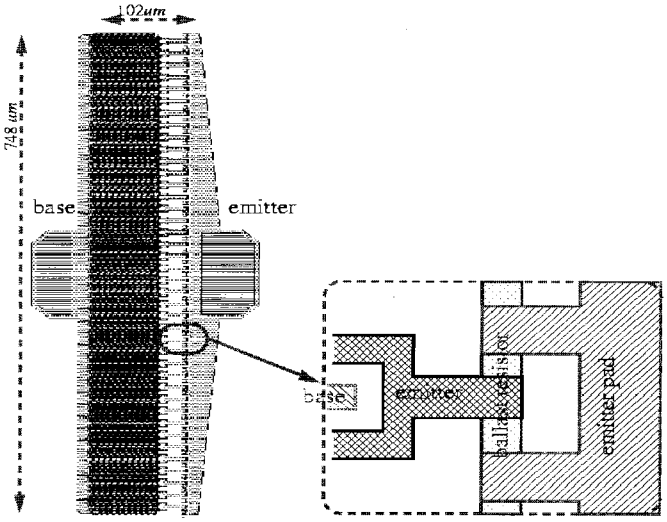

Fig. 1. Modeled RF BJT layout and T-network for parasitic characterization.

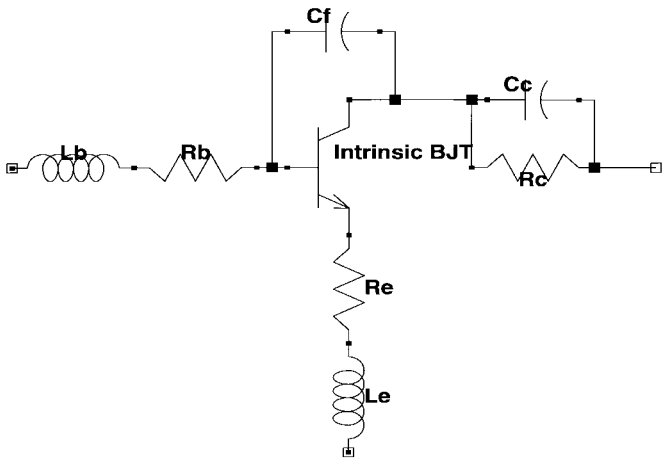

Fig. 2. Modeled T-network for RF BJT.

Manuscript received January 2, 1998; revised May 21, 1998.

J. Jang and R. W. Dutton are with Stanford University, Stanford, CA 94305-4075 USA.

E. C. Kan is with Cornell University, Ithaca, NY 14850 USA.

T. Arnborg and T. Johansson are with Ericsson Components AB, Kista S-164 81 Sweden.

Publisher Item Identifier S 0018-9200(98)05874-0.

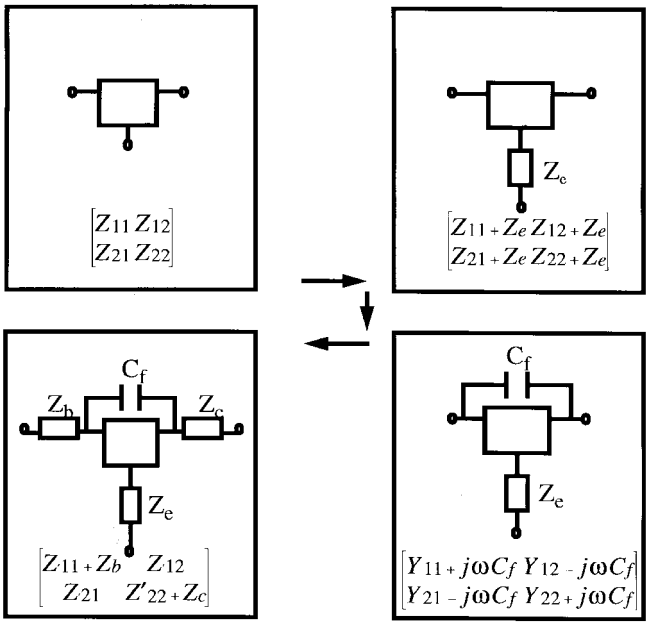

Fig. 3. Inclusion of extrinsic parasitics. The center box represents a intrinsic RF BJT which is modeled with device simulator.

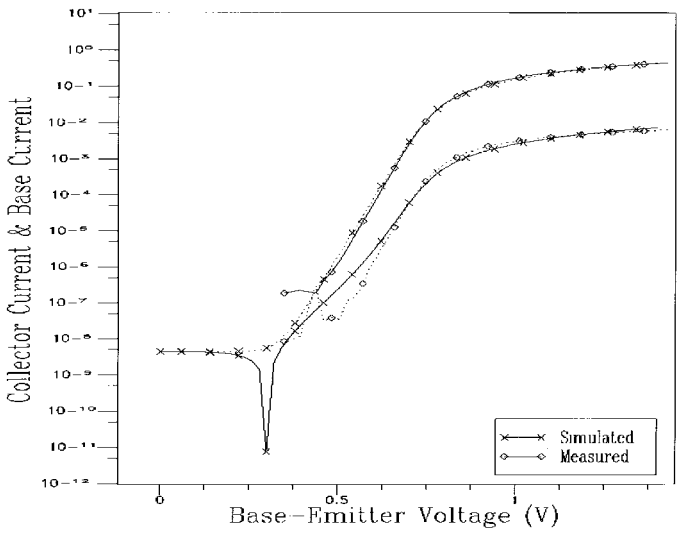

Fig. 4. Fitted Gummel plots using mixed-mode device simulation. Mobility and lifetime are calibrated.

Where Z_{m11}, Z_{m12}, Z_{m21}, and Z_{m22} are measured Z parameters

$$j\omega C_f = \frac{Z_{12} - Z_{21} + Z_{m21} - Z_{m12}}{(Z_{m12} - Z_{m21})(Z_{22} + Z_{11} - Z_{12} - Z_{21})}$$

$$Z_e = \frac{Z_{m12}\det(Z_j) - Z_{12} - j\omega C_f(Z_{11}Z_{22} - Z_{12}Z_{21})}{1 + j\omega C_f(Z_{11} + Z_{22} - Z_{12} - Z_{21})}$$

$$Z_b = Z_{m11} - \frac{Z_{11} + Z_e + j\omega C_f \Delta Z}{1 + j\omega C_f(Z_{11} + Z_{22} - Z_{12} - Z_{21})}$$

$$Z_c = Z_{m22} - \frac{Z_{22} + Z_e + j\omega C_f \Delta Z}{1 + j\omega C_f(Z_{11} + Z_{22} - Z_{12} - Z_{21})}$$

and

$$\Delta Z = Z_{22}Z_{11} - Z_{12}Z_{21} + Z_e(Z_{22} + Z_{11} - Z_{12} - Z_{21})$$
$$\det(Z_j) = 1 + j\omega C_f(Z_{22} + Z_{11} - Z_{12} - Z_{21}).$$

TABLE I
EXTRACTED PARASITIC VALUES FOR T-NETWORK USING MIXED-MODE SIMULATION

C_f	C_C	L_b	L_e	R_b	R_e	R_c
2.3 pF	60 pF	0.7 nH	0.3 nH	0.44Ω	1.20Ω	0.08Ω

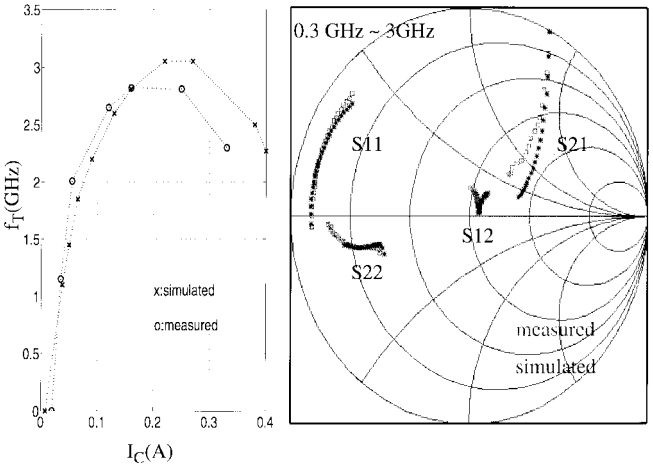

Fig. 5. Comparison between measurement and simulation for I_C versus f_T and S-parameters.

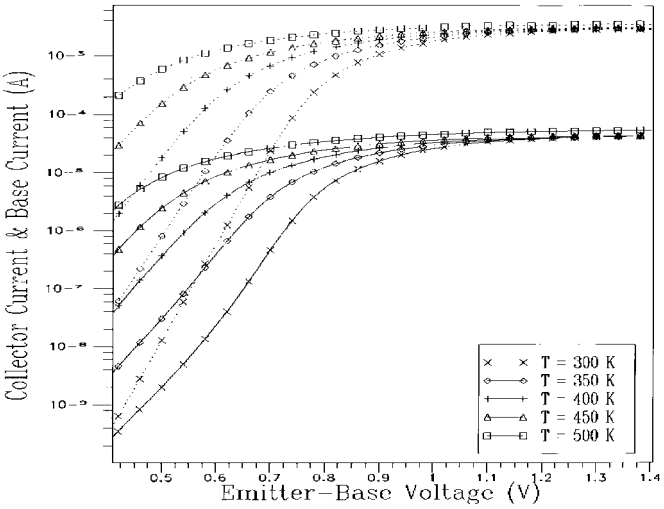

Fig. 6. Gummel plots of a unit cell (a base finger and a emitter finger) with various temperature. I_B and I_C increase as T_L increases.

Thus by comparing measured Z parameters and the simulated intrinsic parameters (Z_{11}, Z_{12}, Z_{21}, and Z_{22}), extrinsic parasitics values (C_f, Z_e, Z_b, and Z_c) can be obtained. Unlike analytical approaches [3]–[5], the numerical method can capture detailed transistor behaviors and electrical couplings with no operation-mode assumption, and hence has a broader range of applicability. Calibrated Gummel plots to measurements at room temperature are shown in Fig. 4. The measured SRP doping profile is also used for calibration. Extracted values of the parasitic elements are listed in Table I [6]. The emitter ballast resistance is about 110 Ω per finger implemented using a p-type diffusion resistor. The f_T as a function of the collector current I_c and the S-parameters are shown in Fig. 5. There is quite good agreement between measurements and simulation.

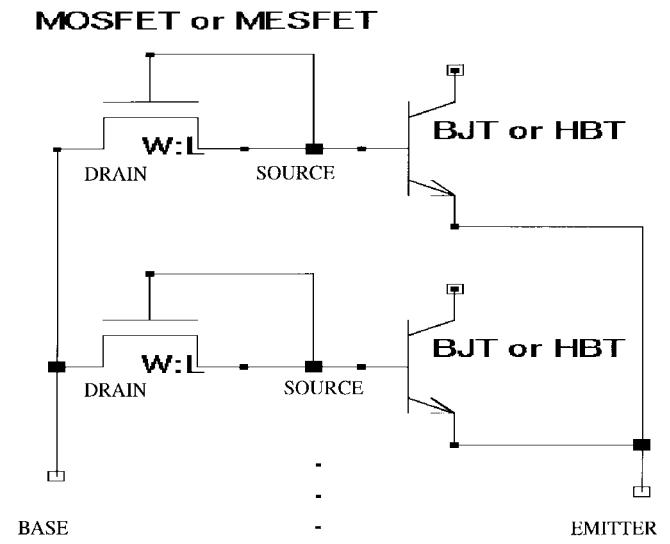

Fig. 7. Circuit diagram for depletion-mode FET. Each base finger is connected to an FET.

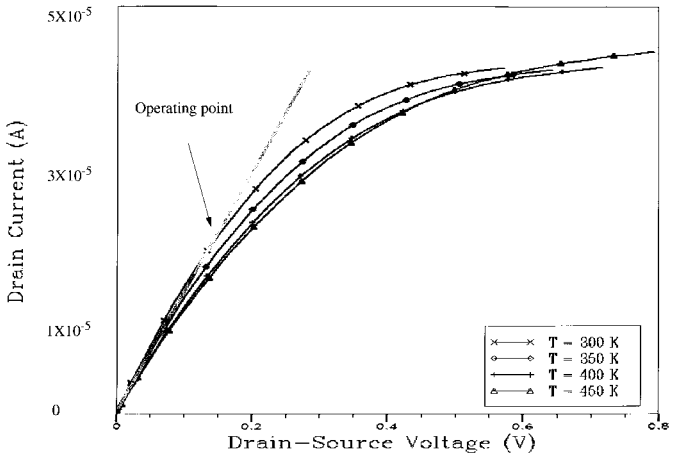

Fig. 8. I_D and V_{DS} characteristics at various temperatures. The operating point should be chosen close to (maximum protection) or below (maximum linearity) the onset of saturating region.

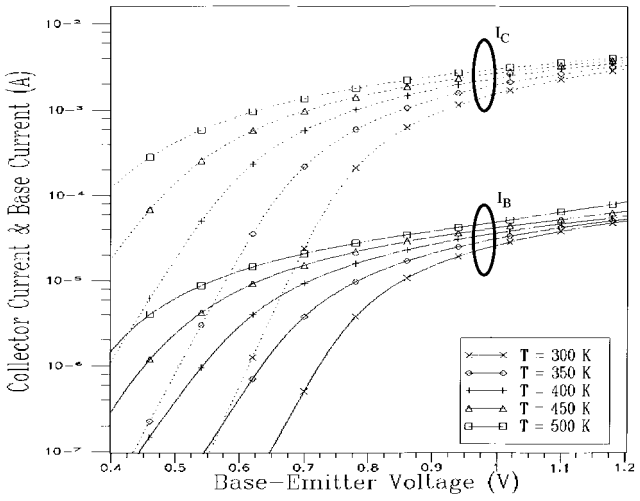

Fig. 9. Gummel plot for BJT with depletion mode MOSFET. I_B and I_C are effectively limited by MOSFET at high current level.

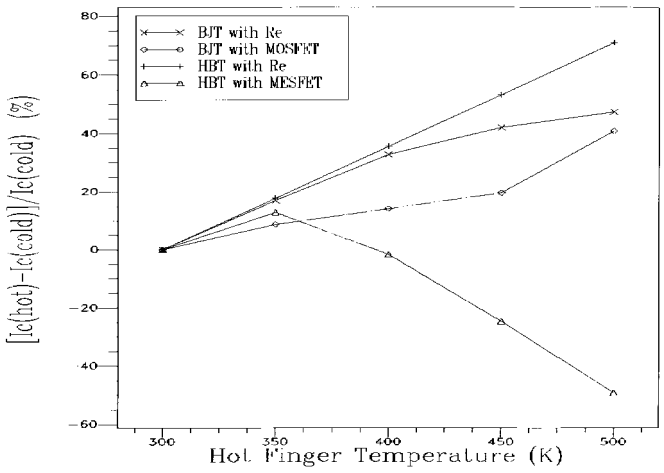

Fig. 10. Percentage difference in I_C (hot finger) compared with I_C (cold finger @ $T = 300$ K).

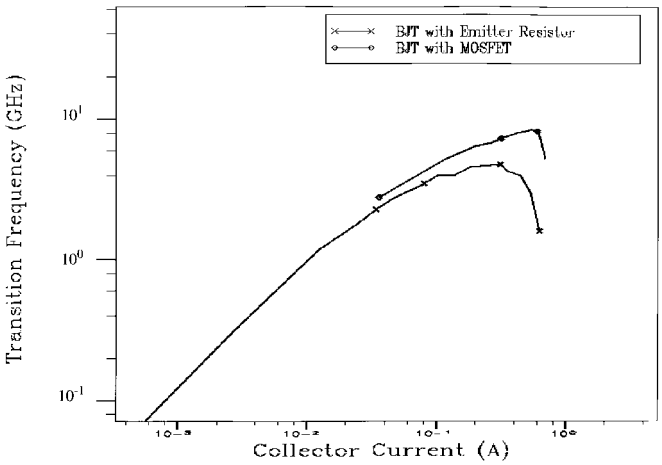

Fig. 11. Transition frequency (f_T) versus total I_C. BJT with depletion-mode MOSFET has higher f_T (@ $V_{CE} = 5$ V, and $T = 307$ K).

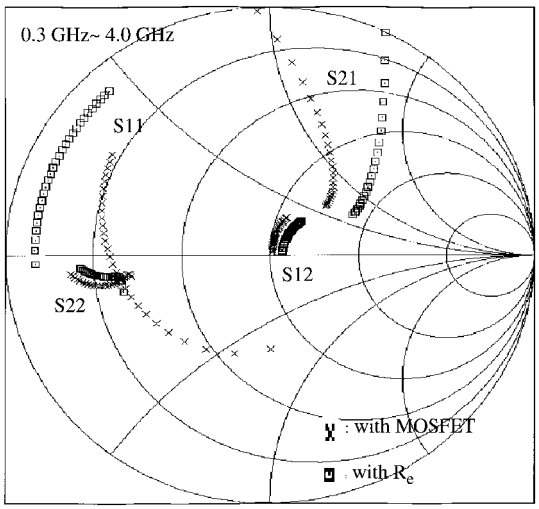

Fig. 12. S-parameter comparison between BJT with depletion-mode ballasting and BJT with emitter ballasting.

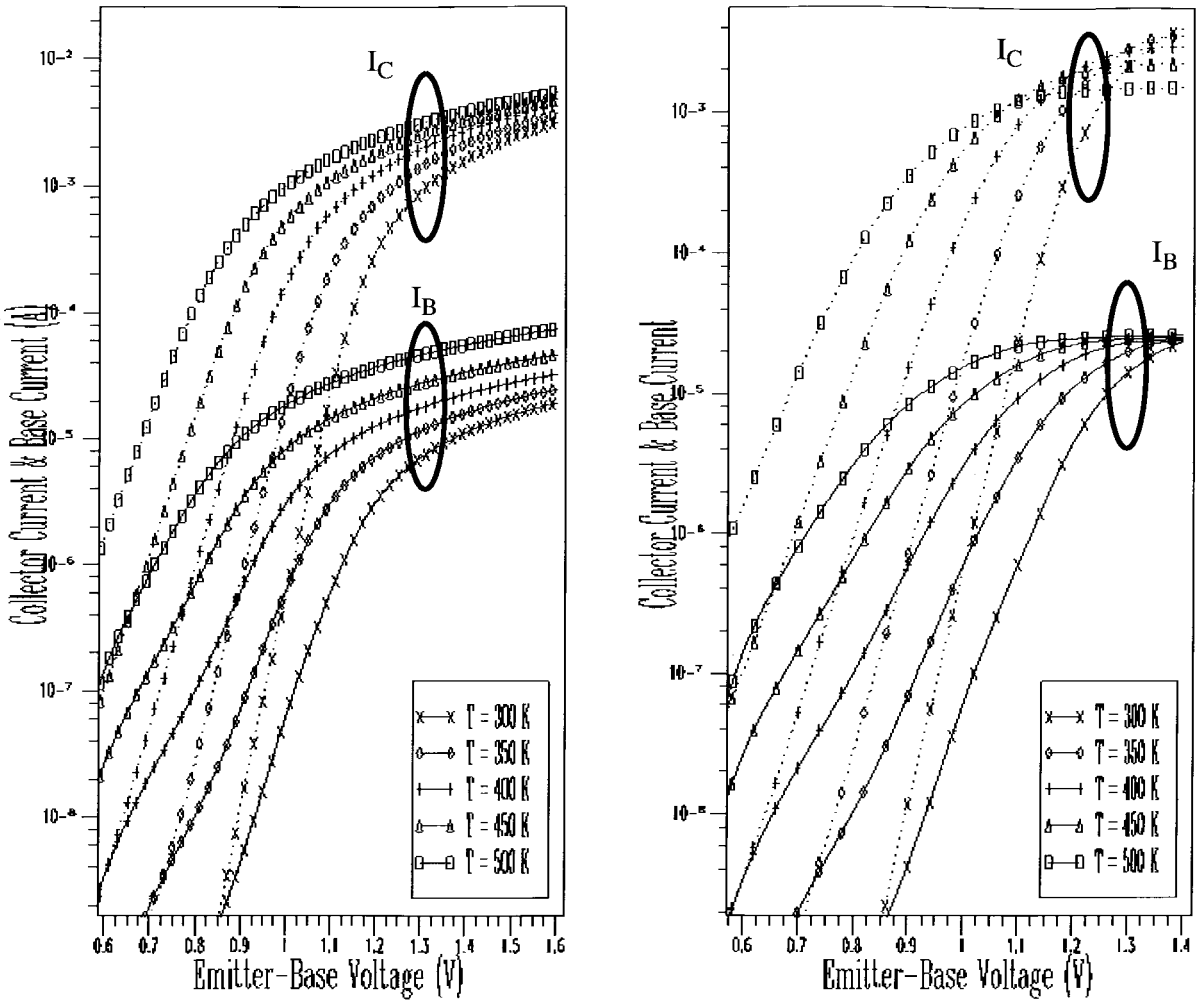

Fig. 13. Gummel plot for (a) HBT with emitter resistor and (b) HBT with depletion-mode base ballasting at various temperatures.

III. Nonlinear Base Ballasting

It is apparent that a nonlinear ballast resistor will be superior to a linear one, since optimal effective resistance values can be separately designed for operating conditions and instability protection. If the ballast resistor is applied to the base end [5], [7], the equivalent resistance can be obtained by multiplying the emitter resistance with the dc current gain. Although it was argued in [7] that base ballasting can only work for heterojunction bipolar transistor (HBT), not BJT, since current gain increases with temperature T_L for BJT, a more careful analysis in Fig. 6 reveals that the base current I_b still increases with T_L, though not as fast as I_c. Therefore, base ballasting can still prevent thermal instability in the BJT, just not as effective as emitter ballasting if the equivalent value is used. A nonlinear emitter ballasting is difficult to implement owing to its small I_{dsat} value and limited area. With a nonlinear base resistor implemented by a depletion-mode MOSFET as shown in Figs. 7 and 8, the saturation region of MOSFET will effectively limit the current through hot fingers, while the linear region will hardly affect the normal operating point of cold fingers. The MOSFET has a channel length and width of 3 and 15 μm, and a threshold voltage of -0.45 V. The dimensions of the depletion-mode FET is determined by setting proper I_{dsat} level for optimal circuit performance and instability protection. Other layouts or devices are also applicable as long as the nonlinear resistance values are chosen appropriately (i.e., an enhancement-mode MOSFET with gate connected to V_{cc}). Fig. 9 shows improved temperature dependence of the Gummel plot by using the nonlinear ballasting scheme. Different ballasting schemes are compared in Fig. 10 in view of instability protection. Due to increased effective g_m of nonlinear ballasting scheme, higher f_T is resulted as shown in Fig. 11. All coupling capacitances have been taken into account. S-parameters with different ballasting scheme is also compared for high frequency characteristics as shown in Fig. 12. It can be seen that the new ballast scheme is strongly favorable to the conventional emitter ballasting.

IV. HBT Applications

The proposed ballast scheme can possibly be applied to power HBT applications, too. The nonlinear resistor can be obtained by MESFET, although more difficult modification

on fabrication is likely. A computational prototype through mixed-mode simulation is built for illustration. The HBT device follows the specification in [7] and the MESFET has a gate length and width of 2 and 5 μm and a threshold voltage of -0.3 V. As shown in Fig. 13, base ballasting using depletion-mode FET is more efficient in HBT due to decreasing current gain with increasing T_L. With proper operating condition, the HBT does not experience current gain collapse since as T_L of the hot finger increases, collector current decreases due to base current is effectively limited by MESFET so that T_L does not increase anymore as illustrated in Fig. 10.

V. Conclusion

A new methodology of parasitic extraction and a novel base ballasting scheme for RF power bipolar transistors have been described in this paper. The nonlinear ballast resistor in series with each base finger is implemented using a depletion-mode FET, which prevents from inhomogeneous temperature distribution without sacrificing performance of the power device.

References

[1] R. H. Winkler, "Thermal properties of high-power transistors," *IEEE Trans. Electron Devices*, vol. 14, pp. 260–264, 1967.

[2] W. Liu, S. Nelson, D. Hill, and A. Khatibzadeh, "Current gain collapse in microwave multi-finger heterojunction transistors operated at very high power density," *IEEE Trans. Electron Devices*, vol. 40, pp. 1917–1927, 1993.

[3] G. Gao, M. S. Unlu, H. Morkoc, and D. L. Blackburn, "Emitter ballasting resistor design for, and current handling capability of AlGaAs/GaAs power heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 38, pp. 185–196, 1991.

[4] W. Liu, "Thermal management to avoid the collapse of current gain in power heterojunction bipolar transistors," in *GaAs IC Symp. Tech. Dig.*, 1995, pp. 147–150.

[5] L. L. Liou and B. Bayraktaroglu, "Thermal stability analysis of AlGaAs/GaAs heterojunction bipolar transistors with multiple emitter fingers," *IEEE Trans. Electron Devices*, vol. 41, pp. 629–636, 1994.

[6] J. Jang, E. C. Kan, L. So, R. W. Dutton, T. Johansson, and T. Arnborg, "Parasitic characterization of radio-frequency (RF) circuit using mixed-mode simulation," in *Proc. CICC*, 1996, pp. 445–448.

[7] W. Liu, A. Khatibzadeh, J. Sweder, and H. Chau, "The use of base ballasting to prevent the collapse of current gain in AlGaAs/GaAs heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 43, pp. 245–251, 1996.

[8] R. Ramachandran *et al.*, "A high efficiency HBT MMIC power amplifier," in *Proc. GaAs IC Symp.*, 1990, vol. 22, pp. 357–360.

[9] U. Schaper and B. Holzapfl, "Analytical parameter extraction of the HBT equivalent circuit with T-like topology from measured S-parameters," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 493–498, 1995.

Jaejune Jang (S'93) received the B.S. and M.S. degrees in electrical engineering from the Michigan State University and Stanford University, in 1993 and 1995, respectively. He is currently a graduate student in the Electrical Engineering Department of Stanford University, Stanford, CA.

His interests are in RF power device design.

Edwin C. Kan (S'86–M'90) received the B.S. degree from National Taiwan University in 1984 and the M.S. and Ph.D. degrees from University of Illinois at Urbana-Champaign in 1988 and 1992, respectively, all in electrical engineering.

From 1984 to 1986, he served as a Second Lieutenant in the Air Force, Taiwan, ROC. In January 1992, he joined Dawn Technologies as the principal developer of advanced electronic and optical device simulators and technology CAD framework. He has been with Stanford University, Stanford, CA, as a Research Associate since October 1993. He joined Cornell University, Ithaca, NY, in July 1997 as an Assistant Professor of School of Electrical Engineering. His main research areas include VLSI technology, semiconductor device physics, composite CAD development, and numerical methods of PDE and ODE.

Torkel Arnborg (S'78–M'79–SM'94) was born on January 9, 1947. He received the M.Sc. degree in 1970 and the Ph.D. degree in 1982 from the Royal Institute of Technology, Stockholm, Sweden.

From 1970 to 1975, he taught analog and digital circuits. His thesis work was on MOS modeling and two-dimensional analysis of semiconductor devices using finite element methods. He joined the process development laboratory at Ericsson Components, Kista, Sweden, in 1983 and worked with applications in smart power, HVIC, VLSI, and optoelectronics for silicon and III–V materials. During 1990–1991, he was a Visiting Researcher at Texas Instruments Incorporated, Dallas, working with models and scaling methods for future BiCMOS technologies. In 1993, he joined the Ericsson Microelectronics Research Center. From 1996–1997, he was a Visiting Scientist at the Center for Integrated Systems, Stanford University, as a Wallenberg stipend receiver. His present interests include RF modeling and new technology simulation techniques useful for telecommunication applications.

Ted Johansson (M'90–SM'96) was born on September 20, 1959. He received the M.Sc. degree in applied physics and electrical engineering in 1985 and the Dr.Tech. and Ph.D. degrees in electronic devices from Linköping Institute of Technology, Sweden, in 1993 and 1998, respectively.

From 1985 to 1989, he worked at Swedish Institute of Microwave Technology/Microelectronics in Stockholm and Kista, doing research in the area of MOS process technology. He joined Ericsson Component AB in 1989 when the development of RF power transistors for cellular base stations started and is presently Project Manager for the next bipolar RF power process generation at Ericsson's semiconductor fab in Kista, Sweden. He has published more than 25 journal and conference papers, holds four patents and has another seven patent applications pending. His research interests include RF related areas on device level, including fabrication and simulations of new device structures.

Robert W. Dutton (S'67–M'70–SM'80–F'84) received the B.S., M.S., and Ph.D. degrees from the University of California, Berkeley, in 1966, 1967, and 1970, respectively.

He is Professor of Electrical Engineering at Stanford University, Stanford, CA, and Director of Research in the Center for Integrated Systems. He has held summer staff positions at Fairchild, Bell Telephone Laboratories, Hewlett-Packard, IBM Research, and Matsushita during 1967, 1973, 1975, 1977, and 1988, respectively. His research interests focus on integrated circuit process, device, and circuit technologies—especially the use of computer-aided design (CAD) and parallel computational methods. He has published more than 200 journal articles and graduated more than four dozen doctorate students.

Dr. Dutton was Editor of the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (1984–1986), winner of the 1987 IEEE J. J. Ebers Award, the 1988 Guggenheim Fellowship to study in Japan, and was elected to the National Academy of Engineering in 1991. In December 1996, he received the Jack A. Morton Award for his "seminal contributions to semiconductor process and device modeling."