Guidelines for the Power Constrained Design of a CMOS Tuned LNA

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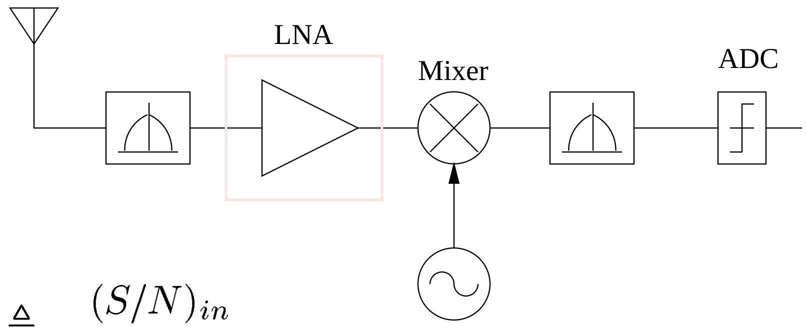
Outline

- Motivation
  - ✧ Optimization Technique
  - ✧ Four Noise Paramters
- Intrinsic MOSFET Noise Characteristics
- Tuned Low Noise Amplifier Analysis
  - ✧ Input Stage
  - ✧ Cascode Stage
  - ✧ Matching Element
- Conclusions

Motivation

(Importance of the LNA in RF Systems)



$$NF \triangleq \frac{(S/N)_{in}}{(S/N)_{out}}$$

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_1} + \cdots + \frac{NF_n - 1}{A_1 \cdots A_{n-1}}$$

When the LNA provides sufficient gain

$$NF_{tot} \approx NF_{LNA}$$

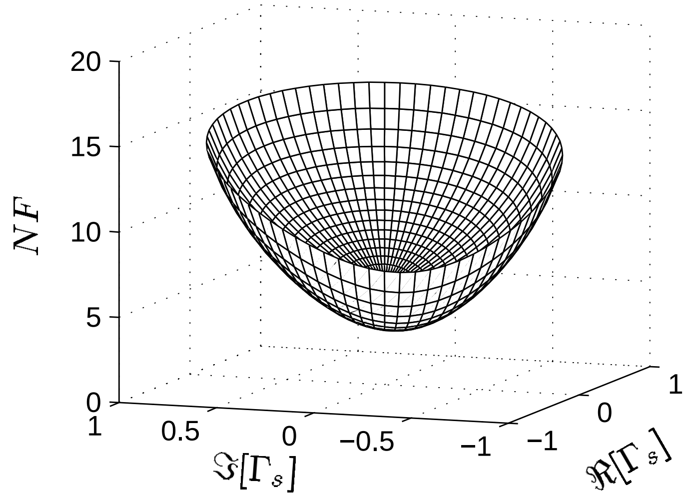
Motivation *(Continue)*
(Noise Optimization)

- Classical Noise Optimization
  - ✧ Given device with fixed geometries and characteristics.
  - ✧ Adjust the source impedance to optimize the noise figure.
- CMOS Noise Optimization
  - ✧ Freedom in tailoring device geometries.
  - ✧ Enable simultaneous optimization of the power, input matching, and noise figure.
  - ✧ Ambiguous optimization procedure due to the poor noise modeling.

Motivation *(Continue)*

(Four Noise Parameters)

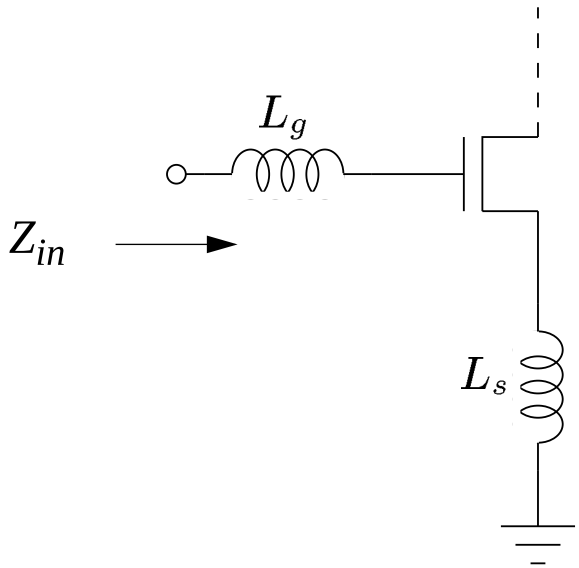
$$
\begin{aligned}
NF &= 1 + 2R_n(G_{opt} + G_c) \\
&\quad + \frac{[(B_s - B_{opt})^2 + (B_s - B_{opt})^2]R_n}{G_s} \\
&\triangleq NF_{min} + \frac{(Y_s - Y_{opt})^2\, R_n}{G_s}
\end{aligned}
$$



- NF_{min} : Best achievable noise performance — shorter L yields lower NF_{min}
- Y_{opt} : Source admittance yielding NF_{min} — scaled by $(1/W)$
- R_n : Sensitivity of NF when Y_s differs from Y_{opt} — scaled by W

Motivation *(Continue)*

(Tuned LNA Architecture)



$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \omega_T L_s$$

$$NF = 1 + \gamma g_{d0} \chi \frac{G_s}{G_s^2 + B_s^2} \left(\frac{\omega_0}{\omega_T} \right)^2$$

$$\chi \triangleq 1 + 2|c| G_s \kappa + \left[G_s^2 + (B_s + \omega_0 C_{gs})^2 \right] \kappa^2$$

$$\kappa \triangleq \frac{\omega_T}{\omega_0^2 C_{gs}} \sqrt{\frac{\delta g_g}{\gamma g_{d0}}}$$

- Shorter L yields lower NF.
- Power/Noise matching conditions are different from the MOSFET.

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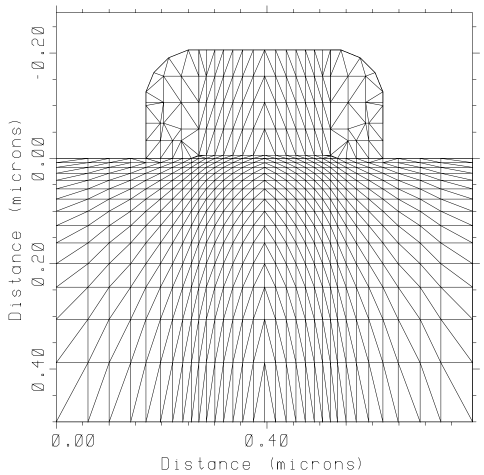
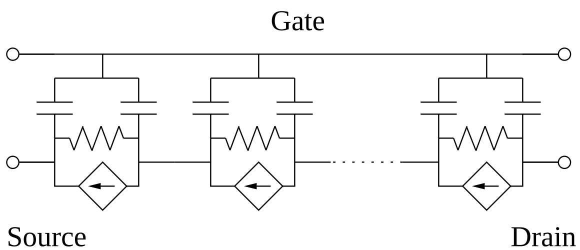
Motivation *(Continue)*
(MOSFET Noise)

- Flicker (*1/f*) Noise
  - ✧ Dominant up to few MHz range.
  - ✧ Significant in mixer circuits (Up-conversion Error).
- Shot Noise
  - ✧ Dominant in the subthreshold region.
- Thermal Noise (Velocity Fluctuation Noise)
  - ✧ Dominant in high frequencies (LNA).
  - ✧ Drain noise + Induced gate noise.

Intrinsic MOSFET Noise

(Thermal Noise Simulation Method)





TSUPREM4 → **MEDICI** → **MONO**

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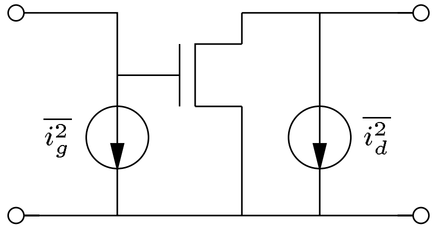
Intrinsic MOSFET Noise *(Continue)*

(Noise Parameters for 0.25μm MOSFET)



$$\gamma = \frac{\overline{i_d^2}}{4\,k\,T\,\Delta f\, g_{d0}}$$

$$\delta = \frac{\overline{i_g^2}}{4\,k\,T\,\Delta f\, \Re[Y_{GS}]}$$

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2}\,\overline{i_d^2}}}$$

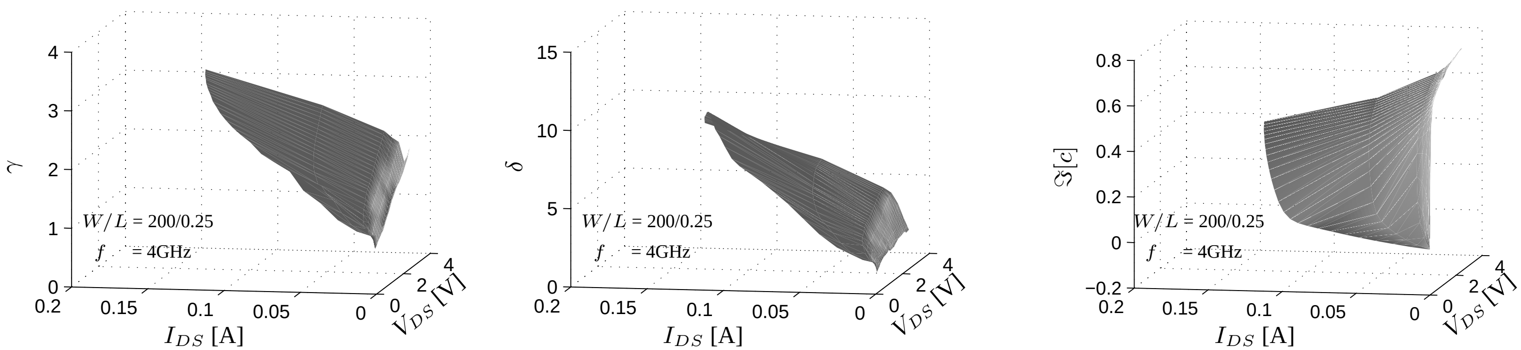
Classical Values

$\gamma = 1.0$ (Linear)

$= 2/3$ (Saturation)

$\delta = 4/3$ (Saturation)

$c = j0.395$ (Saturation)



✧ Good agreement with Toshiba 0.25μm nMOSFET

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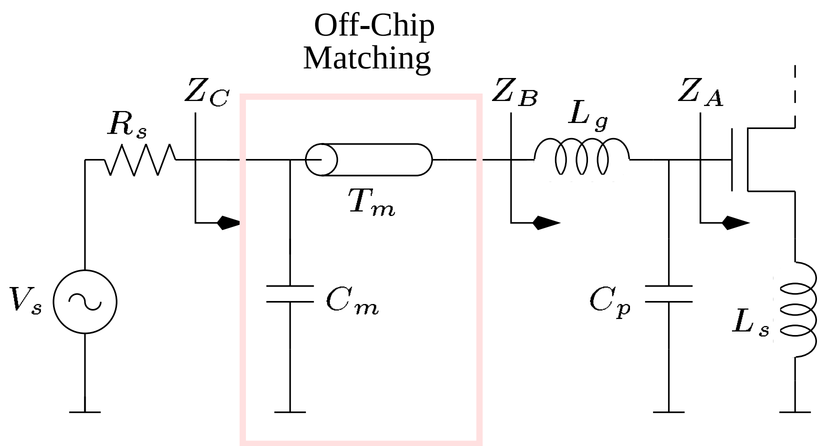
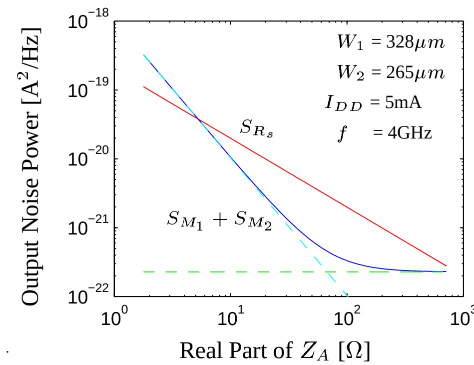
Tuned LNA

(Power Matching)

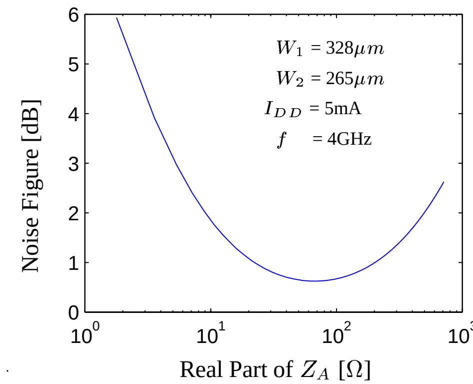




$$G_{m_1} = \frac{1}{2}\frac{1+\Gamma_B}{e^{j\beta l}+\Gamma_B e^{-j\beta l}}\frac{(1/sC_p||Z_A)}{Z_B}\frac{1/sC_{gs_1}}{Z_A}g_{m_1}$$

When $Z_C = R_s$

$$G_{m_1} = \frac{1}{2\sqrt{\omega_T L_s R_s}}\left|\frac{g_{m_1}}{sC_{gs_1}}\right|$$



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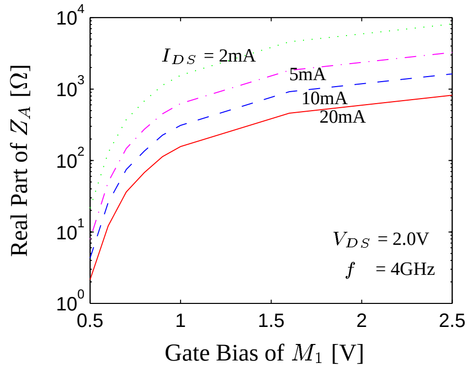
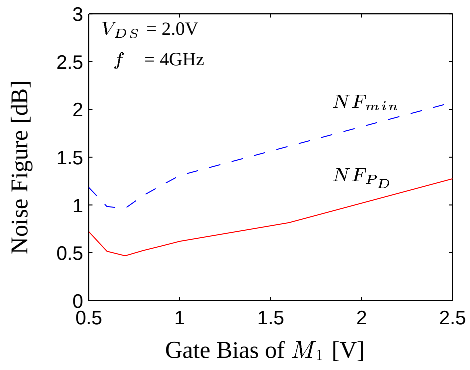
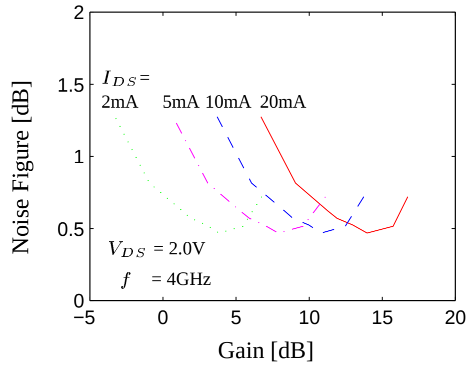
Tuned LNA *(Continue)*

(Power Matching)



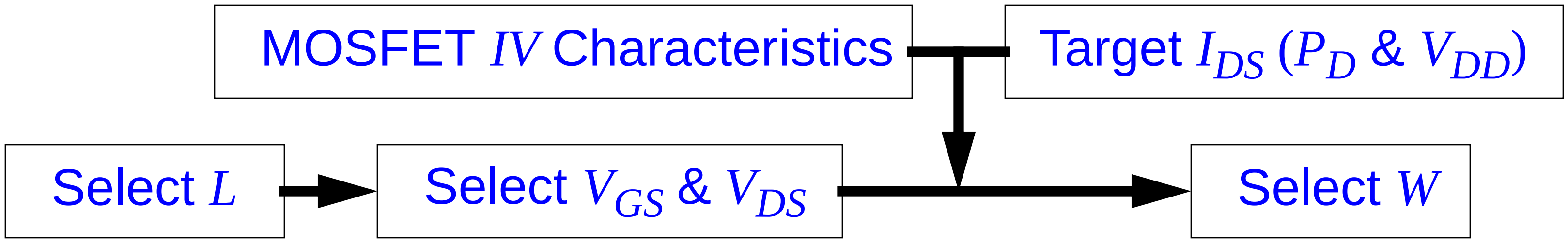


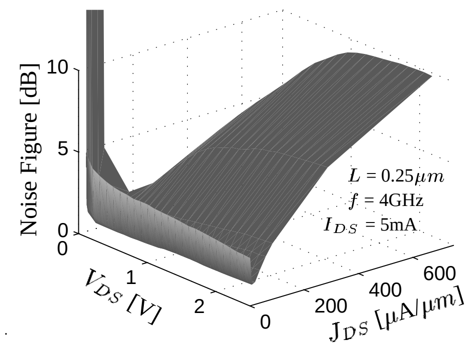


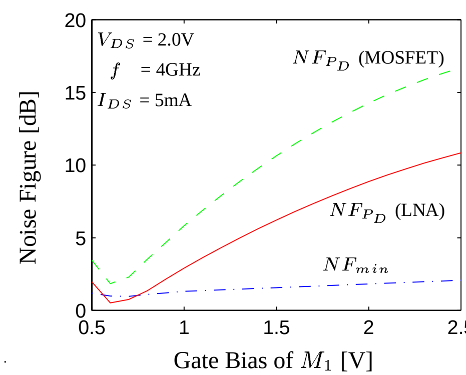
- Optimum L_s is bias dependent and linearly scaled by the current specification.
- The achievable noise figure is independent of the current specification and quite close to the intrinsic NF_{min}.

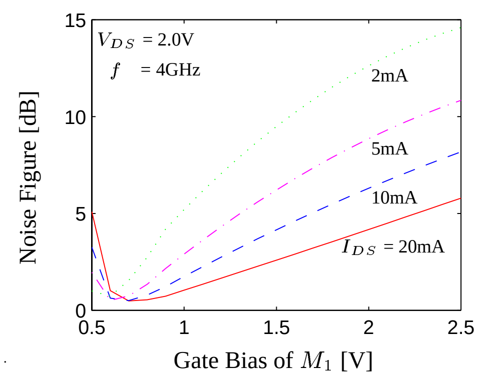
Tuned LNA *(Continue)*

(Power Contrained Noise Figure)









$$NF \approx 1 + \frac{\gamma g_{d0}}{G_s}\left(\frac{\omega_0}{\omega_T}\right)^2 + G_s \frac{\delta\zeta}{g_{d0}}$$

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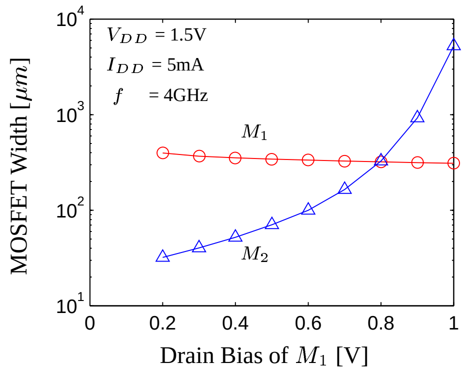
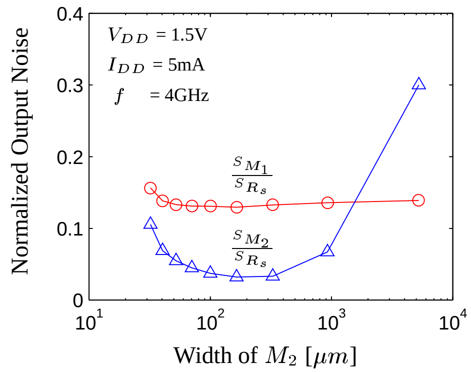
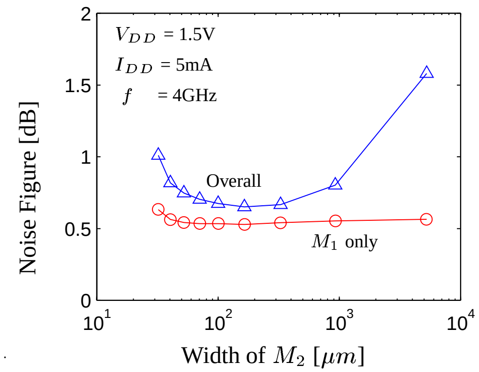
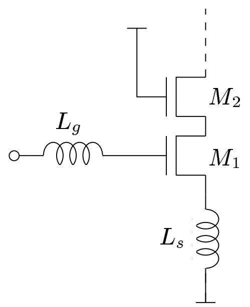
Tuned LNA *(Continue)*

(Cascode Stage)









- Cascode device noise is not significant.
- Drain noise is dominant in M_2.
- $W_1 = W_2$ is OK.

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Conclusions

- Tuned LNA can achieve near NF_{min} at optimum V_{gs}.
- Simultaneous choice of V_{gs} and width of input stage is most critical in design : optimum V_{gs} is usually 0.1~0.3V above V_{th}.
- Cascode stage is not significant. W_1=W_2 is OK.
- Overall NF is affected by L_s : optimum L_s exists.
- Optimal choice of L_s can achieve the noise figure quite close to the intrinsic NF_{min}.