

## Guidelines for the Power Constrained Design of a CMOS Tuned LNA

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### I. INTRODUCTION

The first stage of a receiver is typically an LNA (Low Noise Amplifier) which needs to provide sufficient gain while introducing as little noise as possible. The classical noise optimization technique for LNA design presumes that a device is given with fixed characteristics, and thus offers no explicit guidance on how to best exercise the IC designer's freedom in tailoring device geometries [1].

Recently proposed noise optimization techniques for CMOS RF circuits permit greater flexibility in selection of device geometries as well as matching elements and biasing conditions to minimize the noise figure for a specified gain or power dissipation [1]. Nevertheless such approaches still have ambiguity because intrinsic noise is assumed to be bias-independent. To utilize the new degrees of freedom in noise figure optimization, more complete intrinsic noise information of MOSFETs across the entire bias range is needed. A recent study has reported extensive experimental noise results of the  $0.75 \mu\text{m}$  SOI MOSFET technology [2] but it provided limited guidance for actual LNA design.

A physical noise simulator has been developed using two-dimensional device simulation; successful noise simulation results have been reported for MOSFETs with channel lengths down to  $0.25 \mu\text{m}$  for the first time [3]. Based on intrinsic high frequency noise simulation results, this paper presents explicit design guidelines for a CMOS tuned LNA with power constraints.

### II. HIGH FREQUENCY NOISE PERFORMANCE OF MOSFETs

The thermally noisy channel charge produces effects that are modeled by drain and gate current noise generators [4]. These currents are partially correlated with each other because they share a common origin, and possess spectral power given by the following equations:

$$\overline{i_d^2} \triangleq 4kT\Delta f\gamma g_{d0} \quad (1)$$

$$\overline{i_g^2} \triangleq 4kT\Delta f\delta g_g \quad (2)$$

$$c \triangleq \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2} \overline{i_d^2}}} \quad (3)$$

where  $g_{d0}$  is the drain output conductance under zero drain bias and  $g_g \triangleq \zeta \frac{\omega^2 C_{gs}^2}{g_{d0}}$  is the real part of input admittance. For long-channel MOSFETs, noise parameters ( $\gamma$ ,  $\delta$ ,  $c$ , and  $\zeta$ ) in saturation are  $2/3$ ,  $4/3$ ,  $j0.395$ , and  $1/5$ , respectively [1]. For quite some time, however, it has been known that short-

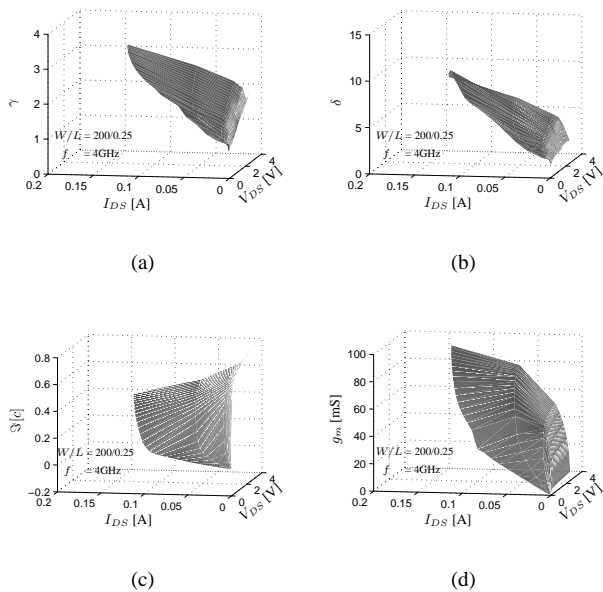


Fig. 1. Intrinsic noise parameters for the entire operating range of  $0.25 \mu\text{m}$  nMOSFET. (a) Drain noise parameter ( $\gamma$ ). (b) Gate noise parameter ( $\delta$ ). (c) Cross correlation between the drain and the gate noise (the imaginary part of c). (d) Transconductance ( $g_m$ ).

channel nMOSFETs in the saturation region exhibit considerably larger broadband RF noise than predicted by long channel theory [5]. This observation has led to speculation that unacceptably poor noise performance might accompany scaling to smaller dimensions. Fig. 1 shows simulated intrinsic noise parameters across the entire operating range. These results have shown good agreement with measured noise performance of an industrial  $0.25 \mu\text{m}$  nMOSFET [3].

The noise performance of a linear circuit is usually characterized by four noise parameters [6] as follows:

$$NF = NF_{min} + \frac{|Y_s - Y_{opt}|^2 R_n}{G_s} \quad (4)$$

where  $NF_{min}$  is the best performance that the circuit can achieve with the optimum source admittance condition ( $Y_s = Y_{opt}$ ), and  $R_n$  determines the sensitivity of  $NF$  when  $Y_s$  differs from  $Y_{opt}$ . Fig. 2 shows the intrinsic noise performance of the MOSFET for the entire operating range using the four noise parameters. Those characteristics are directly transformed from noise factors in Fig. 1 by combining them with network parameters that are secondary outputs of the noise simulator.

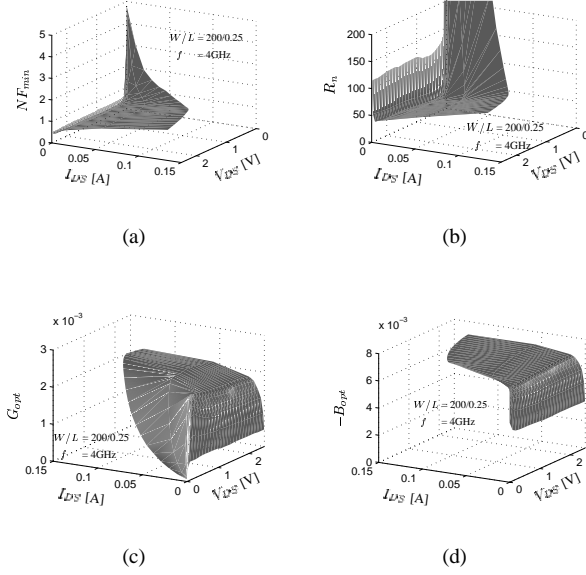


Fig. 2. Intrinsic noise performance for the entire operating range of a 0.25  $\mu\text{m}$  nMOSFET. (a) Minimum noise figure ( $NF_{min}$  [dB]). (b) Equivalent noise resistance ( $R_n$  [ $\Omega$ ]). (c) Optimum source conductance ( $G_{opt}$  [S]). (d) Optimum source susceptance ( $B_{opt}$  [S]).

Fig. 2 (a) and (b) show drastic increases of  $NF_{min}$  and  $R_n$  in the linear region ( $V_{DS} < V_{DSat}$ ); a similar increase of  $R_n$  is observed for low gate bias ( $V_{GS} \approx V_{th}$ ). Such results are mainly attributed to low  $g_m$  as well as a poor correlation factor (c), and suggest that those bias ranges are highly undesirable for circuit implementation. Even in the saturation region, despite good values of  $NF_{min}$  (below 1dB), actual circuit noise performance can easily be degraded due to small  $G_{opt}$  (corresponding  $|\Gamma_{opt}|$  is nearly 1) as well as large  $R_n$  (three to ten times larger than HEMTs [2]). Another observation is that  $NF_{min}$  in Fig. 2 (a) shows negligible drain bias dependence while  $\gamma$  and  $\delta$  in Fig. 1 exhibit substantial drain bias dependence.

In the saturation region for MOSFETs, the four noise parameters can be approximated as:

$$NF_{min} \approx 1 + \frac{\omega}{\omega_T} \sqrt{\gamma \delta \zeta (1 - |c|^2)} \quad (5)$$

$$R_n \approx \frac{\gamma g_{d0}}{g_m^2} \quad (6)$$

$$G_{opt} \approx \frac{g_m \omega C_{gs}}{g_{d0}} \sqrt{\frac{\delta \zeta (1 - |c|^2)}{\gamma}} \quad (7)$$

$$B_{opt} \approx -\omega C_{gs} \left( 1 + |c| \frac{g_m}{g_{d0}} \sqrt{\frac{\delta \zeta}{\gamma}} \right) \quad (8)$$

Equation (5) suggests that the shorter devices yield better noise figures because  $\omega_T$  is proportional to  $1/L_{eff}^2$  while  $\sqrt{\gamma \delta \zeta (1 - |c|^2)}$  becomes at most 6.5 times larger than the

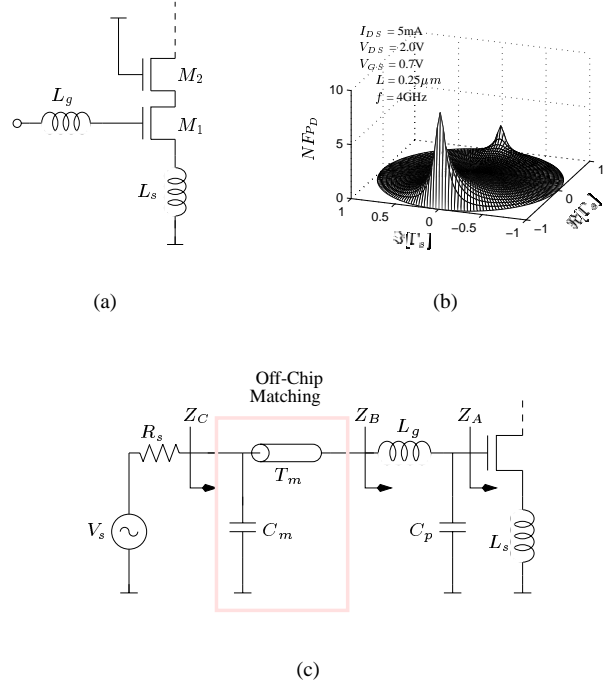


Fig. 3. (a) Tuned LNA architecture employing inductive source degeneration. (b) Dependence of amplifier's noise figure on the source admittance [dB]. (c) Complete schematic diagram of the LNA including off-chip matching circuit. (d) Dependence of output noise power components on  $\Re[Z_A]$ . (e) Noise figure of the LNA as a function of  $\Re[Z_A]$ .

long channel case, down to 0.25  $\mu\text{m}$ . The small drain bias dependence of  $NF_{min}$  also can be explained by (5) since increases of  $\gamma$  and  $\delta$  are mitigated by increasing  $g_m$  and  $c$ .

### III. NOISE PERFORMANCE OF A TUNED AMPLIFIER

#### A. Amplifier Architecture

The tuned amplifier illustrated in Fig. 3 (a) is one of the most broadly used LNA architectures because it offers great potential for achieving the best noise performance. The input impedance of the amplifier in Fig. 3 (a) is:

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \omega_T L_s \quad (9)$$

By choosing  $L_s$  and  $L_g$  independently, the desired input impedance can be obtained for a narrowband. Assuming the intrinsic noise parameters to be constant, Shaeffer *et al.* [1] presented an analytical noise optimization of this architecture that fully utilized design flexibility in the selection of device geometries and bias conditions. Circuit designers might want to understand the noise behavior of the LNA based on the four noise parameters. Unfortunately, as shown in Fig. 3 (b), the noise figure of this architecture exhibits a complex dependence on the source admittance that cannot be simply described by the classical  $F_{min} - R_n - Y_{opt}$  representation.

It is known that the source inductance controls the noise performance of the given architecture [7]. To understand this phenomenon, an off-chip tuner is introduced as shown in Fig. 3 (c). In fact, the off-chip tuner may be required in many practical situations because of poorly controlled elements such as bondwire inductors. When the tuner transforms  $Z_B$  such that  $Z_C = R_s$ , the input stage gain  $G_{m1}$  is affected only by the source inductor  $L_s$ . Then the noise figure of the amplifier is:

$$NF = \frac{S_{R_s} + S_{M_1} + S_{M_2}}{S_{R_s}} \quad (10)$$

$$S_{R_s} = 4kTR_s |G_{m1}|^2 |A_{i2}|^2 \quad (11)$$

$$S_{M_1} = 4kT\gamma_1 g_{d01} \chi |A_{i2}|^2 / 4 \quad (12)$$

$$S_{M_2} = 4kT\gamma_2 g_{d02} \xi \quad (13)$$

$$|G_{m1}| = \frac{\omega_T}{2\omega_0 \sqrt{\omega_T L_s R_s}} \quad (14)$$

$$A_{i2} = i_{out2} / i_{out1} \quad (15)$$

$$\chi \triangleq 1 - 2\omega_0 L_s g_m |c| \kappa + (1 + \omega_0^2 L_s^2 g_m^2) \kappa^2 \quad (16)$$

$$\kappa \triangleq \frac{1}{\omega_0^2 C_{gs1} L_s} \sqrt{\frac{\delta_1 g_{g1}}{\gamma_1 g_{d01}}} \quad (17)$$

$$\xi \triangleq \eta (g_{ds1}^2 + \omega_0^2 C_{tot}^2) + \eta^2 \rho \tau + \eta \tau^2 \quad (18)$$

$$\eta \triangleq \frac{1}{(g_{ds1} + g_{m2})^2 + \omega_0^2 C_{tot}^2} \quad (19)$$

$$\rho \triangleq 2\omega_0 C_{tot} g_{m2} |c| [(g_{ds1} + g_{m2})^2 + \omega_0^2 C_{tot}^2] \quad (20)$$

$$\tau \triangleq g_{m2} \sqrt{\frac{\delta_2 g_{g2}}{\gamma_2 g_{d02}}} \quad (21)$$

$$C_{tot} \triangleq C_{db1} + C_{sb2} + C_{gs2} \quad (22)$$

In Fig. 3 (d), as the real part of  $Z_A$  increases, the output noise contributions from the source resistance and the induced gate noise of  $M_1$  monotonically decrease because of  $G_{m1}$ , while other contributions from the FETs are constants. Hence the LNA yields the best noise figure where the  $L_s$ -dependent term and  $L_s$ -independent term give equal contributions, as shown in Fig. 3 (e).

### B. Power Constrained Design

When the supply voltage and power consumption are fixed, the device width of the input stage corresponding to each bias

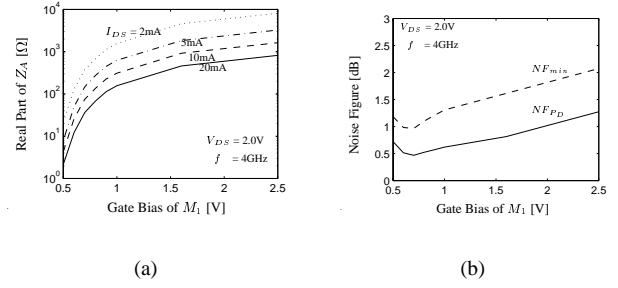


Fig. 4. (a) Optimum  $\Re[Z_A]$  yielding the best noise figure of the given bias. (b) Power constrained noise figure of the LNA with optimum  $\Re[Z_A]$ .

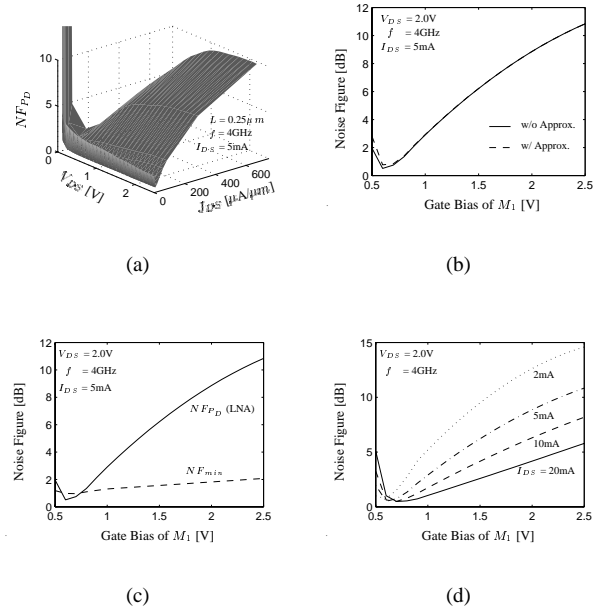


Fig. 5. Power constrained noise figure ( $NF_{PD}$  [dB]) of the tuned amplifier when  $R_s = Z_{in} = 50\Omega$ ,  $L = 0.25\mu m$ , and the current is fixed to 5mA. (a) For the entire operating range. (b) Comparison to the approximation. The solid line is the actual noise figure; the dashed line is the approximated results using (23). (c) Comparison to the intrinsic  $NF_{min}$  of the MOSFET. (d)  $NF_{PD}$  for different current specifications.

condition can be easily calculated from the current density. As shown in Fig. 4 (a), the optimum  $L_s$  is bias dependent and scales linearly with the specified current. However, the noise figure, that is achievable by optimizing  $\Re[Z_A]$ , is independent of the current specification and much lower than the intrinsic  $NF_{min}$  as shown in Fig. 4 (b). Therefore, employing a tuner or an arbitrary value of  $R_s$  allows great flexibility in amplifier design. However, allowing a large range of  $L_s$  is often impractical; in this case choosing an appropriate bias condition becomes critical.

Fig. 5 (a) shows the power constrained noise performance of the LNA for the entire operating conditions with a perfectly matched input impedance of  $50\Omega$ . It exhibits a deep

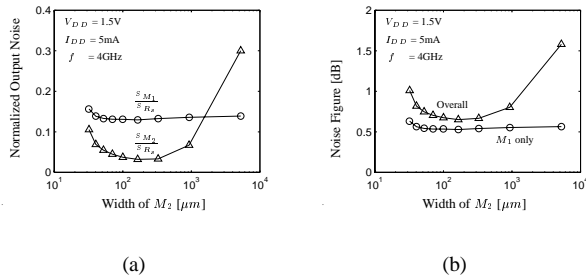


Fig. 6. (a) Output noise contribution of each transistor in the cascoded LNA. (b)  $NF_{PD}$  of the cascoded amplifier in comparison with the non-cascoded.

valley-shaped noise figure profile, and suggests that choosing an appropriate gate bias is critical; somewhat better  $NF_{PD}$  can be achieved by reducing drain bias. If we can ignore the correlated portion in (16), the amplifier noise figure can be approximated as follows:

$$NF \approx 1 + \frac{\gamma g_{d0}}{G_s} \left( \frac{\omega_0}{\omega_T} \right)^2 + G_s \frac{\delta \zeta}{g_{d0}} \quad (23)$$

The comparison in Fig. 5 (b) shows that the approximate formula replicates the original noise characteristics. This formula explains the valley-shaped noise behavior using two independent noise contributions. One originates from the drain noise and is dominant when the gate bias is low. The other contribution originates from the induced gate noise and becomes dominant at higher gate bias. When the current is fixed, these two components have the opposite gate bias dependence to each other; the noise figure thus has minima where they contribute equally to the noise figure. This fact highlights the importance of accurate gate noise modeling for circuit design.

Despite the large gate bias dependence, Fig. 5 (c) demonstrates that for a given tuned amplifier architecture, noise performance better than  $NF_{min}$  can be achieved for a narrow range of gate bias. Although optimum  $Q_L \triangleq (\omega_0 R_s C_{gs})^{-1}$  and its corresponding  $V_{GS}$  decrease as the given power budget becomes smaller, Fig. 5 (d) shows that the achievable noise figure stays about the same regardless of the current specification. It also suggests that the best  $NF_{PD}$  is acquired in the range of  $0.1 \sim 0.3\text{V}$  above the threshold voltage, depending on the power specification. Achieving an exact optimal bias point requires accurate noise modeling or measurement, especially for ultra low power design. The low power LNA design becomes a compromise between the linearity and the noise performance.

### C. Cascode Stage

Adding a cascode stage is a common practice in amplifier design because it improves the stability by shielding the input device from voltage variations at the output. For a fixed current, the size of the cascoding device  $M_2$  ( $W_2$ ) determines

the operating condition and changes slightly the size of  $M_1$  ( $W_1$ ). When  $C_{gb}$  and  $C_{db2}$  are ignored, Fig. 6 suggests that the optimal choice of  $W_2$  is about equal to  $W_1$  and the noise contribution of  $M_2$  is not significant for a wide range of  $W_2$ . Note that the gate noise contribution is extremely small compared with the drain noise contribution in the cascode stage. Although Fig. 6 (b) shows that  $M_2$  adds at least 0.1dB of noise to  $M_1$ , the noise figure of the cascoded design is not worse than the actual non-cascoded case because  $M_1$  produces more noise under the same power supply voltage due to the increased drain bias.

## IV. CONCLUSION

Based on extensive high-frequency noise simulations for a  $0.25 \mu\text{m}$  nMOSFET for the entire operating range, this paper presents explicit design guidelines for a CMOS tuned LNA, given a power constraint. The noise behavior of the LNA cannot simply be described based on the conventional  $F_{min} - R_n - Y_{opt}$  representation. The best noise figure is achieved by optimizing the source inductance and its value is much lower than  $NF_{min}$ , regardless of the current specification. When the choice of the source inductance is restricted, the simultaneous choice of gate bias and device width is very critical. Nonetheless noise figure lower than  $NF_{min}$  can still be achieved. Usually, for  $50\Omega$  input match, the best noise figure is realized in a bias range of  $0.1 \sim 0.3\text{V}$  above the threshold voltage, depending on the power specification. The noise contribution of a cascoding device is usually not significant and its optimal width is about equal to that of the input device.

## ACKNOWLEDGMENTS

This project was initiated by DARPA under contract Army-DABT63-94-C-0055 and then supported by Texas Instruments through customized research under SRC contract 99-NJ-695.

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## CORRECTION

Figure 3 (b) and its interpretation in the first paragraph in p. 271 are wrong. The noise performance of the LNA also can be described by the classical  $F_{min} - R_n - Y_{opt}$  representation. The mathematical derivations are correct but there was a minor error in the actual calculations.