A Computationally Stable Quasi-Empirical Compact Model for the Simulation of MOS Breakdown in ESD-Protection Circuit Design

Shiang Liang Lim[#], Xin Yi Zhang, Zhiping Yu, Stephen Beebe[*], and Robert W. Dutton
[#]Now with Tritech Microelectronics, Singapore
Center for Integrated Systems, Stanford University, Stanford, CA 94305
[*]Advanced Micro Devices Inc. Sunnyvale, CA 943088-3453

Abstract -- This paper presents a simple-to-implement, semi-empirical model for circuit-level simulation of the MOS breakdown region, with application in ESD-protection circuit design. A new formulation for the multiplicative factor M, used to model avalanche current generation, shows good convergence properties when used in circuit simulators. The effects of source/drain series resistance, substrate resistance, and the parameters of the new M expression are described. We describe how to calibrate the parameters for a NMOS device. Finally, we compare the simulated results with experimental data.

I. INTRODUCTION

Modeling a transistor's I-V characteristics in the breakdown region is important for the design of electrostatic discharge (ESD) protection circuits. During an ESD stress, current and voltage levels far exceed the regions of normal transistor operation. The ability to model such high-current behavior in circuit simulators enhances fast and effective design of such protection circuits.

The MOS breakdown region can be modeled with a parasitic bipolar transistor in parallel with the MOS device, together with a current-controlled current source that models the avalanche multiplicative effect [1]. Avalanche occurs near the drain region because of the high electric field, which causes electron-hole pair generation. The electrons flow into the drain while the holes flow through the substrate contacts.

The substrate current creates a potential drop across the substrate-source junction, and eventually turning on the parasitic NPN bipolar transistor (BJT) formed by the drain-substrate-source junctions. This in turn conducts more current and creates more avalanche-generated carriers. The positive feedback process causes the total drain current to increase sharply above the drain breakdown voltage.

Fig. 1 shows a standard circuit used to model this breakdown. The avalanche-generated current is modeled as [1]:

$$\mathrm{Igen} = (\mathrm{M} - 1) \cdot (\mathrm{Ids} + \mathrm{Ic}) \tag{1}$$

where Ids is the MOS surface drain current, and Ic is the parasitic bipolar (BJT) collector current. The multiplication factor, M, is often written in the following form [2]:

$$\mathrm{M} = \frac{1}{1 - \mathrm{K1}\exp\left[-\frac{\mathrm{K2}}{\mathrm{Vd} - \mathrm{Vdsat}}\right]} \tag{2}$$

where k1, k2 are fitting parameters related to the drain depletion width and impact ionization coefficients, and Vdsat is the MOS saturation voltage. At low Vd, M is 1 or close to 1; it increases as Vd increases.

A drawback for the above expression for M is that it causes convergence problems when implemented directly in a circuit simulator such as SPICE. As Vd increases, the denominator goes to zero, thereby creating a discontinuity in M as it goes to infinity. If the initial Ids and Ic are very small, as is the case when Vg is close to 0V, the parasitic bipolar will fail to turn on because the iterations may "jump" across the discontinuity. This causes SPICE to either simulate the wrong behavior or fail to converge. We observe similar problems even when Vg is more than 0.1V if the drain current step increment for the simulation is too large.

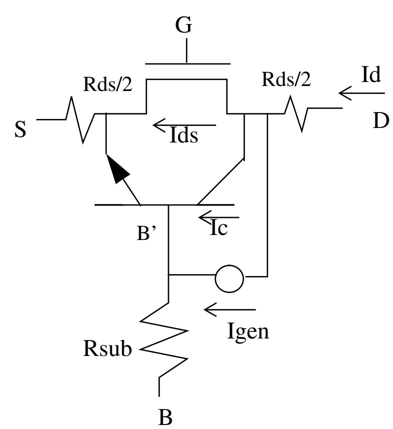

Fig. 1 Circuit schematic for simulating MOS breakdown.

Improving the convergence properties of the breakdown model would increase its usefulness and range of application. In the next section, we introduce an alternative M formulation that is more robust and simple to implement. We then describe the effects of each parameter in this new M expression, of the source/drain series resistance, and of the substrate resistance on the breakdown I-V characteristics. Next, a qualitative description of how to obtain the required parameters from experimental data is given. Finally, the simulated results are compared with measurement.

II. ALTERNATIVE M FORMULATION

The discontinuity in M can be overcome by using a continuous function:

$$M = \exp[k1(Vd - Vdsat - d1)] + \exp[k2(Vd - Vdsat - d2)] \tag{3}$$

where k1, d1, k2, d2, are parameters used to fit measurements. Two exponentials are used to approximate the M function from (2) in the region of interest, namely from M=1 to the point where snapback occurs. The first exponential should have a slower rate of increase relative to the second one (0<k1<k2), but "activated" earlier (0<d1<d2). The result is a reasonably smooth I-V transition from the saturation region to the start of avalanche and snapback. This formulation shows better convergence properties than (2) because of its continuity, and produces the correct I-V behavior even at Vg=0V, without any modification to the SPICE code. This makes it simple to implement and more robust. Like (2), it incorporates the effects of normal field dependence and saturation velocity through Vdsat, which to first order is given by [3]:

$$Vdsat = \frac{Vg - Vt}{1 + \dfrac{(Vg - Vt)}{L \cdot Esat}} \tag{4}$$

where L is the channel length, Vt is the device threshold voltage, and Esat is the saturation electric field.

III. ANALYSIS OF PARAMETERS

The k1 and k2 in (3) determine the rate of increase of M while d1 and d2 are translation factors which determine when avalanche multiplication starts to take place. Fig. 2 shows a comparison between the M factor from (2) and (3). The discontinuity in the old M occurs around Vds=9V, which is the trigger voltage. The new M matches the old one at the trigger voltage and the holding voltage (Vds=5.5V), thus ensuring similar trigger and holding points in the IV snapback curves. We can clearly see the two regions where each of the exponential functions is dominant.

As shown in Fig. 3, K2 affects the "width" of the snapback region, i.e. Vtrigger - Vhold, for Vg=0V. This can be explained by first noting that since the total generated current is very small, a sufficiently high M is needed to generate enough substrate current to forward-bias the parasitic BJT [1]. Our simulations show that this occurs for Vb'~0.8V. Since M increases more slowly for a smaller k2, a higher Vd is needed to achieve the required M.

Since d2 determines when the avalanche multiplication starts generating electron-hole pairs significantly, we expect it to shift the snapback trigger point correspondingly as shown in Fig. 4.

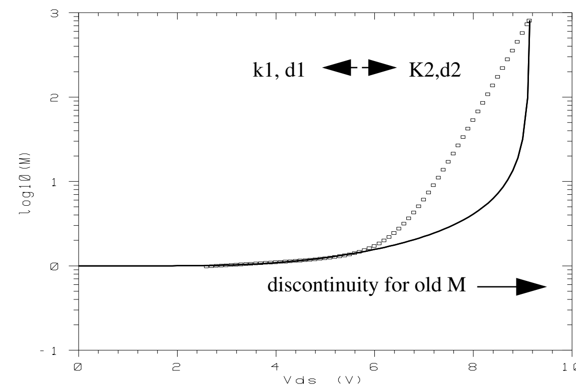

Fig. 2 Comparison between old, discontinuous M (line) and new, continuous M (squares). The point of discontinuity and the region where the new M parameters are dominant, are indicated.

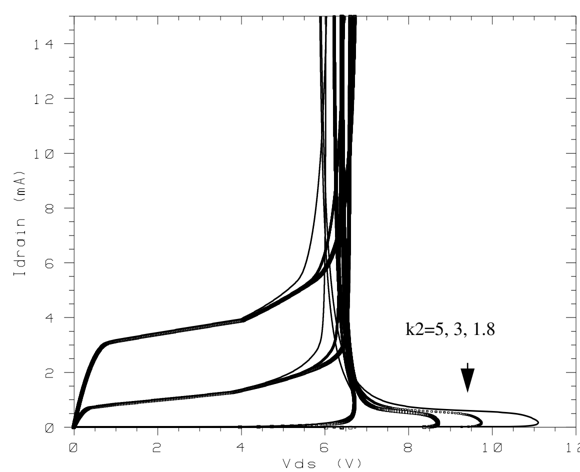

Fig. 3 Variation of snapback width with k2. A lower K2 leads to a wider snapback curve. The gate voltage is stepped from 0V to 1.5V in increments of 0.5V.

Note that for each set of M parameters, at all Vg's, the current level increases rapidly around the same Vd, corresponding to values of M that agree well with a second condition for current regeneration using positive feedback analysis [1]:

$$M = \frac{1}{\beta} \tag{5}$$

where β is the current gain of the parasitic BJT. This corresponds to the case when the current feedback loop gain is +1; hence, the current will increase indefinitely. K1 and d1 affect the M factor between 1 and the point where the current increases dramatically, as given by (5). In other words, k1 and d1 should only matter at the onset of avalanche, by affecting where and how fast the output conductance starts increasing as shown in Figs. 5 and 6.

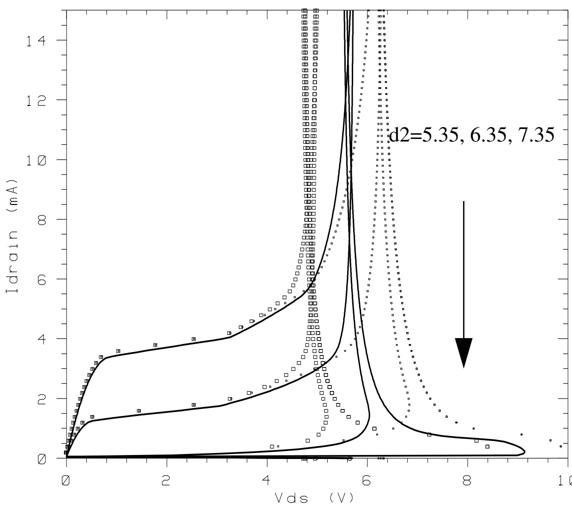

Fig. 4 Variation of snapback trigger voltage with d2. Larger d2 increases snapback trigger voltage.

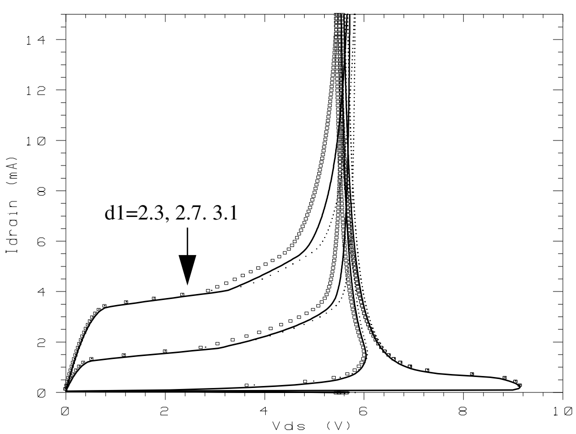

Fig. 5 Effect of d1 on the onset of avalanche. Increasing d1 delays the start of avalanche.

In addition to the M parameters, correctly modeling key resistance such as the substrate resistance (Rsub) is also important, especially in high current regimes. Rsub is the bias resistance for the emitter-base junction of the parasitic BJT. The drain and source resistances (Rds). At high current levels, the extrinsic resistance dominates the intrinsic device resistance and hence determines the I-V slope. To provide more uniform turn on of multi-finger ESD protection structures, increasing Rds is used as a technique for increasing the ballast resistance of the fingers.

Fig. 7 shows that a larger Rsub decreases the "height" of snapback. To turn on the bipolar device at a lower Rsub, a higher trigger currents needed to forward bias the parasitic base-emitter junction. Hence, Rsub can be used as an additional parameter in modeling the snapback region.

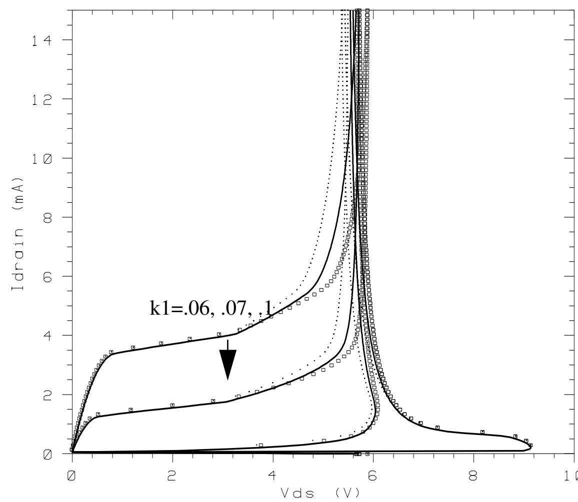

Fig. 6 Effects of k1 on the onset of avalanche. Increasing k1 increases output conductance at the onset of avalanche.

III. CALIBRATION AND RESULTS

Comparison of simulated results using the original M in (2) and the new M formulation in (3) is shown in Fig. 9. The lowest Vg used was 0.12V since (2) does not produce correct behavior for Vg<0.1V. For Vg=0.12V, the snapback curve from (2) is higher than that from (3) because the original M (2) is less than the new expression M (3). Hence, for a given drain current, a higher Vd is required for (2) to produce the same level of avalanche multiplication. In addition, the increase in drain current at the onset of snapback is less abrupt using (3) than (2), a result which is more consistent with measurement data.

Comparison of simulation results with measurements is shown in Figure 10. Tests were done on a 20µ/0.35µ NMOS device. There is a good match for both the triggering voltage and current at Vg=0V. Also, at higher Vg the transition into the avalanche region is good. The avalanche turn-on voltage for the different Vg's corresponds to M ~ 1.3. This is consistent with the use of β=3 in our BJT model (from (4)).

The calibration process begins from the M in (2), which can be extracted using the methodology outlined in [2]. By fitting M near the holding and trigger voltage using k2 and d2 and fitting the output conductance at the beginning of the avalanche using d1 and k1, we can obtain good fit with experiments. In addition, Rsub and Rds can be used to further improve data matching. For our measured device, we used d2=6.7V, $k2=1.8V^{-1}$ and Rsub=1kΩ to achieve an acceptable fit in the snapback region for Vg=0V. For Vd=4V, we used $k1=0.07V^{-1}$ and d1=3.5V to achieve a good fit in that region.

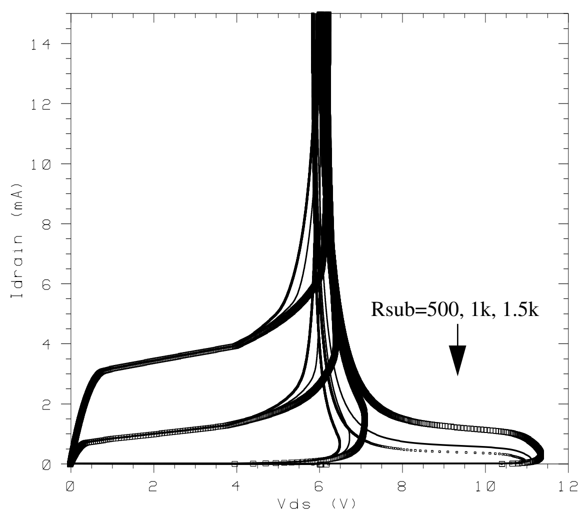

Fig. 7 Variation of snapback height with Rsub. Increasing Rsub decreases snapback height.

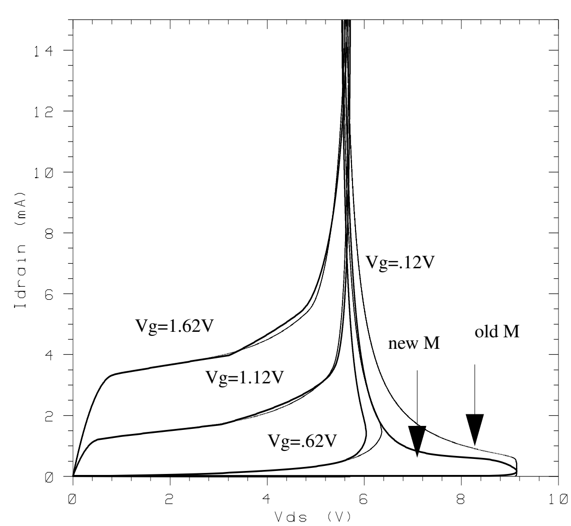

Fig. 9 Comparison of snapback curves obtained using old M (2) and new M (3).

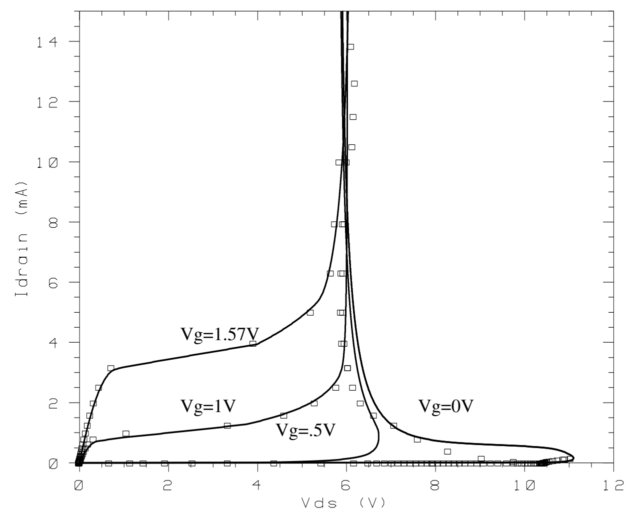

Fig. 10 Comparison of simulation (line) and measurement (square) results.

CONCLUSION

We have presented a more robust, computationally stable formulation for the avalanche multiplicative M factor used in circuit modeling of MOS breakdown. This has useful applications for the design of ESD-protection circuits. Its continuity throughout all voltage range makes it more robust for circuit simulators and improves convergence. The impact of each model parameter on the IV curve was described, and the explanation for these effects are consistent with reported research. Finally, good agreement was obtained by calibrating the model to measurement results.

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