Device/Circuit Simulation for Heterogeneous Technology

Zhiping Yu, Francis Rotella, Boris Troyanovsky, and Robert W. Dutton
Center for Integrated Systems
AEL 204, Stanford University, Stanford, CA 94305, U.S.A.

Key words: device/circuit simulation, S-parameter, optoelectronics, harmonic balance, parasitics

ABSTRACT

The emergence of wireless communication and explosive advancement of the clock frequencies towards the giga-Hz regime in digital circuits demand the heterogeneous technology be employed in IC design and manufacturing. In view of the critical role which parasitics and package play in the circuit performance and applications of mixed digital/analog circuits and optical/electronic devices, a device simulator with extensive circuit analysis and characterization capabilities has been developed. A technique interleaving the analysis in time and frequency domains is described. An S-parameter representation of a linear circuit is coupled to the device simulator, allowing characterization and analysis of parasitics, interconnection, and package together with intrinsic semiconductor devices. Application to the design of GaAs/AlGaAs light emitting diodes and associated driver circuit is shown as an example of the developed software.

INTRODUCTION

The mainstream applications for IC device and circuit simulations are dc, transient, and small signal ac analysis. It is customary to expect that the device simulation can handle only simple circuit boundary conditions such as lumped RC elements and the circuit simulation needs compact models for IC devices as prerequisite. Increasingly, however, this boundary in the functionality between these two tools is blurred, and efforts to develop a mixed-mode device/circuit simulation has been waged for years. At stake are the numerical efficiency and characterization of parasitics. The full-fledged mixed-mode simulation requires considerable computational resources even for circuits with a small number of transistors and transient analysis in time domain is not efficient (and even incapable of practically) in large signal analysis especially for intermodulation distortion analysis. In this paper, we will describe a software environment in which a linear network surrounds a lumped active device(s) which is to be characterized by the device simulator. The linear network can be a representation of parasitics and/or package and may be characterized either by the circuit configuration (as normal R/L/C components) or by S-parameters measurement over a certain frequency range. In such a case, there exists an efficient numerical approach to the analysis. The developed tool has been applied to the design of light emitting diodes made on GaAs/AlGaAs. The detailed analysis results will be shown.

NUMERICAL TECHNIQUE FOR CIRCUIT BOUNDARY CONDITION

In order to conduct the analysis of the entire structure in the framework of device simulation, we need to map the peripheral linear network to the boundary condition acceptable to the device simulation. The general boundary conditions to the device simulation can be classified into two categories: voltage and current boundary conditions. While the expression for the voltage boundary condition is straightforward and does not depend on the external circuit, the current boundary condition in our approach has much broader implication. Basically, we treat all non-voltage boundary conditions as current boundary conditions and they can be expressed in the following general form:

$$\boldsymbol{I}(\boldsymbol{x}) = \boldsymbol{f}(\boldsymbol{V}, \boldsymbol{P}) \qquad \boldsymbol{I}, \boldsymbol{V}, \boldsymbol{f} \in \Re^M, \boldsymbol{x} \in \Re^N, \boldsymbol{P} \in \Re^K \tag{1}$$

where vectors $\boldsymbol{I}$, $\boldsymbol{V}$ represent the terminal currents and voltages for those device contacts which have no direct voltage bias applied. Hence M in the above equation is no more than the number of terminals, a fairly small number. $\boldsymbol{x}$ represents the internal independent variables in the device to be simulated. Since $\boldsymbol{x}$ includes at least the electrostatic potential and carrier concentration(s) at each internal node in the device simulation region, N is usually a very large number, typically several thousands in a 2D device simulation. $\boldsymbol{P}$ represents all the power supply and signal sources and K is the number of the independent sources. The essence of Eq. (1) is that on the one hand the terminal currents can be expressed using the internal variables in the device and on the other hand they are determined by the external circuit, thus Eq. (1) constitutes the equations needed for solving the contact voltages, $\boldsymbol{V}$, in the device simulation. Now the boundary condition problem becomes finding the form of $\boldsymbol{f}$ in Eq. (1). This task can be resolved by tackling the node equations for the external circuit by transforming the non-voltage contacts of the simulated device (or devices) to the voltage source with "known" value of $\boldsymbol{V}$. The goal of this circuit analysis is to find the expression of the currents through these "voltage sources". In a general case, there is no closed form for $\boldsymbol{f}$ available. However, for a linear network, such an analytical form does exist and can be found by solving the external circuit only once. Our algorithmic effort is just aimed at this special class of problems and it turns out that most problems with parasitics fall in this class.

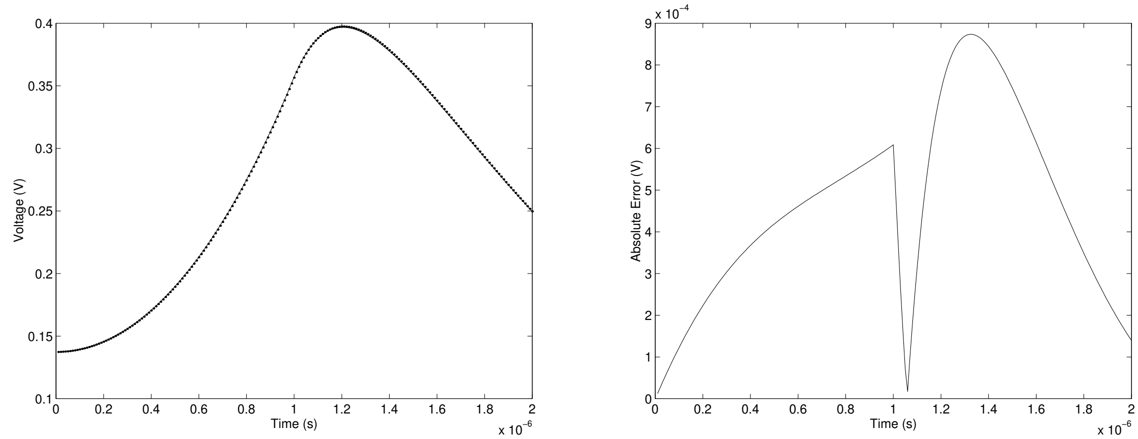
Ideally the peripheral linear circuit is specified by knowing the circuit configuration. But in the parasitic case, due to the distributed nature of the problem it is difficult to extract the equivalent circuit. In the next section, we will describe a methodology of characterizing the passive network using S-parameter measurement and applying this type of characterization in the mixed-mode device/circuit analysis.

CHARACTERIZATION OF LINEAR NETWORK IN FREQUENCY DOMAIN

Parasitics and effects of packaging are easier to measure than to extract for the circuit configuration. Due to the distributed nature of parasitics, it should be characterized over a wide range of frequencies. Among all ac measurement, S-parameters are the choice for high frequency applications. We have developed a methodology in which the peripheral circuit around an active device (or a cluster of devices) is characterized using S-parameters which can be obtained either by measurement or by simulation such as using the EM field solver in the interconnection analysis. This frequency domain characterization is then converted to the impulse response in the time domain using the inverse Fourier transform. As long as the frequency range in which the S-parameters are measured is big enough for the type of parasitics analyzed, this conversion can be done accurately. Once the impulse responses of the peripheral circuit are obtained, they are used in the device simulation to find the time transient response of the entire structure including both the active device(s) and parasitics. The device time transient analysis is performed by the convolution between the signals and impulse response of the parasitics.

The device simulator used in our mixed-mode application has been enhanced to have analysis capabilities in frequency domain in addition to the conventional time transient analysis. In particular, the harmonic balance approach to the large signal analysis has been implemented in PISCES [1], which not only improves the computational efficiency greatly but also is essential for the analysis of intermodulation distortion when multi-tone signals are applied [2].

In the following, we demonstrate the time transient analysis using frequency domain characterization of the peripheral circuit in the mixed device/circuit simulation. The circuit to be analyzed is a simple diode with cathode connected to the ground through a parallel RC branch. The RC branch is characterized using S-parameter as shown in Figure 2, and the simulation is done for the entire set-up using both the plain device simulation by including the RC components as the lumped elements to the device terminal and mixed frequency/time domain analysis. It can be seen in Figure 1 (a) that the results from two methods are almost identical. The maximum discrepancy between two methods is less than 9×10^{-4} V. More realistic test for GaAs MESFETs will be shown in the later publication.



(a) (b)

Figure 1. Comparison of the simulated transient response (a) for a diode with a series RC branch using straightforward device simulation (solid line) and mixed time/frequency domain analysis (dotted line) as described in the text. The agreement is perfect and the discrepancy between two methods is shown in (b).

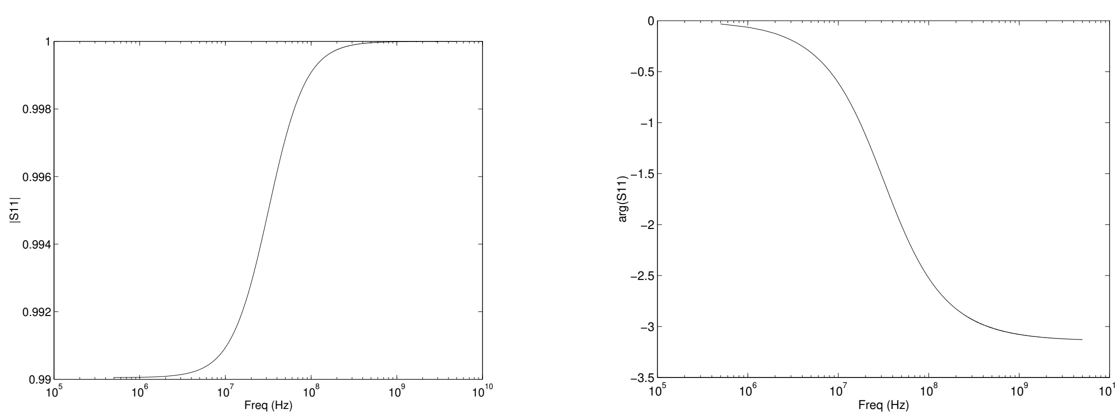


Figure 2. S_{11} for a parallel RC circuit over a frequency range of 5×10^5 to 5×10^9 Hz. The left diagram shows the magnitude and right shows the phase of S_{11}.

A CASE STUDY -- DESIGN OF LIGHT EMITTING DIODES

With the developed software system, designers can optimize a new design and test its performance in a simple circuit. A typical application of heterogeneous technology is the use of an optical device (light emitting diode (LED) in this case) in an electrical circuit which is used in telecommunication.

The example that follows concerns the design improvement of the cylindrical LED shown in Figure 3. The

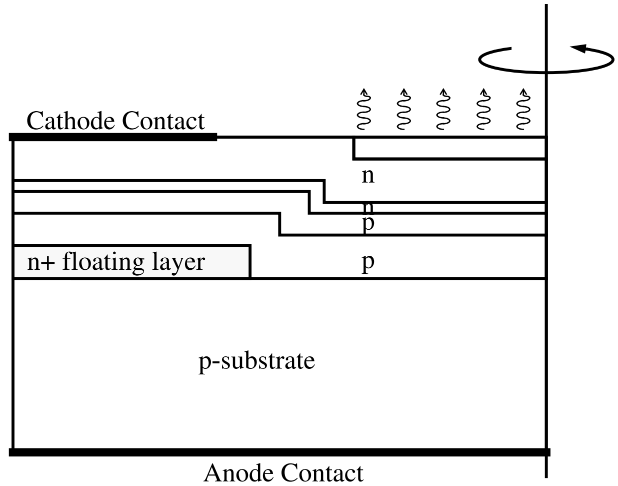


Figure 3. Cross section of the original LED structure. To improve the manufacturability, new design tries to relocate the floating layer on top of the *pn* junction.

n+ floating layer is used to confine the current in the active region where the carrier radiative recombination generates the photon output. The design goal is to improve the manufacturability (i.e. increase the yield and reduce the cost) by relocating the floating layer from beneath the *pn* junction to above and to minimize the leakage current.

With the device simulator which is PISCES in this system, designers can test the impact of various combinations of layer thickness, doping, and Al mole fraction in AlGaAs on the device performance, in particular improving the carrier confinement, reducing the series resistance, and lowering the turn-on voltage where all parameters are measured. The turn-on voltage and resistance can be extracted from the *I-V* characteristics. For the carrier confinement, the solution from PISCES is post-processed to deduce the optical output from the radiative recombination rate. Figure 4 shows the normalized radiative recombination rate for different design parameters: doping level and Al composition. The simulated recombination rate profile for the original device is included as a reference. To examine how close the simulation results are as compared to the experiment data, the measured optical output intensity for the original device is shown in Figure 5. It can be clearly seen that the simulation results (Figure 4) reveal the same feature as the real device behaves, i.e. the peak intensity of the optical output is shifted away from the center of the structure, a phenomenon which may be labeled as the “bat ears”. By examining the simulation results for the new structure, designers can make trade-off among design parameters to achieve the optimal device characteristics.

In addition to the device design, the mixed device/circuit simulation environment allows users to evaluate the device performance in a real circuit and there is no limitation whether a compact model ever exists or not for the device under test. A driver circuit for LED is shown in Figure 6. Even though the direct optical response to the input electrical signal can not be simulated using the present tool[1], the electrical response of the LED is shown favorably as compared to the SPICE simulation using a compact model which has been calibrated by measured data and is used here as experiment. The advantage of using the mixed-model simulation is the direct examination of the impact of structural and processing parameters on the device/circuit performance. This is especially valuable an approach when a novel device emerges in a heteroge-

1. A plan to merge PISCES with MINILASE [3] from University of Illinois is under proposing and full optical and electrical simulation capabilities will be provided.

neous technology where no suitable compact model is available.

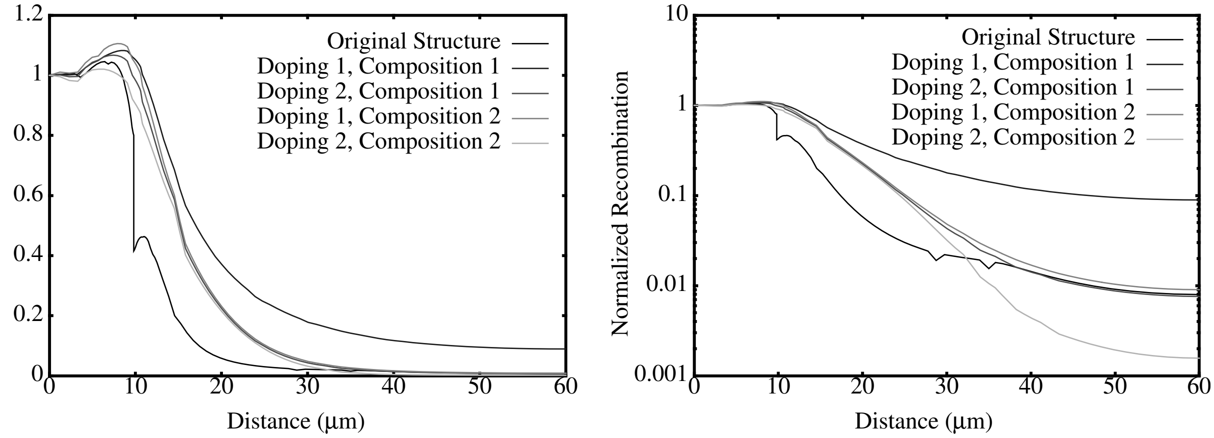


Figure 4. Radiative recombination in the active region as a function of radius in the cylindrical LED structure. Two different doping levels and Al compositions are used for the critical layer. Both improved (left) and original (right) designs are shown.

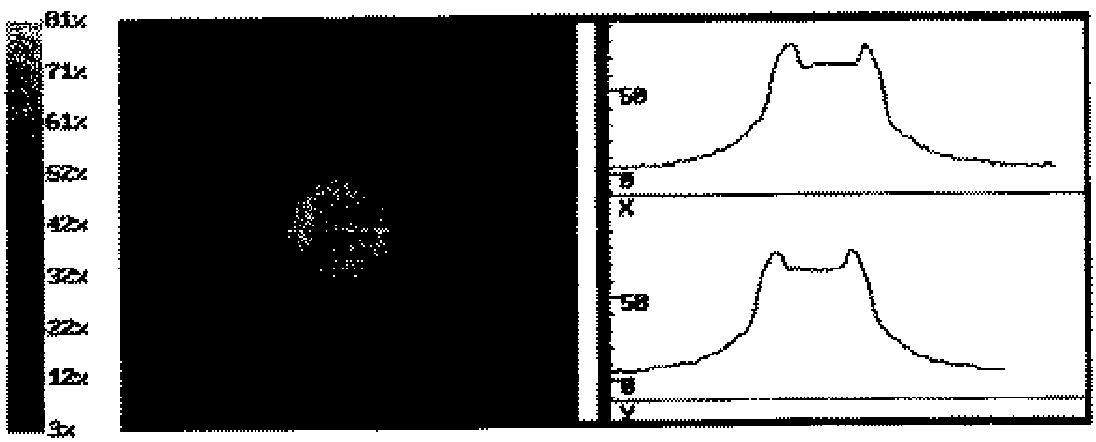
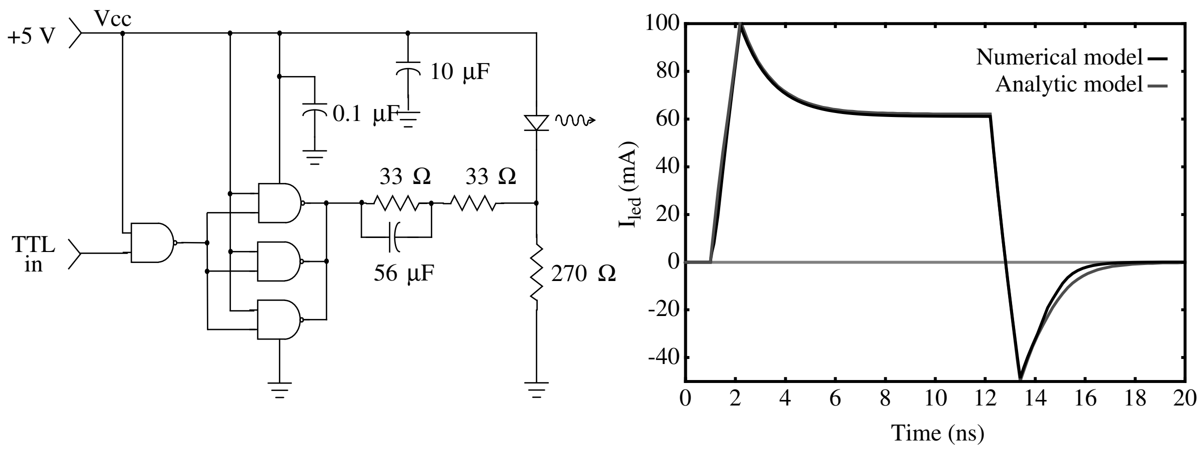


Figure 5. Measured radiation pattern for the original device, showing the intensity of optical output. Note that the peak intensity is not located in the center, a phenomenon the simulation is able to catch accurately.



(a) (b)

Figure 6. The driver circuit for LED (a) and simulated electrical response (b) of the LED from both the mixed device/circuit simulator (i.e. numerical model) and SPICE simulation using the analytic model. The compact model has been calibrated and thus the SPICE simulation can be considered as the same as the measured data. The NAND gates in (a) are modeled using RC switches.

SUMMARY

A 2D device simulator is enhanced to handle extensive linear circuit boundary condition and to have capabilities of conducting frequency domain and mixed frequency/time domain analysis. This mixed device/circuit approach is well suited for the design and analysis of mixed technologies such as the optical telecommunication circuits. A new methodology for characterizing parasitics using S-parameters is also proposed and the overall circuit/device performance can be examined using tools developed. One of the advantages using the proposed approach is the computation efficiency, which is superior to both general mixed device/circuit simulation or pure time domain analysis.

ACKNOWLEDGEMENT

Authors are grateful to the support from various sources including National Science Foundation (ECS-9200560), Semiconductor Research Corp. (SRC 94-SJ-116), Army Research Office (DAAH04-93-G-0178). Collaboration with and contribution from Dr. Chun Lei of Optical Component Division (OCD), HP, is greatly appreciated.

REFERENCES

[1] Z. Yu, D. Chen, L. So, and R. W. Dutton, “PISCES-2ET---Two Dimensional Device Simulation for Silicon and Heterostructures,” Stanford University, Aug. 1994.

[2] B. Troyanovsky, Z. Yu, and R. W. Dutton, “Large signal frequency domain device analysis via harmonic balance technique,” submitted to SISDEP ‘95, Germany, Sept. 1995.

[3] G. H. Song, K. Hess, T. Kerkhoven, and U. Ravaioli, “Two-dimensional simulator for semiconductor lasers,” IEDM Digest, pp. 143-146, Washington D.C., Dec. 1989.