Realization of Digital Noise Emulator for Characterization of Systems Exposed to Substrate Noise

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Abstract- Frequency and timing of digital clocks, digital switching activities, and number of transistors in digital blocks are the key behavior-level parameters to model switching noise generated by complicated digital systems. In this paper, a Digital Noise Emulator (DNE) is implemented on a test chip to study how these parameters impact the performance of a ring-typed-VCO-based PLL. In addition, the proposed DNE can be used for noise cancellation to improve PLL performance in the presence of deterministic noise.

I. Introduction

System-on-a-Chip (SoC) solutions hold promise in reducing the number of large output buffers, lengths of connections between chips, cost of packaging and fabrication, thus leading to improved performance and reduced cost of products. However, as technology evolves, higher operating frequencies, lower power supply voltages, higher transistor density, and integration of different sub-systems on a single chip will complicate signal integrity issues because of crosstalk between the blocks. There are several reports (for example, [1][2]) mentioning that extra effort must be applied to avoid signal integrity issues when integrating sensitive analog/mixed-signal circuits with noisy digital systems. Since the driving force for technology innovation is primarily the cost, it is inevitably a trade-off between how many resources should be allocated in the design and how much benefit can be achieved in realizing SoC applications. Novel approaches to solve signal integrity problems are gaining attention as advocated in ITRS documents [3] and research priorities proposed by SRC [4]. Therefore, characteristics of noise and efficient noise suppression techniques should be studied more extensively in order to support high-performance system design.

Power grid noise and substrate noise are the two major types of digital switching noise (DSN). Although the propagation paths of them are different, the noise contents could be highly correlated due to direct connections between the power grid and substrate through metal contacts. Impacts from power grid noise can be reduced using different supplies for the analog and digital blocks along with decoupling capacitances. However, similar consideration of the substrate leads to the System-in-a-Package (SiP) Technique, which is a different alternative from SoC integration; the battle between the approaches becomes an economic one. The focus of this work will be on how to model DSN in a monolithic substrate, and how to use the model to reduce the impact from DSN in possible SoC applications.

There are reports about how substrate noise affects the performances of the devices or circuits. The components analyzed include MOSFETs, BJTs, sensors, OPAMP, up/down converter, LNA, PLL, and Σ-Δ modulator [5]-[13]. The above list of substrate noise research is not exhaustive. This research will focus on the noise content, and how these it impacts PLL systems. The outline of this article is as follows. Section II proposes a substrate noise model and presents one realization for a digital noise emulator (DNE). Section III provides measurement results from a test chip. Section IV demonstrates a simple technique for canceling deterministic noise using the DNE. The final section summarizes the work.

II. Substrate Noise and Digital Noise Emulator

A. Modeling Substrate Noise

Different digital blocks will have different digital noise signatures [14] in spectra. Deterministic noise generates discrete components in the frequency domain. Continuous spectra are the result of random noise [12]. Therefore, the digital switching noise in the substrate, $N(t)$, should be described as a sum of deterministic, $d(t)$, and stochastic components, $s(t)$:

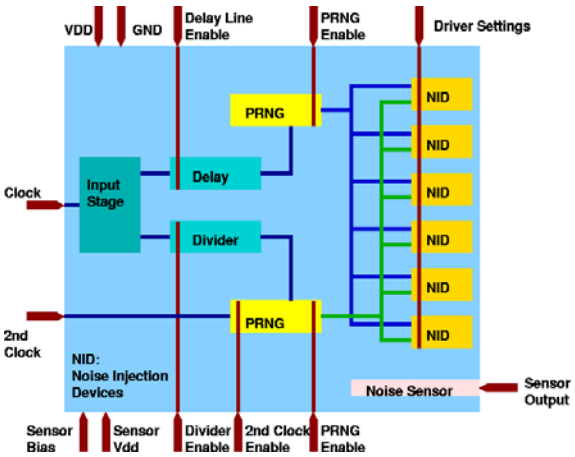

Fig. 1. Block diagram of DNE.

$$N(t) = d(t) + s(t) = \sum_{i=1}^{K} \alpha_i \cos(2\pi \cdot f_i \cdot t + \theta_i) + s(t),$$

where α, f, and θ, are the amplitude, frequency, and phase of deterministic signals from Cosine transforms. Frequency and timing of digital clocks, digital switching activities, and the number of transistors in digital blocks are the parameters which will affect the values of α, f, θ, $s(t)$, and, therefore, the performance of analog/mixed-signal systems. To investigate how system responses to these digital variables, a DNE is proposed for behavior level modeling. The advantage of using the DNE is the controllability of spectral content. It can help to identify different responses caused by different noise parameters efficiently.

For example, in the case of an IEEE 802.11a wireless LAN baseband/MAC processor, the system architecture [15] and measurement data provided by Atheros Communications both indicate that the largest component of its digital switching noise is at the symbol rate, 250 KHz. In behavior level simulations, this complicated system can be replaced by a low-complexity DNE generating a single-tone noise at 250 KHz with added random noise to enhance simulation efficiency. Since the significant components of digital noise spectra are always application and architecture dependent, the concept of using DNE is applicable to most digital designs.

B. Realization of DNE and Measurement Setup

The DNE consists of four major blocks: 1) a deterministic signal generator (CLK), 2) a frequency divider (DIV), 3) a pseudo random noise generator (PRNG), and 4) several noise injection devices (NID).

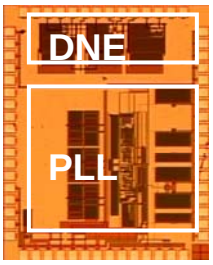

Fig. 2. Micrograph of the DNE and a 200 MHz PLL.

The CLK and DIV are used to generate dual-tone deterministic noise; stochastic behavior, $s(t)$, is emulated by the PRNG; the NIDs, controlling amplitudes, α, are implemented using junction capacitances in different sizes. The detailed architecture (dual-tone) is shown in Fig. 1. Off-chip clocking is recommended because it provides flexibility in selecting clock characteristics, such as frequency, f, phase, θ, and duty cycle. Extending this architecture for multi-tone cases is straight forward, so it will not be repeated here in the paper.

Both software and hardware versions of the DNE are implemented. The software version is realized through Verilog-A HDL. The hardware version of DNE is fabricated next to a 200 MHz PLL using TSMC 0.18 μm 1P6M 1.8 V/3.3 V Logic/Generic technology. Fig. 2 shows a micrograph of the test chip. The die size is 1500 μm by 1900 μm (with DNE 1000 μm by 500 μm), and it is packaged in a 68-pin QFP. The PLL was synthesized using the Miró™ CGS18T PLL Engine provided by Barcelona Design Inc. The core of the PLL is a ring-type VCO, and the reference clock is at 20 MHz. Without losing generality, the Delay block and 2nd Clock input option is removed from the architecture proposed in Fig. 1 because of area and pin constrains in the final tapeout. Layout impact is less significant in this case because the substrate is an epi-type wafer.

The test board has six layers with dedicated power supplies for the DNE, PLL I/O, PLL Analog, and PLL Digital. Each supply has a 3300 pF decoupling capacitance attached to it. The reference clock to the PLL and input clock of the DNE are generated from a Tektronix AWG710 Arbitrary Waveform Generator. The PLL output is connected to a Wavecrest SIA3000 Signal Integrity Analyzer to measure the histograms of the PLL clock cycle, which are chosen as the primary discussion vehicle for illustrating noise impact from substrate. Of course, target systems are not limited to PLLs. ADCs,

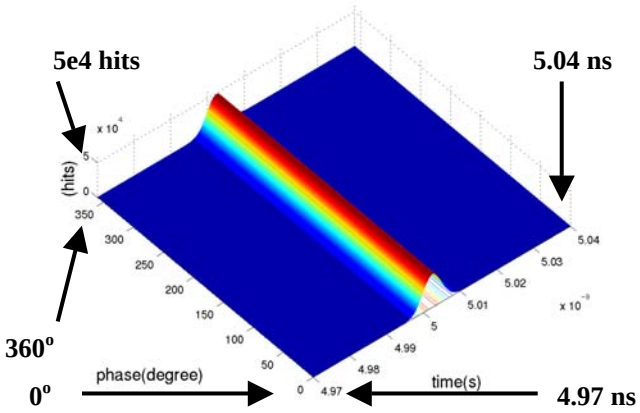

Fig. 3. Phase vs. histogram, w/o substrate noise.

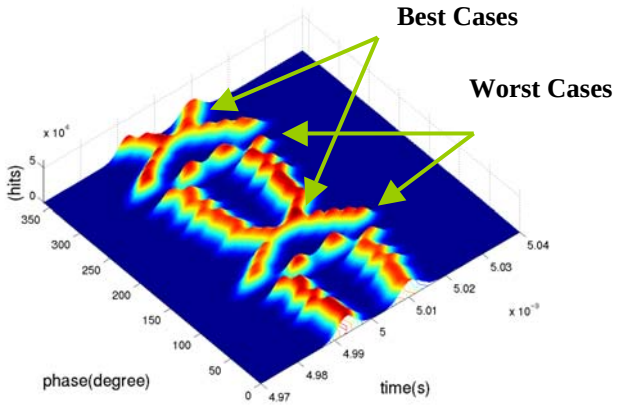

Fig. 4. Phase vs. histogram, DNE at 100 MHz, NID=40 pF (deterministic).

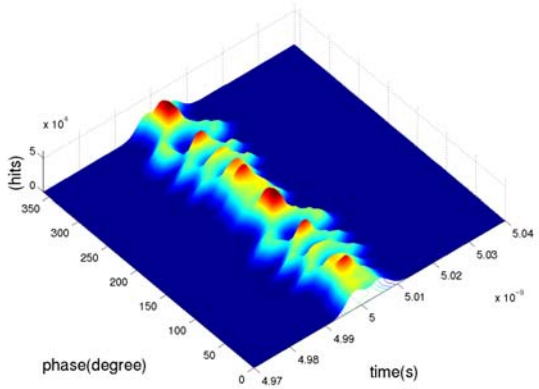

Fig. 5. Phase vs. histogram, DNE at 100 MHz, NID=20 pF (deterministic).

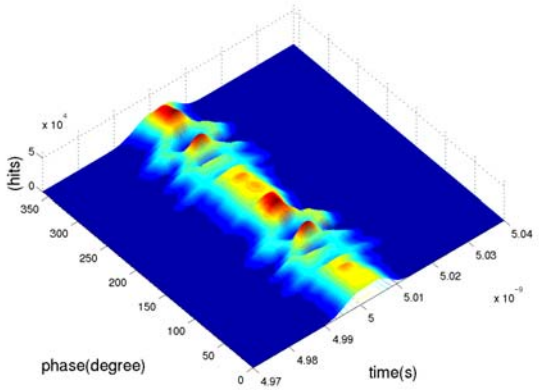

Fig. 6. Phase vs. histogram, DNE at 100 MHz, NID= 20 pF(deterministic) + 20 pF(random).

DACs, PAs, and LNAs can as well characterized using the methodology proposed.

III. Measurement Results

To understand the results, it is necessary to first define the phase difference (at input pins) between the DNE clock and the PLL reference clock as ϕ (w.r.t. the DNE clock). Histograms at different ϕ will be plotted in 3D surfaces and compared. As it will be demonstrated, these surfaces will be changed accordingly, depending on different digital noise content. At each specific ϕ, the period of PLL clock cycle was measured 500,000 times in each histogram. As the basis for comparison, Fig. 3 illustrates the histogram with no substrate noise impact. The histogram of the PLL clock cycles with no effects coming from the DNE is normally distributed with a standard deviation of 2.51 ps in these cases. It is demonstrated in the following 3D histogram plots how digital noise affects the performance of the PLL. All the dimensions of 3D histogram plots are fixed unless specified otherwise.

The experiments start with injecting deterministic noise at 100 MHz with coupling capacitance set at 40 pF. The measurement data in Fig. 4 show how the histogram varies as the ϕ changes. By properly controlling ϕ, a 71% improvement in jitter standard deviation from the worst case (14.394 ps) relative to best case (4.042 ps) was observed. In Fig. 5, the coupling capacitance is reduced from 40 pF to 20 pF. The locations of the best and worst cases remain the same, however, the distance, between the peaks decreases. In Fig. 6, 40 pF is divided into two parts, 20 pF is dedicated to deterministic noise coupling, and the other 20 pF is used to inject random noise into the substrate. Although the total coupling capacitance in Fig. 4 and Fig. 6 are the same, system performances are very different from each other. This is because deterministic

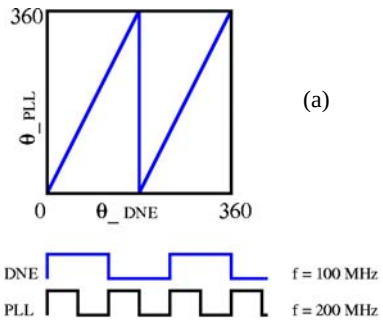

Fig. 7. (a) Relative phases between the DNE and PLL clock; (b) DNE and PLL waveforms.

noise moves the peaks, while random noise makes the distribution wider.

Fig. 7(a) plots the relative phases between the DNE and PLL clock. At the rising and falling of the deterministic clock edges, the DNE injects current into the substrate. If the injected noise aligns with the PLL clock edges, the PLL performance will be the worst. When shifting the edge positions of the deterministic noise from 0^o to 360^o, the relative phases to PLL would have gone through two complete cycles as shown in Fig. 7(a). This explains why the PLL output in Fig. 4-6 has two cycles. Fig. 7(b) shows that the impact repeats every two PLL cycles, that's why two peaks can be observed in each histogram. Fig. 8(a) is a 2-D projection of the 3-D plot in Fig. 5, where the duty cycle of the DNE clock is 50%. Fig. 8(b) is plotted for the case with 45% duty cycle. The worst case moves 18^o (i.e. 5% of 360^o). This again confirms the PLL output is sensitive to the DNE clock edge.

Fig. 9 shows the measurement data with DNE clocked at 160 MHz. It has 5 cycles along the phase direction, while in the 100 MHz case, 2 cycles are observed. The relative edge positions between digital clocks and PLL clocks are the explanation to this observed behavior.

As a demonstration, Fig. 10 provides a phase vs. histogram plot generated by a Verilog-A based system level simulation (software realization of a simplified DNE, with detailed models in the substrate network, power grid parasitic, and the studied PLL). In this case, the major frequency component of the input noise is 160 MHz. The result is consistent with the measurement data.

In general, define the ratio R= (PLL output frequency / deterministic noise frequency)=(m/n), assuming $m \geq n$ for most practical cases, the distribution $H(t)$ can be expressed as:

$$H(t) = \sum_{i=1}^{K} \alpha_i \exp(-(t-\mu_i)^2/(2\sigma_i^2)).$$

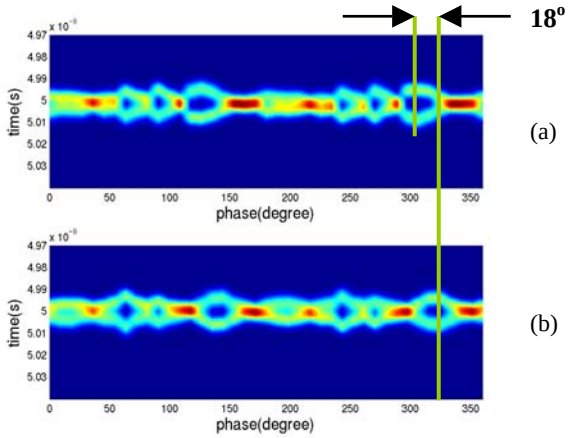

Fig. 8. 2-D projection of the 3D plot: (a) duty cycle = 50%; (b) duty cycle = 45%.

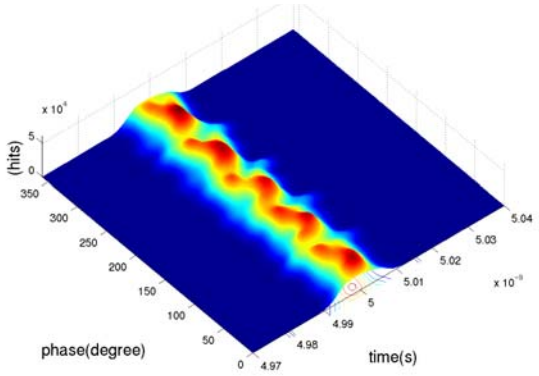

Fig. 9. DNE at 160 MHz, phase vs. histogram, NID=20 pF(deterministic).

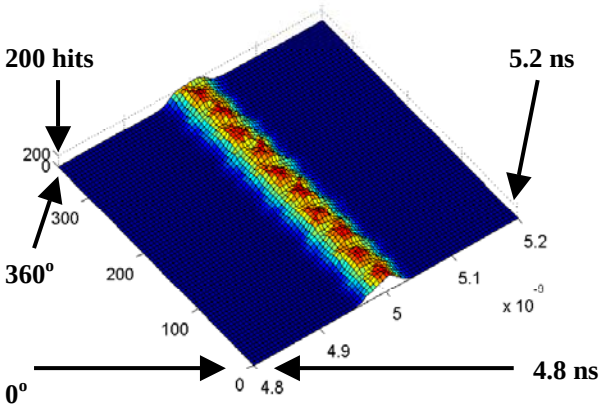

Fig. 10. DNE at 160 MHz, phase vs. histogram, NID=20 pF(deterministic), from simulation.

where K, the maximum number of Gaussian distributions needed to describe $H(t)$ (same as the number of cycles observed along the phase direction), equals:

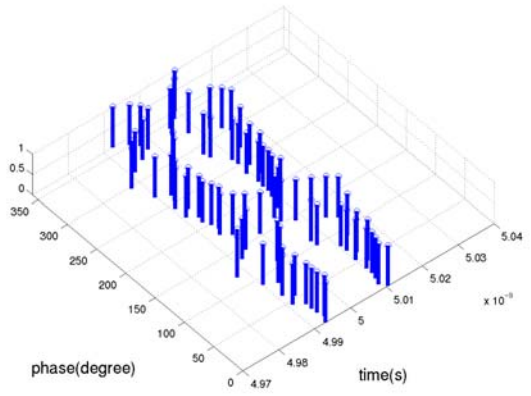

Fig. 11. Positions of peaks, extracted from Fig. 4.

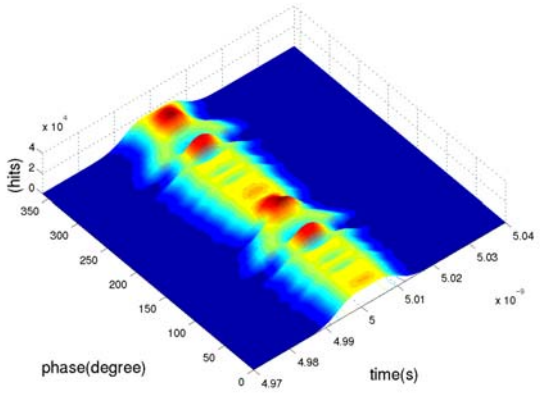

Fig. 12. Phase vs. Histogram, estimated data for the case with NID=20 pF(deterministic)+20 pF(random).

(1) $m \in N, n = 1$, (subharmonic), K=m/n;

(2) $m, n \in N - \{1\}$, (ultra-subharmonic), K=m;

(3) $\frac{m}{n} \notin Q$, K=1.

In the case of operating DNE at 100 MHz, two Gaussian curves are used to model the histogram, *H(t)*, at each specific phase:

$$\tilde{H}(t) = \alpha[\exp(-(t-\mu_1)^2/(2\sigma^2)) + \exp(-(t-\mu_2)^2/(2\sigma^2))].$$

At some ϕ, the two peaks merge with each other. In these degenerated cases, the histograms can be modeled as a single Gaussian curve instead.

Fig. 11 shows the traces of μ_1 and μ_2 (extracted from the measurement data in Fig. 4, NID=40 pF) in the equations above. For a linear system, the spacing between μ_1 and μ_2 is propositional to the value of (deterministic) coupling capacitance. In the case that the NID for the CLK and PRNG blocks are both 20 pF, the predicted 3D plot can be obtained by scaling the distance between μ_1 and μ_2 in Fig. 11 by 0.5, and choosing σ = 4.1 ps. Fig. 12 presents the predicted phase vs. histogram plot, which shows good consistency with Fig. 6.

For a specific system, for example, a PLL, a lookup table (Table I) recording μ, α, and σ at selected phases and frequencies can be constructed, using either HW or SW realization of the DNE plus the target system. In Table 1, $(\mu, \alpha, \sigma)_{ii}$ is an array containing K by 3 elements, where K is defined on the previous page. 3D plots at different NID values can be estimated using the numbers in the table and method mentioned above. The predicted number will provide insight to assist in system-level planning.

From the results demonstrated in this section, both timing (phase) and frequency selection are critical to system performance. Consequently, the DNE and proposed methodology offer a powerful approach to investigate the impact of substrate noise at the beginning of SoC design. A standard procedure to characterize noise impacts is:

TABLE I.

Lookup Table For Histogram Reconstruction

NID_{CLK}=**X** NID_{PRNG}=**Y**	$freq_1$	$freq_2$	....	$freq_M$
$phase_1$	$(\mu,\alpha,\sigma)_{11}$	$(\mu,\alpha,\sigma)_{12}$	....	$(\mu,\alpha,\sigma)_{1M}$
$phase_2$	$(\mu,\alpha,\sigma)_{21}$	$(\mu,\alpha,\sigma)_{22}$	....	$(\mu,\alpha,\sigma)_{2M}$
: :	: :	: :	: :	: :
$phase_N$	$(\mu,\alpha,\sigma)_{N1}$	$(\mu,\alpha,\sigma)_{N2}$	....	$(\mu,\alpha,\sigma)_{NM}$

(1) Estimate digital noise spectra based on the architecture and previous experiences, i.e. estimate the variables, α, *f*, and *s(t)*, in $\sum_{i=1}^{K} \alpha_i \cos(2\pi \cdot f_i \cdot t + \theta_i) + s(t)$.

(2) Use DNE to emulate the spectra estimated in (1) for system-level analysis.

In most cases, software realization of DNE, such as using Verilog-A HDL, will save cost and time. However, it is more convincing for analog/mixed-signal intellectual-property (IP) design companies to characterize the robustness of their IPs using actual silicon samples with DNE and their IPs fabricated on the same test chip.

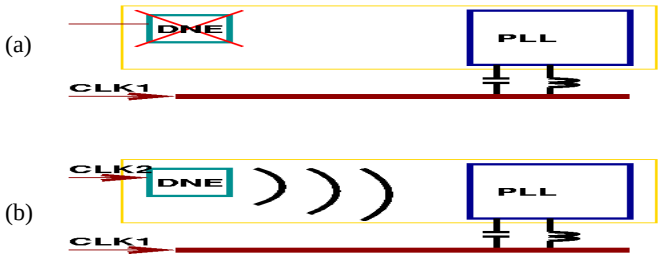

Fig. 13. (a) Noise injected from a trace; (b) Activate DNE to suppress deterministic noise.

IV. Noise Cancellation

The DNE can be used not only to benchmark system performance but also to partially cancel deterministic noise coupling from other sources. The experiment setup used to demonstrate the concept is illustrated in Fig. 13(a). In the first configuration, with DNE off, a deterministic clock is injected to a trace on the test board and coupled to the targeted PLL. From the dynamic theory [16][17], the PLL system can be expressed as:

$$\dot{x}(t) = A(t)x(t) + \begin{bmatrix} B_{11}(t) \\ B_{21}(t) \\ \vdots \\ B_{n1}(t) \end{bmatrix} u(t)$$

$$= A(t)x(t) + B(t)\begin{bmatrix} u(t) \\ 0 \\ \vdots \\ 0 \end{bmatrix},$$

where transition matrix, *A(t)*, distribution matrix, *B(t)*, state vector, *x(t)*, and the noise coupled from the trace to the substrate, *u(t)*, can be expressed as:

$$A(t) = \begin{bmatrix} A_{11}(t) & A_{12}(t) & \cdots & A_{1n}(t) \\ A_{21}(t) & A_{22}(t) & \cdots & A_{2n}(t) \\ \vdots & \vdots & \ddots & \vdots \\ A_{n1}(t) & A_{n2}(t) & \cdots & A_{nn}(t) \end{bmatrix},$$

$$B(t) = \begin{bmatrix} B_{11}(t) & B_{12}(t) & \cdots & B_{1m}(t) \\ B_{21}(t) & B_{22}(t) & \cdots & B_{2m}(t) \\ \vdots & \vdots & \ddots & \vdots \\ B_{n1}(t) & B_{n2}(t) & \cdots & B_{nm}(t) \end{bmatrix}, \quad x(t) = \begin{bmatrix} x_1(t) \\ x_2(t) \\ \vdots \\ x_m(t) \end{bmatrix},$$

and $u(t) = \sum_{i=1}^{K} \alpha_i \cos(2\pi \cdot f_i \cdot t + \theta_i) + s(t)$, respectively.

In the second configuration, Fig. 13(b), by activating the DNE, extra noise is coupled through the substrate. In general, if there are (m-1) DNEs, the system equations can be revised as following:

$$\dot{x}(t) = A(t)x(t) + B(t)\begin{bmatrix} u(t) \\ u_{dne\_1}(t) \\ \vdots \\ u_{dne\_(m-1)}(t) \end{bmatrix}.$$

The problem becomes an optimization problem of:

$$\min\{\max_j\{\left\| B_{j1}(t)u(t) + \sum_{k=2}^{m} B_{jk}(t)u_{den\_(k-1)}(t) \right\|\}\}.$$

Given the PLL is a periodic time varying system,

$$B_{jl}(t) = \sum_{l=1}^{K} \beta_{jl}(t)\cos(2\pi \cdot f_l \cdot t + \theta_l).$$

With no random logic in the DNE, the noise spectra generated can be approximated by:

$$u_{den\_h}(t) = \sum_{m=1}^{K} \gamma_m(t)\cos(2\pi \cdot f_m \cdot t + \theta_m).$$

The goal (in deterministic part) can be written as:

$$\min\{\max_j\{\left\| \sum_{p=1}^{K}\sum_{q=1}^{K} \kappa_{jpq}(t)\cos(2\pi \cdot (f_p \pm f_q) \cdot t + \theta_{pq}) \right\|\}\}.$$

In our experiment, noise source is a 100 MHz square wave. Consequently, by properly adjusting the phase and the magnitude of the second noise generated by a DNE at 100 MHz, the optimal point can be achieved without great difficulty. In the first configuration as shown in Fig. 13(a), the worst case of the standard deviation is 5.068 ps (ϕ=45°). In the second configuration, the phase of CLK1 is fixed at 45°, and the phase of CLK2 is varied. As

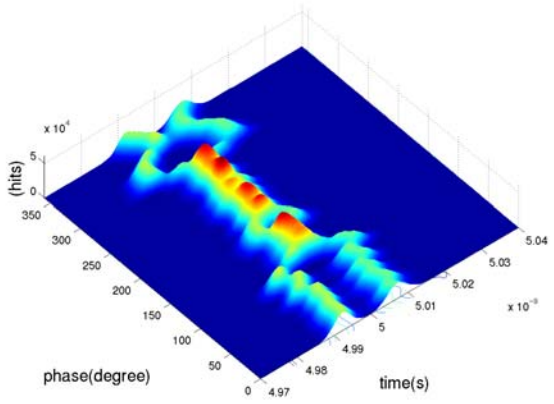

Fig. 14. Phase vs. histogram with improved performance in the region between 90° and 270°.

shown in Fig. 14, when the phase difference between CLK2 and the PLL reference clock is in the range between –90° and 90°, the performance is worse. However, in the region between 90° and 270°, the performance is improved.

In the best case, the standard deviation is reduced from 5.068 ps to 2.501 ps, which represents a 50% improvement when compared to the case operating without the DNE, Fig. 15. The impact caused by the deterministic noise (two peaks) is suppressed and peaks are merged, owing to the signal injection by the DNE. Fig. 16 shows the negative gradient of Fig. 14 in the direction of phase. From Fig. 16, between 90° and 270°, the negative gradient is small, which implies that even the operating point of DNE deviates from the designated point, the effectiveness of noise cancellation will not degrade too fast because of the wide margin. Therefore, the feasibility of the technique has been demonstrated.

In practical digital design cases, *u(t)* could be much more complicated than the case demonstrated. However, as the key deterministic components are identified, the techniques proposed in this section can be used to reasonably reduce the noise impact. It should be mentioned that this approach is less likely to be applicable for canceling stochastic noise. It is because to generate a stochastic signal highly correlated to the existing random noise is not as easy as its deterministic counterpart. The goal (in random part) is:

$$\min\{\max_{j}\{\left\| B_{j1}(t)s(t) + \sum_{k=2}^{m} B_{jk}(t)s_{den\_(k-1)}(t) \right\|\}\}.$$

From the equation, it is clear that the result can be either constructive or destructive for random noise. More complicated systems, such as [13] and [18], could be considered if necessary.

V. Conclusions

A behavior-level DSN model containing both random and deterministic components is proposed to describe the substrate noise generated by complicated digital systems. Frequency and timing of digital clocks, digital switching activities, and number of transistors in digital blocks are the key parameters of this model. A DNE is fabricated based on the proposed model and used to characterize the system impact of substrate crosstalk. For PLL applications, deterministic noise can cause peak splitting in jitter histograms, and random noise makes the jitter distribution wider. Results show that both timing and frequency properties of the digital noise are important. By properly controlling the phase of digital inputs with respect to the PLL reference clock, a 71% improvement in jitter standard deviation from the worst case relative to best case was

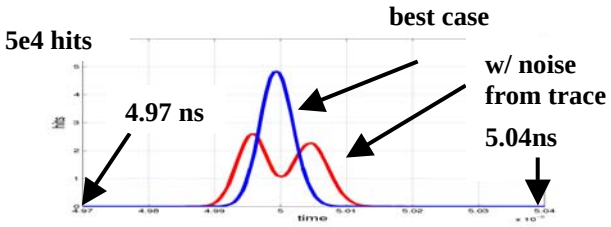

Fig. 15. Comparison between histograms.

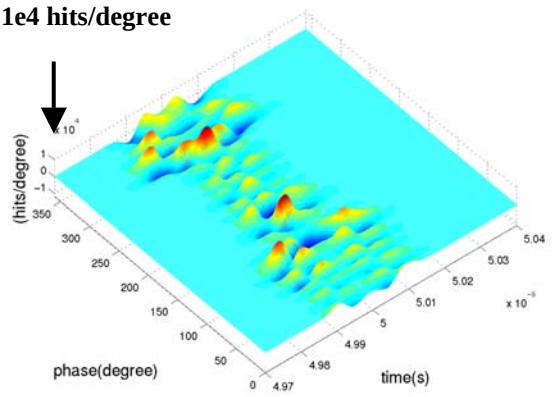

Fig. 16. Negative gradient plot of Fig. 14 in the direction of phase.

observed. A 50% reduction in jitter standard deviation was obtained by using a DNE to cancel deterministic noise coupled from other sources.

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