# Design Methodology for Power-Constrained Low Noise RF Circuits

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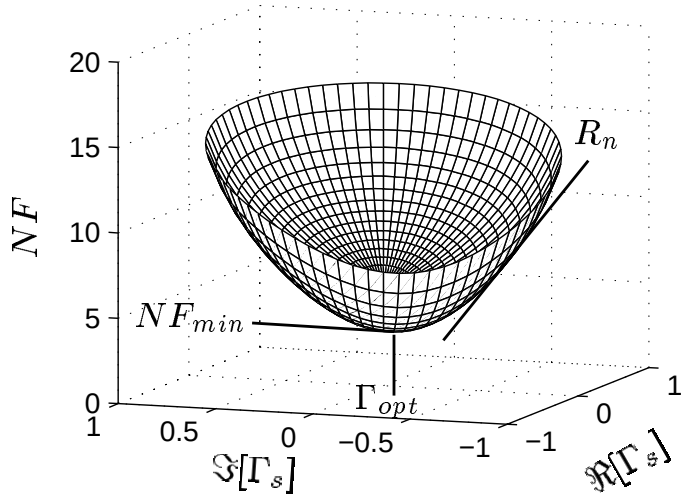
# Four Noise Parameters

- Minimum Noise Factor ($F_{min}$) : Best achievable noise performance
- Optimum Source Admittance ($Y_{opt}$) : Source admittance yielding $NF_{min}$
- Equivalent Noise Resistance ($R_n$) : Sensitivity of $NF$ when $Y_s$ differs from $Y_{opt}$

$$F = F_{min} + \frac{(Y_s - Y_{opt})^2 R_n}{G_s}$$

*Desired to be*

- Low $F_{min}$
- Small $R_n$
- $Y_s \cong Y_{opt}$





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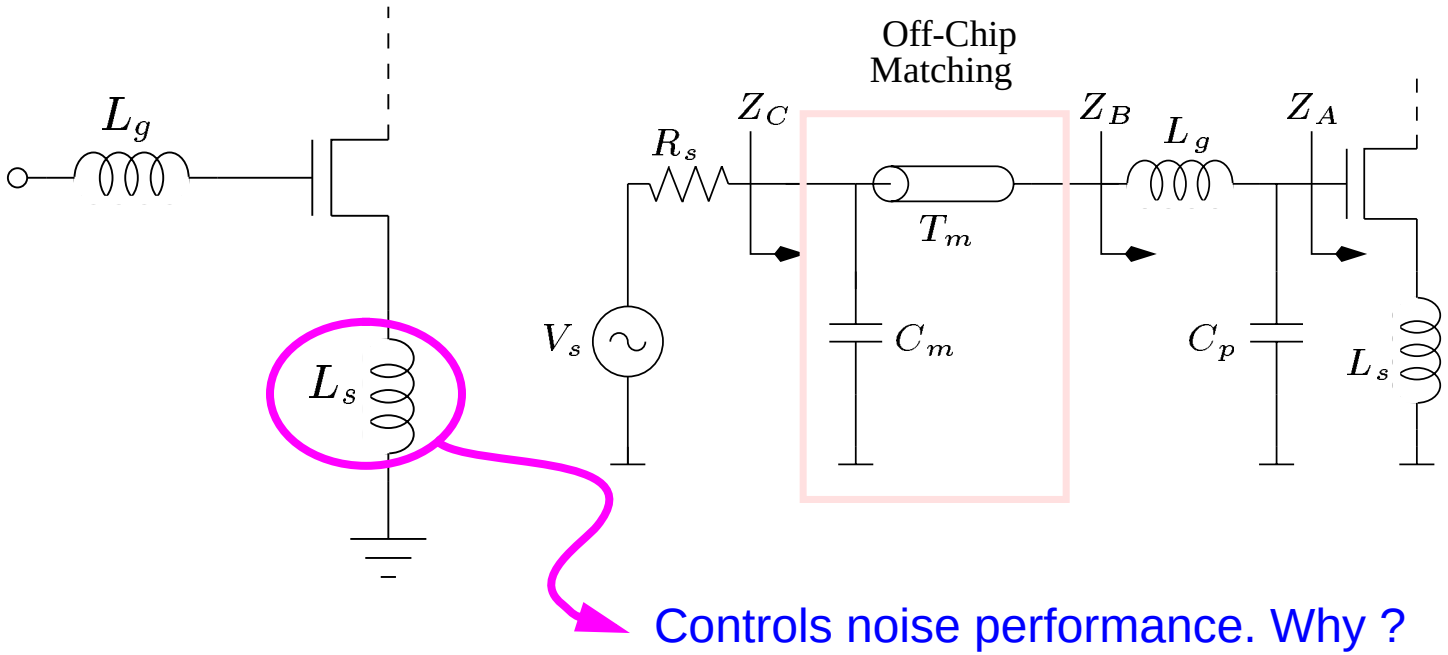
# Integrated LNA Design

## (Tuned LNA Architecture)

Basic Architecture

Conjugate Power Match




Controls noise performance. Why ?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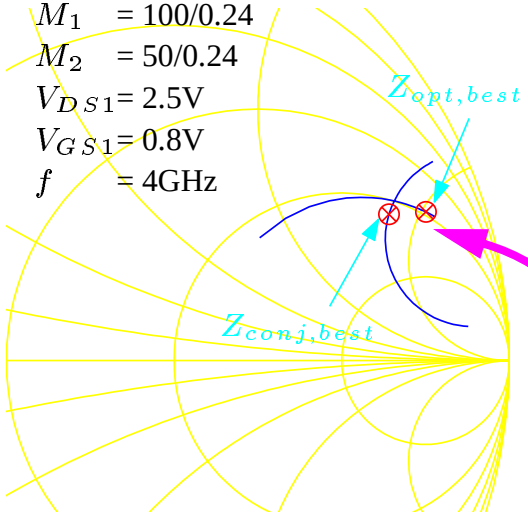
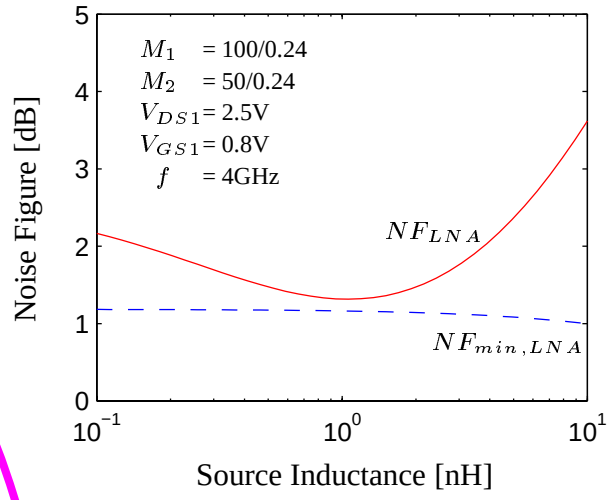
# Integrated LNA Design (*Continue*)

## (Power Matched Design)




$$F = F_{min} + \frac{(Y_s - Y_{opt})^2 R_n}{G_s}$$



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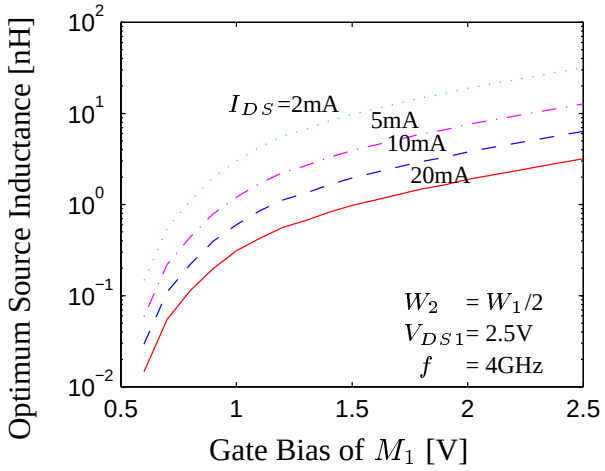
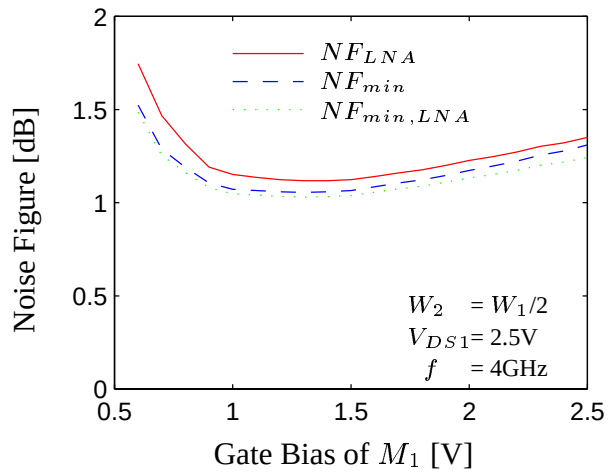
❀ $M_2$ contribution is excluded.

# Integrated LNA Design (*Continue*)

## (Power Matched Design)

❀ $M_2$ contribution is excluded.




- Optimum $L_s$ is bias dependent and linearly scaled by the current specification.
- The achievable noise figure is independent of the current specification and quite close to the intrinsic $NF_{min}$.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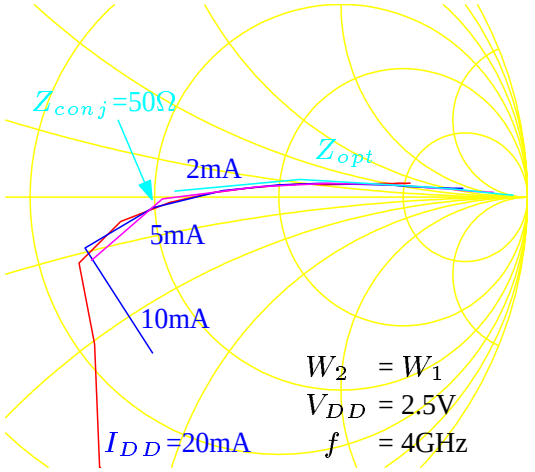
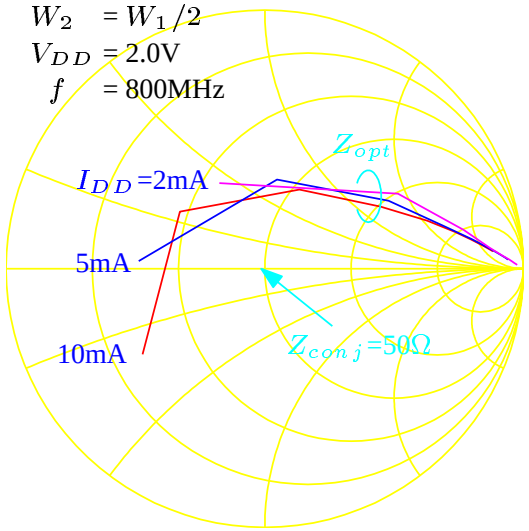
# Integrated LNA Design (*Continue*)

## (Power Constrained Performance, $Z_s$=$Z_{in}$=50Ω)

### Optimum Impedance ($Z_{opt}$)




Matched Cascode




Mismatched Cascode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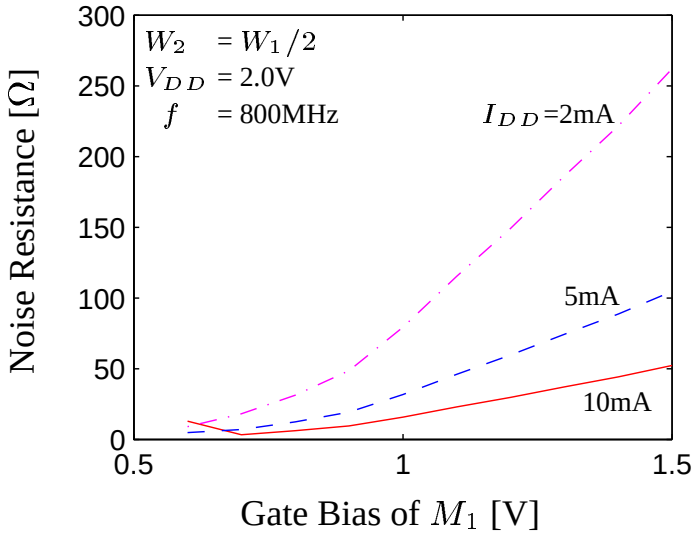
$$F = F_{min} + \frac{(Y_s - Y_{opt})^2 R_n}{G_s}$$

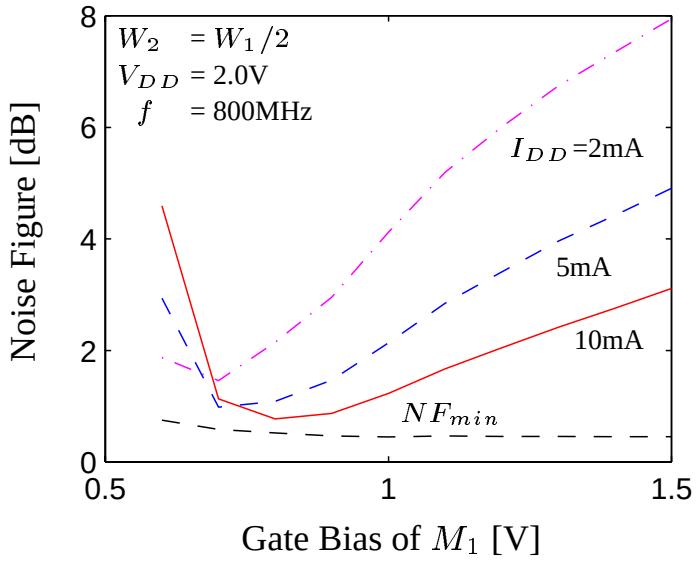
# Integrated LNA Design (*Continue*)

## (Power Constrained Performance, $Z_s$=$Z_{in}$=50Ω)

### Noise Resistance ($R_n$)




### Noise Figure ($NF$)





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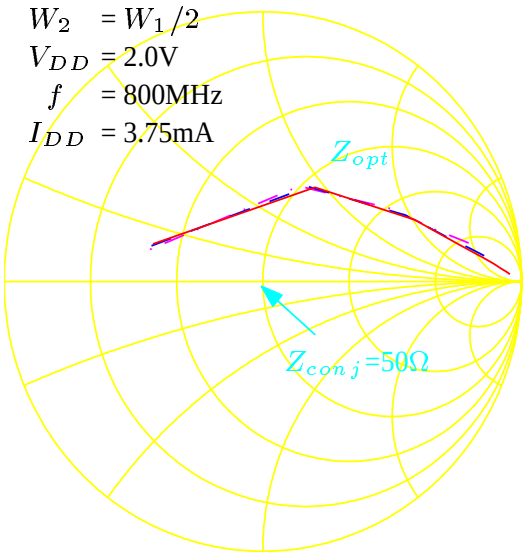
$$F = F_{min} + \frac{(Y_s - Y_{opt})^2 R_n}{G_s}$$

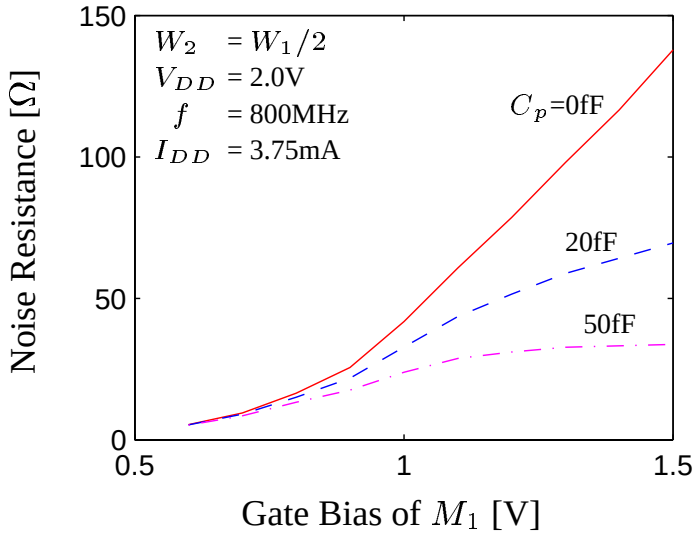
# Integrated LNA Design (*Continue*)

## (Impact of Pad Capacitance, $Z_s$=$Z_{in}$=50Ω)

### Optimum Impedance ($Z_{opt}$)




### Noise Resistance ($R_n$)




$$F = F_{min} + \frac{(Y_s - Y_{opt})^2 R_n}{G_s}$$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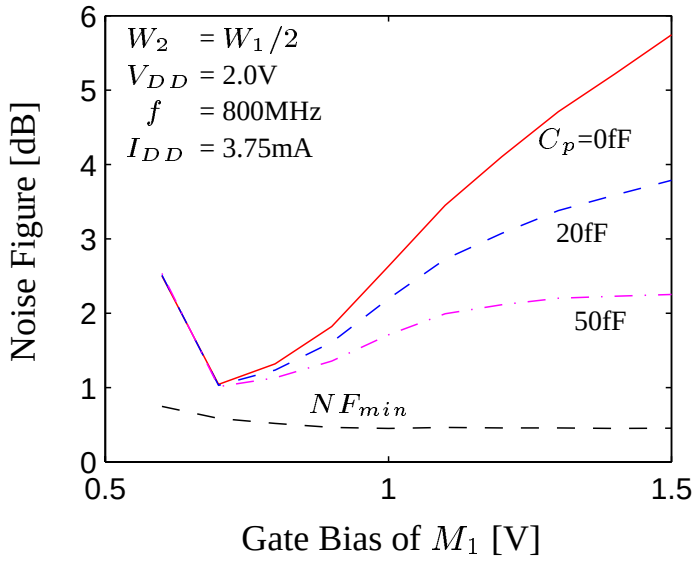
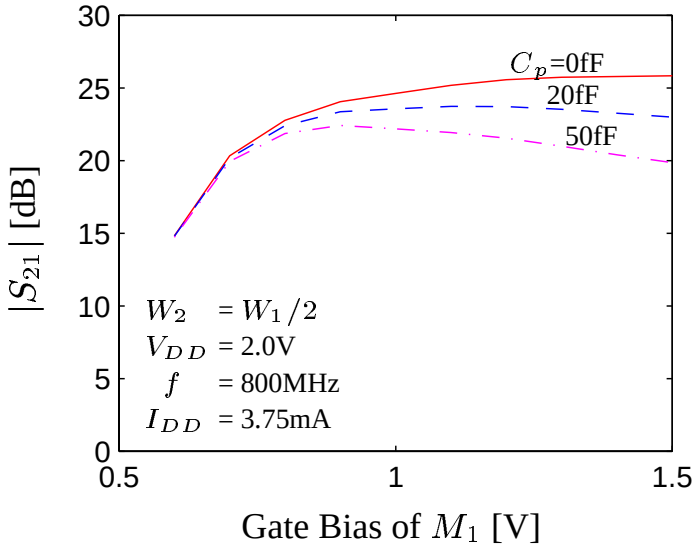
# Integrated LNA Design (*Continue*)

## (Impact of Pad Capacitance, $Z_s$=$Z_{in}$=50Ω)

### Noise Figure (*NF*)




### Gain ($s_{21}$)





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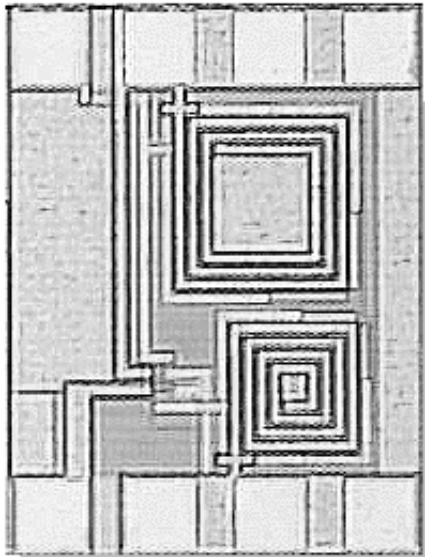
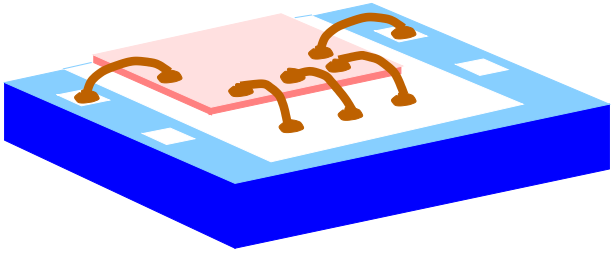
# LNA Implemenation (*Continue*)

## (Implementation , $Z_s$=$Z_{in}$=50Ω)





- 800MHz single-ended
- 0.24μm, silicided-poly, 5-metals
- $W_1$=90, $W_2$=45 (not optimized)
- 5μm-long gate fingers
- M5 spiral inductors w/ patterned ground shield
- M5/M1 pad capacitors
- 24-pin LLP package
- An off-chip inductor for $L_g$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# LNA Implemenation (*Continue*)
## (Performance)

| Parameters | Measured Value |
|---|---|
| Frequency | 800 MHz |
| Supply Voltage | 2.0 V |
| Power Consumption | 7.5 mW |
| Noise Figure | 0.9±0.2 dB |
| Available Gain | 8.8 dB |
| $s_{11}$ | -38.1 dB |
| IIP3 | 7.1 dBm |
| Die Area | 0.19 $mm^2$ |

Just adds 0.3dB to $NF_{min}$


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# Conclusions

- Overall $NF$ is controlled by $L_s$ : Optimal $L_s$ achieves $NF$ close to intrinsic $NF_{min}$ with a perfect power match.
- For a fixed $Z_s$, simultaneous choice of $V_{gs}$ and width of input stage is most critical in design.
- Mismatched cascode stage determines the lower limit of noise figure.
- Pad capacitance provides another design flexibility.
- CMOS LNA can be competitive with GaAs and Bipolar in low GHz range.


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