Design Methodology for Power-Constrained Low Noise RF Circuits

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Abstract—**Based on measured four-noise parameters and two-port noise theory, guidelines for integrated LNA (low noise amplifier) design are presented. If arbitrary values of source impedance are allowed, an optimal LNA design is obtained by adjusting the source degeneration inductance. Even for a fixed source impedance, the integrated LNA can achieve near NF_{min} by choosing an appropriate device geometry along with an optimal bias condition. An 800MHz LNA has been implemented in a standard 0.24μm CMOS technology. The amplifier possesses a 0.9dB noise figure while drawing 7.5mW from a 2.0V power supply, demonstrating that the proposed methodology can accurately predict noise performance of integrated LNA designs.**

I. Introduction

The first stage of a receiver is typically an LNA (low noise amplifier) which needs to provide sufficient gain while introducing the least noise possible. The traditional noise optimization technique for LNA design starts with a given device with fixed characteristics; the optimum bias condition and source impedance are then determined. By contrast, in full custom ICs, the designer can choose the desired device geometries, which offers an important degree of freedom. Nevertheless most designers still rely on classical optimization techniques [1], [2], [3] because no explicit guidance is generally available on how to best exercise the IC designer's freedom in tailoring device geometries. Achieving a good noise figure often results in poor gain, a bad input match, or unacceptably high power consumption. It is possible to achieve an optimum noise figure with acceptable input mismatching (typical $s_{11} \approx$ -10dB) but the potential of integrated LNAs is not fully exploited. Recently proposed noise optimization techniques for CMOS RF circuits permit greater flexibility in the selection of device geometries as well as matching elements and biasing conditions to minimize the noise figure for a specified gain or power dissipation [4], [5]. However, they use simplified small-signal models as well as constant noise characteristics. These techniques also rely heavily on mathematical derivations that provide limited intuitive design guidance.

This paper presents explicit guidelines for LNA design based directly on measured noise parameters and two-port noise theory; the approach requires neither sophisticated noise modeling nor circuit simulation to be used. All the analyses are based on MOSFET designs but the same methodology can be applied to other IC technologies as well, for example, design using more advanced HBT technology [6]. Section II reviews the intrinsic noise model of the MOSFET and considers its relation to LNA design. Section III explains how the noise performance of the LNA differs from that of the intrinsic device; explicit design guidelines for a CMOS tuned LNA with power constraints are presented. Finally Section IV presents experimental results for an implementation using integrated CMOS technology to realize an LNA.

II. High Frequency Intrinsic Noise Performance of MOSFETs

In the case of the MOSFET, the thermal fluctuations of channel charge produce effects that are modeled by drain and gate current noise generators [7]. These currents are partially correlated with each other because they share a common origin, and possess a spectral power given by the following equations:

$$\overline{i_d^2} \triangleq 4\,k\,T\,\Delta f\,\gamma\,g_{d0} \quad (1)$$

$$\overline{i_g^2} \triangleq 4\,k\,T\,\Delta f\,\delta\,g_g \quad (2)$$

$$\overline{i_g i_d^*} \triangleq c\sqrt{\overline{i_g^2}\,\overline{i_d^2}} \quad (3)$$

where γ, δ, and c are bias dependent factors; g_{d0} is the drain output conductance under zero drain bias; and $g_g \triangleq \zeta\frac{\omega^2 C_{gs}^2}{g_{d0}}$ is the real part of gate-to-source admittance. These expressions imply that the spectral power density scales with the device width (W).

The noise performance of a circuit is usually characterized by a parameter called *noise factor* (F) or *noise figure* ($NF \triangleq 10\log F$), that represents how much the given system degrades the signal-to-noise ratio [8]:

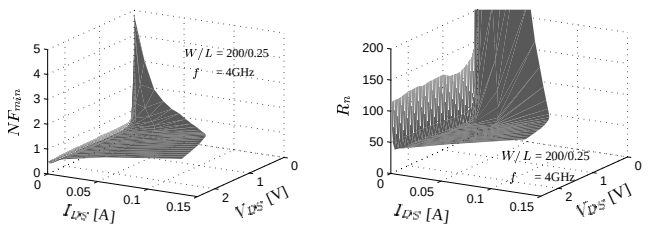
$$F \triangleq \frac{(S/N)_{in}}{(S/N)_{out}} \quad (4)$$

$$= \frac{\text{Total Output Noise Power}}{\text{Output Noise Power by Source Impedance}} \quad (5)$$

At one frequency, the noise factor of a linear circuit shows a parabolic dependence on the source admittance driving the given circuit. This behavior results in constant noise circles on a Smith chart and can be characterized in terms of the four-noise parameters [9] as follows:

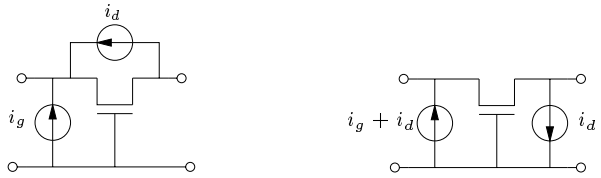
$$F = F_{min} + \frac{|Y_s - Y_{opt}|^2\,R_n}{G_s} \quad (6)$$

where F_{min} is the minimum noise factor, $Y_{opt} = G_{opt} + jB_{opt}$ is the optimum source admittance (also known as the noise matching condition), and R_n is the equivalent noise resistance. When the source admittance (Y_s) is equal to Y_{opt}, the circuit yields the best achievable noise performance F_{min}. If Y_s dif-



(a) (b)

Fig. 1. Intrinsic noise performance for the entire operating range of a 0.25 μm nMOSFET. (a) Minimum noise figure (NF_{min} [dB]) (b) Equivalent noise resistance (R_n [Ω]).



(a) (b)

Fig. 2. Noise power of the MOSFET in a common-gate configuration. (a) Original (b) Equivalent

fers from Y_{opt}, its impact on F is amplified by R_n. Even if F_{min} is sufficiently low, large R_n and a poor proximity between Y_s and Y_{opt} result in an unacceptably large noise figure in the actual circuit.

The intrinsic noise parameters of a MOSFET are shown in Fig. 1 for the entire operating range: the $x-y$ plane spans the $I-V$ operating characteristic curves and z axis gives the noise parameter at the respective bias points. These characteristics are transformed from simulated noise factors by combining them with network parameters that are secondary outputs of the noise simulator. In the linear region ($V_{DS} < V_{Dsat}$), NF_{min} and R_n show drastic increases; a similar increase of R_n is observed for low gate bias ($V_{GS} \approx V_{th}$). Such results are mainly attributed to the low g_m as well as a poor correlation factor (c) in this regime, and suggest that those bias conditions are highly undesirable for circuit implementation. Even in the saturation region, despite a good value for NF_{min} (below 1dB), actual circuit noise performance can easily be degraded due to small G_{opt} (corresponding $|\Gamma_{opt}|$ is nearly 1) as well as large R_n (three to ten times larger than that observed for HEMT devices [10]). Another observation is that NF_{min} in Fig. 1 (a) shows negligible drain bias dependence while γ and δ usually exhibit substantial drain bias dependence.

The four noise parameters can be derived[1] from current noise spectral power, given in Eq. (1) – (3), as follows:

$$F_{min} \approx 1 + \frac{\omega}{\omega_T}\sqrt{\gamma\delta\zeta(1-|c|^2)} \quad (7)$$

$$R_n \approx \frac{\gamma g_{d0}}{g_m^2} \quad (8)$$

$$G_{opt} \approx \frac{g_m\omega C_{gs}}{g_{d0}}\sqrt{\frac{\delta\zeta(1-|c|^2)}{\gamma}} \quad (9)$$

$$B_{opt} \approx -\omega C_{gs}\left(1 - c\frac{g_m}{g_{d0}}\sqrt{\frac{\delta\zeta}{\gamma}}\right) \quad (10)$$

Equation (7) suggests that shorter devices yield better noise figures because ω_T is proportional to $1/L_{eff}$ while $\sqrt{\gamma\delta\zeta(1-|c|^2)}$ becomes at most 6.5 times larger than the long channel case, down to 0.25 μm [5]. Likewise, Eq. (8) also suggests that shorter devices improve R_n. The small drain bias dependence of NF_{min} also can be explained by Eq. (7) since increases of γ and δ are mitigated by increasing g_m and c.

[1]Exact expressions can be derived based on the two-port theory presented in Appendix I. The approximated Eq. (7) – (10) neglect the distributed and Miller effects and their derivations are found in [11].

A. Scaling of the Noise Parameters

In realizing a custom IC design of the LNA, one of the key issues is to understand the device scaling effects on the noise parameters. The prior discussion suggests that the selection of device geometries for the LNA design requires width scaling of the device, consistent with the shortest channel length that can be realized. In Eq. (7) – (10), $g_{d0} - g_m - C_{gs}$ scale linearly with the device width (W) while noise factors $\gamma - \delta - \zeta - c$ are width-independent. These results thus suggest the dependence of the four-noise parameters with respect to device width as follows:

$$NF_{min} \quad \text{no width dependence} \quad (11)$$

$$R_n \propto 1/W \quad (12)$$

$$G_{opt} \propto W \quad (13)$$

$$B_{opt} \propto W \quad (14)$$

B. Conversion of Noise Characteristics into Common-Gate Mode

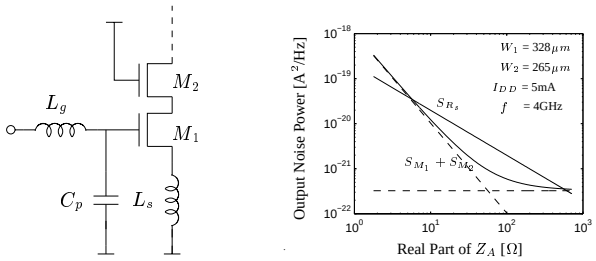
Adding a cascode stage is a common practice in amplifier design because it improves the stability by shielding the input device from voltage variations at the output. The four-noise parameters of the cascode stage can be directly obtained by measuring the common-gate mode MOSFET. The equivalent I/O noise power also can be obtained from characteristics of the common-source model, using Fig. 2 as a reference for the parameters.

$$\overline{i_1^2} = \overline{i_g^2} + \overline{i_g i_d^*} + \overline{i_d i_g^*} + \overline{i_d^2} \quad (15)$$

$$\overline{i_1 i_2^*} = -\overline{i_g i_d^*} - \overline{i_d^2} \quad (16)$$

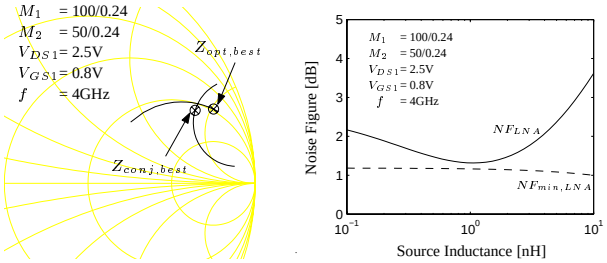
$$\overline{i_2^2} = \overline{i_d^2} \quad (17)$$

The four-noise parameters of the cascode stage in turn can be obtained using the two-port noise theory [12], described in Appendix I. Note that the body effect is not taken into account in these calculations.



(a) (b)

Fig. 3. (a) Tuned LNA architecture employing inductive source degeneration. (b) Dependence of output noise power components on $\Re[Z_A]$ where Z_A is the input impedance at the gate electrode of M_1.



(a) (b)

Fig. 4. The noise performance of the LNA for varying L_s. The noise contributions of M_1 substrate and M_2 are excluded and C_p=0. (a) Optimum source impedance (b) Noise figure.

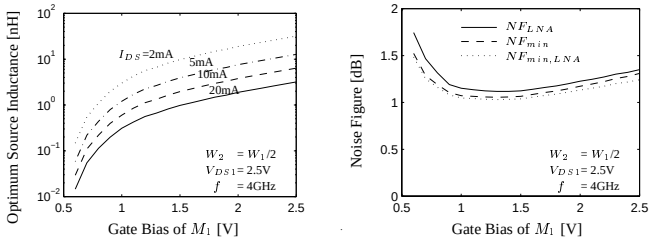
III. Design Guidelines for a Tuned Amplifier

The four-noise parameters and s-parameters were measured from a 0.24 μm nMOSFET with W = 100 μm, using the ATN NP5B system [13]. The resulting data were then smoothed for the frequency as well as the bias dependences, and in turn used in the following analyses.

A. Basic Architecture

The tuned amplifier illustrated in Fig. 3 (a) is one of the most broadly used LNA architectures because it offers the potential of achieving the best noise performance. The desired input impedance[2] of the amplifier is obtained for a narrow frequency band by choosing L_s and L_g independently. It is known that the source degeneration inductance (L_s) controls the noise performance of a given architecture [14] yet the reasons are not well understood. Figure 3 (b) shows that each component[3] contributing output noise has a different dependence on the real part of the input impedance ($\Re[Z_A] \approx \omega_T L_s$) when the source impedance offers a conjugate power match. Since the feedback of L_s reduces the current gain, as L_s increases, the output noise contributions from the source resistance (S_{R_s}) and the induced

[2]The input impedance calculation is explained in Appendix II-A.
[3]Derivations for each component are found in Appendix II-B.



(a) (b)

Fig. 5. (a) Optimum L_s yielding the best noise figure of the LNA for the given bias condition under the power constraint. (b) The best noise figure of the LNA with optimum L_s. The noise contributions of M_1 substrate and M_2 are excluded and C_p=0.

gate noise of M_1 (S_{i_g,M_1}) monotonically decrease but their slopes are different due to different feedback effects. On the other hand, the contribution from the induced gate noise of M_2 (S_{i_g,M_2}) is negligibly small; the contributions from drain current noise (S_{i_d,M_1} and S_{i_d,M_2}) have almost unity gain thus result in an L_s-independent term. Hence the LNA yields the best noise figure when the L_s-dependent term and L_s-independent term give equal contributions, as shown in Fig. 3 (b).

Figures 4 (a) and (b) graphically explain how L_s changes the performance of the LNA[4]. As L_s increases, the optimum noise matching condition (Z_{opt}) and the power matching condition ($Z_{conj} = Z_{in}^*$) exhibit independent trajectories as shown in Fig. 4 (a). Therefore, when L_s brings Z_{opt} and Z_{conj} to the point where they are in the closest proximity, the best achievable noise figure with a power match is obtained as shown in Fig. 4 (b). This fact implies that an accurate calculation of the input impedance is critical in the noise optimization process; approximate values are of limited use. Another beneficial impact of using a source inductance is the resulting improvement of NF_{min} and R_n. Thus the LNA can in principle achieve a better noise figure than NF_{min} of the MOSFET alone if Z_{opt} coincides with Z_{conj}.

B. Power Constrained Design

The power budget is usually constrained for integrated circuit implementations, thus a design approach oriented toward low power is very important. When the supply voltage and power consumption are fixed, the device width of the input stage corresponding to each bias condition can be easily calculated from the current density. Since the measured four-noise parameters are valid only for one device size, they need to be properly scaled based on the width dependences as noted in Eq. (11) – (14). Figure 5 (a) demonstrates the optimum L_s is bias dependent and it scales linearly with the specified current. However, the noise figure achieved by optimizing L_s is independent of the current specification and very close to the intrinsic NF_{min} as shown in Fig. 5 (b). Therefore, an arbitrary value of the source impedance, in conjunction with the proper

[4]The analysis procedure is described in Appendix II-C.

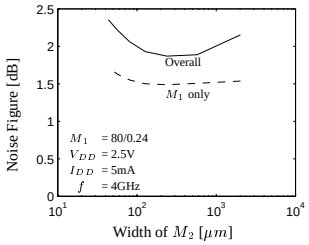


Fig. 6. The impact of the cascode transistor on the overall noise figure under the power constraint. $R_s = Z_{in} = 50\Omega$.

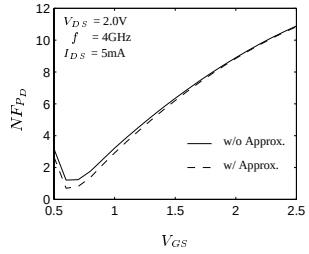


Fig. 7. Power constrained noise figure of the tuned amplifier when $R_s = Z_{in} = 50\Omega$. The solid line is the actual noise figure; the dashed line is the approximated results using Eq. (18).

choice of inductance used for source degeneration, offers the possibility of simultaneously achieving a good noise figure as well as a perfect power match.

C. Cascode Stage Design

While it is known that increasing the width of the cascode device monotonically improves shielding from the output, its impact on the noise performance is not well understood. As the width of the cascode stage increases, the generated noise power from the cascode stage also increases, but the required L_s for a specific Z_{in} decreases. Thus, the different width of the cascode stage consequently yields a different noise match condition as well as different value of noise resistance; an optimal width exists as shown in Fig. 6. For the given topology, with $W_2 \approx 3W_1$, the cascode stage introduces 40% extra noise power to the input stage, which in turn increases NF by about 0.5dB.

D. Design with A Fixed Source Impedance

In many RF applications, the source impedance has a fixed value of 50Ω, thus $NF_{50\Omega}$ is considered to be a more reasonable parameter than NF_{min}. Even if the source impedance is 50Ω, however, $NF_{50\Omega}$ does not represent the power-matched noise performance unless the input impedance is also adjusted to 50Ω. In this section, the MOSFET sizes are adjusted to satisfy the given power constraint and the inductors L_s and L_g are chosen to provide a 50Ω input impedance for the LNA.

Figure 7 is calculated analytically using formulae in Appendix II-B. It exhibits a deep valley-shaped noise figure profile, and suggests that choosing an appropriate gate bias is critical. If we can ignore the correlated portion in Eq. (43), the

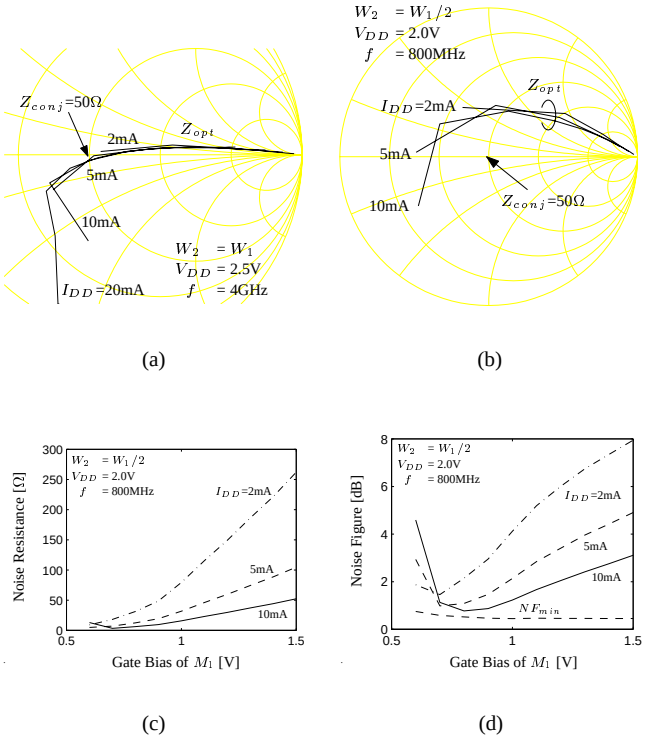


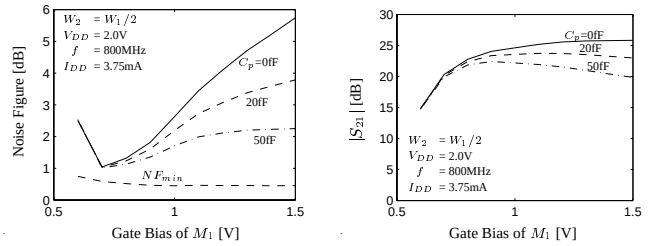
Fig. 8. The power constrained noise performance of the LNA when $R_s = Z_{in} = 50\Omega$. The noise contributions of M_1 substrate and M_2 are included and C_p=0. (a) Optimum source impedance at f=4GHz (b) Optimum source impedance at f=800MHz (c) Equivalent noise resistance (d) Noise figure.

amplifier noise figure can be approximated as follows:

$$F \approx 1 + \frac{\gamma g_{d0}}{G_s}\left(\frac{\omega_0}{\omega_T}\right)^2 + G_s\frac{\delta\zeta}{g_{d0}} \qquad (18)$$

The comparison in Fig. 7 shows that the approximate formula replicates the original noise characteristics. This formula explains the valley-shaped noise behavior using two independent noise contributions. One originates from the drain noise and is dominant when the gate bias is low. The other contribution originates from the induced gate noise and becomes dominant at higher gate bias. When the current is fixed, these two components have the opposite gate bias dependence to each other; the noise figure thus has minima where they contribute equally to the noise figure. This fact highlights the importance of accurate gate noise modeling for circuit design.

Figure 8 (a) demonstrates that Z_{opt} of the LNA is almost purely real at 4GHz, unlike the intrinsic MOSFET. It also suggests that a proper choice of the width makes Z_{opt} so close to 50Ω that a simultaneous matching of the impedance and noise can be achieved. Another Z_{opt} for a different topology, shown in Fig. 8 (b), exhibits larger deviation from the power match condition, which is caused not by the operating frequency but by the poorly optimized cascode stage. Nevertheless, this deviation does not substantially degrade the noise figure since the



(a) (b)

Fig. 9. The power constrained noise performance of the LNA when $R_s = Z_{in} = 50\Omega$ for different pad capacitance. The noise contributions of M_1 substrate and M_2 are included. (a) Noise figure (b) Gain.

noise resistance of the LNA shown in Fig. 8 (c) is reduced by a factor of as much as 5, in comparison to the MOSFET by itself. As a result, noise figures close to NF_{min} can be achieved as shown in Fig. 8 (d). The achievable noise figure is primarily limited by the extra noise contribution from the cascode stage which is also subject to the given power constraint.

E. Secondary Considerations

In the process of practical LNA design, as illustrated in Fig. 3, the bonding pad introduces an extra ac current path to ground. In silicon technology, this can deteriorate severely the noise figure if the path contains a resistive component, such as the conductive substrate [15]. If the resistive component is suppressed, however, the bonding capacitance simply increases the required inductance value for the designated input impedance. This consequently brings the noise match condition closer to 50Ω and also makes the noise resistance smaller. Figures 9 (a) – (b) demonstrate that a proper choice of bonding pad size can be utilized to improve the gate bias dependence by trading-off the noise figure with the gain.

IV. Experimental Results

To evaluate the LNA performance, a single-ended LNA targeting sub-1.0dB of noise figure was designed using a 0.24μm silicide CMOS technology. The die photo of the LNA is given in Fig. 10. The LNA was designed based on the characteristic in Fig. 9 (a). First, the supply voltage and power consumption were chosen to 2.0V and 7.5mW, respectively. The gate bias was set to 0.7V to achieve the best noise figure based on the characteristic in Fig. 9 (a); its corresponding size of M_1 was 90/0.24 for the given power budget. At the time of design, the cascode stage was not fully optimized; the sizes of M_2 was chosen to be 45/0.24. For the given topology, it is expected to improve the noise figure by 0.1dB with W_2 = 80μm. To minimize the distributed gate resistance, the MOSFETs were segmented into 5μm-long gate fingers and each of the fingers was contacted at both ends [16]. The spiral inductor L_s was implemented using the metal-5 layer and its value was chosen to be 1.1nH to provide 50Ω of real part of the input impedance, in combination with C_p. The inductor was designed based on the compact model presented by [17]; a patterned ground shield

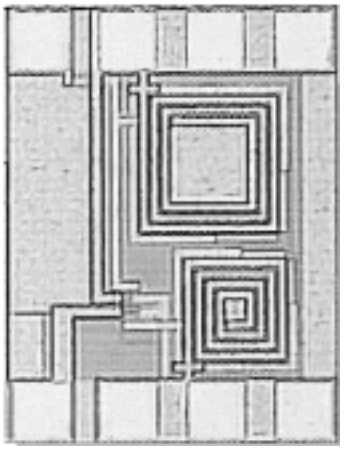


Fig. 10. Die photo of the LNA

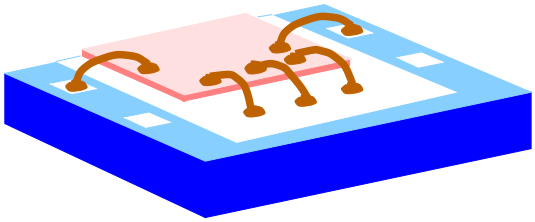


Fig. 11. Wire-bonding illustration of the LLP package

was employed to reduce the substrate parasitics of the spiral inductor [18]. To suppress extra noise, the pad capacitor was implemented using metal-5 and metal-1 layers, giving 47fF of capacitance. Since the required gate inductor L_g to cancel out the imaginary part of the input impedance was 36nH, which is too large to be integrated, an external inductor was used along with a bondwire inductor. Finally, to control the parasitic inductance from L_s to ground, the die was mounted on a special LLP package [19], that allows direct downbonding to the large ground plane as shown in Fig. 11.

The real term of the input impedance of the fabricated LNA was 54Ω and was adjusted to 50Ω using an off-chip tuner. The following table summarizes the performance of the LNA:

Parameters	Measured Value
Frequency	800 MHz
Supply Voltage	2.0 V
Power Consumption	7.5 mW
Noise Figure	0.9±0.2 dB
Available Gain	8.8 dB
s_{11}	-38.1 dB
IIP3	7.1 dBm
Die Area	0.19 mm^2

With 3.75mA of bias current, the LNA achieves about 0.9dB of noise figure, which is the lowest reported noise figure with a perfect power match for a CMOS LNA and adds just 0.3dB

to the NF_{min} of the intrinsic MOSFET device. The measured noise figure is also quite close to the expected value and demonstrates that the proposed methodology accurately predicts the noise performance of custom integrated LNA designs. Since the threshold voltage is relatively high in the given technology, further process adjustments can potentially reduce the supply voltage as well as the power consumption.

V. Conclusion

Based on the measured noise parameters of the $0.24\mu m$ MOSFET, and on the results derived from two-port noise theory, explicit guidelines for a integrated LNA design are presented. The measured noise parameters can be scaled directly with the device width; device sizing can be utilized for power-constrained design. The noise performance of the tuned LNA is primarily controlled by the source degeneration inductance, which determines both the power matching and the noise matching conditions. Therefore, if arbitrary values of source impedance are allowed, the optimal LNA design can be obtained by adjusting the source inductance. Even if the source impedance is fixed, the integrated LNA can achieve noise performance near NF_{min} by choosing an appropriate device geometry and optimizing the bias conditions. The cascode stage usually introduces at least 40% extra noise power to the input stage; thus its width needs to be optimized.

Although the demonstrated LNA uses a single-ended architecture, future LNA designs will require differential operation since further scaling of the device sizes requires smaller values of source inductance. Fully integrated inductors with large values and high Q-factors, required for L_g, are an ongoing challenge. The results demonstrate that CMOS can be a good candidate for high performance LNA designs, competitive with GaAs and bipolar LNAs.

Acknowledgments

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Appendix I : Noisy Two-Port

Two-port theory provides a means to represent a noisy two-port in terms of a noiseless two-port and its corresponding two noise sources [20]. Depending on the type of noise sources, many representations can be derived but the following three representations are particularly useful: admittance for parallel connections, impedance for series connections, and ABCD for cascade [12]. Each of these cases are now considered.

A. Admittance Representation

This representation is useful when two networks $\boldsymbol{Y}_1$ and $\boldsymbol{Y}_2$ are connected in parallel:

$$\boldsymbol{C}_Y = \boldsymbol{C}_{Y_1} + \boldsymbol{C}_{Y_2} \tag{19}$$

$$\boldsymbol{C}_Y \triangleq \begin{bmatrix} C_{i_1 i_1^*} & C_{i_1 i_2^*} \\ C_{i_2 i_1^*} & C_{i_2 i_2^*} \end{bmatrix} = 2kT\Re[\boldsymbol{Y}] \tag{20}$$

where $\boldsymbol{C}_Y$ denotes the correlation matrix of the admittance representation, in which $C_{i_m i_n^*}$ is the self- or cross-power spectral densities of the input and output current noise sources, and $\boldsymbol{Y}$ is the admittance matrix.

B. Impedance Representation

This representation is useful when two networks $\boldsymbol{Z}_1$ and $\boldsymbol{Z}_2$ are connected in series:

$$\boldsymbol{C}_Z = \boldsymbol{C}_{Z_1} + \boldsymbol{C}_{Z_2} \tag{21}$$

$$\boldsymbol{C}_Z \triangleq \begin{bmatrix} C_{v_1 v_1^*} & C_{v_1 v_2^*} \\ C_{v_2 v_1^*} & C_{v_2 v_2^*} \end{bmatrix} = 2kT\Re[\boldsymbol{Z}] \tag{22}$$

where $\boldsymbol{C}_Z$ denotes the correlation matrix of the impedance representation, in which $C_{v_m v_n^*}$ is the self- or cross-power spectral densities of the input and output voltage noise sources, and $\boldsymbol{Z}$ is the impedance matrix.

C. ABCD (Chain) Representation

This representation is useful when two networks $\boldsymbol{A}_1$ and $\boldsymbol{A}_2$ are cascaded:

$$\boldsymbol{C}_A = \boldsymbol{A}_1 \boldsymbol{C}_{A_2} \boldsymbol{A}_1^\dagger + \boldsymbol{C}_{A_1} \tag{23}$$

$$\boldsymbol{C}_A \triangleq \begin{bmatrix} C_{v_n v_n^*} & C_{v_n i_n^*} \\ C_{i_n v_n^*} & C_{i_n i_n^*} \end{bmatrix} \tag{24}$$

$$= 2kT \begin{bmatrix} R_n & \frac{F_{min}-1}{2} - R_n Y_{opt}^* \\ \frac{F_{min}-1}{2} - R_n Y_{opt} & R_n |Y_{opt}|^2 \end{bmatrix} \tag{25}$$

where $\boldsymbol{C}_A$ denotes the correlation matrix of the ABCD representation, in which $C_{v_m i_n^*}$ is the self- or cross-power spectral densities of the input referred noise sources, and $\boldsymbol{A}$ is the ABCD matrix.

D. Transformation to Other Representations

Each representation can be transformed into another by the matrix operation:

$$\boldsymbol{C}' = \boldsymbol{T}\boldsymbol{C}\boldsymbol{T}^\dagger \tag{26}$$

where $\boldsymbol{C}$ and $\boldsymbol{C}'$ are the noise correlation matrices of the original and resulting representations respectively, $\boldsymbol{T}$ is the trans-

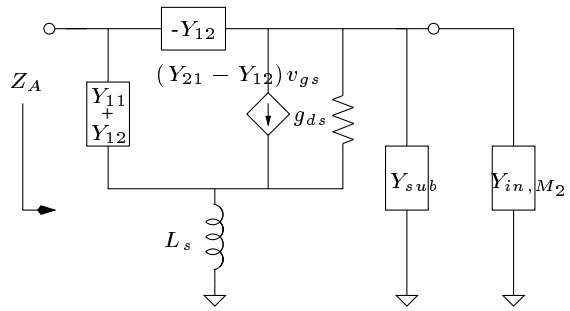

Fig. 12. Schematic diagram for input impedance calculation of the LNA

formation matrix given in the following table, and $\boldsymbol{T}^{\dagger}$ is the transpose conjugate of $\boldsymbol{T}$.

		Original Representation		
		Admittance	Impedance	ABCD
Resulting Representation	Admittance	$\begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix}$	$\begin{bmatrix}y_{11} & y_{12}\\ y_{21} & y_{22}\end{bmatrix}$	$\begin{bmatrix}-y_{11} & 1\\ -y_{21} & 0\end{bmatrix}$
	Impedance	$\begin{bmatrix}z_{11} & z_{12}\\ z_{21} & z_{22}\end{bmatrix}$	$\begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix}$	$\begin{bmatrix}1 & -z_{11}\\ 0 & -z_{21}\end{bmatrix}$
	ABCD	$\begin{bmatrix}0 & a_{12}\\ 1 & a_{22}\end{bmatrix}$	$\begin{bmatrix}1 & -a_{11}\\ 0 & -a_{21}\end{bmatrix}$	$\begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix}$

APPENDIX II : LNA ANALYSIS METHOD

A. Input Impedance

The simplified circuit diagram for input impedance calculations is illustrated in Fig. 12. Note that the output admittance has been divided into two components since the source electrode of the MOSFET is not grounded while the substrate is still grounded. Then the input impedance is:

$$Z_{in} = \frac{T_1+T_2+T_3}{T_4+T_5} \quad (27)$$
$$T_1 = 1 - Y_{12}Z_L \quad (28)$$
$$T_2 = Z_{L_s}[Y_{11}+Y_{21}-Y_{12}Z_L(Y_{11}+Y_{21})] \quad (29)$$
$$T_3 = g_{ds}(Z_L+Z_{L_s}+Y_{11}Z_LZ_{L_s}) \quad (30)$$
$$T_4 = -Y_{12}Y_{21}(Z_L+Z_{L_s}) \quad (31)$$
$$T_5 = Y_{11}[1+(g_{ds}-Y_{12})(Z_L+Z_{L_s})] \quad (32)$$

where

$$Y_{sub} = Y_{12}+Y_{22}-g_{ds} \quad (33)$$
$$Y_{in,M_2} \approx Y_{11,M_2}+Y_{21,M_2} \quad (34)$$
$$Z_L \triangleq 1/(Y_{sub}+Y_{in,M_2}) \quad (35)$$
$$Z_{L_s} = j\omega L_s \quad (36)$$

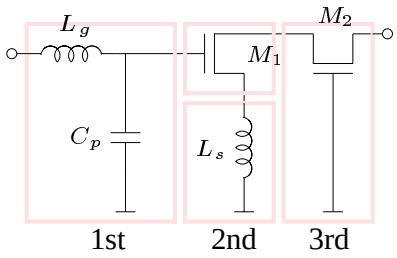

Fig. 13. Noise performance evaluation sequence for the LNA

B. Analytical Calculation of Noise Figure

When an off-chip tuner performs a power match by transforming the input impedance of the LNA to 50Ω, the noise figure of the amplifier is:

$$F = \frac{S_{R_s}+S_{M_1}+S_{M_2}}{S_{R_s}} \quad (37)$$
$$S_{R_s} = 4kTR_s|G_{m_1}|^2|A_{i_2}|^2 \quad (38)$$
$$S_{M_1} = 4kT\gamma_1 g_{d0_1}\chi|A_{i_2}|^2/4 \quad (39)$$
$$S_{M_2} = 4kT\gamma_2 g_{d0_2}\xi \quad (40)$$
$$|G_{m_1}| = \frac{\omega_T}{2\omega_0\sqrt{\omega_T L_s R_s}} \quad (41)$$
$$A_{i_2} = i_{out_2}/i_{out_1} \quad (42)$$
$$\chi \triangleq 1-2\omega_0 L_s g_m|c|\kappa+(1+\omega_0^2L_s^2g_{m_2}^2)\kappa^2 \quad (43)$$
$$\kappa \triangleq \frac{1}{\omega_0^2 C_{gs_1}L_s}\sqrt{\frac{\delta_1 g_{g_1}}{\gamma_1 g_{d0_1}}} \quad (44)$$
$$\xi \triangleq \eta(g_{ds_1}^2+\omega_0^2C_{tot}^2)+\eta^2\rho\tau+\eta\tau^2 \quad (45)$$
$$\eta \triangleq \frac{1}{(g_{ds_1}+g_{m_2})^2+\omega_0^2C_{tot}^2} \quad (46)$$
$$\rho \triangleq 2\omega_0 C_{tot}g_{m_2}|c|[(g_{ds_1}+g_{m_2})^2+\omega_0^2C_{tot}^2] \quad (47)$$
$$\tau \triangleq g_{m_2}\sqrt{\frac{\delta_2 g_{g_2}}{\gamma_2 g_{d0_2}}} \quad (48)$$
$$C_{tot} \triangleq C_{db_1}+C_{sb_2}+C_{gs_2} \quad (49)$$

In these derivations, the overlap capacitance C_{gd} is neglected for the sake of simplicity. Despite the use of a cascoded stage, this simplification introduces errors. Nevertheless, this analytical approach helps understanding the behind noise contribution mechanism of the LNA.

C. Noise Analysis Based on Two-Port Theory

As illustrated in Fig. 13, the LNA consists of three cascading stages. The noise matrix of the first stage ($\boldsymbol{C}_{A,1st}$) can be easily found based on the network parameters. In the second stage, using Eq. (26), the four-noise parameters of the MOSFET (M_1) need to be transformed into the impedance noise matrix form ($\boldsymbol{C}_{Z,M_1}$) first and then added to the source inductor component ($\boldsymbol{C}_{Z,L_s}$). Finally the noise matrix of the third stage ($\boldsymbol{C}_{A,3rd}$) can be obtained using (15) – (17). Note that the noise contribution from Y_{sub} needs to be subtracted from

the second stage and added to the third stage. Finally the noise performance of the entire LNA is given by cascading the three stages using (23):

$$\boldsymbol{C}_{A,LNA} = \boldsymbol{A}_{1st}\boldsymbol{C}_{A,2nd+3rd}\boldsymbol{A}_{1st}^{\dagger} + \boldsymbol{C}_{A,1st} \quad (50)$$

$$\boldsymbol{C}_{A,2nd+3rd} = \boldsymbol{A}_{2nd}\boldsymbol{C}_{A,3rd}\boldsymbol{A}_{2nd}^{\dagger} + \boldsymbol{C}_{A,2nd} \quad (51)$$

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