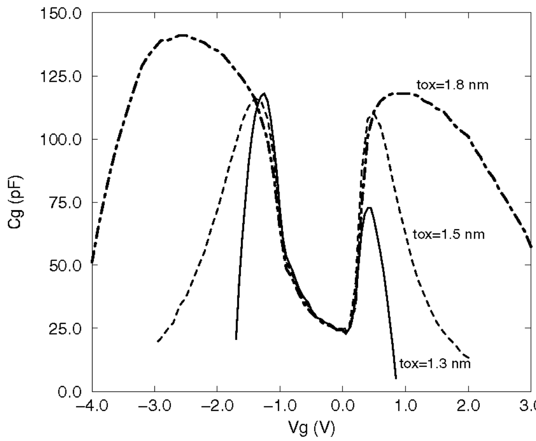


Fig. 1. Experimental MOS C-V for t_{ox}=1.3, 1.5, and 1.8 nm, respectively.

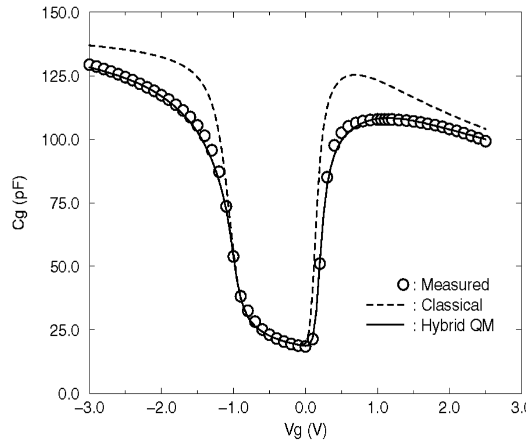


Fig. 2. Experimental C-V and simulated by using hybrid QM correction model for NMOS capacitors with t_{ox}= 2.1 nm.

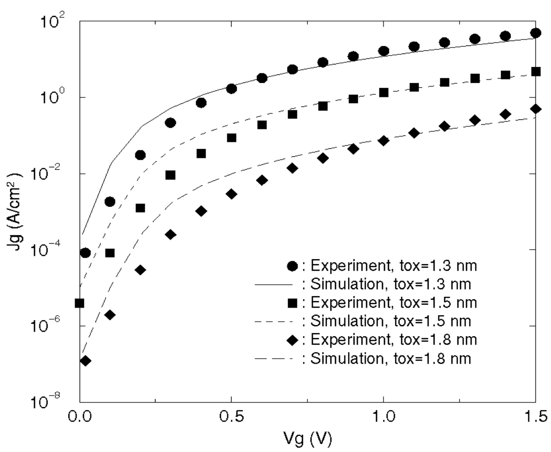
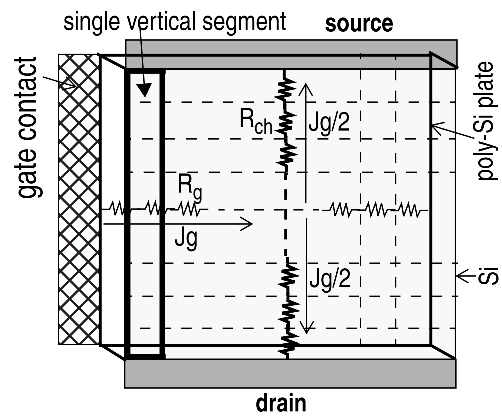
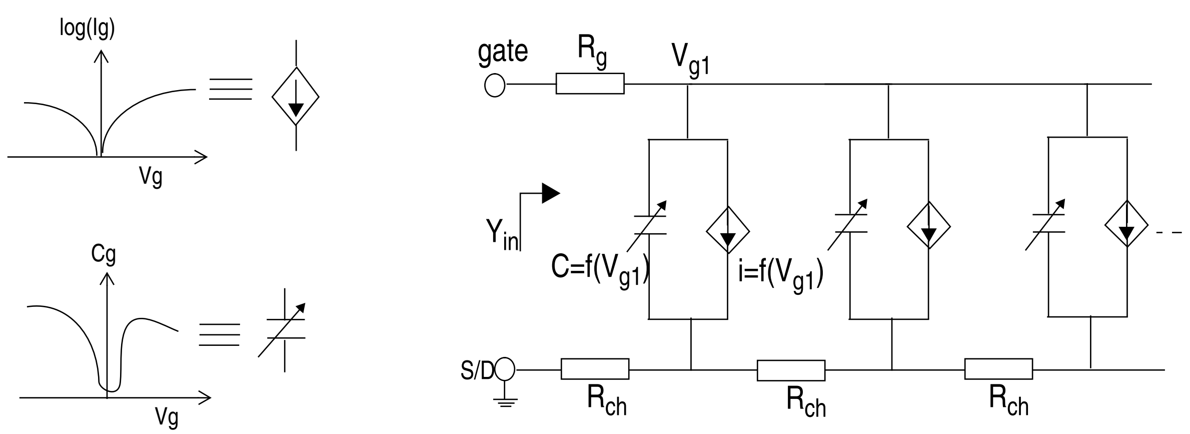


Fig. 3. Measured and simulated gate tunneling current using a 1D Green's function solver for t_{ox} = 1.3, 1.5, and 1.8 nm.



(a) top view of a NMOS capacitor with source/ drain grounded (area = 100 x100µm)



(b) Distributed RC network with the non-linear capacitors and current sources to model the gate tunneling current

Fig. 4. An equivalent RC circuit of a MOS capacitor for gate oxide thicknesses thinner than 2.0 nm .

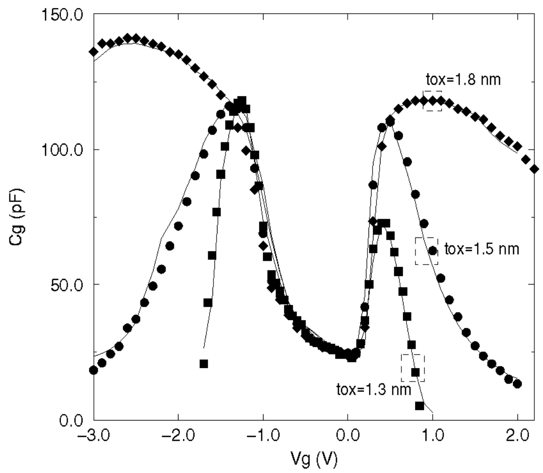


Fig. 5. Results of AC network analysis for the equivalent circuit in Fig. 4, Symbols represent measured C-V, and lines are simulated C-V obtained by taking the imaginary components of input admittance (Yin).

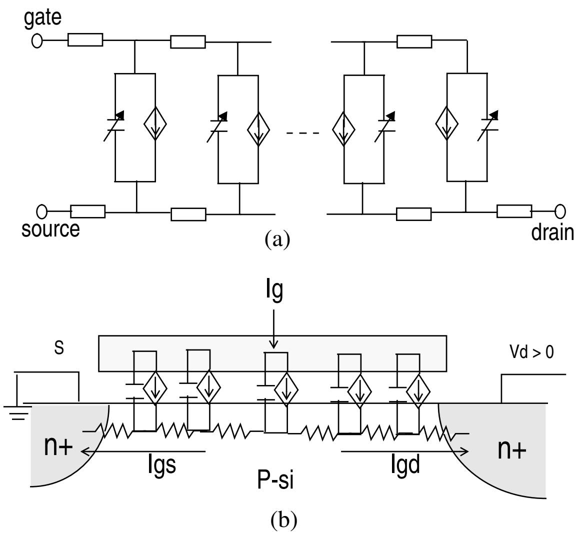


Fig. 6. Modeling of gate tunneling current considering drain bias effects, (a) equivalent circuit for MOSFET (b) Ig (=Igs+Igd) on MOSFET cross-section

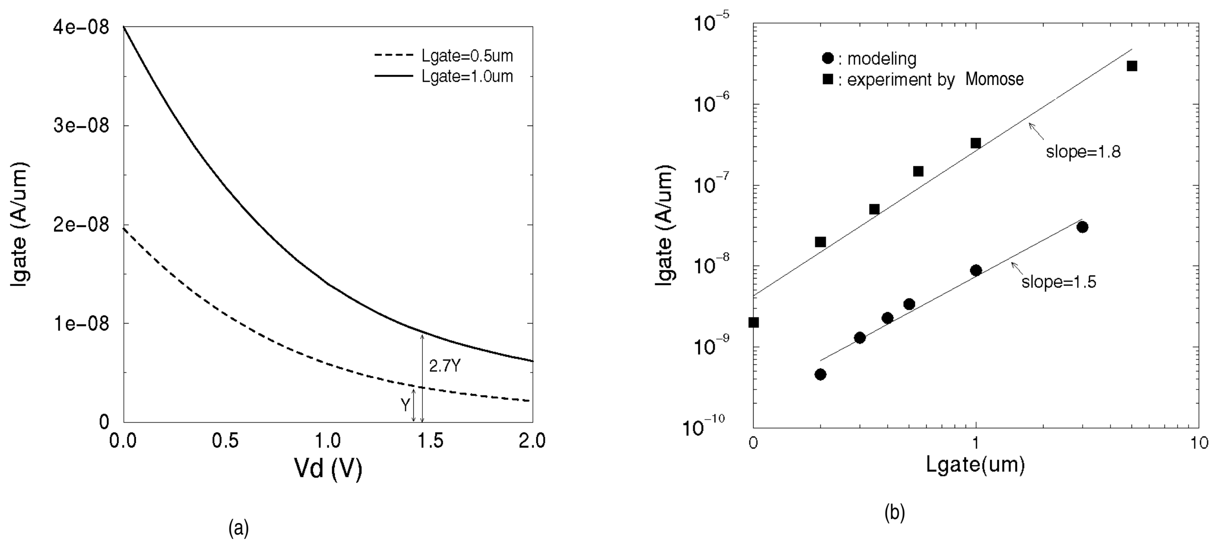
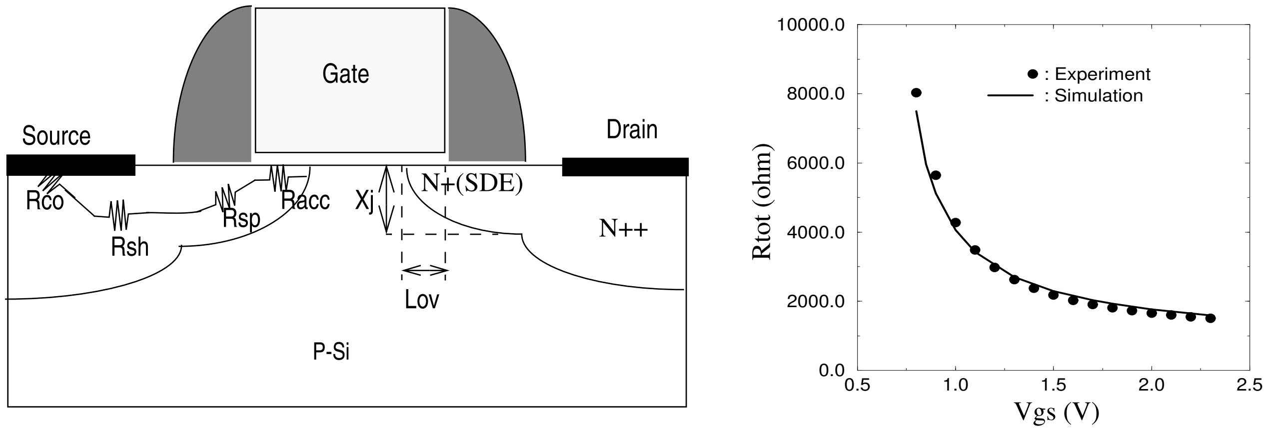
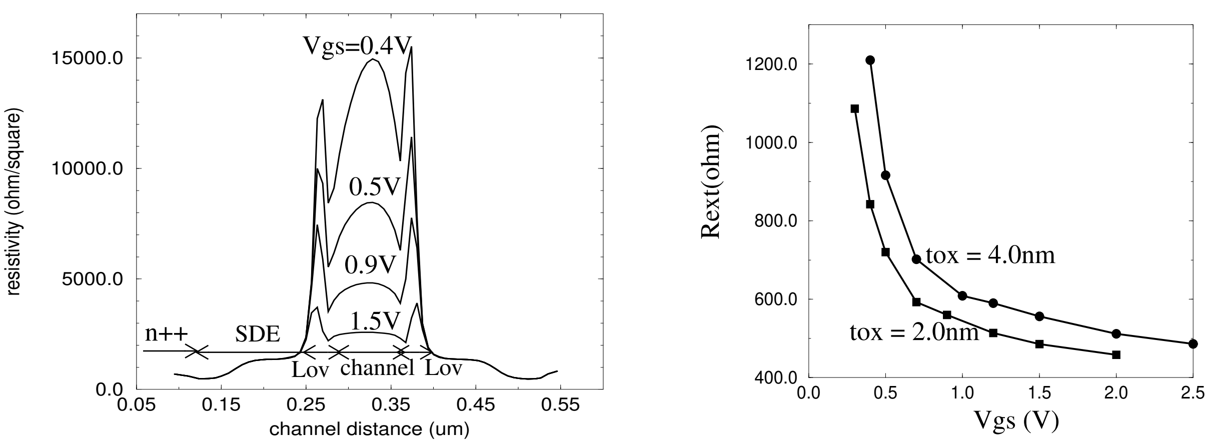


Fig. 7. Drain bias and gate channel length dependence of gate tunneling current of tox=1.5nm, (a) Ig vs. Vds for Lg=0.5 and 1.0 μm when Vg=1.5V, (b) dependence of Ig vs. Lg, modeling of this work and experiments of ref [10] when Vd=Vg=1.5V.



(a) (b)

Fig. 8. External resistance in High-Doped Drain (HDD) NMOS
(a) External resistance components in source/drain extention (SDE) NMOS (R_{acc}:accumation, R_{sp}:spreading, R_{co}:contact, R_{sh}:sheet resistance)
(b) Comparisons of experimental and simulated total resistance (R_{tot}=R_{ch}+R_{ext}) of L_{eff}=0.25 μm NMOS for Vds=0.1V, the unified mobility model for inversion/accumulation is used in device simulation.



(a) (b)

Fig. 9. Simulated external resistance with respect to Vgs biases (Vds=0.05V), L_{eff}=0.08 μm and X_j=40 nm.
(a) Resistivity along channel direction at t_{ox}=2.0 nm.
(b) R_{ext} (=R_s+R_d) for Vgs when tox's are 2.0 and 4.0 nm, respectively.

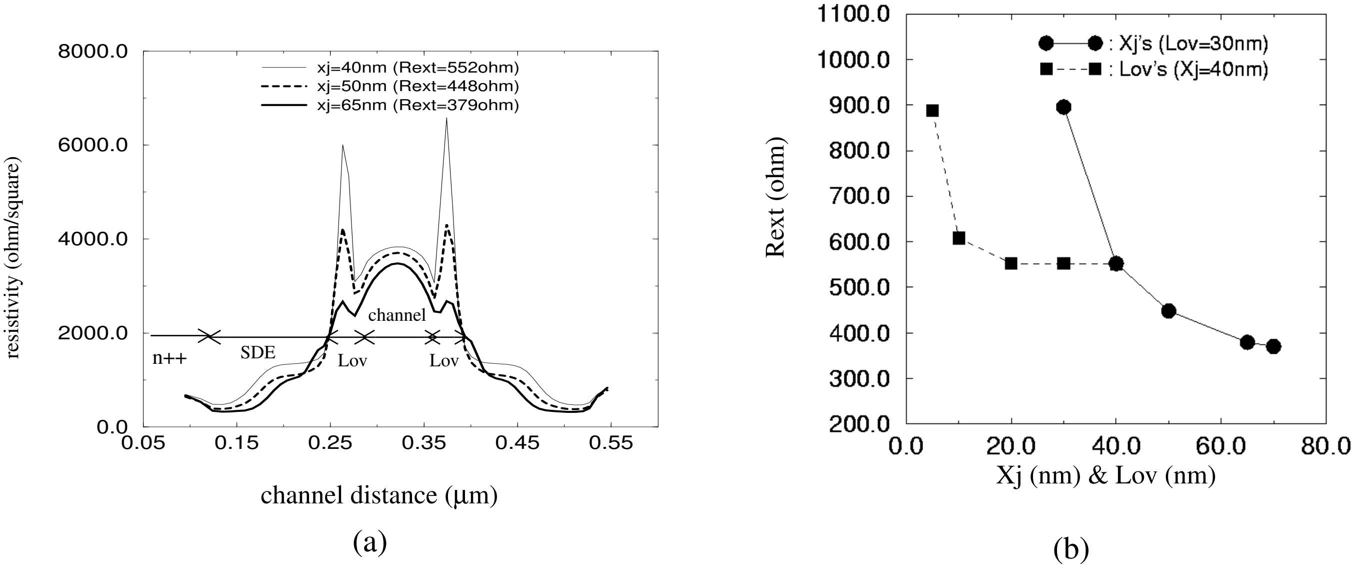


Fig. 10. Simulated external resistance with respect to SDE depths (X_j) when Vgs=1.5V and Vds=0.05V (L_{eff}=0.08 μm and t_{ox}=4.0 nm).
(a) Resistivity along channel direction for Xj=40, 50 and 65 nm, respectively.
(b) Rext (=Rs+Rd) for different X_j and overlap length (L_{ov}).

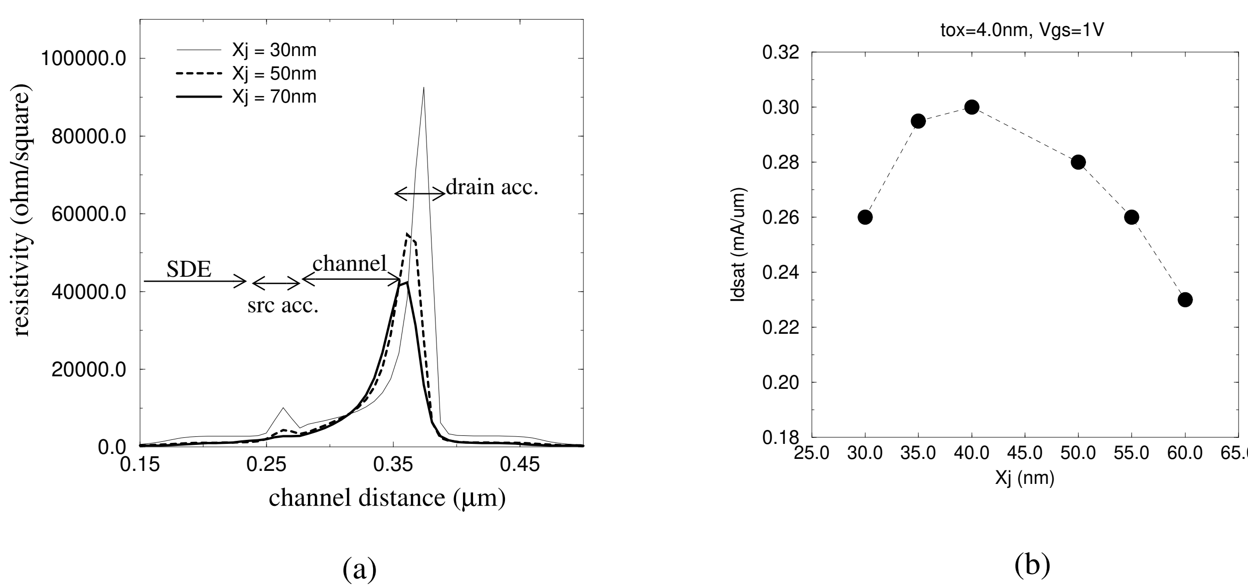


Fig. 11. External resistance for different X_j at saturation bias condition.
(a) Rext with respect to X_j at Vds=Vgs=1.5V
(b) Simulated Idsat (I_{on} current) for Vds at I_{off}=1 nA/μm of leakage current.

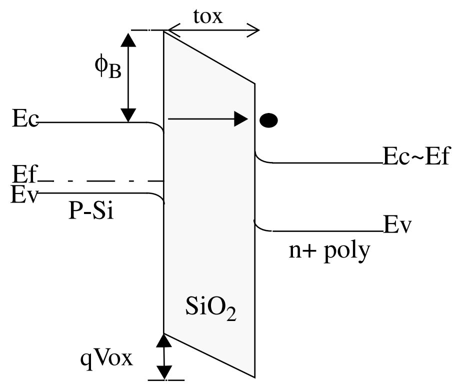


Fig. 12. Direct tunneling at n+-poli / SiO2 / p-sub. structure (Vox < ϕ_B).

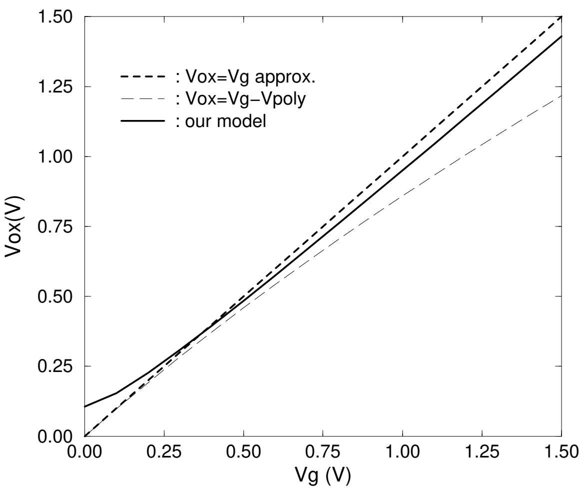


Fig. 13. Simulated gate current using Vg approximation, Vg-Vpoly, and surface potential based model. Symbols are obtained from NEMO, an approximated Schrodinger's equation solver (tox=1.5 nm)

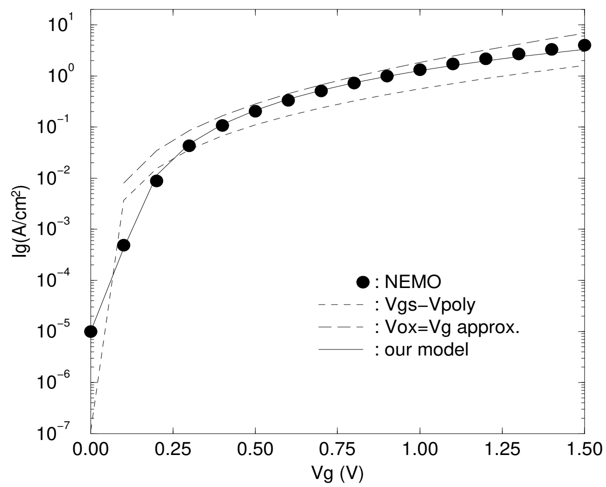


Fig. 14. Simulated gate current using Vg approximation, Vg-Vpoly, and surface potential based model. Symbols are obtained from NEMO, an approximated Schrodinger's equation solver (tox=1.5 nm)

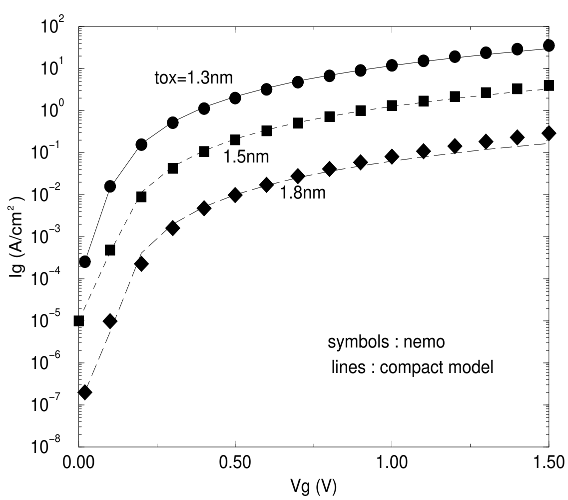


Fig. 15. Comparisons of simulated gate current using new model for different tox's (1.3, 1.5 and 1.8 nm). Symbols denote the results from NEMO.

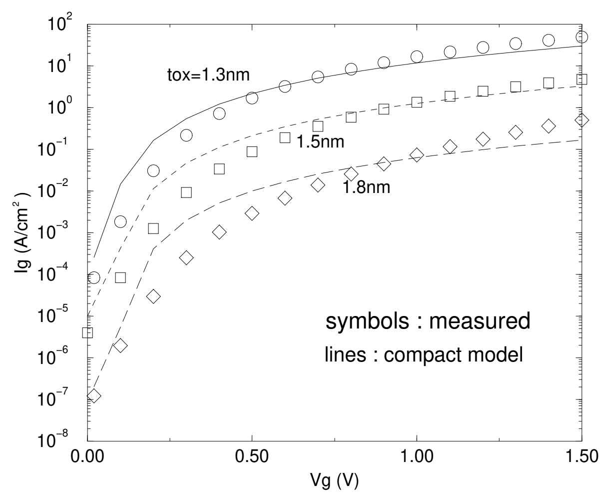


Fig. 16. Comparisons of gate current between the new model and real measured data for tox=1.3, 1.5 and 1.8nm. Symbols represent the measured data.

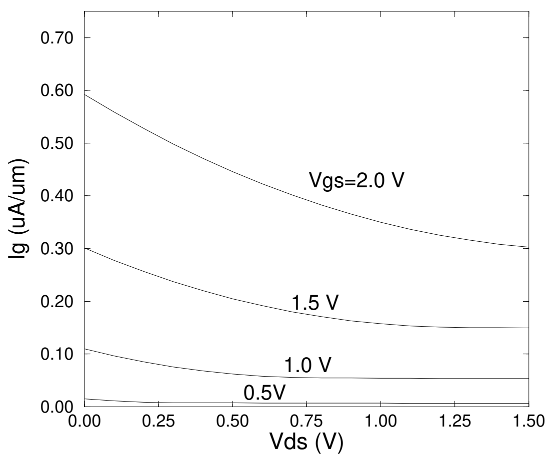


Fig. 17. Simulated gate tunneling current w.r.t Vds bias for different gate biases (tox=1.5 nm).

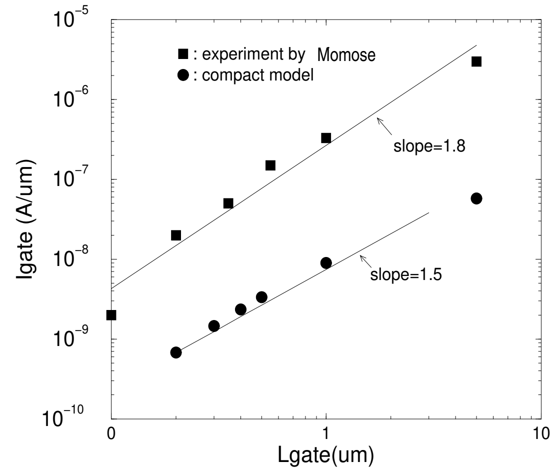


Fig. 18. Gate length dependence of gate tunneling current for tox=1.5 nm, the simulated slope is comparable with ref. [10] due to consideration of DIBL effect.

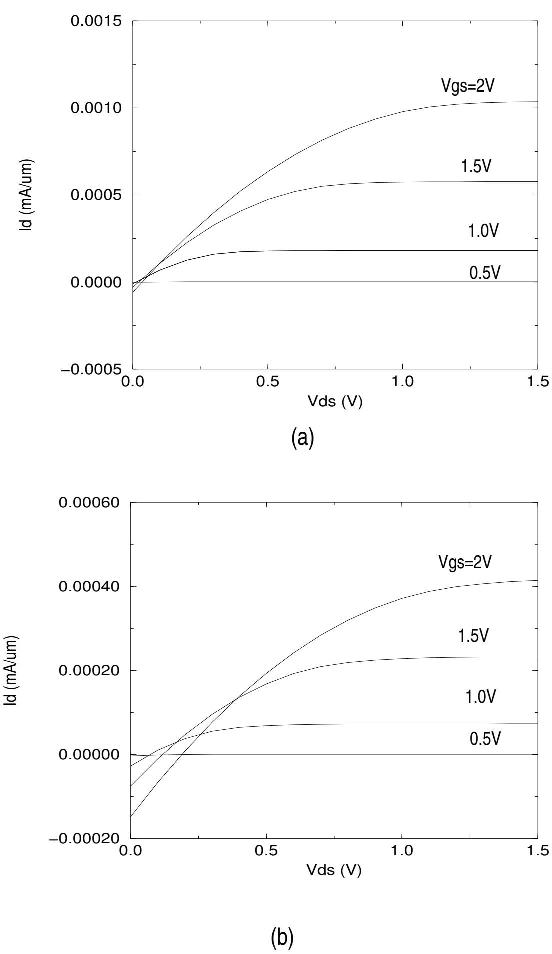


Fig. 19. Simulated drain current (Id) vs. Vds for tox=1.5 nm, (a) Lg=20 μm (b) Lg=50 μm.

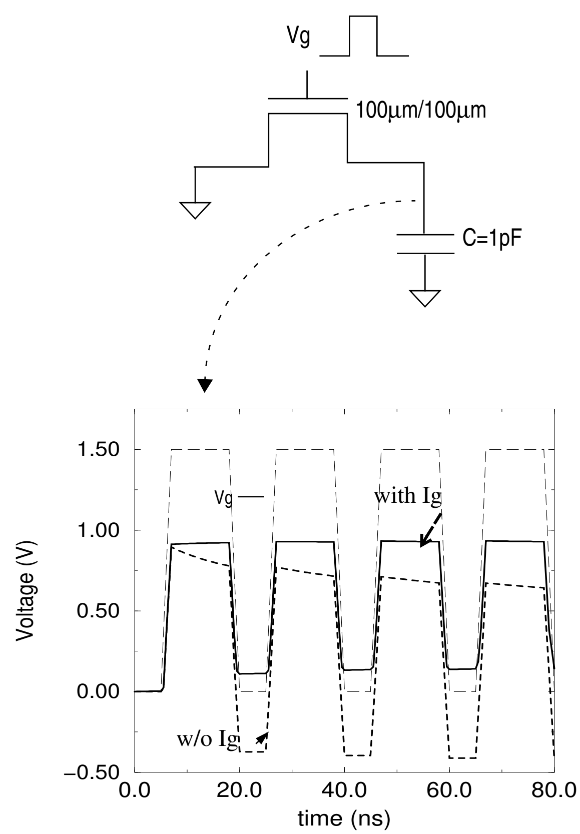


Fig. 20. Transient circuit simulation with and without gate tunneling current models, W/L=100 μm/100 μm and tox=1.5 nm.