Technology Limits and compact model for SiGe Scaled FETs

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ABSTRACT

Stress relaxation in strained-Si MOSFETs can be significant in the presence of compressive stress imposed by trench isolation, especially for highly scaled active regions. Stress of the strained region is reduced by ∼2/3 when the active region is scaled from L_{active}=0.4 μm to 0.1 μm. Mobility can be lower by 50 % for narrow active widths resulting from the strain relaxation. The strain relaxation may restrict the use of strained-Si MOSFETs for technology nodes beyond 25 nm. Electrical and thermal characteristics of strained-Si devices are investigated and a compact junction capacitance model for strained-Si MOSFET suitable for circuit simulation is proposed.

Keywords: Strained-Si, STI, stress, ESD, capacitance.

1 Introduction

Strained-Si MOSFET becomes a promising device for CMOS beyond the 50 nm node to overcome scaling limitations, since the strained-Si layer grown on relaxed SiGe increases carrier mobility. However, recent studies show that the mobility of strained Si NMOS degrades as the gate length becomes shorter [6], which raises scalability issues in strained-Si MOSFETs. Also, the thermal conductivity of $Si_{0.8}Ge_{0.2}$ is 15 times lower than that of bulk-Si, such that self-heating problems similar to that for SOI can cause performance degradation in strained-Si devices [6]. This article investigates technology limits of of strained-Si devices in terms of electrical and thermal characteristics.

2 STI Effects on Strained Si

Shallow Trench Isolation (STI)-induced compressive stress reduces carrier mobility and drive current in bulk NMOS transistors as design rules continue to shrink [2]. The compressive stress in silicon from trench isolation makes the NMOS drive current highly sensitive to the transistor layout. Thus, problems arise when the process-induced stress can relax the tensile stress in the strained layer for scaled active regions. In this work, stress analysis is performed based on lattice and thermal mismatch models for SiGe and silicon depositions, as well as STI formation by using 2 & 3D process/device simulations [3].

Fig. 1 shows the cross-section of a strained Si layer, which is grown on the relaxed SiGe seed layer with a Ge mole fraction of 0.2. The lattice constant of SiGe is based on Vegard's law and the lattice mismatch strain is calculated when Si is grown on the SiGe layer. Stress relaxation is calculated for a structure where the trench is etched out and oxide filling is then used.

Fig. 2 shows two-dimensional stress analysis results of a strained active region with STI for different lengths of active layers (L_{active}). The initial stress (S_{xx}) in the strained Si layer is ∼1400 MPa for L_{active} = 0.4 μm (L_G = 0.1 μm), which is reduced to 1033 Mpa after the STI process. The tensile stress in the strained layer is reduced down to 600 MPa and 350 MPa as L_{active} is scaled to L_{active} = 0.2 μm (L_G = 50 nm) and L_{active} = 0.1 μm (L_G = 25 nm), respectively.

3 Stress Relaxation and Mobility

Strain relaxation is dependent not only on the device geometry, but also on thermal annealing. Three-dimensional device simulations are performed based on the stress-induced bandgap change model, in which the bandgap varies with regard to mechanical stress and strain tensors in silicon region [4]. In addition, the stress-induced mobility model combined with phonon and surface scattering mobility models are utilized to account for mobility corrections due to the mechanical stress; electron mobility becomes anisotropic for stress-induced band shifts and changes in effective mass. The longitudinal and transverse effective electron masses are based on the $k-p$ theory for Si grown on the $Si_{0.8}Ge_{0.2}$ surface [5]. Fig. 3 shows simulated $I_D - V_G$ and $g_m - V_G$ based on stress calculations for different annealing conditions after STI process - 1s, 800°C and 10s, 850°C. This implies that mobility enhancement degrades for the higher temperature annealing condition that enhances strain relaxation. Fig. 4(a) shows S_{xx} contours for different active widths; stress relaxation in the strained layer is enhanced for the narrower active width due to impact of the surrounding STI. As a result, mobility enhancement of the narrow width device (i.e. W = 0.2 μm) is reduced by more than 50 % compared to that of the wider device (i.e. W = 1.7 μm), as shown in Fig. 4(b).

4 Modeling for High Current Operation

The thermal conductivity of $Si_{0.8}Ge_{0.2}$ is 15 times lower than that of bulk-Si, such that self-heating problems similar to that for SOI can cause performance degradation in strained-Si devices [6]. Fig. 5(a) shows device structure of a

bulk NMOS and a strained-Si NMOS. In order to determine energy band structures of the strained-Si device, material parameters are used based on Ref. [7]. Fig 5(b) are simulated energy band diagrams for a strained- and a bulk-Si devices by using MEDICI. $E_{n,\parallel}$ is the electric field into current flow direction. In order to determine the phonon mean free path for electrons (λ_n) of strained-Si, the energy relaxation times are calculated, as the mean free path is closely related to the energy relaxation times in the scattering process. Fig. 6 represents calculated energy relaxation times of electrons for strained-Si and bulk-Si with respect to electric field and electron temperature, based on full-band Monte Carlo (FBMC) device simulation [8]. In the Ref. [6] the energy relaxation time was increased by roughly a factor of two from the bulk-Si device. The FBMC simulation results in Fig. 6 show that the increase of energy relaxation time of the strained-Si relative to bulk-Si is reduced as the electric field increases (i.e. at high electron temperature). In this work, λ_n of the strained-Si on $Si_{0.75}Ge_{0.25}$ layer has been assumed to be increased by 20% from that for the bulk-Si (λ_n = 10 nm for bulk-Si).

5 Electro-Thermal Simulation

Fig. 7(a) shows simulated I_D-V_D curves for strained- and bulk-Si devices (V_G = 0 V). The snapback voltage of the strained-Si device is lower than that for bulk-Si device. The hold voltage (V_h), that is the minimum voltage required for the bipolar operation, is also lower for the strained-Si device. The second breakdown triggering current (I_{t2}) for strained-Si device is higher relative to bulk-Si device. As a result, the power density and peak lattice temperature during the parasitic bipolar operation are lower for the strained-Si device than that for bulk-Si device. The main current path is the strained-Si layer during normal operation, while the main current path during the parasitic bipolar action is the buried SiGe layer. Fig. 7(b) shows peak temperature versus drain current (I_D) for bulk- and strained-Si devices. There is an abrupt increase of lattice temperature at ~0.008 A/μm of drain current for the bulk-Si device. As a result, thermal failure occurs for the bulk-Si device ($T > T_c$~1650°K) when the drain current is ~0.01 A/μm (I_{t2}) due to its high power density. This implies that even though the thermal dissipation of strained-Si is worse compared to silicon due to the 30 times lower thermal conductivity of SiGe layer, the local temperature overheating can effectively be suppressed in strained-Si devices owing to the higher bipolar gain (β) and current uniformity.

6 Compact Junction Capacitance Model

Higher permittivity and smaller bandgap of SiGe result in higher junction capacitance in strained-Si devices, which degrades circuit performance of S-Si MOS circuits. Fig. 8 shows drain-to-bulk junction capacitance obtained from device simulations, for strained-Si/$Si_{0.75}Ge_{0.25}$ and unstrained (bulk)-Si NMOS devices. The increase of junction capacitance in strained-Si is about 16% compared to bulk-Si NMOS at the zero-bias, while the increase is 8% for V_{DB} = 2.0 V. The sharper decrease of bias-dependent junction capacitance in strained-Si device can be attributed to the reduced junction built-in potential (ϕ_{BA} and ϕ_{BSW}) for strained-Si, which should be considered in a compact model. Fig. 9 represents junction capacitance components for strained-Si NMOS. It should be noted that sidewall junction capacitance (C_{JSW}) consists of two capacitance components, $C_{JSW,SSi}$ and $C_{JSW,SiGe}$, to take into account the different material parameters– permittivity, bandgap and built-in potential. As a result, the sidewall junction capacitance of S-Si device can be expressed as shown in the equation in the figure.

Fig. 9 shows calaculated drain-to-bulk junction capacitance (C_{DB}) versus V_{DB} of strained-Si NMOS based on the compact model; curves are shown for various Ge mole fractions, x = 0 (unstrained-Si), 0.15, 0.25, 0.35, while other parameters remain same. The good agreemetns between the compact model and the numerical model can be attributed to considerations of the two different junction sidewall capacitance components for the strained-Si layer and the SiGe layer.

7 Summary

Stress relaxation in strained-Si layers can be significant in the presence of compressive stress imposed by trench isolation, especially for highly scaled active regions. Stress of the strained region is reduced by ~2/3 when the active region is scaled from 0.4 μm to 0.1 μm. The strain relaxation may restrict the use of strained-Si MOSFETs for technology nodes beyond 25 nm. However, the strained-Si NMOS has higher bipolar current gain and impact ionization rate due to its narrower energy band gap and longer phonon mean-free-path. Thus, contrary to SOI devices, the strained-Si NMOS can be used as an effective ESD protection device, despite its self-heating problems caused by the lower thermal conductivity of SiGe layer. A compact junction capacitance model for strained-Si MOSFET has been developed, which shows good agreement with device simulation results due to considerations of junction sidewall capacitances for both strained-Si and SiGe layers.

Acknowledgment

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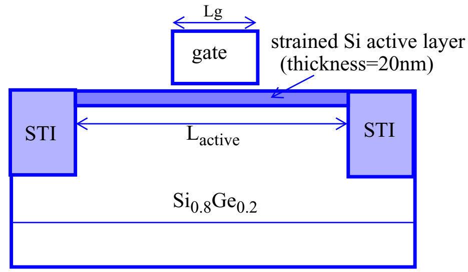
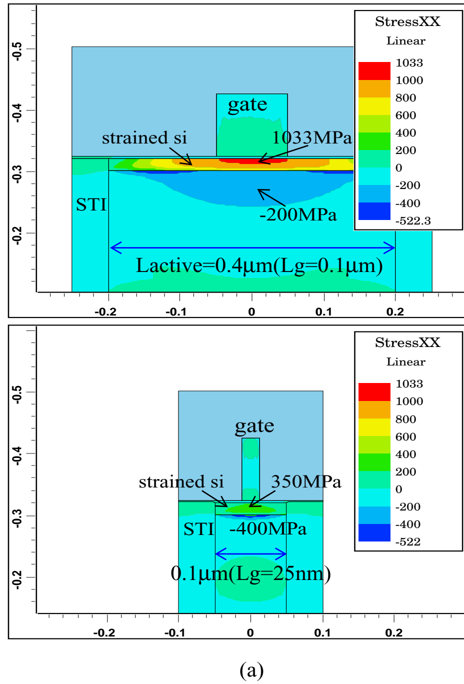
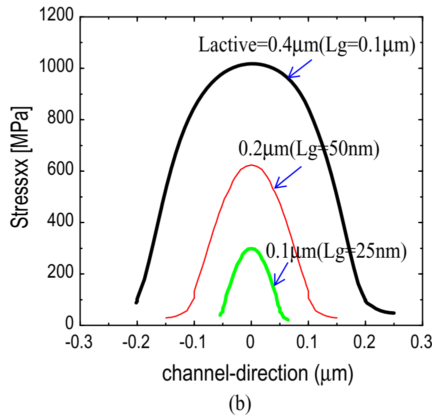


Fig. 1. A cross-section of strained Si active layer on $Si_{0.8}Ge_{0.2}$ layer.



(a)



(b)

Fig. 2. Two-dimensional stress analysis of strained actives with STI effects (a) stress (Sxx) contours for Lactive=0.4µm (Lg=0.1µm) and Lactive=0.1µm (Lg=25nm) (b) comparison of tensile stresses in strained layer along the channel direction for different active lengths (Lactive) .

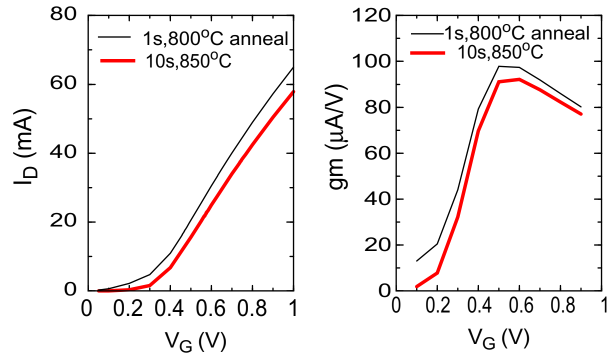
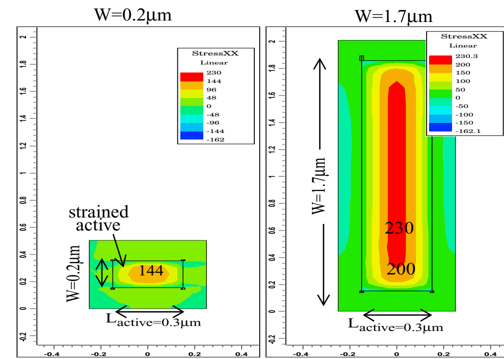
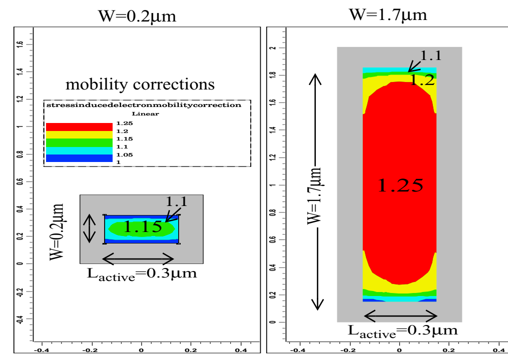
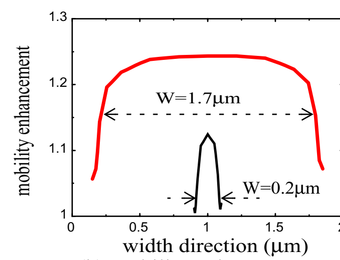


Fig. 3. Simulated I_D-V_G and gm-V_G based on stress calculation for different annealing conditions after STI process - 1s, 800°C and 10s, 850°C.



(a) Sxx





(b) mobility enhancement

Fig. 4. STI effects for narrow width active strained region, (a) Sxx contours for W/L = 0.2µm/0.1µm and 1.7µm/0.1µm (b) Szz (c) stress-induced mobility enhancements for W=0.2 and 1.7µm.

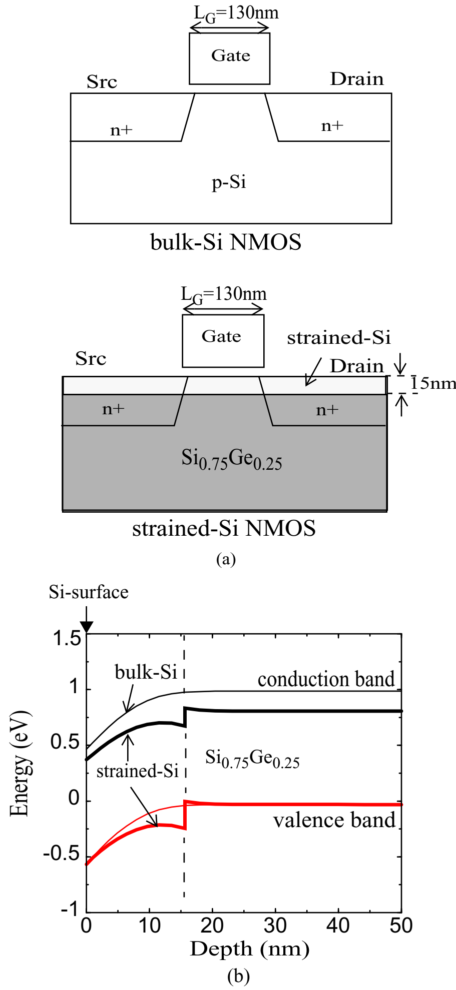


Fig. 5.. Strained Si NMOS and its band diagrams, (a) bulk-Si NMOS and strained-Si NMOS with 15nm strained layer thickness on $Si_{0.75}Ge_{0.25}$, (b) band-diagrams of the device at V_G=0 V into the depth direction at the position denoted in (a) with an arrow.

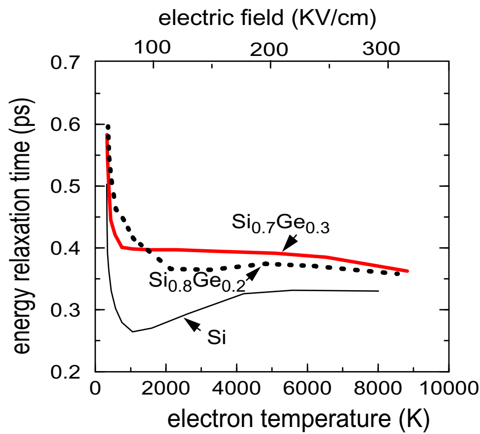


Fig. 6. Electron energy relaxation times vs. electron temperatures for strained-Si and bulk-Si devices from full-band Monte Carlo simulation.

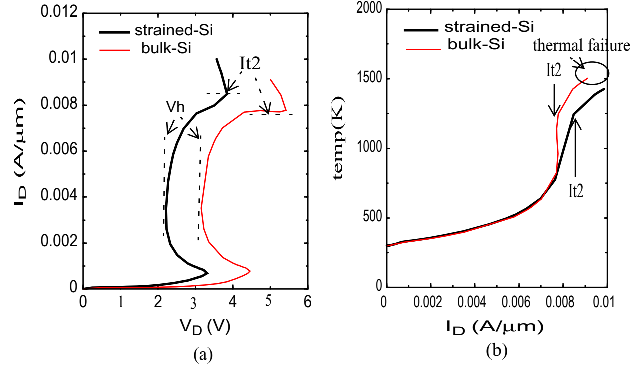


Fig. 7. I_D/V_D vs. temperatures for strained-Si NMOS and bulk-Si NMOS, (a) V_D vs. lattice temperature (b) I_D vs. lattice temperature.

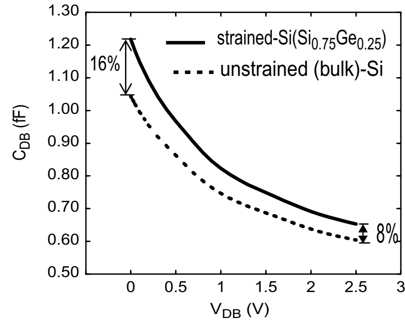
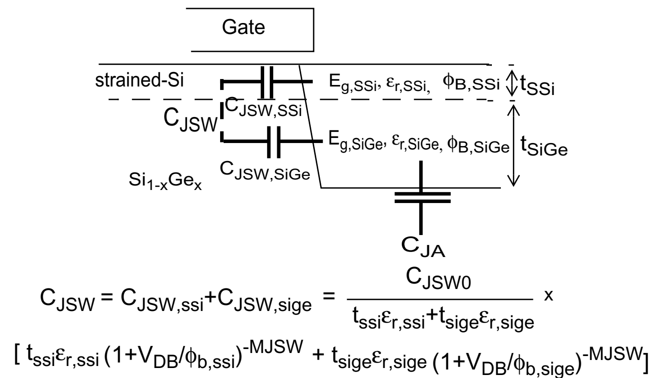


Fig. 8. Simulated drain-to-bulk junction capacitance for strained-Si and bulk (unstrained) Si MOSFETs.



$$C_{JSW} = C_{JSW,ssi}+C_{JSW,sige} = \frac{C_{JSW0}}{t_{ssi}\varepsilon_{r,ssi}+t_{sige}\varepsilon_{r,sige}} \times$$
$$[\, t_{ssi}\varepsilon_{r,ssi}\,(1+V_{DB}/\phi_{b,ssi})^{-MJSW} + t_{sige}\varepsilon_{r,sige}\,(1+V_{DB}/\phi_{b,sige})^{-MJSW}]$$

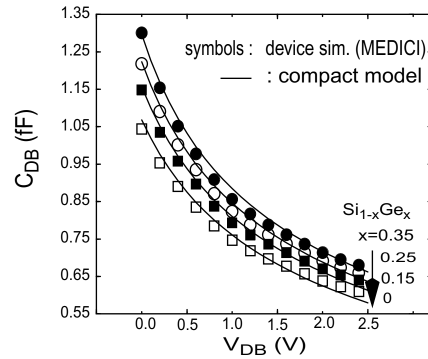


Fig. 9. Comparisons of junction capacitances betwwen the obtained from the compact model and device simulation.