Parasitic Characterization of Radio-Frequency (RF) Circuits Using Mixed-Mode Simulation

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Abstract

Accurate estimation of the parasitics in high-speed circuits is critical in optimizing circuit performance. A new method for parasitic characterization of high-speed circuits employing mixed-mode circuit and device simulation is proposed. The intrinsic characteristics are captured using a device simulator and the equivalent circuit for passive extrinsic elements are evaluated in a straightforward manner from impedance and admittance representation of measured S-parameters. This decoupling enables total performance optimization based on separate tuning of layout and the fabrication process recipe.

I. Introduction

For monolithic microwave and RF integrated circuit applications, accurate modeling of parasitic element is critical for the device performance analyses such as power gain, bandwidth and stability analyses. Usually, the small-signal equivalent circuit is obtained at many bias settings using S-parameter (Scattering parameter) measurements over the frequency range of interest, either by analytical methods or using optimization techniques. The disadvantage of the optimization approach is that the results can vary depending upon the fitting method and the starting guess. In the case of analytical parameter fitting, additional test structures are usually required to consider de-embedding the S-parameters from the parasitic environment, and other steps (cold measurements [1]) are necessary to distinguish between bias dependent and independent elements.

In this paper, we use a mixed-mode (circuit and device) simulation approach for characterization of device-level behavior modeling. The circuit is separated into the intrinsic and extrinsic parts. The active intrinsic device characteristics are modeled using device simulation [3, 4] instead of a fixed equivalent circuit model such as the Gummel-Poon representation. The extrinsic lumped elements are extracted analytically by comparing simulated S-parameters of the intrinsic device and experimental S-parameters

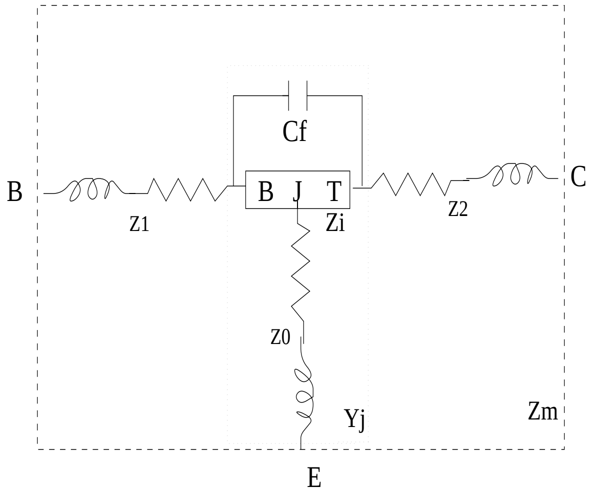

Figure 1: A T-like network for characterization of monolithic RF BJT devices.

extracted from the entire circuit. This method decouples the circuit element dependencies between layout and doping profiles; hence the distributive aspects of the intrinsic device can be taken into consideration directly. Due to inefficiencies in simulating the entire multi-finger structures, only a 2-D cut of a single emitter and base finger structure is considered in device simulation. The full structure is analytically combined to represent the intrinsic part. More accurate simulation is possible using 3-D simulations, at the cost of more computational power.

II. Methodology

The basic tool for parasitic extraction is the mixed-mode circuit and device simulator [2] which interfaces Stanford's device simulator PISCES-2ET [4] and UC Berkeley's circuit simulator SPICE-3f2. The characterization of device performance at high frequencies using S-parameter extraction is widely accepted. For devices which are fabricated on monolithic substrate, the circuit often exhibits parasitic behavior due to elements that can be represented by a two-port network configuration as shown in Fig. 1.

This T-like topology has been used successfully by many authors [5, 6] . For this network it is assumed

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that over the frequency range of concern (from 300 MHz to 3 GHz) the equivalent circuit composed of lumped RLC elements, can be described using general interconnect parasitics. In reality, at high frequencies the interconnect circuit parameters such as resistance may vary with frequency, due to skin and other distributive effects. However, for the frequency range considered here, frequency-independent modeling parameters are usually sufficient.

Accurate physical modeling of the intrinsic device, excluding any other parasitics such as interconnect, bond wire, and contacts is performed using the device simulator. The input doping profiles are extracted from SUPREM 1D simulation, calibrated with measurements. For electrical characteristics, the Gummel plot and the cut-off frequency f_T are fitted to measurements. Standard bipolar models such as Auger, concentration dependent SRH, and concentration dependent mobility are used and parameters such as lifetimes and ambient temperature are adjusted slightly. Also adaptive gridding is essential for accurate simulation at low current levels. This device is then simulated using mixed-mode approach at specific bias conditions; Y-parameters are thus obtained. Using this procedure, V_{be} of the intrinsic device can be determined at the same current levels as those used in measurements, since Gummel plots are used for calibration. The effect of small variations of V_{ce} on S-parameters are negligible. Hence, V_{ce} of the intrinsic device can be chosen by comparing with measured external V_{ce}. Another method for determining bias conditions of the intrinsic device is to first perform extraction at a small V_{be} level since the effects of resistive parasitics plays a negligible role there.

As shown in Fig. 1, construction of the two-port matrices from the inner shell $[Z_i]$ to the outer one $[Z_m]$ or vice versa is straightforward. The analytical expression for Z_m, obtained by expanding from the intrinsic matrix Z_i, is shown below.

The intrinsic device is characterized using a two port network.

$$Z_i = \begin{vmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{vmatrix}$$

Inclusion of Z_0 and C_f results in,

$$Y_j = \frac{1}{\Delta Z} \begin{vmatrix} Z_{22}+Z_0 & -Z_{12}-Z_0 \\ -Z_{21}-Z_0 & Z_{11}+Z_0 \end{vmatrix}$$

$$+jwC_f \begin{vmatrix} 1 & -1 \\ -1 & 1 \end{vmatrix}$$

$$\Delta Z = Z_{22}Z_{11} - Z_{12}Z_{21} + Z_0(Z_{22}+Z_{11}-Z_{12}-Z_{21})$$

$$Z_0 = R_0 + jwL_0$$

Inclusion of Z_1 and Z_2 at the input and output ports gives,

$$Z_m = \frac{1}{det(Z_j)} \begin{vmatrix} Z_{j11} & Z_{j12} \\ Z_{j21} & Z_{j22} \end{vmatrix} + \begin{vmatrix} Z_1 & 0 \\ 0 & Z_2 \end{vmatrix}$$

$$det(Z_j) = 1 + jwC_f(Z_{22}+Z_{11}-Z_{12}-Z_{21})$$

$$Z_{j11} = Z_{11} + Z_0 + jwC_f\Delta Z$$

$$Z_{j12} = Z_{12} + Z_0 + jwC_f\Delta Z$$

$$Z_{j21} = Z_{21} + Z_0 + jwC_f\Delta Z$$

$$Z_{j22} = Z_{22} + Z_0 + jwC_f\Delta Z$$

$$Z_1 = R_1 + jwL_1$$

$$Z_2 = R_2 + jwL_2$$

The first step is to obtain C_f from

$$Z_{m12} - Z_{m21} = \frac{Z_{12}-Z_{21}}{det(Z_j)}$$

By inserting the extracted C_f in Z_{m12}, Z_{m11}, and Z_{m22}, all other parasitics Z_0, Z_1, and Z_2 can be found.

$$jwC_f = \frac{Z_{12}-Z_{21}+Z_{m21}-Z_{m12}}{(Z_{m12}-Z_{m21})(Z_{22}+Z_{11}-Z_{12}-Z_{21})} \tag{1}$$

$$Z_0 = \frac{Z_{m12}det(Z_j) - Z_{12} - jwC_f(Z_{11}Z_{22}-Z_{12}Z_{21})}{1+jwC_f(Z_{11}+Z_{22}-Z_{12}-Z_{21})} \tag{2}$$

$$Z_1 = Z_{m11} - \frac{Z_{11}+Z_0+jwC_f\Delta Z}{1+jwC_f(Z_{11}+Z_{22}-Z_{12}-Z_{21})} \tag{3}$$

$$Z_2 = Z_{m22} - \frac{Z_{22}+Z_0+jwC_f\Delta Z}{1+jwC_f(Z_{11}+Z_{22}-Z_{12}-Z_{21})} \tag{4}$$

III. Simulation Results and Discussion

It is critical to model the intrinsic device as accurately as possible. The cross sectional view of the modeled intrinsic device and the fitted Gummel plot is shown in Figs. 2 and 3. The most sensitive parameters in fitting the Gummel plot are carrier lifetimes and doping profiles in the active transistor region. Mobility is a relatively insensitive parameter in fitting the Gummel plot. For f_T, the simulated value of 3.5 GHz is achieved in comparison with a measured value of 3.15 GHz.

Using the parasitic extraction method previously described, each component is calculated over the frequency range of 300 MHz to 3 GHz, which is plotted in Figs. 4 and 5. The measured S-parameters have included heuristic system and probe error compensation. The C_f, L_0,and L_1 are almost constant

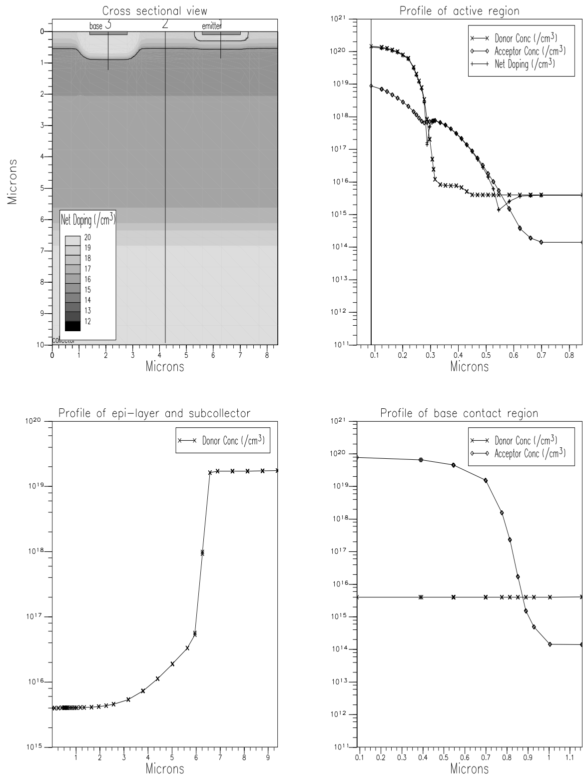

Figure 2: Cross section and doping profiles used for modeling the intrinsic device.

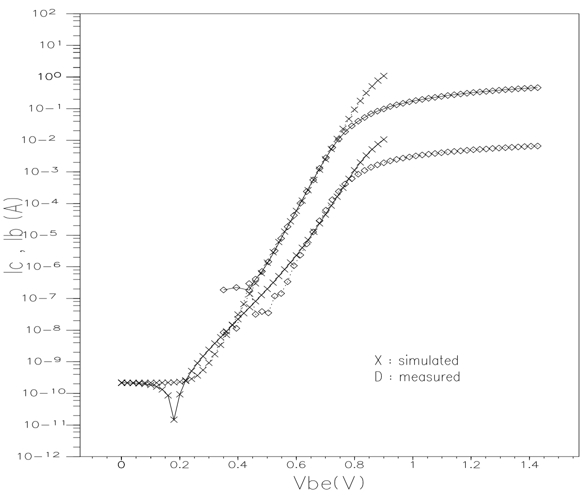

Figure 3: The cross symbols are the Gummel plot at V_{ce}=5V for the intrinsic device. Simulation data and direct measurements on the intrinsic device (a single finger without packaging) have been matched completely for $V_{be} > 0.5V$. The diamond symbols are measured data from the entire circuit with multiple fingers and packaging. The currents of the intrinsic device is multiplied by the number of fingers for easy comparison.

throughout the frequency range. However, the resistance noise and the fact that L_2 is negative can be explained in two ways. First, those extracted values can be comparable to the noise included in measurements. Second, presently the intrinsic device is calibrated *only* against the Gummel plot and f_T. The device behavior in the collector contact region (in this case, an epi-layer) is not accurately accounted for during the calibration, as is manifested in the fact that both the Gummel plot and f_T will have negligible change for large variations of V_{ce}. More detailed calibration with the test structure including only the base-collector junction can remove this error. Also, modeling parameters will affect some of the parasitic values. Mobility has a significant influence on subcollector resistance. If higher mobilities are used, R_2 will become larger due to the reduced resistance of the intrinsic device. The extracted values of R_0, R_2, C_f, L_0,and L_2 are very sensitive to the V_{be} hence an accurate estimation of the bias conditions for the intrinsic device are necessary. On the other hand, for small variations of V_{ce}, only slight variations of C_f are observed. Presently the final resistance values are determined as below. R_1 is first selected by comparing the resistive component of S_{11}, since R_1 dominates the resistive part of S_{11}. By satisfying the bias conditions and the current constraints, R_0 can be determined. R_2 is selected in the same manner as for selecting R_1. These selected resistance values are actually in the range of extracted data from (2), (3), and (4).

Using the average values of extracted data for L_0, L_1, and C_f over the frequency range, and using resistance values from the above procedure, the full circuit is simulated and compared with experimental data in Fig. 6. It can be seen that the high-frequency circuit behavior is well captured by the mixed-mode simulation with frequency-independent parasitic elements. As mentioned before, the extraction procedure can be further improved by minor mobility adjustments (distinguishing majority and minority mobilities) and inverted-mode measurements of the intrinsic device.

After the parasitic characterization procedure, a mixed-mode representation of the RF circuit is obtained. High-frequency performance optimization can be obtained from separate adjustments of the mask layout and the doping profiles. Also, other virtual instrument techniques such as the harmonic balance analyzer [7] can be applied for detailed analyses of the analog circuit behavior.

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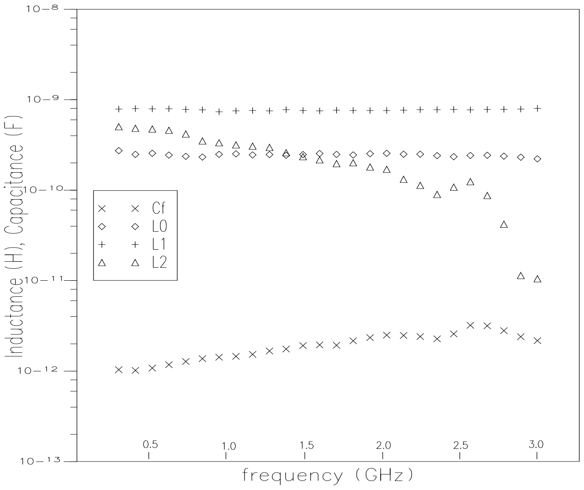

Figure 4: The extracted inductances and capacitance using (1) to (4) (absolute values of L2 are used).

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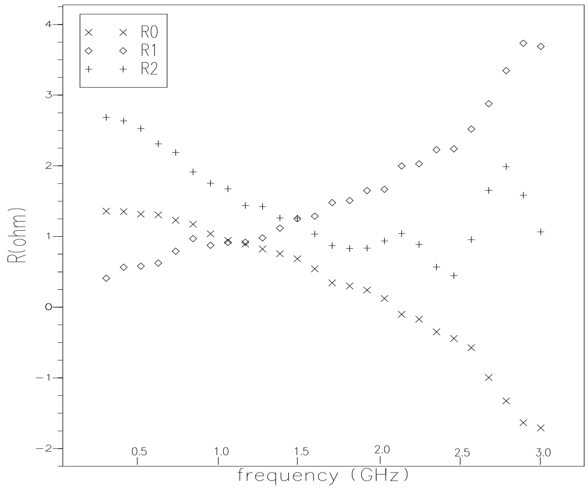

Figure 5: Extracted parasitic resistances using (2) to (4).

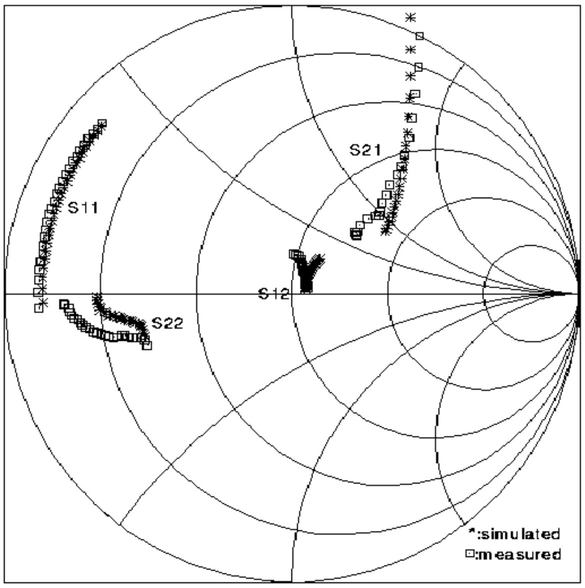

Figure 6: Simulated and measured S-parameters at V_{be}=0.82 V and V_{ce}=5V.

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