On-Chip Inductance Modeling of VLSI Interconnects

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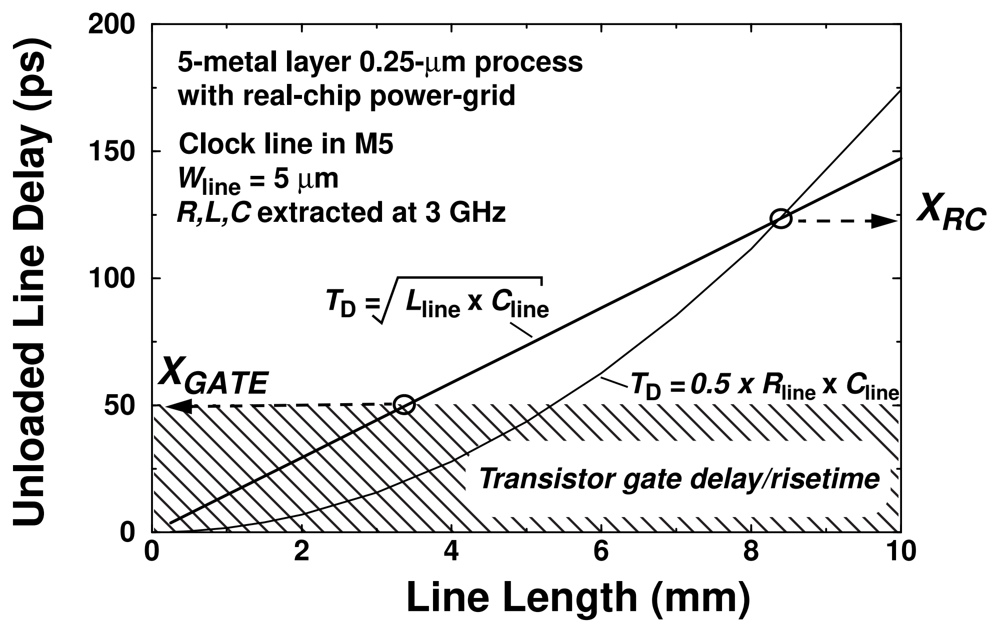
Outline

- Background and motivation
- 3D geometry modeling and inductance extraction using EM field solvers
- Analytical formulae for inductance calculation
- Measurements and simulation results
- Summary

Background and Motivation

- At gigahertz frequencies, long interconnects exhibit transmission line behavior.
- For major signal and P/G lines, the inductance impedance is comparable to resistive component.
- Due to the inductance, delay increases, over-shoot occurs, and inductive cross-talk can no longer be ignored.

Background and Motivation



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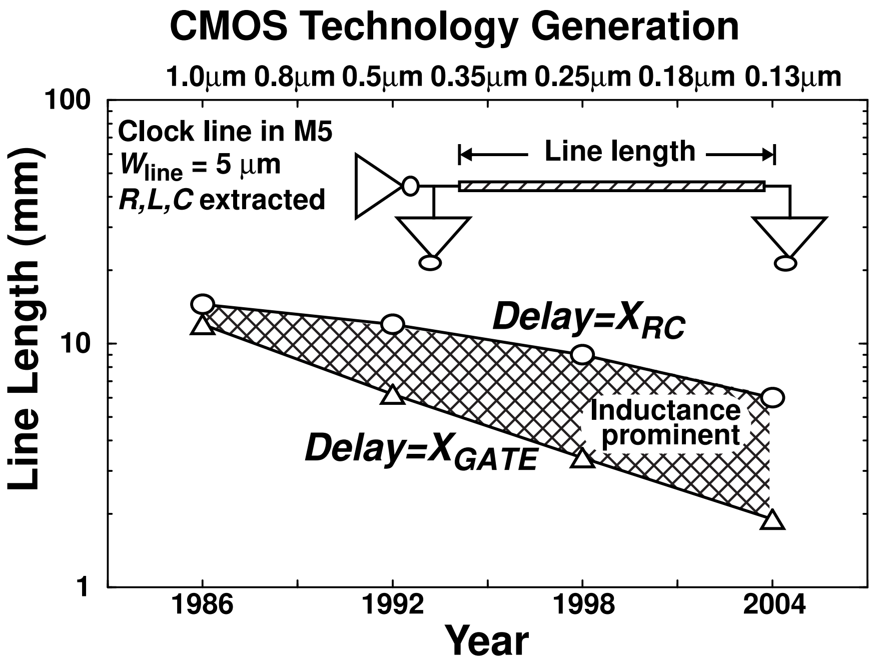

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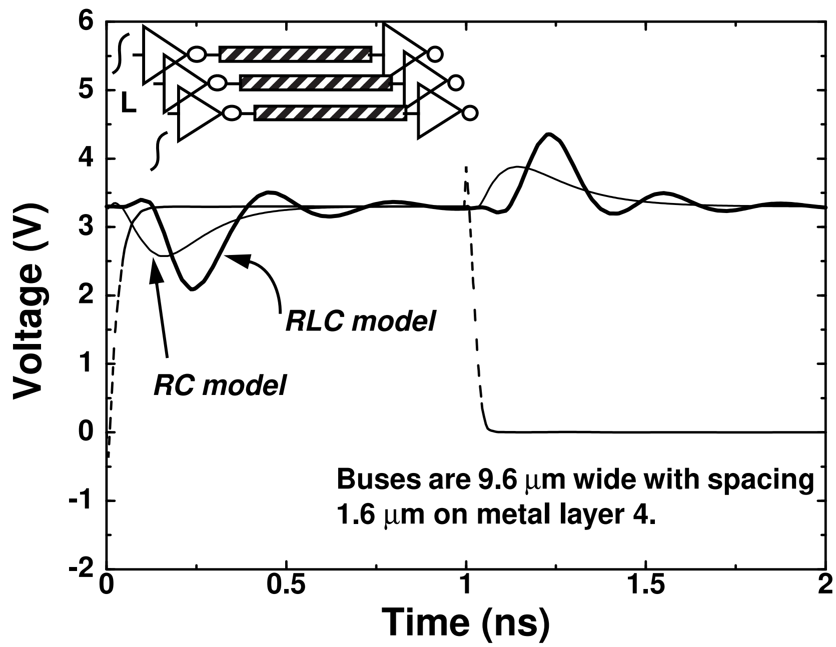
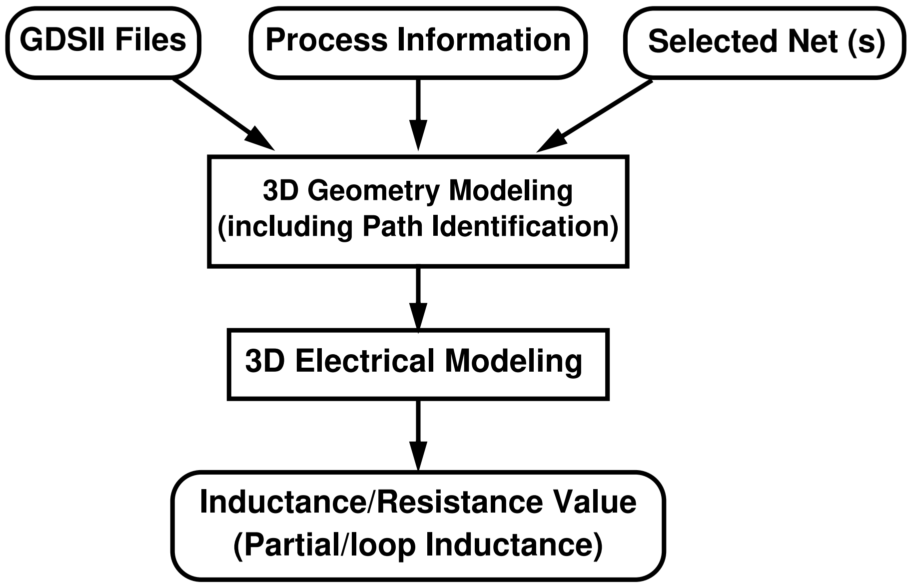
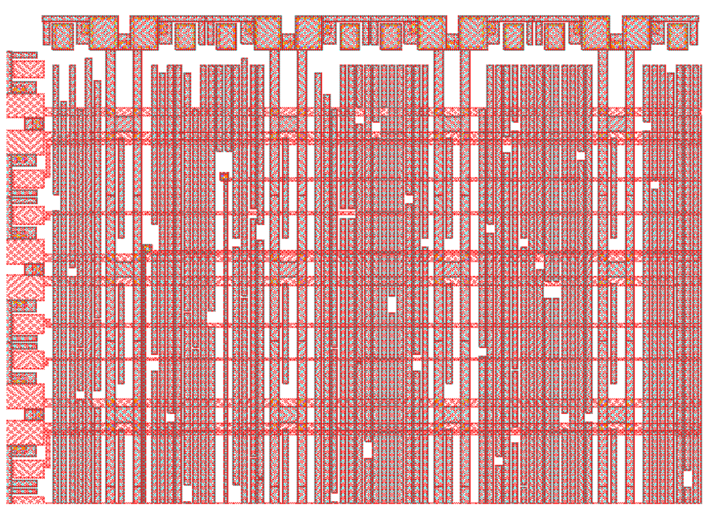


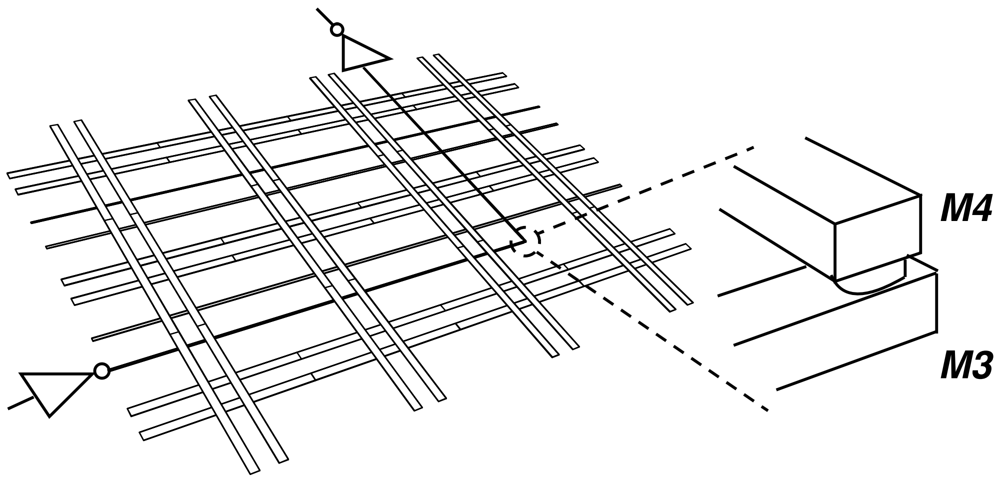
System Flow Chart



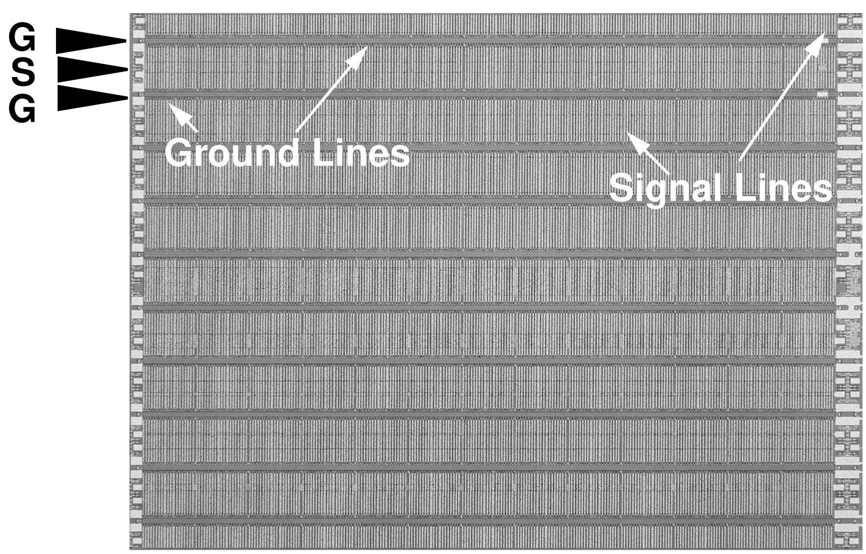
A Corner of A Test Chip with Signal and Power/Ground Lines



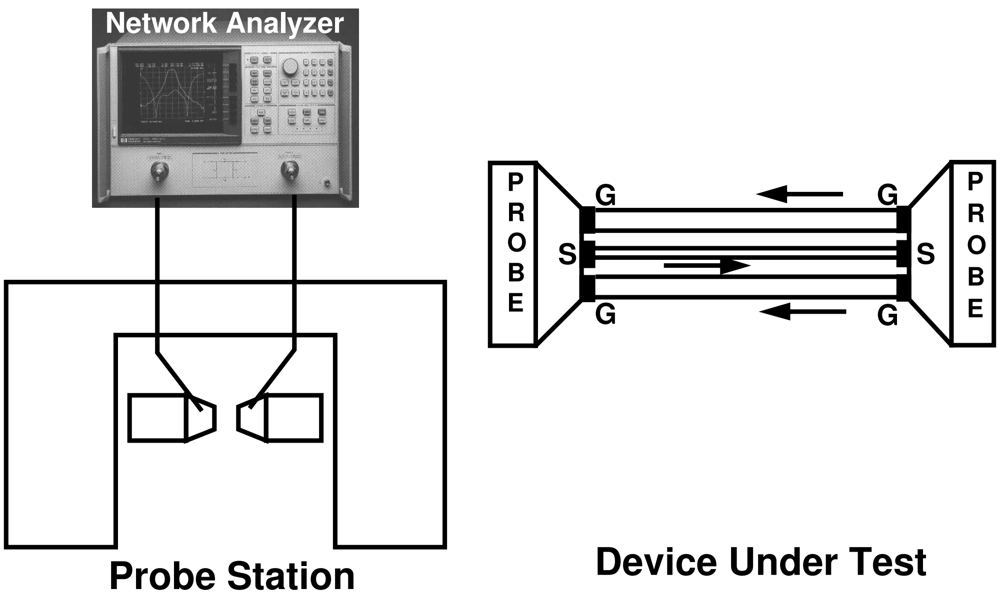
Extracted 3D Geometry with Signal and Power/Ground Lines



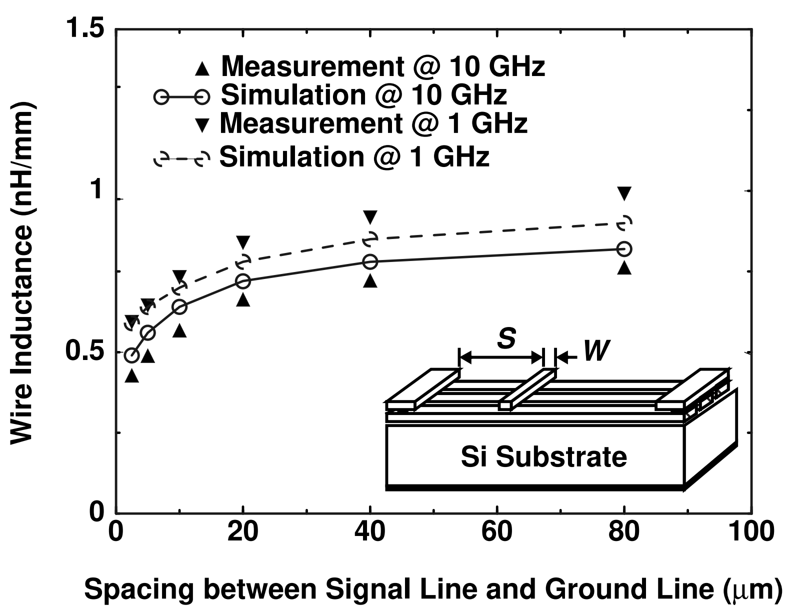
Die Photo of A Test Chip



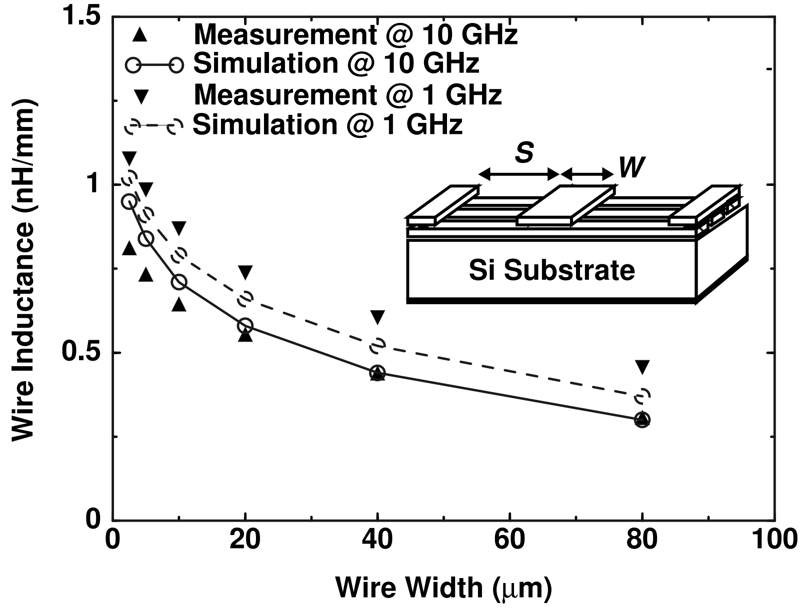
Measurement Setup



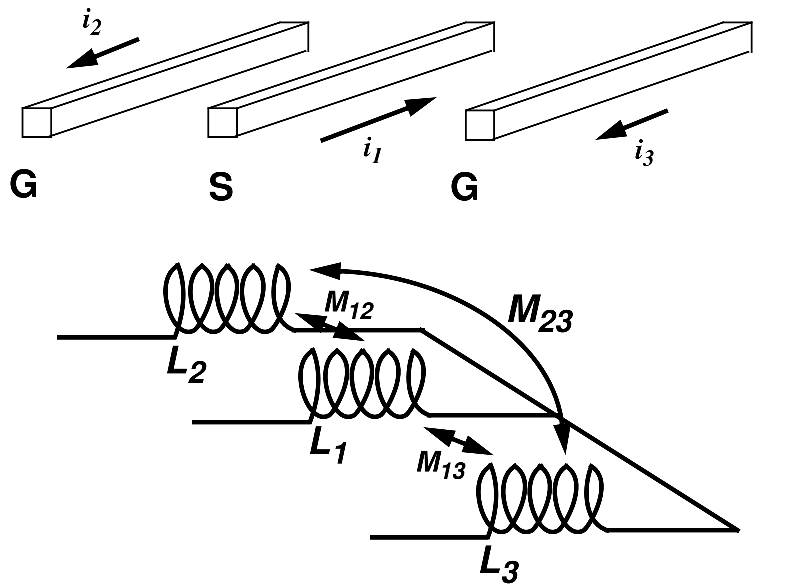
Measurement and Simulation Comparison



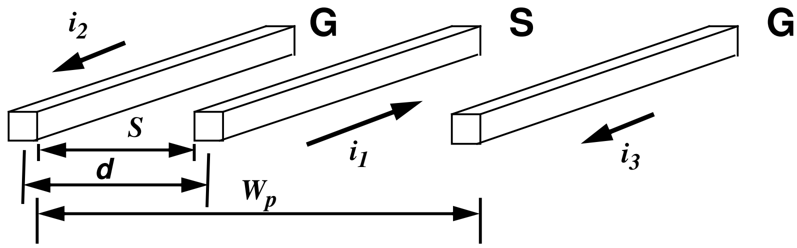
Measurement and Simulation Comparison



Inductance Equivalent Circuit



Analytical Formula



$$\hat{L} = \frac{\mu_0}{2\pi}\left[\ln\frac{d}{r_{sig}} + \frac{1}{2}\ln\frac{d}{r_{gnd}} + \frac{1}{2}\ln\left(1-\frac{1}{\alpha}\right) + \frac{1}{2}\frac{\ln\frac{w_p}{(\alpha-1)r_{gnd}}}{\ln\frac{w_p}{r_{gnd}}}\ln(\alpha-1)\right]$$

α: W_p/d

r_{sig}, r_{gnd}: equivalent radii of signal and ground lines

Simplified Formulae

$$\hat{L} = 3\ln\left(\frac{s+w}{w+t}\pi\right) - \ln 2 + l \qquad 2 \le \alpha < 4$$

$$\hat{L} = 3\ln\left(\frac{s+w}{w+t}\pi\right) + 1 + l \qquad \alpha \ge 4$$

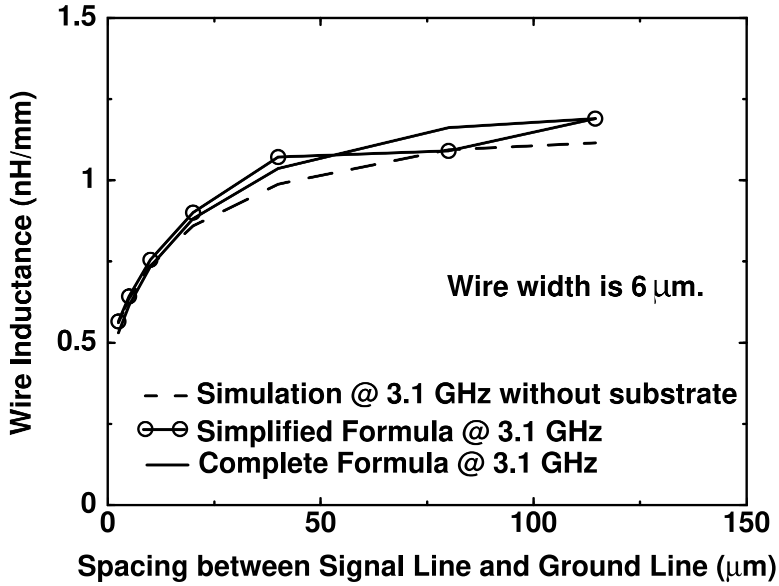
$$l = 0.75\tanh\left(\frac{2\delta\pi}{w+t}\right) \quad \delta = \frac{1}{\sqrt{\pi\sigma f\mu}}$$

w: width of the signal wire

t: thickness of the signal wire

Inductance units: 10^{-1} nH/mm

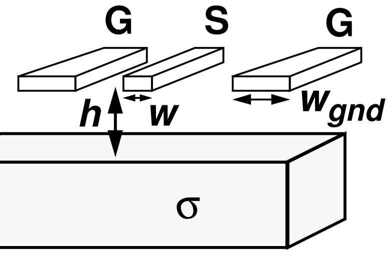
Formulae and Simulation Comparison



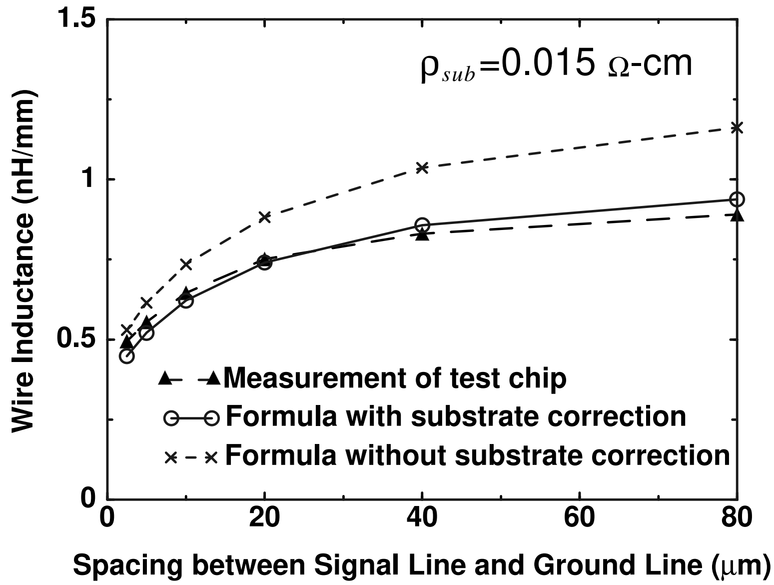
Formula with Substrate Correction

$$\hat{L}_{total} = \hat{L}_{previous} - k\frac{\mu_0}{2\pi}\ln\left[\frac{\sqrt{\left[s + \frac{(w_{gnd} + w)}{2}\right]^2 + h^2}}{h + \frac{1}{2\sqrt{\pi f \sigma \mu_0}}}\right]$$

K: the current distribution factor



Wire Inductance with Substrate Effect



Summary

- Results show the growing impact of on-chip inductance.
- Physical modeling includes accurate 3D geometry.
- Analytical formulae, benchmarked with simulations, demonstrate accuracy suitable for design and CAD tools.

Acknowledgment

- **Dr. Norman Chang at HP Labs, Palo Alto, Dr. Mohiuddin Mazumder at Intel.**
- **The project is supported by *Focus Center Research Program for Interconnects for Gigascale Integration.***