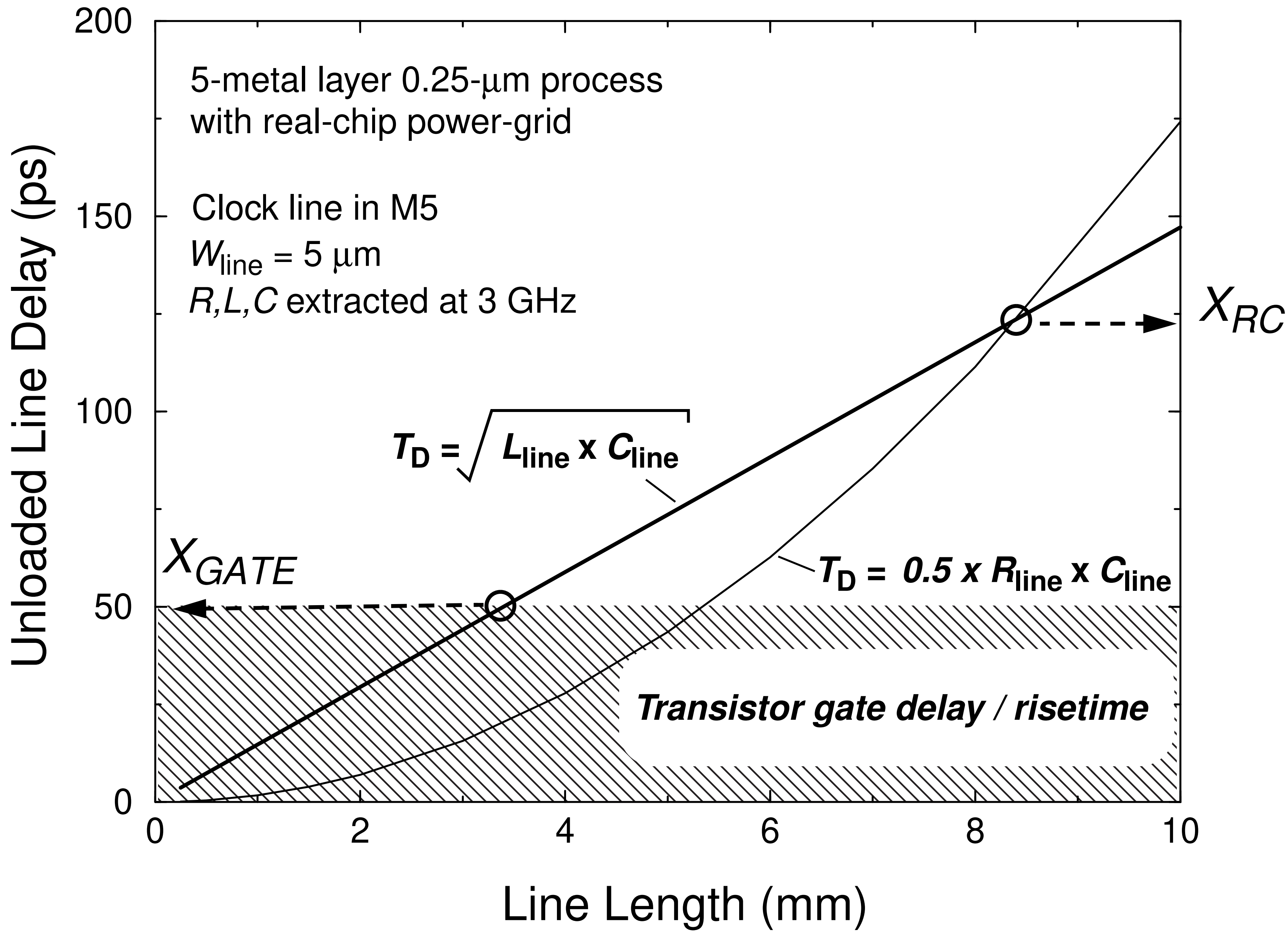

Fig. 10.4.1(a) Line delay for different delay models.

Xiaoning Qi, Bendik Kleveland, Zhiping Yu, Simon S. Wong, Robert W. Dutton and Tak Young

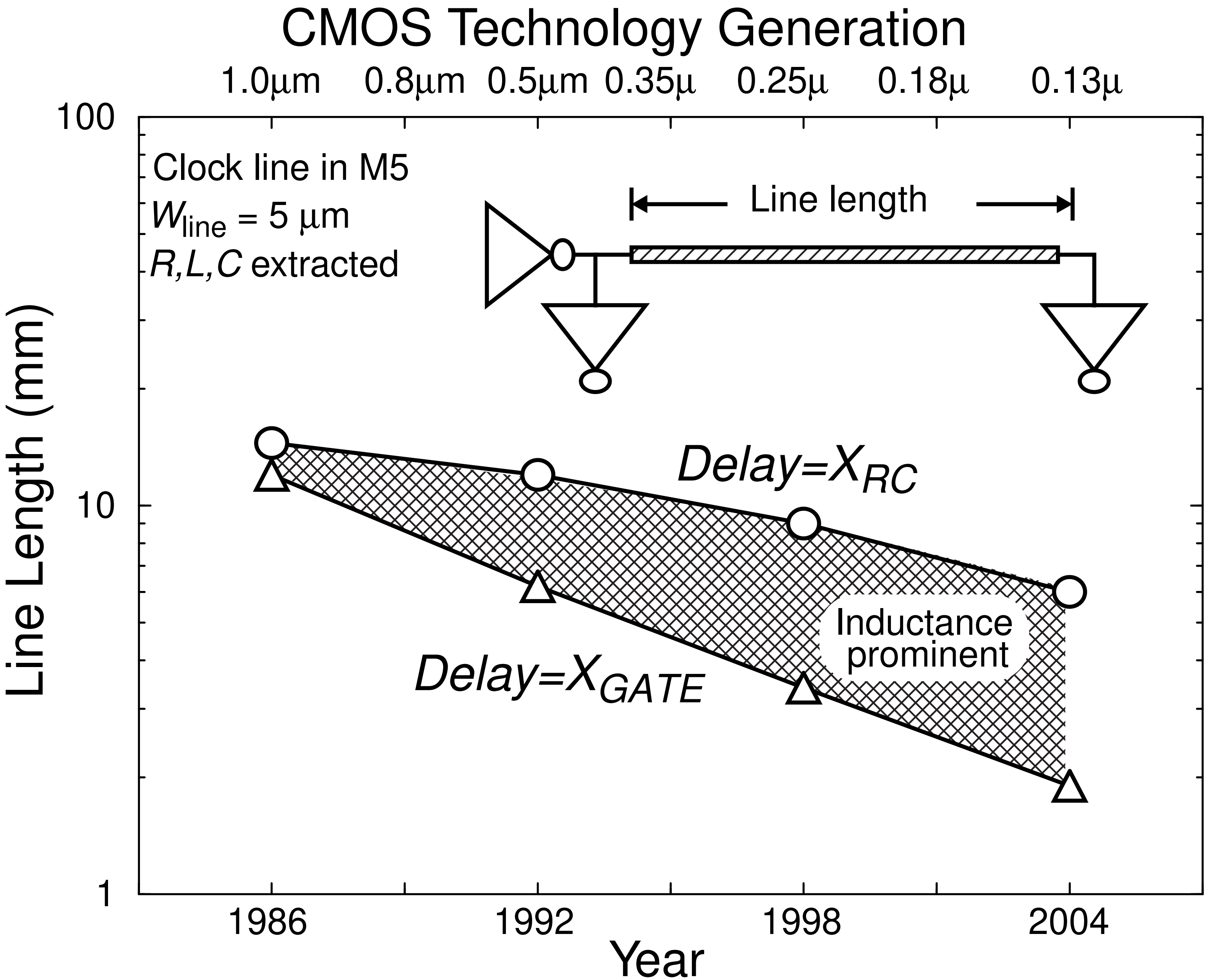

Fig. 10.4.1(b) Inductive effects vs. technology scaling.
Xiaoning Qi, Bendik Kleveland, Zhiping Yu, Simon S. Wong, Robert W. Dutton and Tak Young

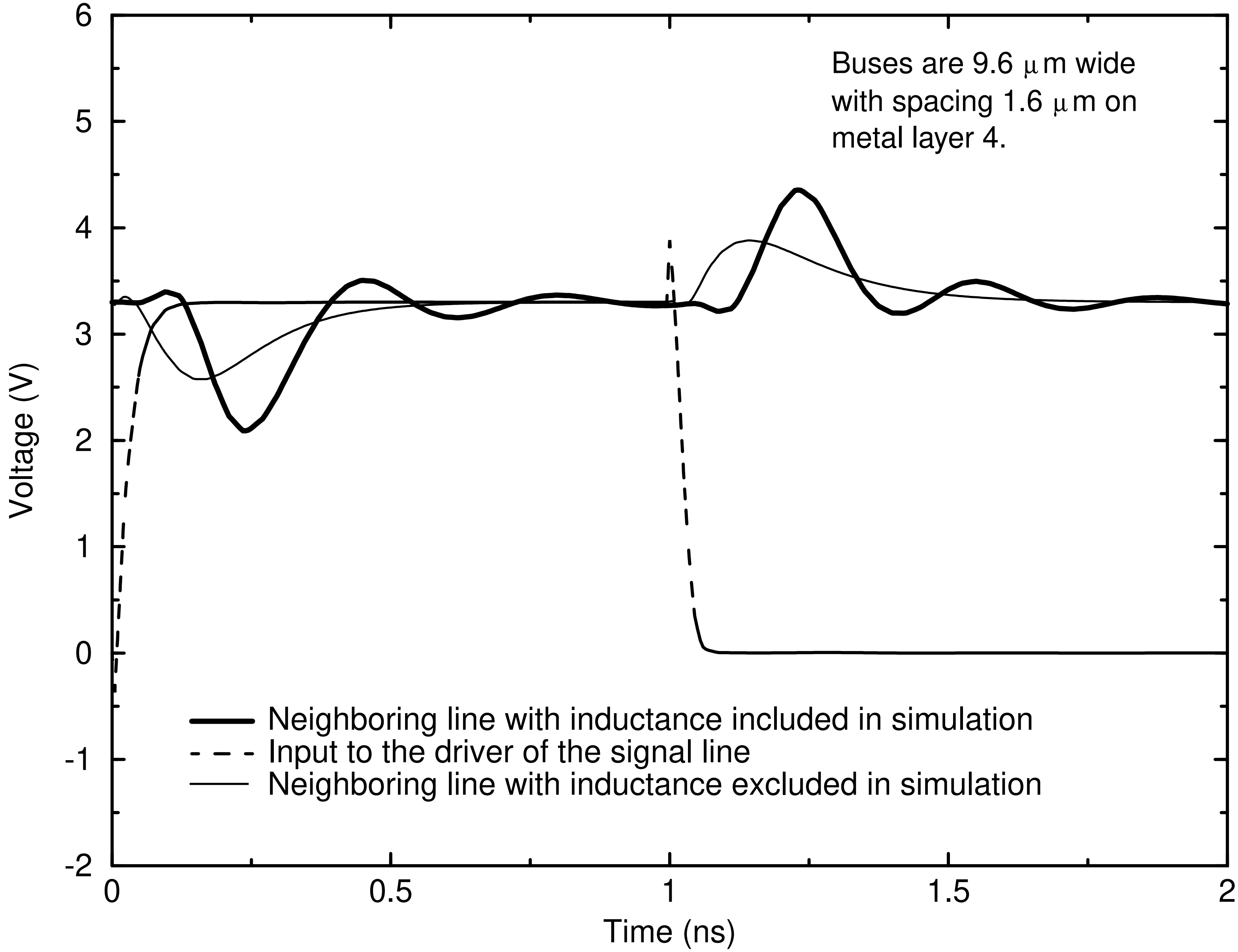

Fig. 10.4.2 Inductance effects on cross talk.
Xiaoning Qi, Bendik Kleveland, Zhiping Yu, Simon S. Wong, Robert W. Dutton and Tak Young

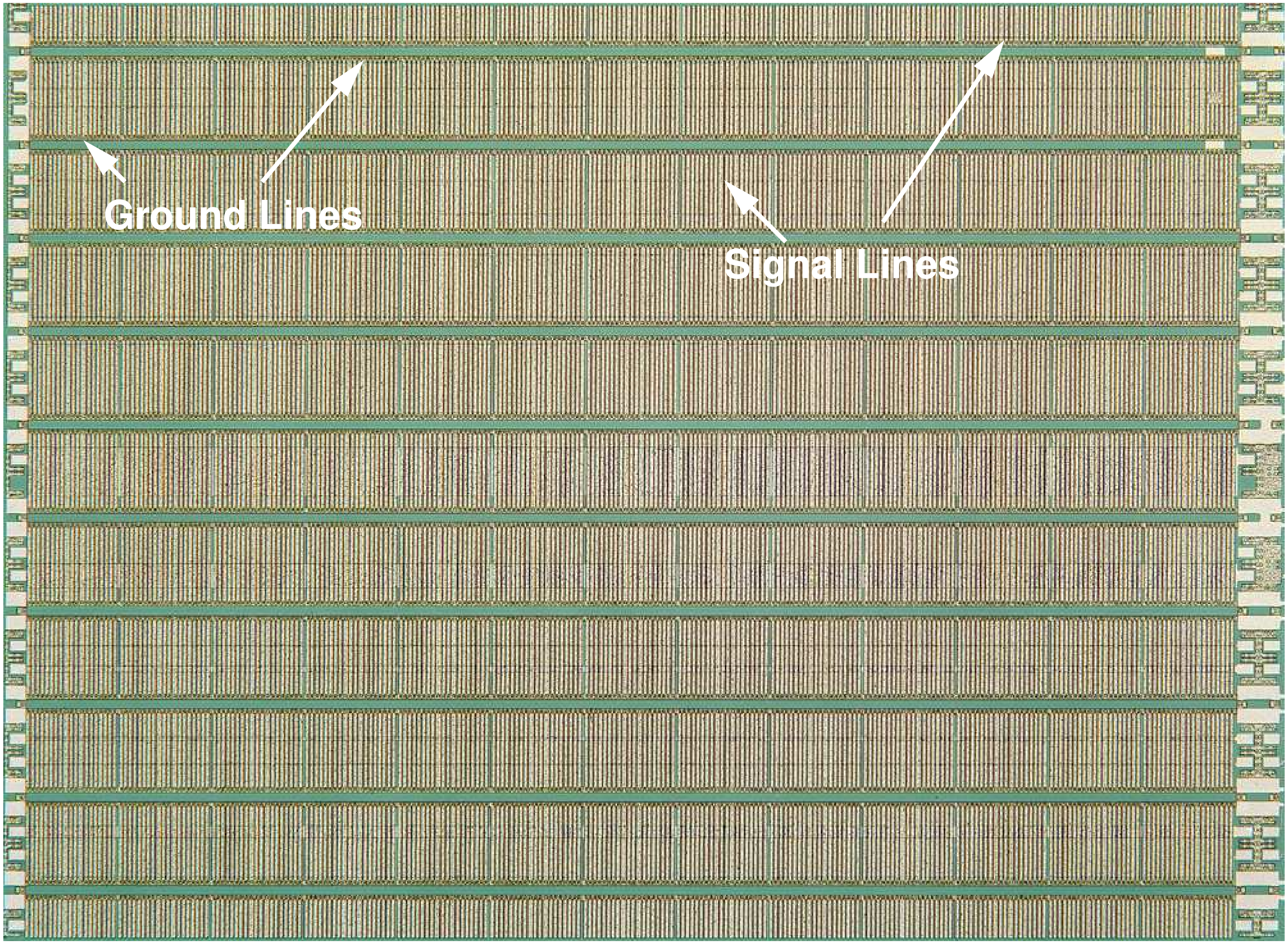

Fig. 10.4.3 Photo of the test chip.
Xiaoning Qi, Bendik Kleveland, Zhiping Yu, Simon S. Wong, Robert W. Dutton and Tak Young

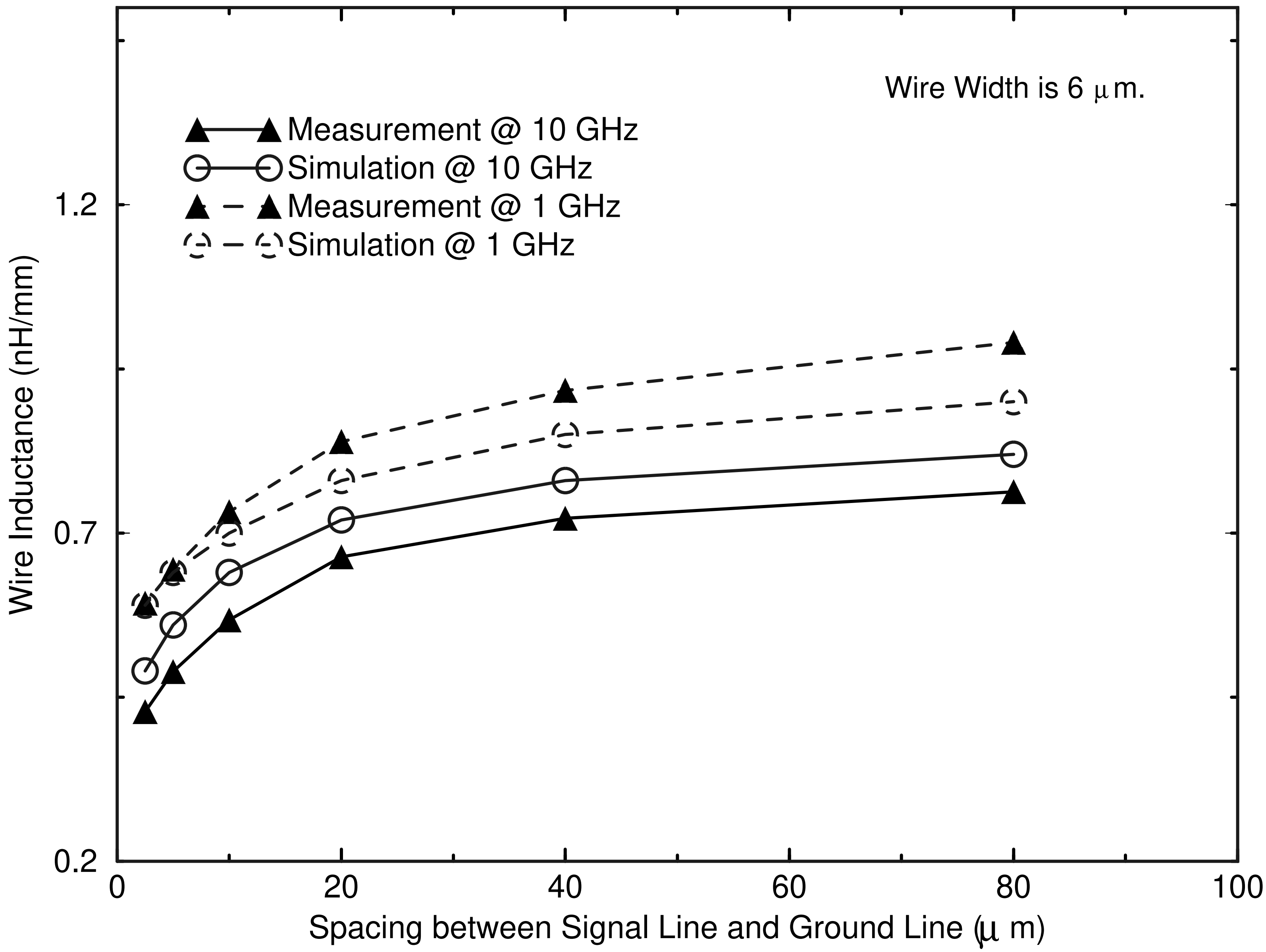

Fig 10.4.4. Measurement and simulations comparison.
Xiaoning Qi, Bendik Kleveland, Zhiping Yu, Simon S. Wong, Robert W. Dutton and Tak Young

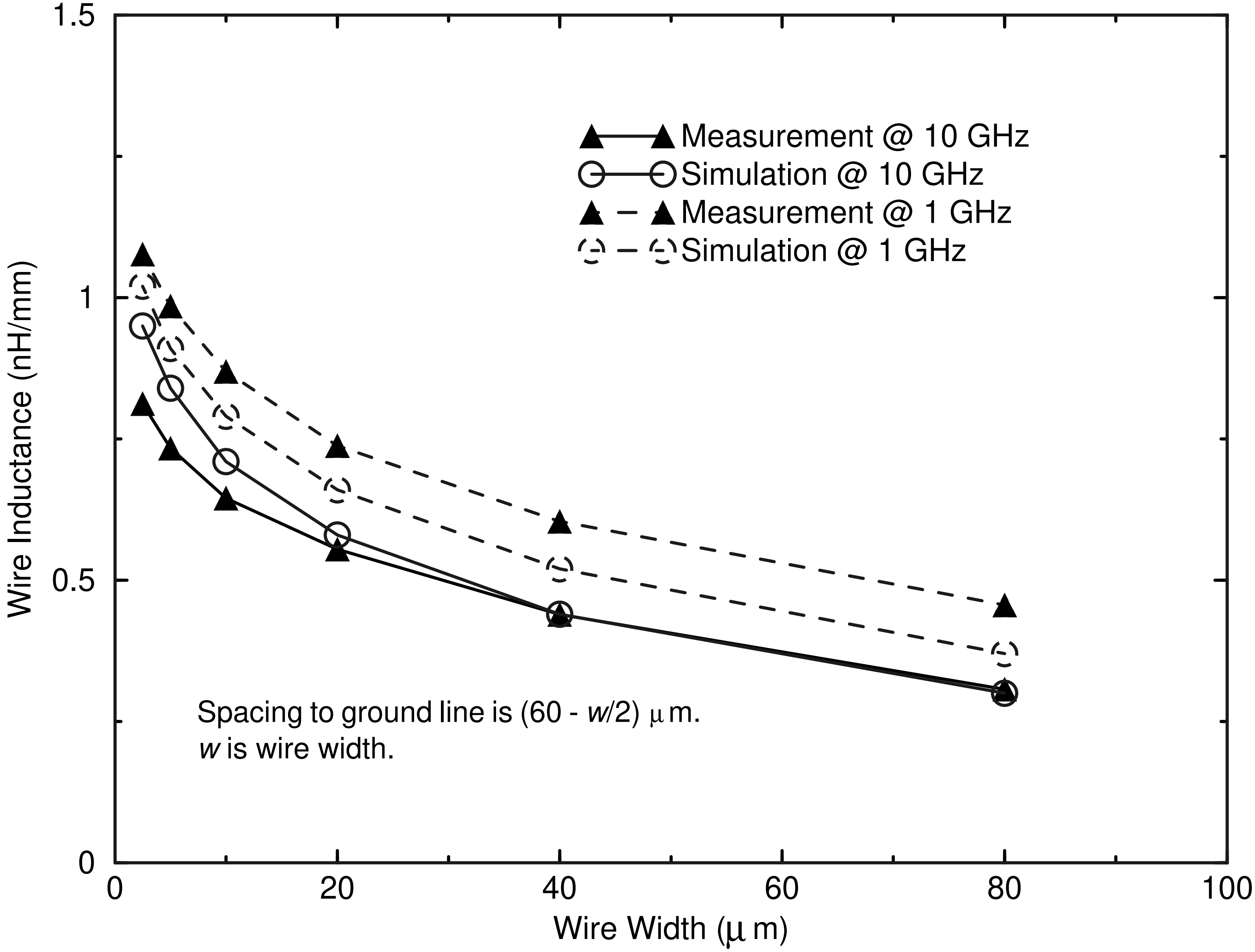

Fig. 10.4.5 Measurement and simulations comparison.
Xiaoning Qi, Bendik Kleveland, Zhiping Yu, Simon S. Wong, Robert W. Dutton and Tak Young

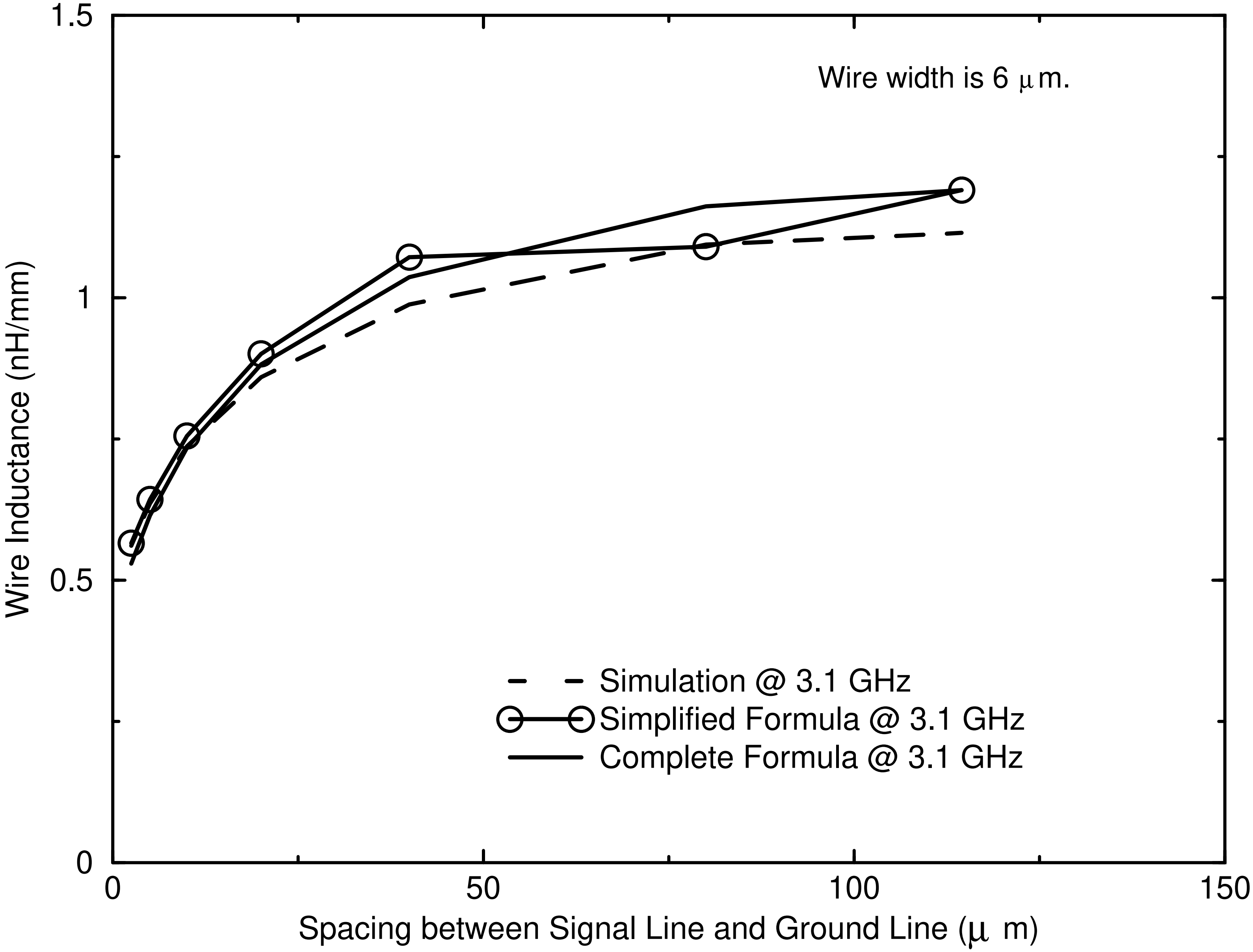

Fig. 10.4.6 Wire inductance formulae.
Xiaoning Qi, Bendik Kleveland, Zhiping Yu, Simon S. Wong, Robert W. Dutton and Tak Young

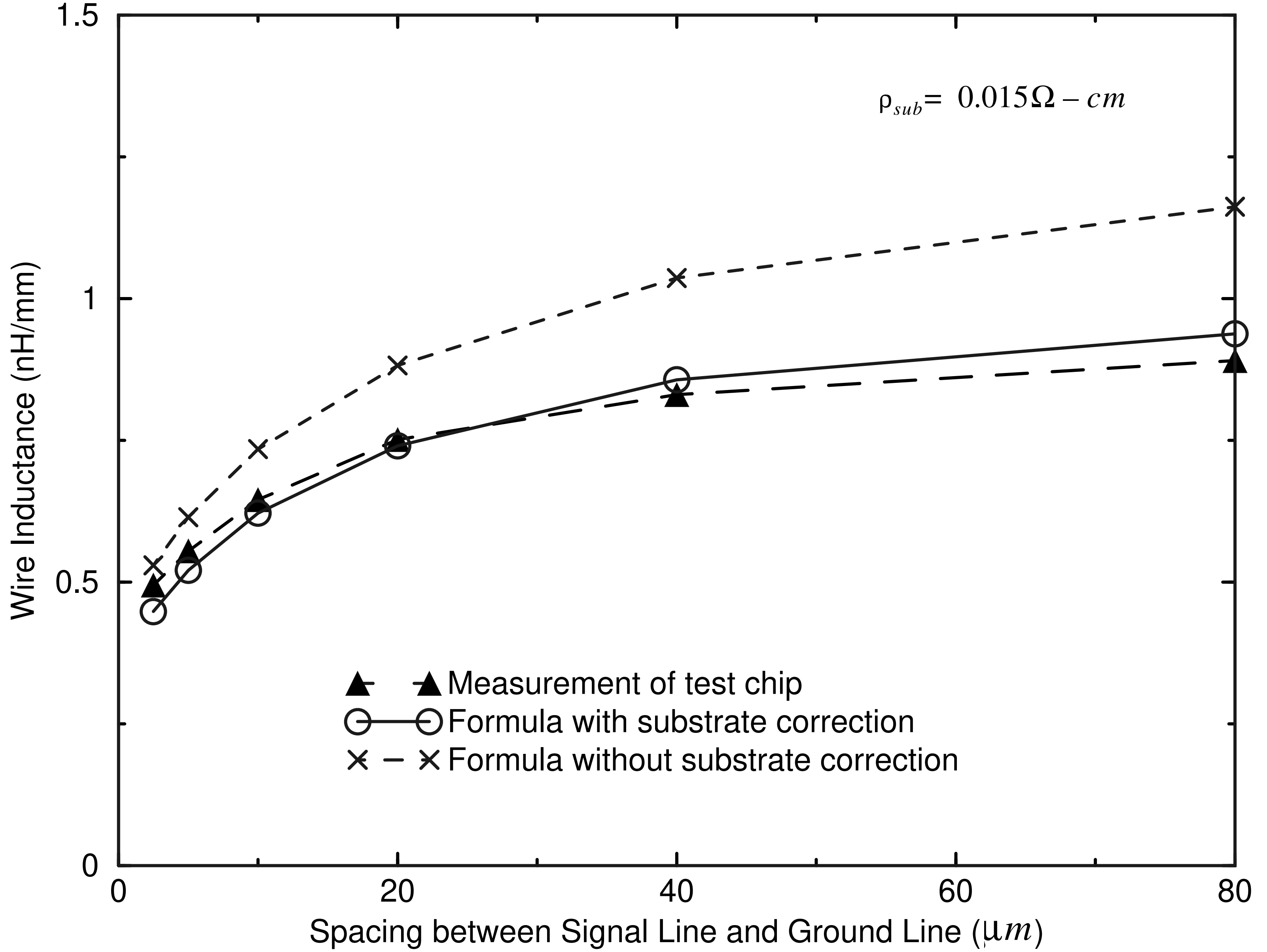

Fig. 10.4.7 Wire inductance with substrate effect.
Xiaoning Qi, Bendik Kleveland, Zhiping Yu, Simon S. Wong, Robert W. Dutton and Tak Young