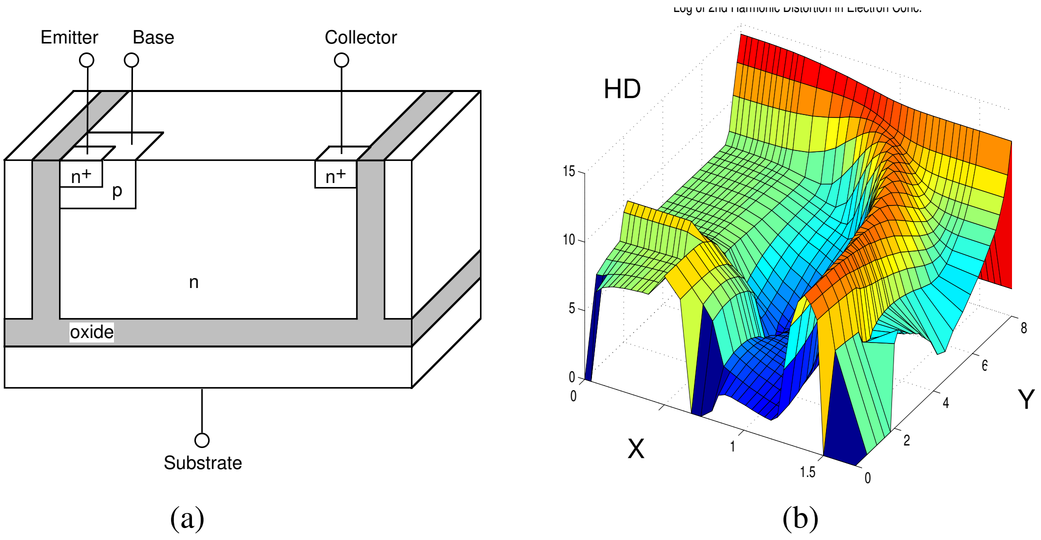


Figure 5: (a) 3D schematic of SOI bipolar transistor structure [6], (b) Logarithmic plot of HD2 for electron concentration inside the device.

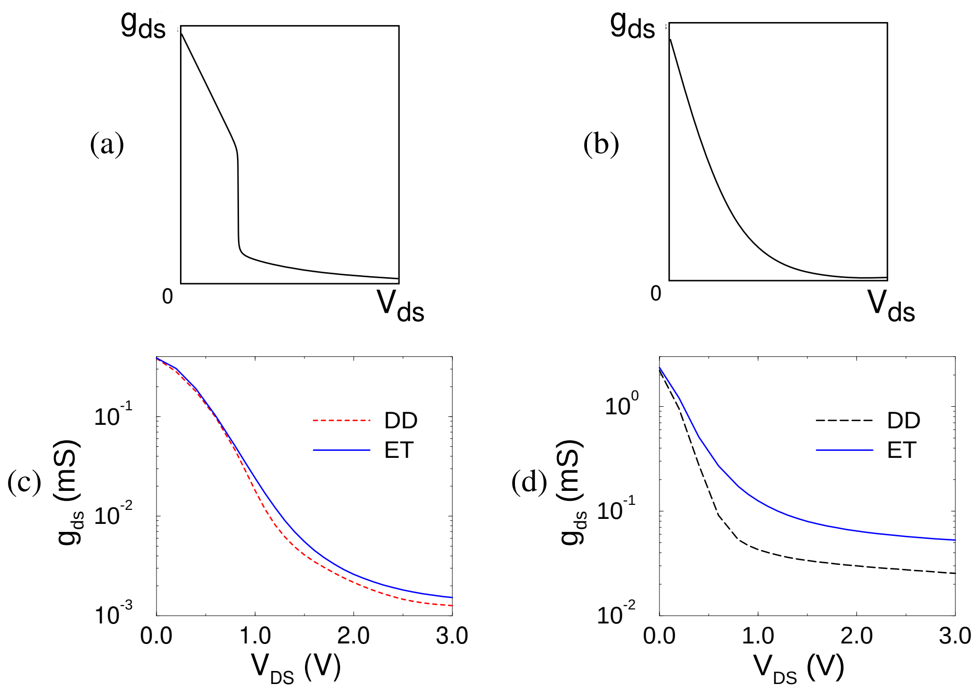
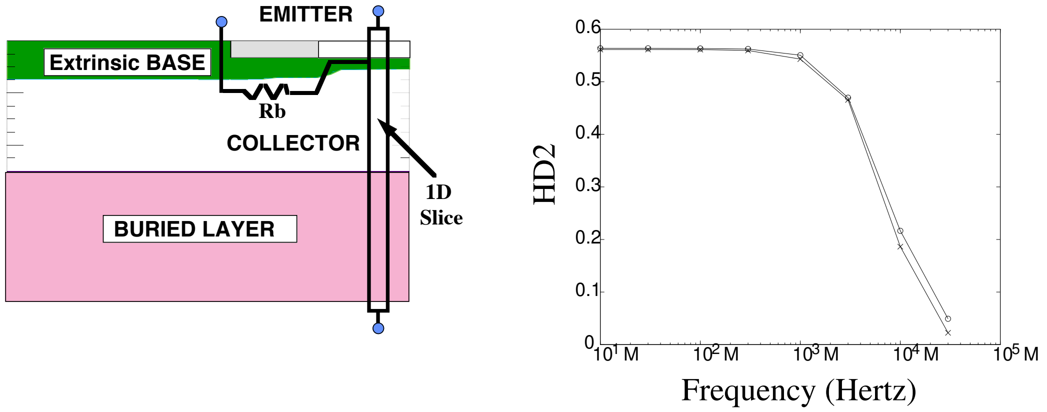
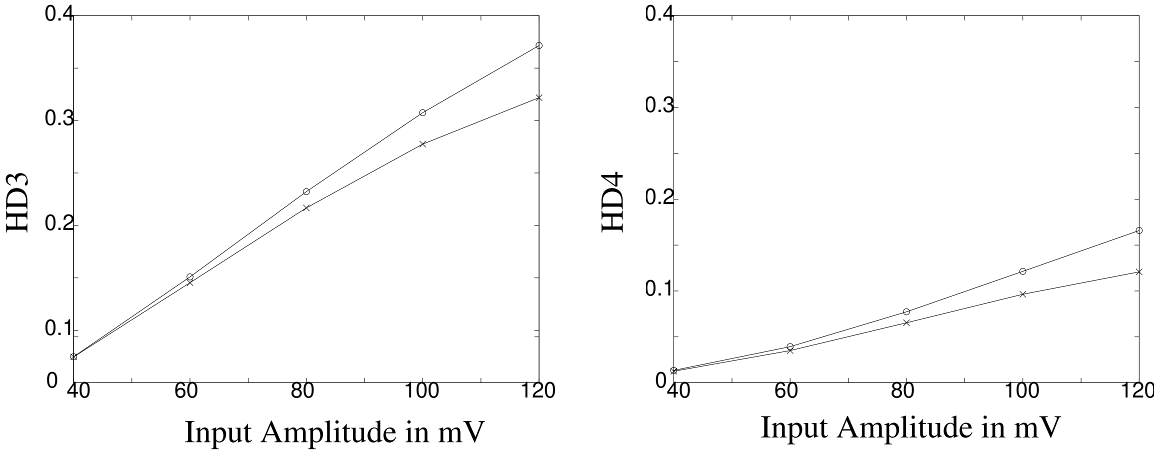


Figure 6: Output conductance of an n-MOSFET: (a) present SPICE-2 model, (b) qualitative correct curve from [7], (c) PISCES simulation for a 0.8 μm channel-length MOSFET, and (d) for a 0.2 μm MOSFET.



(a) (b)

Figure 3: Computed harmonic distortion (HD) of a RF bipolar device: (a) device cross-section, (b) HD2 versus log frequency (both 2D (o) and 1D (x) results).



(a) (b)

Figure 4: Comparison of various distortion components versus signal level at 1 GHz using both 2D (o) and 1D (x) models: (a) HD3 versus signal level and (b) HD4.

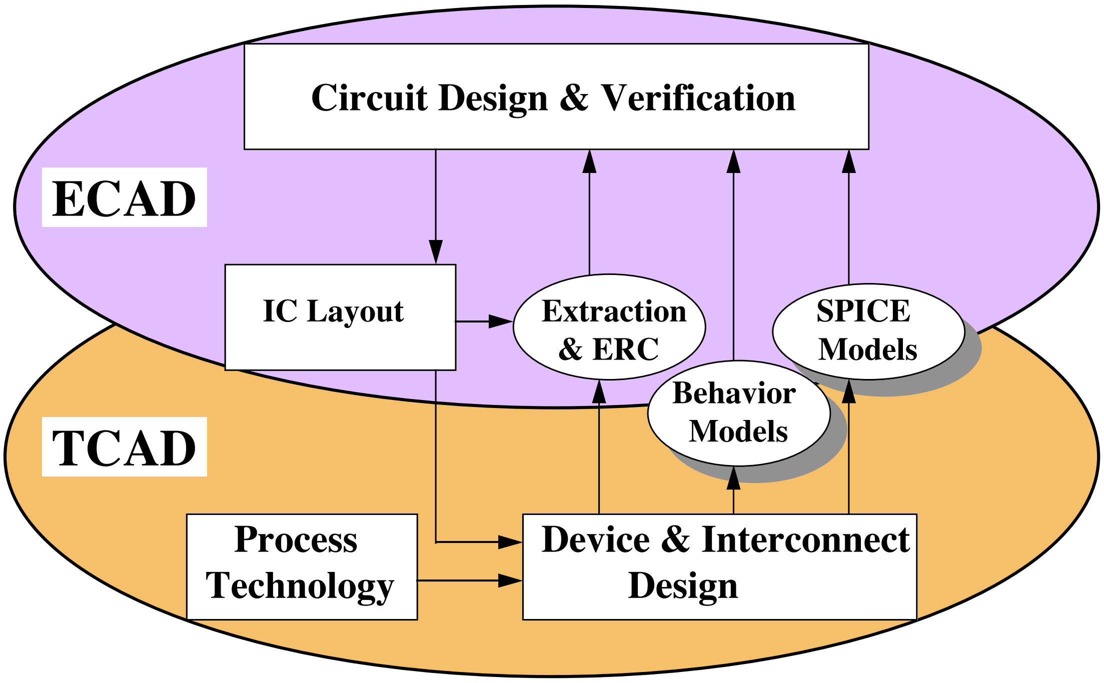


Figure 1: Coupling of electronic design (ECAD) with technology design (TCAD); emphasizing modeling issues that can be uniquely supported by TCAD.

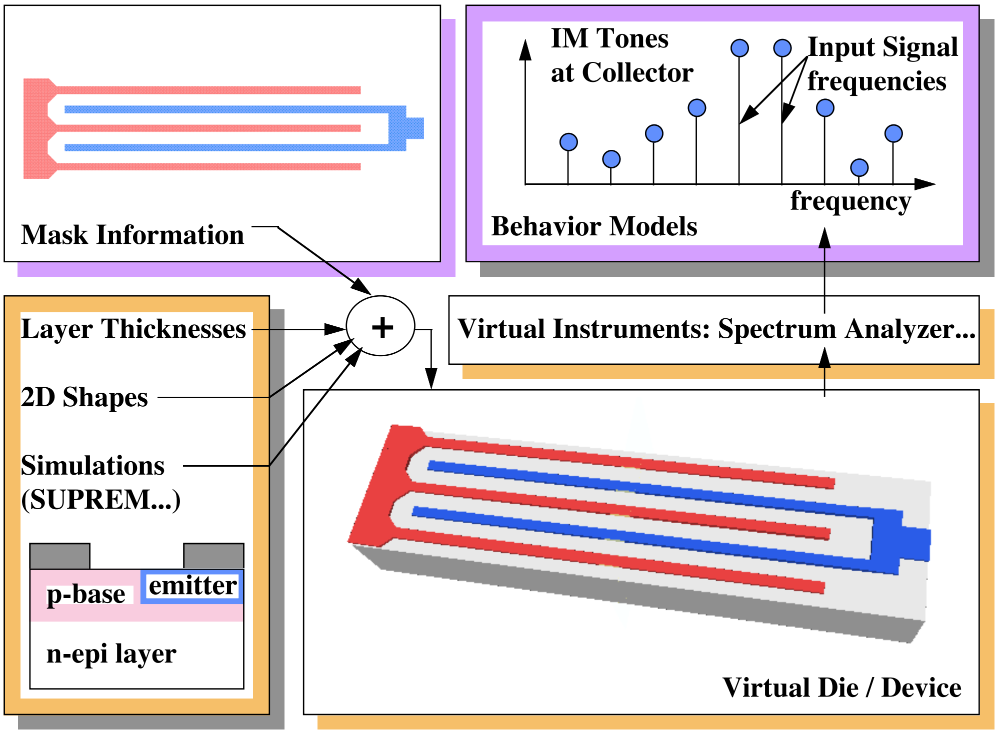


Figure 2: Information flow in the design of a RF power device; intermodulation (IM) distortion extracted using a virtual spectrum analyzer.

conditions accordingly.

IV. Applications--Unique capabilities of TCAD-based virtual instrumentation are illustrated in Figure 5 where a high voltage SOI bipolar device is shown along with results of harmonic balance analysis. The SOI device is being considered for application in telephone line circuits where high voltage requirements are combined with needs for low distortion [6]. Here the TCAD analysis shows in detail (via contour plots in Figure 5b) where harmonic distortion occurs inside the device, primarily along the depletion layer boundary as it reaches the SOI interface. For backgate bias beyond 10V, there is a noticeable drop in distortion as an accumulation layer forms at the back interface. There are other technological choices to improve device performance, for example, an additional implanted layer that can be explored and optimized using the technique.

Another example of predictive model generation from the TCAD-based approach is shown in Figure 6. Limitations of typical SPICE models for predicting output conductance in a MOS device are shown along with both qualitatively correct [7] and still more accurate TCAD results. It is clear that the traditional compact model discontinuities are a major problem for analog design. It can also be observed from the TCAD-based results that in addition to generating smooth curves, the physics of technological changes can be directly captured by TCAD. The impact of hot carrier transport on output conductance are clearly more apparent for MOS devices with shorter effective channel length. Similar effects can also be directly predicted for capacitance effects [8] which have significant performance implications for circuit speed and bandwidth.

V. Summary--This paper presents a new look at transistor modeling issues for analog design in the context of emerging technologies--both pure analog and as specializations of mainstream VLSI. Aggressive application of TCAD can fill the gap in improving analog device models and in providing help in targeting new technologies to meet the needs of both analog and digital designers.

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TCAD for Analog Circuit Applications: Virtual Devices and Instruments

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I. Introduction--The need for and application of analog circuits is growing. Wireless communications, including both RF and optical, have taken center stage as key system technologies. Analog-digital conversion is the workhorse for system interfaces and the growing field of micro-electro-mechanical systems (MEMS) has brought forth a seemingly endless set of new applications.

Along with the growing needs for analog circuits are the challenges of designing with technologies that are primarily targeted for digital systems--for example, emphasis on minimum propagation and interconnection delays. In order to both understand the analog limits of VLSI technologies and to specify new technologies for mixed-signal applications, there is a critical need for design tools and models. Capabilities for analog modeling of advanced transistors are demonstrated based on new tools and techniques developed to specifically support technology development. In addition to providing support for more accurate analog modeling, there is the opportunity to predict technology dependencies and therefore to selectively target technology optimization for analog performance.

II. Technology CAD--The term “technology files” is well-known among circuit designers and specifically means the relevant circuit modeling information that contains technology dependencies. Technology computer-aided design (TCAD) provides powerful analog capabilities to directly predict not only the technology files but also a wide range of other critical behavior information about devices and circuits that depend directly on technology. Figure 1 shows the intersection of conventional electronic circuit design (ECAD) with TCAD as well as information and capabilities that it provides in direct support of IC design needs. Predictive SPICE model extraction includes both intrinsic devices and parasitic analysis for problems such as latchup, ESD [1], and substrate noise [2]. Recent developments of “virtual instruments” provide new characterization techniques [3] for devices imbedded in parasitic networks of both active and passive devices. Predictive support of technology files and innovative applications of virtual instruments for mixed-signal analysis are now presented.

III. Virtual Wafers and Instruments--Accurate specification of devices and circuit modules to be analyzed is critical. Figure 2 shows the information flow and intermediate results for the computational prototyping of an RF bipolar power transistor [4]. Starting with IC mask information and process specifications--including layer thicknesses, edge contours and simulated process details such as 1D or 2D SUPREM profiles--solid modeling techniques are used to create a fully 3D virtual die or device. The same techniques have been applied to cells and arrays for SRAM applications [5]. The 3D model, including multilayers of interconnection can also support direct extraction of parasitics such as capacitance and inductance. The results shown here use the virtual spectrum analyzer to extract intermodulation (IM) and harmonic distortion (HD) directly from a 2D device cross-section using the harmonic balance approach.

Virtual instruments provide the means to extract IC behavior using TCAD tools and techniques. Figure 3 shows in greater detail the analysis of harmonic distortion (HD) for a giga-Hertz bipolar transistor using the virtual spectrum analyzer. Figure 3a shows the technology cross-section for the device (full 2D and 1D simplification) and Figure 3b shows the spectral content of the HD term for a single tone sinusoidal input at different signal frequencies from 10 MHz to 30 GHz. For the signal level shown (V_{be} = 0.7 V + 80 mV sin $\omega_c t$), there is substantial harmonic content up to 6-8 terms and the time domain representation of the data shows waveform clipping due to the 80 mV input signal swing. The virtual spectrum analyzer also allows direct evaluation of the physical effects involved and their interpretation as shown in the next section.

In addition to directly predicting distortion characteristics, the virtual spectrum analyzer facilitates development of improved compact models and critical comparison of technology trade-offs. Figure 4 shows a comparison between the complete 2D technology slice and 1D simplification. For sinusoidal inputs up to 120 mV the HD3 and HD4 terms are shown for an input signal frequency of 1 GHz. The agreement is rather good but tends to diverge at higher bias and with increased frequency (see Fig. 3b). The 1D model has several key advantages: 1) more than 15x reduced CPU time, 2) one-for-one correspondence to SPICE compact models, and 3) leverage for comparative technology studies (i.e., SiGe HBT vs. pure silicon BJT). It is also possible to optimize technologies and circuit operating