On-Chip Inductance Modeling of VLSI Interconnects (TA10.4, ISSCC 2000)

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Introduction

At gigahertz frequencies, long interconnect wires exhibit transmission line behavior. Using copper and wider wires for major signal and power/ground lines, inductive impedance ($j\omega L$) could become comparable to the resistive component of the wire (R). Due to the inductance, delay increases, over-shoot occurs, and inductive cross-talk can no longer be ignored. Inductive effects were recently demonstrated in 4-*mm* long lines in a 0.25 μm process [1]. The extracted *RC* and $\sqrt{LC}$ delays of a typical clock line from this test chip are shown in Fig 10.4.1(a). While the $\sqrt{LC}$ delay is a linear function of line length, the *RC* delay increases with the square of the line length. As a result, the inductive effects are actually more prominent for lines with intermediate lengths. (3 to 8 *mm* as shown in Fig. 10.4.1(a)) The inductive effects for the intermediate length buses as well as local clocks must be considered. As technology is scaled, the gate delay time will continue to be reduced while the delay of short, low-resistive clock lines will remain constant. The inductive effects will therefore become prominent for progressively shorter lines as illustrated in Fig 10.4.1(b). Fig. 10.4.2 shows simulated inductance effects on cross talk. Larger coupling and ringing effect are observed when inductive coupling is included in the simulation. Currently, the inductive effects are only considered for a few global clocks and buses, which is insufficient for future designs. Although 3D electromagnetic full wave solvers are available, they can not manage the complexity of today's integrated circuits. To model the inductive effects of intermediate-length buses as well as local clocks, a fast automated inductance extraction and verification tool will be necessary. In this paper, an efficient 3D modeling method is presented which captures 3D geometry effects directly from layout design and critical process technology information. Analytical formulae are derived to estimate inductance in order to establish guidelines for circuit design. Test chips have been fabricated to emulate high frequency behavior in VLSI circuits; simulation and analytical formulae are compared with measured data.

Layout-based 3D Geometry Extraction and Analytical Formulae Derivation

Layout-based 3D geometry extraction combines 2D information from layout design (e.g. GDS II files) with the specified process technology information file which includes details of layers thicknesses and other material parameters. Inductance modeling requires information on current flow direction which is based on the user specified sources and sinks. Electromagnetic simulators such as FASTHENRY [2] are used to extract the inductance for the 3D structures. Fig. 10.4.3 shows the test chip which includes ground lines and signal lines. Details of the test chip technology are presented elsewhere.[1]

Although accurate inductance estimation based on simulations is essential to future designs, analytical inductance calculations are desirable as efficient design guidelines. Based on electromagnetic field theory, analytical formulae for some typical interconnect structures including coplane waveguide have been derived. For the coplanar waveguide case, the signal line is sandwiched between two ground lines. The loop inductance of the coplanar waveguide per unit length can be shown to have the form:

$$\hat{L} = \frac{\mu_0}{2\pi}\left[\ln\frac{d}{r_{sig}} + \frac{1}{2}\ln\frac{d}{r_{gnd}} + \frac{1}{2}\ln\left(1-\frac{1}{\alpha}\right) + \frac{1}{2}\frac{\ln\frac{w_p}{(\alpha-1)r_{gnd}}}{\ln\frac{w_p}{r_{gnd}}}\ln(\alpha-1)\right] \qquad \alpha \geq 2 \qquad (1)$$

Where α is the ratio of ground wire pitch to the distance between the signal wire and the nearest ground wire. r_{sig} and r_{gnd} are equivalent radii of signal and power lines, respectively. w_p is ground wire pitch. d is the distance of a signal wire to the nearest ground wire. As long as the signal wire width is smaller than that of the ground wire, the ground lines' width can be approximated by the signal wire width at high frequencies because of the proximity effect. Skin effect can also be included [3]. Considering the rectangular cross-section typical for VLSI interconnects, the following simplified formulae can be used:

$$\hat{L} = 3\ln\left(\frac{s+w}{w+t}\pi\right) - \ln 2 + I \qquad 2 \le \alpha < 4 \qquad (2)$$

$$\hat{L} = 3\ln\left(\frac{s+w}{w+t}\pi\right) + 1 + I \qquad \alpha \ge 4 \qquad (3)$$

where s is spacing between signal wire and the nearest ground wire. (With units of 10^{-1} *nH/mm*). w is the width of signal wire and t is the thickness of the metal layer. I is the frequency dependent internal inductance given by $I = 0.75\tanh\left(\frac{2\delta\pi}{w+t}\right)$, with $\delta = \frac{1}{\sqrt{\pi\sigma f\mu}}$, the skin depth of the material, where f is frequency, σ is the conductivity and μ is the permeability of the metal layer.

Experimental and Simulation Results

Test chips were fabricated and the two-port *S*-parameters were measured using an HP 8510 Network Analyzer and Cascade Microtech coplanar ground-signal-ground probes. Measurement results and simulations are compared in Figs. 10.4.4 and 10.4.5.

Inductance increases monotonically with the spacing between the wire and ground lines; current returns through the closer ground line in the cases of smaller spacing. Larger spacing distributes the return path of the current between the two ground lines and increases the current return loop and hence inductance. The inductance increases slower when spacing is large and become maximum when the wire has equal distances to the two ground lines. Wire inductance decreases monotonically with wire width since wider traces result in smaller loops and its associated magnetic flux. Higher frequency results in smaller inductance because of the skin effect. When frequencies increase from 1 *GHz* to 10 *GHz*, measured inductance is systematically reduced compared to simulated inductance, which indicates that shorter return paths exist for these test chips. As a result, the inductance is decreased due to coupling capacitances between the wires and capacitances that offer ac return paths involving the wires to substrate. This effect is first seen for the small spacing cases. Fig. 10.4.6 compares the inductance from the analytical formulae and simulations.

Since the substrate is connected to ground, it could support part of the return current. To model this effect, the substrate can be treated as a return path beneath the signal wire according to proximity effects. Substrate skin depth is used to calculate effective distance between signal and ground wires. The revised formula, including substrate effects can be written as:

$$\hat{L}_{total} = \hat{L}_{previous} - k\frac{\mu_0}{2\pi}\ln\left[\frac{\sqrt{\left[s+\frac{(w_{gnd}+w)}{2}\right]^2+h^2}}{h+\frac{1}{2\sqrt{\pi f\sigma\mu_0}}}\right] \qquad (4)$$

where $\hat{L}_{previous}$ is the inductance without substrate effects, h is the distance of metal layer from the substrate, w_{gnd} is the width of the ground lines, σ is the conductivity of the substrate, and k is the percentage of current returns via substrate. k is approximated by the current distribution for the dc case which is around 30% in this study. When the spacing between signal wires and the ground lines is larger than 20 μm, with a ground line pitch of 251 μm, analytical calculations without substrate correction become inaccurate as seen in Fig. 10.4.7. With spacings larger than 40 μm, more current tends to return via the substrate which forms a smaller current loop comparing to the ground lines resulting in an 18% reduction of wire inductance.

The spacing between the signal wire and the closest ground line is a critical factor that determines the loop inductance. Internal inductance is small compared to external inductance at high frequencies. Three critical factors that determine substrate effects are spacing between signal line and ground line, distance between signal line and substrate and substrate conductivity.

Conclusion

Results from both measurements and simulations show the growing impact of on-chip inductance for sub-0.25 μm VLSI. Inductance is now a critical factor for intermediate (*mm*-scale) length lines. New physical modeling includes accurate (3D) geometry and consideration of substrate effects. Analytical formulae, benchmarked with simulations, demonstrate accuracy suitable for design.

Reference:

[1] Bendik Kleveland et al., “Line inductance extraction and modeling in a real chip with power grid”, IEDM’99, Dec. 1999.

[2] M. Kamon et al., “FASTHENRY: a multipole accelerated 3D inductance extraction program”, *IEEE Trans. Microwave Theory & Techniques*, pp. 1750, 1994.

[3] E. B. Rosa et al., “Formulas and tables for the calculation of mutual and self-inductance”, Government Printing Office, 1916.

Figure captions:

Fig. 10.4.1(a) Line delay for different delay models.

Fig. 10.4.1(b) Inductive effects vs. technology scaling.

Fig. 10.4.2 Inductance effects on cross talk.

Fig. 10.4.3 Die photo of the test chip.

Fig. 10.4.4 Measurement and simulations comparison.

Fig. 10.4.5 Measurement and simulations comparison.

Fig. 10.4.6 Wire inductance formulae.

Fig. 10.4.7 Wire inductance with substrate effect.