A PMOSFET ESD Failure Caused by Localized Charge Injection

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ABSTRACT

A new failure mechanism of PMOSFET devices under ESD conditions is reported and analyzed by investigating various I/O structures. Localized turn-on of the parasitic pnp transistor can be caused by localized charge injection into the body of the PMOSFET. Critical layout parameters affecting this problem are discussed based on 2-D device simulations. A general strategy for avoiding this failure mode is also suggested.

INTRODUCTION

In the development of ESD protection devices, PMOS transistors have not attracted much attention due to low β of the parasitic lateral pnp BJT, which results in small snapback and high on-resistance characteristics. As CMOS technology advances [1], the performance of PMOS in the snapback mode has improved continuously [2,3]. For instance, the high current beta for a PMOS device in 0.1 μm technology becomes close to that of an NMOS in 0.13 μm. Furthermore, the PMOS device shows more uniform conduction if n-well resistivity is sufficiently high, which allows reasonably high I_{T2} (>4mA/μm). While performing well in snapback conduction mode has shown promise for the PMOS to be employed as a positive ESD clamp, it can also be turned on inadvertently, leading to competing current paths in I/O circuits which raises new reliability issues [4]. Recently, design methodologies for minimizing these reliability concerns have been suggested at the process, device and circuit levels [3].

In this paper, a new ESD failure phenomenon of a PMOS pull-up device is presented. This failure was observed despite devices being sized large enough to endure the expected ESD stress. The new failure mechanism was examined using TLP (Transmission Line Pulsing) tests for various I/O structures using fully salicided, 3.3V, 0.13μm CMOS technology, and 2-D circuit/device mixed mode simulations.

ESD FAILURES of PMOSFET PULL-UP DEVICES

Figure 1 shows the schematic of a generic output driver which includes an I/O pad, a pull-up PMOSFET (M1), a pull-down NMOSFET (M2), a rail clamp with gate-coupled and substrate-pump [5] NMOS devices, and a negative strike diode (D1). When the I/O is stressed negative with respect to Vdd (or equivalently, V_{DD} positive with respect to I/O pad), the stress current is supposed to flow from the Vdd pad to the I/O, through the rail clamp and the negative strike diode (path 1 in Figure 1). Depending on the effective on-resistance of path 1 and the applied ESD stress level, the voltage at the Vdd pad can rise high enough to force the pull-up PMOS into the snapback conduction mode, and path 2 in Figure 1 starts to shunt current and compete with path 1. If the on-resistance of PMOS in a snapback conduction mode is low enough to draw a significant amount of current from the path 1, the PMOS can easily reach its second breakdown [3]. Figure 2 shows an example of this PMOSFET failure in an actual inverter. As indicated by the circle, the damaged site is located at the center of the PMOSFET and shows the source-to-drain silicide filaments caused by the pnp triggering. Boselli et al. [3] suggested various solutions to avoid this failure event, and the simplest method is to estimate the minimum PMOSFET width required to sustain the expected current level and make the PMOSFET larger than this minimum width.

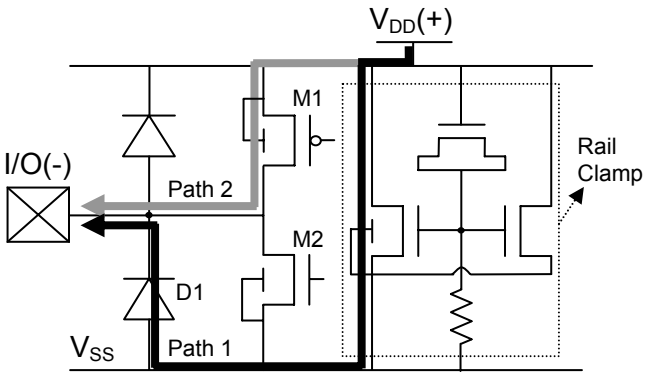

Figure 1: The generic configuration of an ESD protection circuit, where the pull-up PMOSFET has been reported to unexpectedly fail when a negative stress is applied between the I/O and the Vdd.

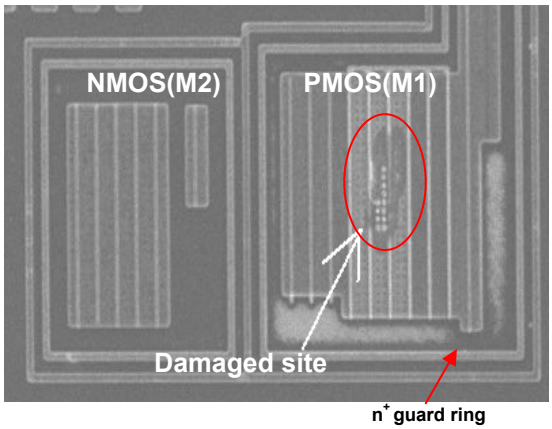

Figure 2: Location (circled) of the PMOS failure in an actual inverter. The pull-up PMOSFET (M1 in Figure 1) and pull-down NMOSFET are shown.

Figure 3 gives TLP measurement for Vdd positive to I/O. Note that the PMOSFET is properly sized to endure the expected stress level. This figure also provides an *Id-Vd* curve of an isolated PMOSFET measured with connected gate and source, showing a snapback behavior and the triggering voltage, V_{TI} (~ 8.5 V). The complete I/O circuit has a soft turn-on behavior inherited from the gate-coupled substrate-pump clamp [5]. The *I-V* characteristics of the complete I/O circuit also shows that the voltage difference exceeds V_{TI} of the isolated PMOSFET, which means the parasitic pnp of M1 is triggered and the stress current flows through both of path1 and path 2, as described in Figure 1. As can be seen from Figure 3, there is a distinct change of slope as the clamping voltage reaches the

triggering voltage of the PMOS, leading to a decreased on-resistance. In this I/O circuit, a large amount of current (> 2.5 A) can be sustained even after the stress voltage exceeds the V_{TI}, since the PMOSFET is sized large enough to endure this level of ESD stress. It is also worth pointing out that the ESD damage was observed in the rail clamp, not in the PMOSFET (M1).

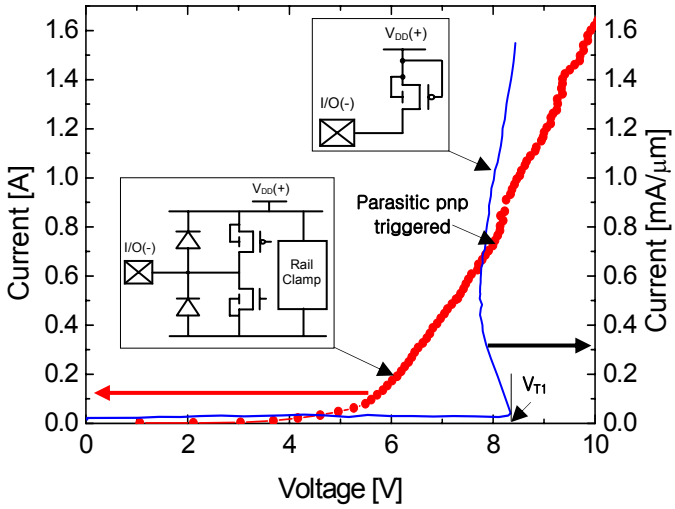

Figure 3: *IV* curves generated by TLP tests of an output driver circuit and an isolated PMOS transistor. A large current (> 2.5 A) can be sustained by the output driver even after the stress voltage exceeds the V_{TI}. There is a distinct change of slope at I = 0.65A where the parasitic pnp transistor is triggered on.

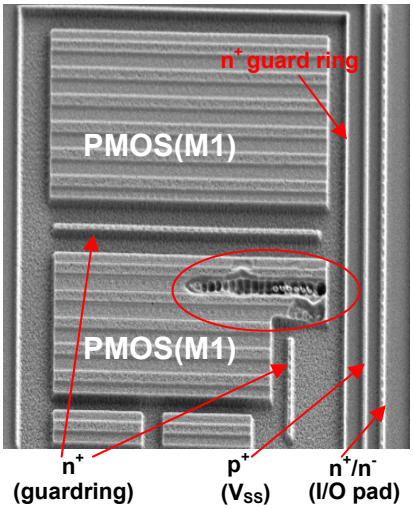

Figure 4: An example of PMOS failure in an actual I/O circuit. PMOS (M1 in Figure 1) devices are located in two different blocks. A negative strike diode (D1 in Figure 1) which consists of p+ (Vss) and n+/n- (I/O pad) is at the rightmost side. Between the two PMOS blocks and at the right side of the lower PMOS block, there are n+ diffusion lines connected to the guard ring. An ESD damaged site (the circled region) is observed close to the negative strike diode.

However, although the PMOSFET is sized large enough to endure the required stress level, we consistently encountered the PMOSFET ESD damage phenomenon in certain I/O circuits. The pattern of this behavior is quite different from that of the typical PMOSFET failure described in Figure 2. Figure 4 shows an example of new PMOSFET failure patterns. This specific I/O has a complex guard ring shape with a short n^+ stripe at the right side of the lower PMOSFET block and another n^+ stripe between the two PMOSFET blocks. The two vertical stripes at the rightmost side are p+ diffusion (connected to Vss) and n+/n-well diffusion (connected to I/O pad), forming a negative strike diode (D1 in Figure 1). It should be noted that the ESD damaged site with molten drain/source contacts [6, 7] is observed close to the negative strike diode but not at the center as in Figure 2. This failure pattern appeared consistently in certain I/O circuits with failing at 2.2 kV HBM condition even though they are designed to endure more than 5 kV. This fact indicates that there is a systematic effect which lowers ESD immunity level.

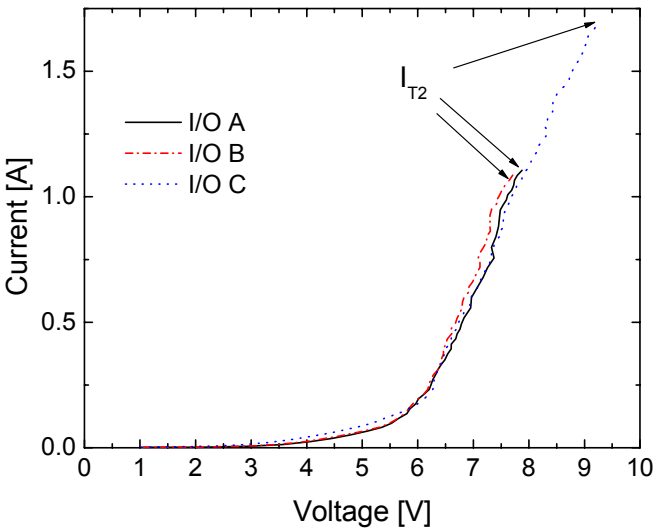

Figure 5: Measured *IV* curves of various I/O structures up to failure points, generated by TLP tests.

Table 1: The layout information and ESD test results of various I/O circuits. DR1 is the distance between the negative strike diode and the guard ring (see the representation of layouts in Figure 6).

	DR1	n^+ guard ring	HBM Fail Level
I/O A	0.8 μm	Incomplete	2.2 kV
I/O B	0.8 μm	Incomplete	2.4 kV
I/O C	> 0.8 μm	Incomplete	2.9 kV
I/O D	1.0 μm	Incomplete	3.4 kV
I/O E	22 μm	complete	> 5 kV

Figure 5 shows TLP *IV* curves of three different I/O circuits which have similar failure patterns displayed in Figure 4. The design parameters and I_{T2} (translated to HBM failure level) of each device are listed in Table 1. In Table 1, DR1 is the distance between the negative strike diode and the guard ring, as illustrated in the simplified layout diagrams of Figure 6. While the I_{T2} of I/O E (of which the measured *I-V* curve is shown in Figure 3) is higher than 2.5 A (~5kV HBM), I/O A and B fail even before the voltage reaches V_{TI} of an isolated PMOSFET and show the HBM level lower than 2.5 kV. All device dimensions such as the width of PMOSFETs and power clamps are almost identical, whereas their layouts have some variations in the guard ring shape and the distance between the negative strike diode and the guard ring (named as DR1) etc. For example, DR1 of I/O E is larger than 22 μm, but I/O A, B have 0.8 μm DR1. In I/O C, the PMOS block is not located parallel to the diode, and the shortest path from the diode to the guard ring around the PMOS block is about 0.8 μm long. The guard ring of I/O E is completely closed as in Figure 2, while in other I/O circuits the one side of the guard ring does not have metal contacts (see Figure 6b in the next section).

Two observed facts should be emphasized here; first the damaged spots of I/O A,B,C and D are always located in the PMOS transistor near the negative strike diode as can be seen in Figure 4. Second, when DR1 increases from 0.8 µm to 1.0 µm the ESD failure level increases by about 1 kV. These TLP test results show that the distance between the negative strike diode and the guard ring(DR1), and the shape of the guard ring can be critical parameters determining ESD immunity of I/O circuits. The physics involved in this phenomenon will be clarified in the next section.

ANALYSIS OF A NEW FAILURE MECHANISM

In Figure 6, schematics of the I/O layout are illustrated for facilitating the following discussions. The location of the ESD damaged spot is indicated in each schematic. The p-substrate to n-well diode (D1) are located adjacent to PMOS pull-up devices (M1), and ESD damage occurs in the vicinity of the diode and around the center of gate fingers. The distance from p^+ V_{SS} to n^+ guard ring is noted as DR1, and the distance between p^+ V_{SS} and n^+ diffusion connected to I/O is DR2. The guard ring shown in Figure 6a has metal contacts at every closure, but in Figure 6b one stripe between the PMOS and the diode does not have a metal contact in order to achieve a more compact design. The influence of this difference in the guard ring shape will be discussed in detail in the next section.

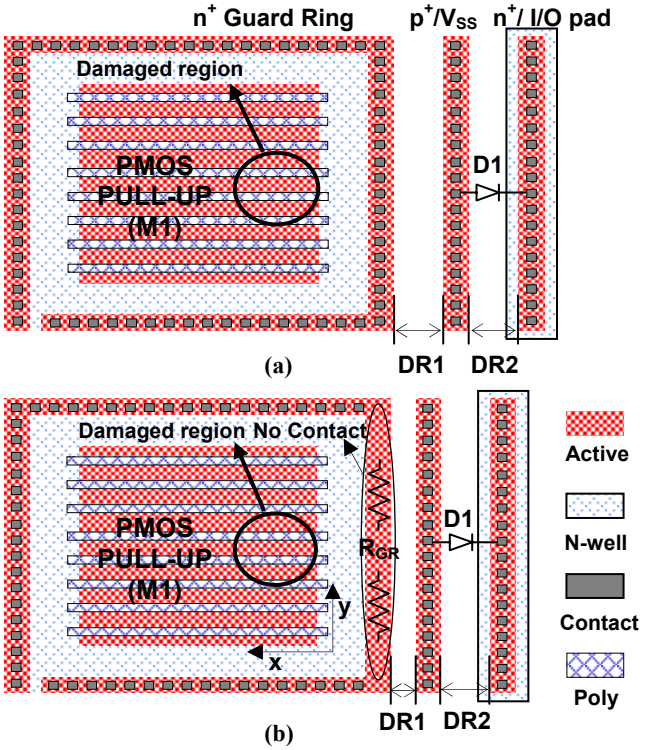

Figure 6: Simplified diagrams of I/O layout. Only PMOS pull-up devices(M1 in Figure 1) and negative strike diodes(D1 in Figure 1) are illustrated. a) Its guard ring has metal contacts at every closure, b) metal contacts are missing at one stripe.

Figure 7 shows the schematic of the equivalent circuit of an I/O circuit under ESD conditions, which includes the devices involved in both path 1 and path 2 of Figure 1. Here, R_{well_1} and R_{well_2} represent the resistance of n-well from source/n-well junction to the n+ guard ring (see also Figure 8a). R_{GR} is the extra resistance caused by incomplete contact formation as illustrated in Figure 6b. If the diode D1 is far from the pull-up PMOS device and decoupled from each other, path 1 and path 2 can be analyzed independently. In this case, the parasitic pnp BJT (T1) is triggered through self-biasing using the internal avalanche generation of carriers (I_{AV}) [8]. Here R_{well_1}, R_{well_2} and R_{GR} act as effective body resistance of the PMOSFET. However, if these two devices are moved closer, the analysis with D1 in Figure 7 is no longer valid and the parasitic npn BJT (T2 in the dotted box of Figure 7) should be considered instead of D1; this npn transistor supplies the external triggering current (I_{inject}) to the base of pnp transistor. This explanation can be clarified by the simulation results shown in Figure 8.

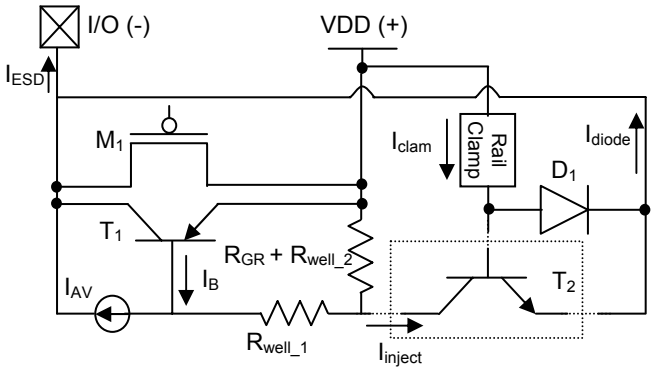

Figure 7: Schematic of the equivalent circuit under ESD conditions. The parasitic npn BJT in the dotted box (T_2) should be considered only if a negative strike diode is placed close to the pull-up PMOSFET (M1).

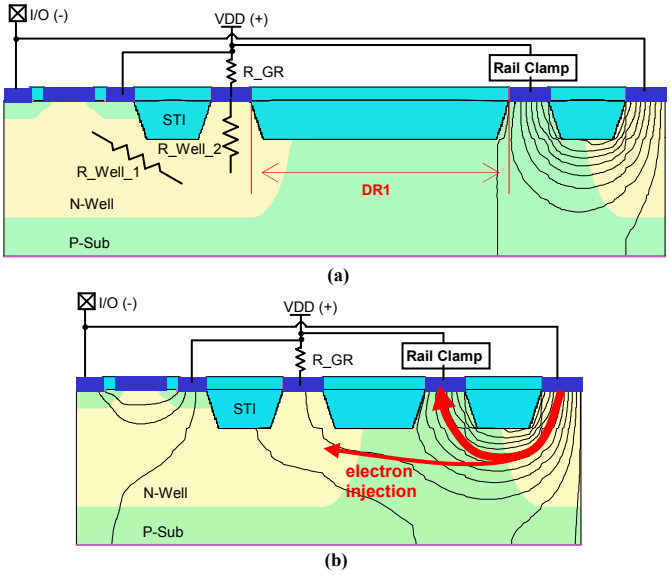

Figure 8: Current Flow lines under ESD conditions. a) The PMOS transistor is separated away from the negative strike diode (DR1 = 3 µm), b) the PMOS is close to the diode, therefore the two devices are electrically coupled (DR1 = 1 µm).

In order to investigate the influence of each layout parameter variations, circuit/device mixed mode simulations were performed. The device structure and external circuit components employed in the simulation are illustrated in Figure 8. The rail clamp in Figure 8 is implemented with a constant resistance, R_{clamp}, since the on-resistance of rail clamps can be considered constant in a wide high-current range [3]. The value of R_{clamp} is extracted from the measurement results when parasitic pnp transistors are triggered. This figure also shows the simulated current flowlines of I/O devices represented by the equivalent circuit of Figure 7. In Figure 8a, the negative strike diode is located distantly from the n^+ guard ring (DR1 ≈ 3 µm), therefore most of the electrons emitted through n-well/substrate junction from the I/O pad recombine with the holes from V_{SS} which is connected to

the rail clamp. However, if the two devices are located close to each other (DR1 ≈ 1 μm), some portion of electrons from the diode are injected into the n-well body of the PMOSFET, modulating the base potential of the pnp transistor (T1 in Figure 7). This process results in early turn-on of the parasitic pnp transistor. If R_{GR} increases as in the case of Figure 6b, the base potential is further modulated due to the voltage drop across the R_{GR}, resulting in lower triggering voltage.

These simulation results and the analysis of the equivalent circuit in Figure 7 explain the cause of the PMOS failure reported in the previous section. The structure of Figure 6b has several drawbacks compared to the guard ring structure of Figure 6a. First, due to the smaller distance from the diode, the body potential of PMOSFET (the base potential of the pnp transistor) is modulated by the current injected from the diode. Second, incomplete guard ring metal causes spatial variations of the effective body resistance, which is reflected in R_{GR} of the equivalent circuit. These two drawbacks cause the non-uniform turn on of pnp transistors and degrade ESD immunity of I/O circuits.

INFLUENCE OF LAYOUT PARAMETER VARIATIONS

Considering that the BJT is a current controlled device, we can formulate the triggering voltage for the case that the PMOS and the negative strike diode are electrically coupled, with reference to the equivalent circuit of Figure 7.

$$I_{inject} = I_{clamp} \cdot \beta \quad \text{(eq. 1)}$$

$$V_{DD\_Pontential} = I_{clamp} \cdot R_{clamp} + V_{diode} = I_{inject} \cdot \frac{1}{\beta} \cdot R_{clamp} + V_{diode} \quad \text{(eq. 2)}$$

$$V_{body,\,trig} \approx (R_{GR} + R_{well\_2}) \cdot (I_{AV} - I_B + I_{inject,\,trig}) + R_{well\_1} \cdot (I_{AV} - I_B) \quad \text{(eq. 3)}$$

Here, β is the common emitter current gain of the npn transistor (in the dotted box of Figure 7). I_{inject} is the electron current from the negative strike diode into n-well of the PMOS transistor, and it is assumed that most of this electron current flows directly to the guard ring contacts through R_{well2} as shown in the current flowlines of Figure 8. V_{diode} is the voltage drop through the negative strike diode and is a function of DR2 in Figure 6. $I_{inject,\,trig}$ is I_{inject} at the pnp triggering point. $V_{body,\,trig}$ is the body potential near the source/body junction with reference to V_{DD} at the triggering point, and can be considered as constant. In equation 3, $I_{inject,\,trig}$ is much larger than I_{AV} if the PMOS and the diode are located in proximity to each other, and then equation 2 can be approximated as follows.

$$V_{DD\_Potential}\,@\,pnp\ \ triggering = V_{T1} \approx \frac{V_{body,\,trig}}{R_{GR} + R_{well\_2}} \cdot \frac{1}{\beta} \cdot R_{clamp} + V_{diode} \quad \text{(eq. 4)}$$

As DR1 decreases, the common emitter current gain (β) of parasitic npn increases, hence V_{T1} decreases as expected in equation 4. As can be seen in Figure 9, the triggering point of parasitic pnp of the PMOSFET is a strong function of DR1. For instance, when DR1 is reduced from 1.2 μm to 1.0 μm, V_{T1} decreases by ~ 1 V. The device with 0.8 μm DR1 is triggered around 5.7 V, without showing snapback behavior. However, if DR1 is larger than 1.2 μm, V_{T1} is not sensitive to DR1 variation. In other words, the localized electron injection from the negative strike diode into the body of PMOSFETs increases significantly if DR1 is less than a certain value, and causes non-uniform conduction along the x-direction in Figure 6, therefore deteriorating the ESD robustness of I/O circuits

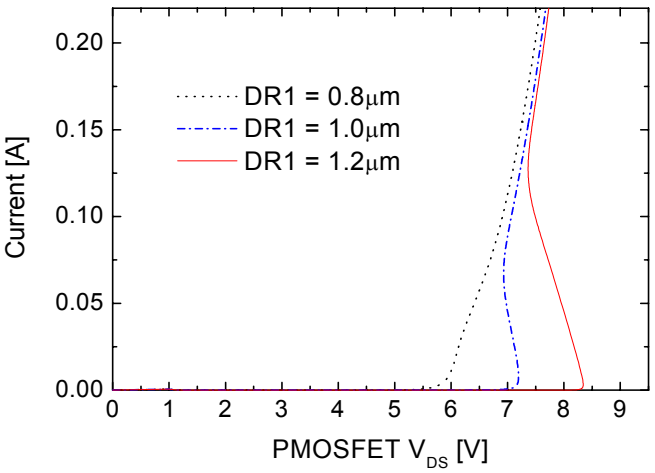

Figure 9: Simulated *Id-Vd* characteristics of PMOS transistor in I/O circuits with various distances between the guard ring and negative diode. DR1 lower than 1.2 μm considerably affects the triggering voltage of pnp transistors. Here, R_{GR} is 0 Ohm and DR2 is 0.6 μm.

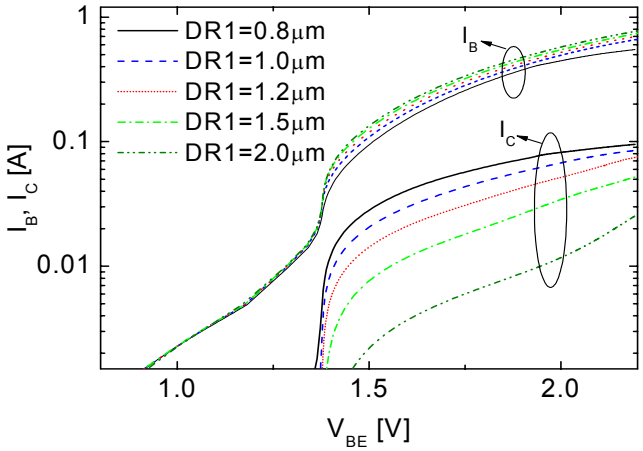

Figure 10: Simulated collector and base currents of the parasitic npn transistor (T2 in Figure 7) as functions of the emitter-base voltage with various distances between the negative strike diode and guard ring (DR1).

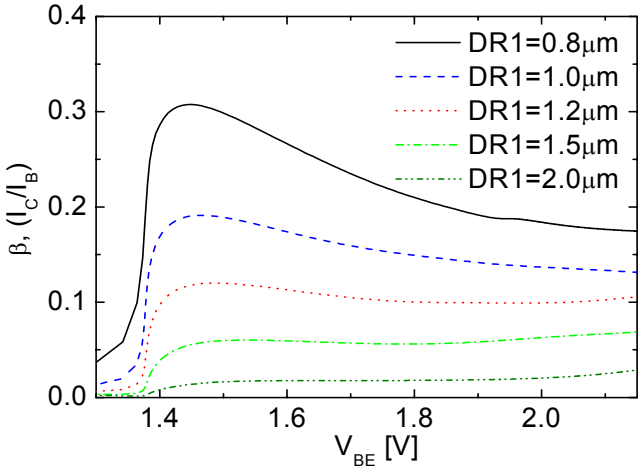

Figure 11: Simulated current gains as functions of emitter-base voltage with various distances between the negative strike diode and guard ring (DR1).

In order to investigate the effect of DR1 variations on the characteristics of the parasitic npn transistor, collector current (I_C, same as I_{inject}), base current (I_B, same as I_{clamp}) and the static common-emitter current gain, β are plotted in Figure 10 and Figure 11. Since the doping concentration of the emitter (n-well) is not much higher than that of the base (p-substrate), emitter efficiency (γ) is much smaller than 1. If DR1 is larger than 1.5 μm, the base transport factor (α_T) is much less than unity, therefore β is less than 0.1. However, the peak β increases over 0.1 as DR1 decreases to 1.2 μm, and a large current is injected into the body of PMOSFET, causing early turn-on of the pnp transistor.

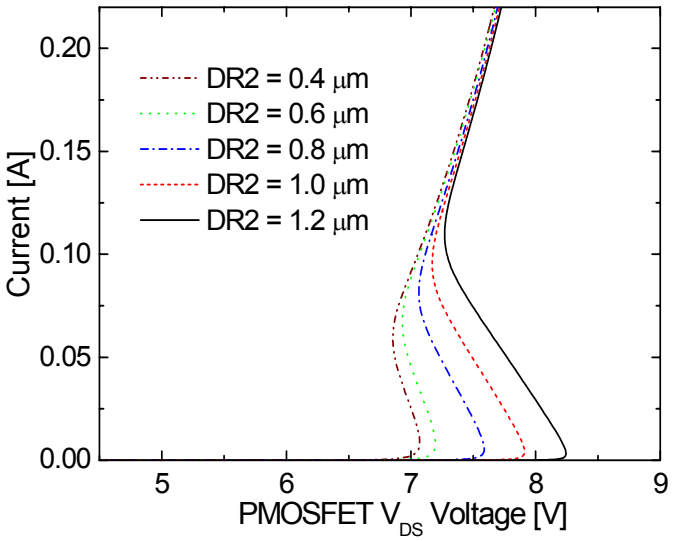

Figure 12: Simulated *Id-Vd* characteristics of PMOS transistor in I/O circuits with various distances between the p+ diffusion and n+ diffusion of the negative diode (DR2). Here, R_{GR} is 0 Ohm and DR1 is 1.0 μm

Figure 12 shows that as the DR2 (the distance between p+ VSS and n+ diffusion connected to I/O pad) increases, the triggering voltage also increases, due to the decrease of T2's β and the increase of V_{diode} in equation 4. However this also causes the on-resistance of path 1 in Figure 1 to be increased, therefore increasing DR2 is not an efficient solution to mitigate the stress on the PMOS in path 2.

In the mixed mode simulations, a lumped resistor, R_{GR} is employed in order to reflect the finite conductivity of n+ diffusion layer of guard ring (see Figure 6b). However, all segmented devices are connected also through the n-well as well as through n+ diffusions, therefore the spreading resistance should be calculated for extracting an effective R_{GR}. As shown in Figure 13, 3-dimensional simulations were performed for calculating the distributed well resistance and investigating the effect of guard ring structure variation on the well resistance. In Figure 13, two guard ring structures are shown; the one is the closed guard ring as in Figure 6a and the other is the U-type guard ring in which one stripe does not have metal contacts but has only n+ diffusion as in Figure 6b. In each structure, a contact is located inside the guard ring closure for injecting electron current which flows to the guard ring. By measuring the voltage difference between this contact and the guard ring, we can extract effective R_{well} from a certain location inside the guard ring closure to the guard ring. Figure 14 shows R_{well} variations in two guard ring structures along the line A-A' (close to the negative strike diode) of Figure 13b. The extracted resistance values are normalized with reference to the value at the middle of A-A'. At the location away from the center of A-A' by 3 μm, the R_{well} of the U-type guard ring structure decreases by ~7 %, while the variation of R_{well} inside the closed guard ring is less than 1 %. The variation of R_{well} along the line B-B' is also plotted in Figure 15. As shown in Figure 14 and Figure 15, the device with an U-shape guard ring shows considerable variation of the spreading R_{well}, which may cause non-uniform conduction along both x and y directions.

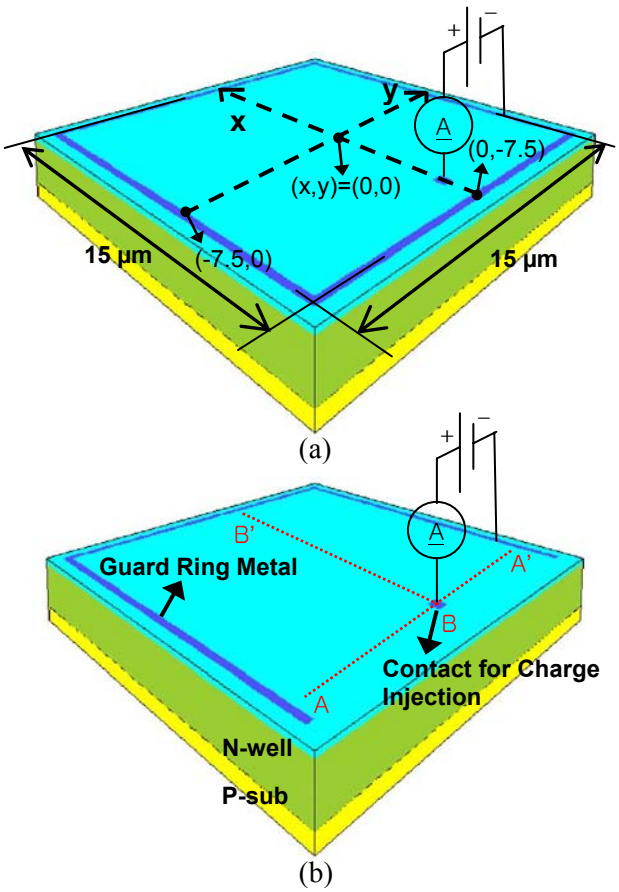

Figure 13: Extraction of spreading well resistance (R_{well}) (a) closed guard ring as in Figure 6a, and (b) U-shape guard ring as in Figure 6b**.**

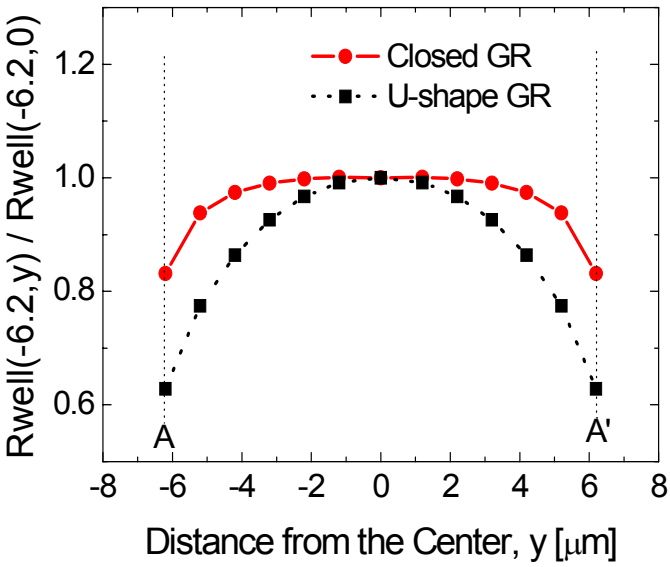

Figure 14: Variations of the spreading well resistance along y-direction near guarding (x = - 6.2 μm, along the line A-A'). The spreading well resistance is normalized with reference to the value at the center.

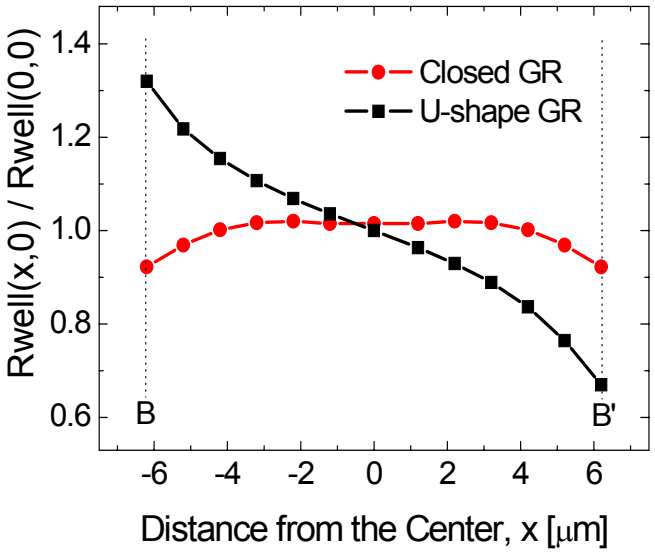

Figure 15: Variations of the spreading well resistance along x-direction (y = 0 μm, along the line B-B'). The spreading well resistance is normalized with reference to the value at the center.

For thorough investigation of the effect of this R_{well} variation on ESD immunity, 3-D ESD simulations with various guard ring structures should be performed. However, in this work the effect of R_{well} variation is investigated with 2-D simulation by simply varying the lumped resistance, R_{GR} between V_{DD} and the n+ guard ring. In 2-D simulation, the well resistance, R_{well0} (= R_{well1}+R_{well2}, of Figure 7) is extracted from I_{sub} vs I_d curve [8, 9] with zero R_{GR}, and then a certain fraction of R_{well0} is applied to R_{GR}. As expected from equation 4, higher R_{GR} causes the body potential of the PMOSFET to rise higher and the pnp transistor is triggered at lower V_{T1}. Figure 16 shows that the triggering voltage with R_{GR} of 2% R_{well0} is lower than the triggering voltage with zero R_{GR} by ~ 0.4 V. This observation implies that the finite resistance of the n+ guard ring without a metal contact results in non-uniform potential distributions across the body of PMOS transistors and the localized current conduction.

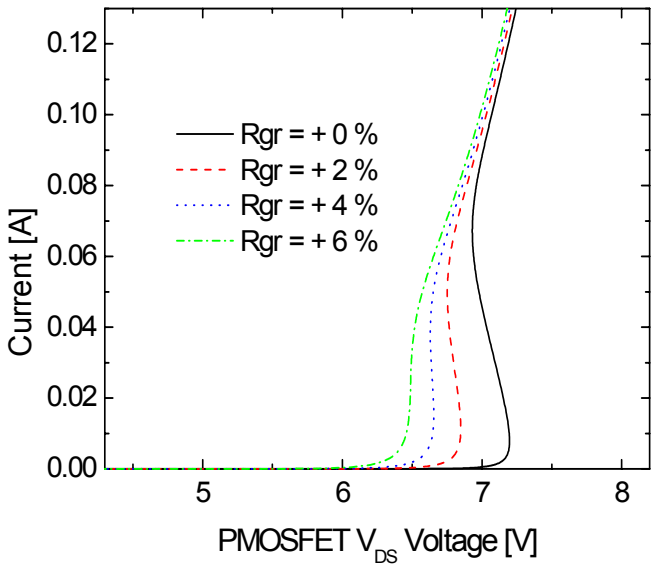

Figure 16: *Id-Vd* characteristics of PMOS transistors in I/O circuits with various external resistance between the body contact and the V_{DD}. DR1 and DR2 are 1.0 μm and 0.6 μm, respectively.

DESIGN IMPACT

This paper demonstrates the layout of the PMOS relative to diffused regions connected to the I/O pin, can play a role in the effectiveness of the overall protection at the pad. The best possible option is to move the PMOS layout more than 20 μm away from the I/O protection devices. However, in most cases this may not be practical. In an ASIC environment various types of buffers would use the same protection cell at the pad but the output NMOS and PMOS are laid out differently depending on the design features. Some buffers might tolerate a series resistor between the I/O pad and the PMOS and in these cases the interference from the PMOS is not relevant and the final protection level is determined by the current limited to the PMOS, or the failure current limit of the Vdd protection device itself. However in common output buffer designs, a resistor is not tolerated, along with the fact that the PMOS device sizes are different depending on the designed buffer's performance. For example, a 4 mA buffer would have relatively larger PMOS than a 2 mA buffer. However, if the layout is ineffective then the PMOS size does not matter. Once the layout is made more effective as described in this paper, then the PMOS size would play a role in determining the overall protection level. In this case, for ESD purposes it is desirable to make the 2 mA buffer PMOS look like the 4 mA buffer. This may be achieved with the introduction of a dummy PMOS as mentioned in [3,4]. Of course the critical factor is the layout. Specifically, in an ASIC library environment the placement of the protection devices and the latchup guard rings can be complex due to the available macro pitch and the bus architecture. If the negative diode at the pad has to be placed in proximity to the PMOS then it is essential to completely close the guard ring around the PMOS with full contacts and maintain DR1 in Figure 6 to be > 2 μm. If this spacing can be >10 μm then the guard ring shape should not matter.

CONCLUSIONS

A new failure phenomenon of PMOSFET pull-up devices under ESD conditions has been reported and analyzed by investigating various I/O structures of 3.3 V, 0.13μm CMOS technology. The physical mechanism and the influence of layout parameters such as the distance between a negative strike diode and an n+ guard ring(DR1), guard ring shape, and effective resistance of the rail clamp, were investigated through Transmission Line Pulse (TLP) testing and device/circuit mixed mode simulations.

Localized turn-on of the parasitic pnp BJT of the PMOSFET pull-up device can be caused by the localized charge injection into the body of PMOSFET from the negative strike diode. The most critical layout parameter regarding this failure is DR1. Values of DR1 greater than 2 μm are recommended for a safe design with the technology used in this study. This phenomenon can be implicated in ESD failures of all future ASIC I/O circuits which require more compact layouts.

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