# Modeling of Temperature Dependent Contact Resistance for Analysis of ESD Reliability

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## ABSTRACT

A physically based model has been formulated to represent temperature-dependent specific contact resistance. The new model can generate silicided contact resistance values at high temperatures and is capable of predicting high current behavior of silicided deep submicron devices. Implications for failure analysis of advanced silicided devices are also considered. Using the model, it has been demonstrated how current localization is affected by increased temperature, which is critical for predicting ESD reliability.

## INTRODUCTION

As CMOS technology advances, the junction depth of the source/drain and size of other associated device features are being aggressively reduced. Therefore, the impact of source/drain parasitic resistances on device performance becomes increasingly significant since the parasitic resistance component does not scale with device dimensions and thereby contributes an appreciable fraction of the total resistance, resulting in significant degradation of the current driving capability [1-4]. Hence, in advanced CMOS technologies, understanding of the physics involving the parasitic resistance is essential for optimization of high performance devices used in various VLSI circuit applications [5, 6]. Additionally, accurate modeling of the silicide/Si contact resistance is also necessary for the analysis of Schottky contact MOSFETs [7].

The contact resistance component of parasitic resistances is not scalable since it simply increases with decrease in contact size commensurate with device scaling. Thus, highly conductive silicide films such as $TiSi_2$, $CoSi_2$ and NiSi have been implemented on the gate and source/drain surfaces for reducing the contact resistances associated with the scaled devices [8, 9]. Moreover, since the sheet resistivity of the silicide film is much lower than that of Si in the source/drain region, the silicide layer practically shunts all the currents leading to increase of effective contact sizes. Due to this beneficial effect, salicidation is a standard process for advanced devices.

Furthermore, it is known that the current flow or current distribution associated with the silicided contact system in the source/drain structure is strongly influenced by the contact resistance value itself. Therefore, it is important to identify carrier transport mechanisms determining the silcided contact resistance value for improved understanding of its implications for optimizing device performance. In this regard, in order to investigate the impact of the contact resistance on device and circuit performance, a transmission line model for silicided contact systems was developed [10] and based on the model, circuit performance degradation due to increased parasitic source/drain resistance and high current effects on contact resistivity were intensively addressed [11]. Another theoretical investigation also emphasized the importance of contact resistance in circuit performance with device scaling [1].

Through various technology nodes, it is also empirically well known that the application of silicided process can severely degrade ESD reliability [12] and thus for the protection devices requiring higher ESD robustness, the silicided layers on the source/drain can be partially or fully blocked to alleviate the current crowding effect under high current and temperature conditions. In addition, it has been shown that for silicided NMOS devices the source/drain contact spacing has a significant impact on ESD performance [13].

As a result, the impact of the contact resistance on the current distribution also has important implications for ESD reliability through localized heating effects with current localization during ESD events [4]. Thermal effects involved in the contact resistance become more important in the deep submicron device regime, especially under high current stress conditions such as ESD, since the scaled devices become more susceptible to ESD induced thermal failures due to the decreasing power dissipation volume.

Therefore, there is a growing demand to comprehend the high current behavior of silicided contact systems. In device simulation, distributed resistor networks are often used to reproduce the silicide effect in the source/drain contact systems, but the temperature dependency is hard to incorporate. Also, silicide models are not readily available in commercial device simulation tools and thus device simulation is not very effective for analysis of ESD performance of silicided devices.

It has been demonstrated that the contact resistance's sensitivity to temperature and/or current is strongly influenced by the silicide thickness due to the difference in the interface doping concentration, which, in turn, influences the transport mechanism across the silicide/Si interface [4]. However, the temperature dependence of contact resistance and associated high current behavior has not been fully investigated for ESD reliability analysis. Although a theoretical model of silicided contact resistance has been developed in [14], high current behavior cannot be predicted with this model since it did not account for any temperature dependency.

Therefore, in this work, based on refinement of established analysis we propose a new temperature dependent specific contact resistance model for generating contact resistance values depending on temperature, and for predicting high-current behavior of silicided deep submicron devices. The new model is useful for analysis of both parasitic source/drain resistance and ESD reliability in deep submicron devices.

## MODELING of TEMPERATURE DEPENDENT SPECIFIC CONTACT RESISTANCE

For a metal semiconductor junction, the specific contact resistance $\rho_c$ is defined as

$$\rho_c = \left(\frac{dV}{dJ}\right)_{V=0} \tag{1}$$

where $J$ is the current density of a metal semiconductor contact and $V$ is the applied voltage across the junction. Using the theoretical relation of current-voltage characteristics for a metal semiconductor junction, $\rho_c$ can be formulated. In general, for a metal semiconductor contact, the carrier transport mechanisms can be separated into three regions: field emission (FE) [15-17], thermionic-field emission (TFE) [17, 18], and thermionic emission (TE) [15-17], depending on the background doping concentration of the semiconductor.

In advanced CMOS devices, the source and drain are formed with a moderate or high doping concentration (i.e., typically, $N \geq \sim 10^{18}$ cm$^{-3}$). Therefore, for advanced devices, the carrier transport mechanisms for a metal semiconductor junction in the source/drain region are limited to thermionic field emission (TFE) or field emission (FE) process.

For a metal semiconductor contact system with a higher doping concentration, the specific contact resistance $\rho_c$ can be written by [14, 17]

$$\rho_c = [\frac{A^* T \pi q}{k_B \sin(\pi c k_B T)} \exp(\frac{-q\phi_b}{E_{00}}) - \frac{A^* q}{c k_B^{\,2}} \exp(\frac{-q\phi_b}{E_{00}} - cE_F)]^{-1} \quad (2)$$

where

$$c = \frac{1}{2E_{00}} \ln(\frac{4q\phi_b}{E_F}) \quad (3)$$

$$E_{00} = \frac{qh}{4\pi} \sqrt{\frac{N}{\varepsilon_s m^*_{tun}}} \quad (4)$$

$A^*(=4\pi q k_B^2 m^*/h^3)$ is the effective *Richardson* constant, T is the temperature, $\phi_b$ is the barrier height, $E_F$ is the Fermi energy with respect to the energy band edge in the semiconductor bulk, and the quantity $E_{00}$ is a characteristic energy related to the tunneling probability, depending on the doping concentration N, the tunneling effective mass $m_{tun}$*, which is the effective mass component in the direction of current flow [19].

As $E_{00}$ increases with N, the barrier for the tunneling process becomes thinner, and in turn results in increased tunneling of carriers, since the carrier transmission rate $P$, is exponentially increasing with $E_{00}$ as given by [15]

$$P \sim \exp(-q\phi_b / E_{00}) \quad (5)$$

Therefore, the ratio of $k_BT/E_{00}$ can be used as a measure indicating the relative significance of the thermionic emission process with respect to the field emission (tunneling) process [17, 19]: For a lightly doped semiconductor where $k_BT/E_{00} >> 1$, the TE dominates, and for a heavily doped semiconductor where $k_BT/E_{00} << 1$, the FE dominates. Otherwise, for an intermediately doped semiconductor where $k_BT/E_{00} \approx 1$, the TFE dominates.

The above criterion also implies that the carrier transport mechanism can be changed by the temperature rise for a given doping concentration. For a given high doping concentration where the FE dominates, Eq. (2) is valid if [17]

$$T < \frac{1}{k_B[c + (2E_{00}E_F)^{-1/2}]} \quad (6)$$

The above condition also gives a lower limit of doping concentration for the field emission process at a given temperature. At room temperature, the lower limit of doping concentration for the FE process is approximately $N \approx 6.6\times10^{19}$cm$^{-3}$ for a $TiSi_2$ contact system with $q\phi_b$ =0.6eV and $m_{tun}$*=0.19$m_o$ [14].

For a highly doped region, the carrier distribution by *Boltzmann* statistics is erroneous in determining the location of Fermi energy $E_F$.

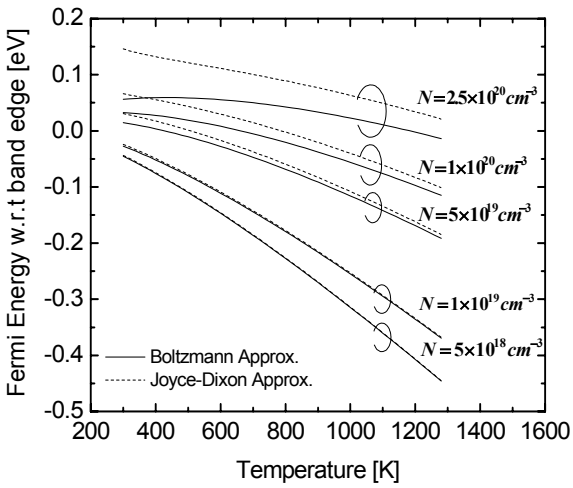


**Figure 1:** The comparison of *Boltzmann* approximation and *Joyce-Dixon* approximation [20] for determining the position of Fermi energy $E_F$ for various doping concentrations as a function of temperature. The difference of Fermi energy between the two models increases as the doping concentration increases.

Therefore, the position of $E_F$ with respect to the energy band edge should be estimated by a more accurate distribution model such as the *Joyce-Dixon* approximation, which is given by [20]

$$E_F = k_B T[\ln(\frac{N}{N_c}) + \frac{1}{\sqrt{8}}\frac{N}{N_c} - (\frac{3}{16} - \frac{\sqrt{3}}{9})(\frac{N}{N_c})^2] \quad (7)$$

where $N_c$ is the effective density of states in the conduction band.

For silicon, the density of states in the conduction and valence bands, $N_c$ and $N_v$, respectively, can be expressed as a function of temperature by [21]

$$N_c = 2.86\times10^{19}(T/300)^{1.58} cm^{-3} \quad (8)$$

$$N_v = 3.10\times10^{19}(T/300)^{1.85} cm^{-3} \quad (9)$$

The intrinsic concentration $n_i$ is also given by

$$n_i = \sqrt{N_c N_v} \exp(-E_g(T)/2k_BT) \quad (10)$$

where $E_g$ (T) is the temperature dependent energy bandgap.

In Fig.1, using the two different approximations for carrier distribution, the theoretically estimated Fermi energy $E_F$ is shown with the temperature for the various doping concentration. As the doping concentration increases (i.e., $N > N_c$), errors arising from using the *Boltzmann* distribution become more significant. For advanced CMOS technologies, the sheet resistivity of the source/drain junction typically ranges from ~50 to ~500 Ω/□, which corresponds to an effective doping concentration in the source/drain junction of $5.1\times10^{20} \sim 3.8\times10^{19}$ cm$^{-3}$. Therefore, for analysis of contact resistance in advanced technologies, the position of $E_F$ should be estimated based on an accurate carrier distribution model. For an intermediate doping regime, the thermionic-field emission (TFE) is the dominant mechanism for carrier transport. In this condition, the specific contact resistance, $\rho_c$ is also given by [17]

$$\rho_c = [\frac{k_B^{\,2}}{qA^*}] \frac{\cosh(\frac{E_{00}}{k_BT})}{\sqrt{\pi(q\phi_b + E_F)E_{00}}} \sqrt{\coth(\frac{E_{00}}{k_BT})} \exp(\frac{E_F}{E_0} - \frac{E_F}{k_BT} + \frac{q\phi_b}{E_0}) \quad (11)$$

where

$$E_0 = E_{00}\coth(\frac{E_{00}}{k_B T}) \tag{12}$$

The above Eq. (11) is valid if

$$\frac{\cosh^2(\frac{E_{00}}{k_B T})}{\sinh^3(\frac{E_{00}}{k_B T})} < \frac{2(q\phi_b + E_F)}{3E_{00}} \tag{13}$$

which also gives a lower bound on the doping concentration needed for thermionic-field emission. Typically, the transition from the thermionic-field emission (TFE) to the thermionic emission (TE) occurs at doping concentrations of $10^{17}$ ~ $10^{18}$ $cm^{-3}$ at room temperature. Therefore, for advanced CMOS technology, the carrier transport in a metal-silicon junction at the source/drain structure is governed by a combination of FE and TFE.

In order to predict the dependence of $\rho_c$ on the temperature, primary physical parameters should also be expressed as a function of the temperature. In general, $\rho_c$ is exponentially dependent on the barrier height, doping concentration, and tunneling effective mass ($m_{tun}$*).

For a metal-semiconductor junction, the barrier height is strongly dependent on the density of surface states and properties of interfacial layer, which is strongly process dependent; the Fermi level $E_F$ is known to be pinned roughly at about one third of band gap, $E_g$ [15, 22, 23]. Assuming that the temperature dependence of the density of surface states is negligible, we can express the temperature dependence of the barrier height to be approximately equal to that of the energy gap $E_g$ [22]:

$$\frac{\partial q\phi_b}{\partial T} \cong \frac{\partial E_g}{\partial T} \tag{14}$$

Using the empirical model of temperature dependent energy gap $E_g(T)$, which is given by [24, 25],

$$E_g(T) = 1.17 - \frac{7.02\times10^{-4}T^2}{T+1108} \tag{15}$$

the temperature dependence of the barrier height can be simply expressed by

$$q\phi_b(T) \cong q\phi_b(T_0) + \frac{\partial E_g}{\partial T}(T - T_0) \tag{16}$$

where $T_0$ is the ambient temperature of interest.

As mentioned previously, the tunneling effective mass $m_{tun}$* is also a critical parameter in the field emission (FE) process [26]. Since a large value of tunneling effective mass gives rise to a small transmission coefficient *P* [in Eq. (5)], the specific contact resistance is exponential with the tunneling effective mass as shown in the equation given by

$$\rho_c \propto \exp(\frac{q\phi_b\sqrt{m^*_{tun}}}{\sqrt{N}}) \tag{17}$$

For any particular ellipsoid on a constant energy surface in *k*-space, the $m_{tun}$* is given by [19]

$$m^*_{tun} = (\frac{l^2}{m_x} + \frac{m^2}{m_y} + \frac{n^2}{m_z})^{-1} \tag{18}$$

where *l*, *n*, and *m* are the direction cosines of the ellipsoid relative to the principle axis, and $m_x$, $m_y$, and $m_z$ are the tensor masses. Silicon has a total of six ellipsoids in the conduction band. For N-type silicon on <100> surface, there are two tunneling effective masses associated with the transverse ($m_t$*) for four of the ellipsoids and the longitudinal effective mass ($m_l$*) for two ellipsoids in the ellipsoidal constant energy surfaces. Based on the low temperature cyclotron resonance studies [21], the $m_{tun}$* is given by $0.916m_0$ (from $m_l$*) and $0.19m_0$ (from $m_t$*) where $m_0$ is the electron mass in free space [26]. Since the tunneling process is exponential with $m_{tun}$*, the $m_{tun}$* from transverse $m_t$* will dominate. The temperature dependence of $m_t$* is experimentally known to be relatively weak and that for $m_l$* is theoretically considered to be even weaker.

In this work, as used in [21], $m_l$* is assumed to be independent of temperature and $m_t$* is weakly temperature dependent as much as on temperature dependent energy scaling factor, which is given by

$$m^*_t(T) = 0.19m_0\frac{E_{g0}}{E_g(T)} \tag{19}$$

where $E_{g0}$ is the value of energy band gap $E_g(T)$ at T=0 K. The effective mass m* in *Richardson* constant A* is different from $m_{tun}$* and is given by [26, 27]

$$m^* = (l^2 m_y m_z + m^2 m_x m_z + n^2 m_x m_y)^{1/2} \tag{20}$$

For computing the *Richardson* constant, the number of equivalent ellipsoids corresponding to the $m_{tun}$*, *M* should be included (*M* = 4 from $m_t$* and $A^*=M4\pi m^* q k_B^2/h^3$).
Using the $m_{tun}$* values, m* for <100> Silicon is given by [26]

$$m^* = \sqrt{m^*_l m^*_t} \tag{21}$$

If the temperature dependence of $m_t$* is neglected, m* is calculated to be $0.417m_0$. K. Varahramyan et al. [14] proposed a unified model of specific contact resistance for the TFE and FE based on similarity between the functional forms of $\rho_c$ in the two different emission mechanisms as given by

$$\rho_c = \frac{k_B}{qA^*T}\underline{C}\exp(\frac{q\phi_b}{E_0}) \tag{22}$$

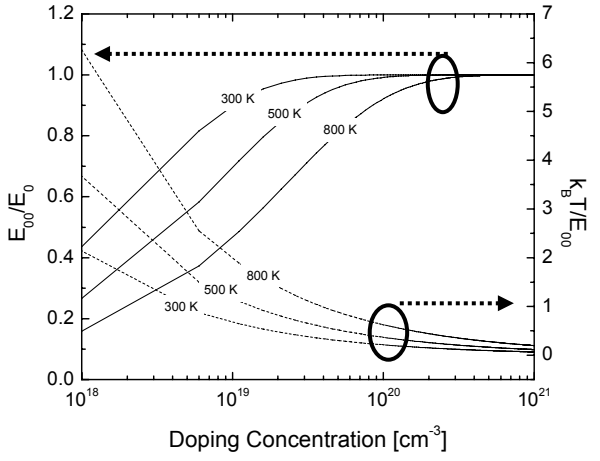


**Figure 2:** $E_{00}/E_0$ and $k_BT/E_{00}$ versus doping concentration. It shows that the relative importance of field emission (FE) with respect to the thermionic field emission (TFE) decreases as temperature increases for a given doping concentration.

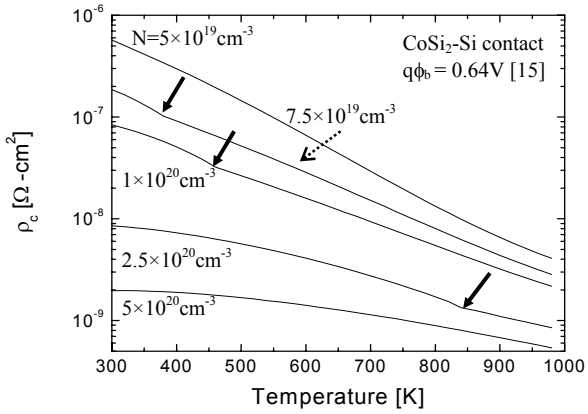


**Figure 3:** Theoretical curves for the specific contact resistance $\rho_c$ with temperature for $CoSi_2$-contact system for various background doping concentration. The thick arrows indicate that the carrier transport mechanism changes from the FE to the TFE as temperature increases.

where $\underline{C}$ = 0.425 for n-type silicon and $\underline{C}$ = 0.335 for p-type silicon, for a wide range of doping concentration ($10^{16}$ cm$^{-3}$ ≤ N ≤ $10^{21}$ cm$^{-3}$).

Although the proposed model is valid at room temperature, it starts to deviate from the FE or the TFE models as temperature increases. Since several primary physical parameters in the specific contact resistance model are strong functions of temperature, the average value of $\underline{C}$ is no longer constant with variations of temperature.

Fig. 2 clearly shows that the dominant carrier transport mechanism changes strongly depending on the temperature for a given doping concentration. Furthermore, it also implies that for analysis of device behavior at high temperatures the thermionic field emission process should be accounted for even in highly doped regions.

In order to demonstrate the proposed temperature dependent contact resistance model, a $CoSi_2$ process is considered since $CoSi_2$ is currently being employed in place of $TiSi_2$ for advanced CMOS technologies. Also, it does not suffer significantly from linewidth effects. At room temperature, the barrier height ($q\phi_b$) of $CoSi_2$/N-type Silicon is reported to be 0.64 eV [15].

For doping concentrations ranging from $5\times10^{19}$ to $5\times10^{20}$ cm$^{-3}$, which are practical values of interest for advanced technologies, theoretical $\rho_c$ curves are created as shown in Fig. 3. As can be seen, the specific contact resistance dramatically decreases with increase in temperature depending on the doping concentration. This is consistent with experimental data reported in [4].

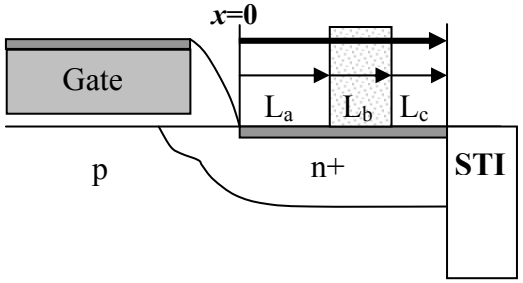


**Figure 4:** Schematic of the contact structure of a MOS transistor for analyzing impact of the temperature dependent $\rho_c$ on current localization effects where $L_a$ is the distance from the spacer edge to contact hole, $L_b$ is the width of the contact hole and $L_c$ is the distance from the edge of the contact hole to the STI boundary.

For instance, the $\rho_c$ of $5\times10^{19}$ cm$^{-3}$ at about 1000 K is almost the same as that of $2.5\times10^{20}$ cm$^{-3}$ at about 300 K. For the temperature range from 300 K to 1000 K, the specific contact resistance is reduced by at least a factor of 10. In addition, it is shown that the carrier transport mechanism changes from the FE to the TFE with increase in temperature as indicated by the thick arrows.

Since the theoretical $\rho_c(T)$ shows a considerable dependence on temperature, it is also important to understand its impact on ESD performance. Therefore, in the next section, using the derived contact resistance model, implication of high-current behavior on ESD reliability is discussed in terms of the temperature dependent current localization effects.

## IMPLICATIONS ON ESD RELIABILITY

In order to investigate the implications of high-current effects in silicided contact structures on ESD reliability, the derived temperature dependent specific contact resistance model is applied to the structure shown in Fig. 4. The basic idea of this work is to examine how severe the current localization effect is with increased temperature arising from ESD stress.

To investigate the impact of temperature dependence of contact resistance on ESD current distribution, a *1-D* contact resistance model [10] is applied. In the *1-D* model the thickness of silicide is assumed to be effectively zero. For advanced devices, the parameters $L_a$, $L_b$ and $L_c$ associated with the source/drain contact structure are generally comparable in the submicron regime. Therefore, from the 1-*D* transmission line model, the total contact resistance $R_T$ including $L_a$, $L_b$ and $L_c$ can be expressed as,

$$R_T = \frac{\rho_s \rho_d}{\rho_s + \rho_d}\frac{L_a}{W} + R_C \tag{23}$$

where

$$R_C = \frac{\frac{\rho_d^{\,2}}{\rho_s \beta W}\sinh\beta L_a + \frac{R'_C\,\rho_d}{\rho_d+\rho_s}\left(2+\frac{\rho_s^{\,2}+\rho_d^{\,2}}{\rho_s\rho_d}\cosh\beta L_a\right)}{\frac{\rho_s+\rho_d}{\rho_s}\cosh\beta L_a + \frac{R'_C}{\rho_s}\beta W\sinh\beta L_a} \tag{24}$$

$$R'_C = \frac{\rho_d}{\alpha W}\frac{\cosh\alpha L_b + \frac{\rho_d}{\rho_s+\rho_d}\frac{\beta}{\alpha}\tanh\beta L_c \sinh\alpha L_b}{\sinh\alpha L_b + \frac{\rho_d}{\rho_s+\rho_d}\frac{\beta}{\alpha}\tanh\beta L_c\cosh\alpha L_b} \tag{25}$$

$\rho_d$ is the sheet resistivity of the diffusion, $\rho_s$ is the sheet resistivity of the silicide diffusion, W is the diffusion width. Also, the parameters α and β are given by $(\rho_d/\rho_s)^{1/2}$ and $[(\rho_d+\rho_s)/\rho_c]^{1/2}$, respectively.

In Eq. (23), the first term is the geometrical line resistance and the second term is the contact resistance. Since the sheet resistivity of the silicide diffusion $\rho_s$ is negligible compared with the sheet resistivity of the diffusion $\rho_d$, for this analysis, it has been assumed that $\rho_s \approx 0\ \Omega/\square$. Although, to be more precise, the high-current conduction effects in the silicide films must be taken into account [28]. Therefore, the total resistance is approximated to be the same as the contact resistance $R_c$ itself [in Eq. (24)]. Also, the temperature dependence of $\rho_d$ is much less significant than that of $\rho_c$; for simplicity in this work $\rho_d$ is considered to be constant with temperature. However, for increased accuracy, it is recommended to account for the temperature dependence of $\rho_d$, which can be realized in terms of the temperature dependence of silicon bulk mobility [25, 29]. When $\rho_s$ is negligible, another important parameter of the silicided contact system is the transfer contact length $L_T$, which is given by

$$L_T = \sqrt{\rho_c / \rho_d} \tag{26}$$

The contact transfer length $L_T$ characterizes the distance over which the current moves from the silicide into the diffusion. It simply means that the contact resistance abruptly increases if $L_a << L_T$. Therefore, for previous technologies, $L_a$ was designed to be much longer than $L_T$. For advanced technologies, using the $\rho_c$ at room temperature (~ $10^{-6}$ to ~$10^{-9}$ Ω–cm$^2$) in Fig. 3, however, $L_T$ is estimated to be a few tens of nanometers to ~ 1 μm. These values are roughly comparable to the values of $L_a$, $L_b$, and $L_c$ and thus it can be expected that the current distribution in the silicide contact system is strongly influenced by such design parameters [13].

From Eq. (26), as temperature increases, the contact transfer length $L_T$ decreases through reduction in the specific contact resistivity $\rho_c(T)$. This implies that under high current conditions, the current distribution becomes more localized beneath the silicide/silicon contact system since device can be heated up due to the self-heating. Therefore, it can be inferred that at high temperature, the current can be more localized resulting in early thermal failure.

Using the derived temperature dependent $\rho_c$, the current crowding effect has been investigated. According to the 1-*D* transmission line model for contact resistance, the position ($x$) dependent fraction of current in the diffusion $I_D(x)/I$ for each segmented region can be obtained [10].

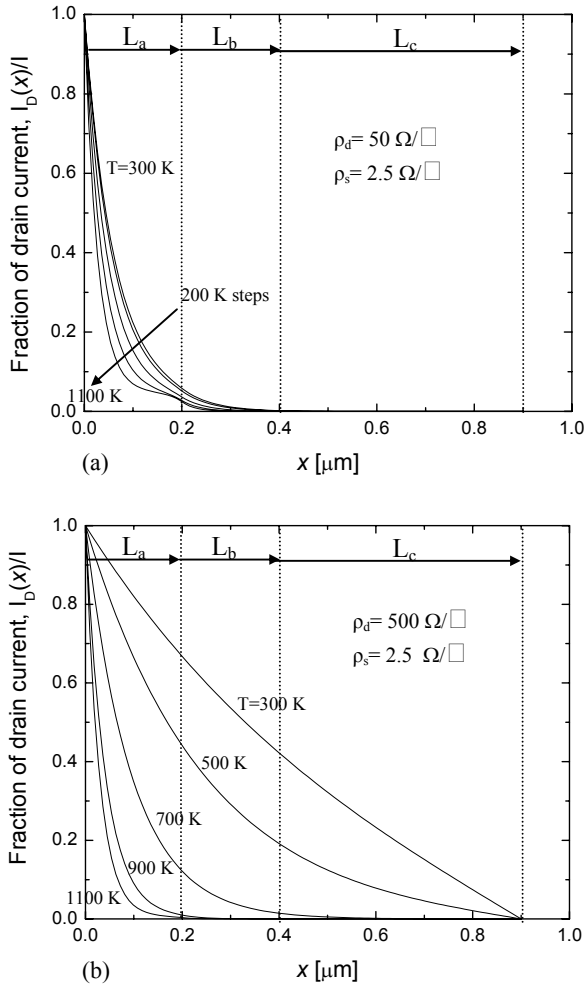


**Figure 5:** Fraction of the drain current as a function of the position from the edge of the spacer $x$ (as in Fig. 4) where $L_a$=0.2 μm, $L_b$=0.2 μm, $L_c$=0.5 μm and W=1 μm. (a) highly doped source/drain ($\rho_d$=50Ω/□) and (b) moderately doped source/drain ($\rho_d$=500 Ω/□).

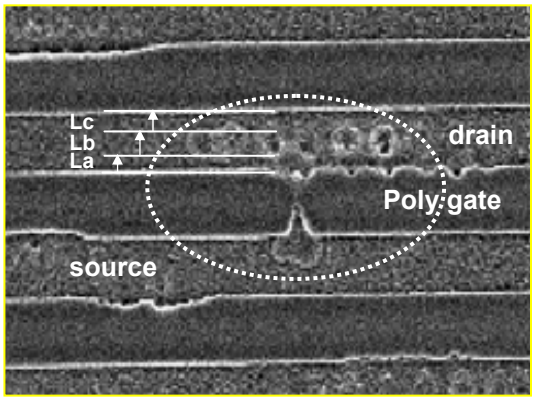


**Figure 6:** Damage site of a MOS transistor with NiSi diffusion. Due to high current induced heating effect, the device thermally failed. In particular, the damage sites can be observed in the regions of $L_a$ and $L_b$ implying severe current localization there.

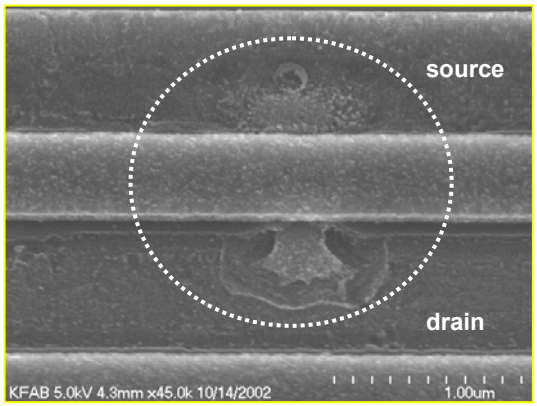


**Figure 7:** Failure sites for a multifinger device. It shows the symmetrical melt filament in the source/drain side, which is very typical for silicided devices.

Since temperature dependencies of other parameters except $\rho_c$ are ignored, thermal effects on the current distribution can be seen directly from thermal behavior of $\rho_c$. Fig. 5 clearly shows how current distribution under the silicide contact is affected by temperature, depending on the sheet resistivity of the source/drain diffusion. Compared to the current distribution at room temperature, the current is severely localized with temperature since most of the current flows in the region of $L_a$ with increased temperature. Also, the impact of temperature is more prominent for the case of the higher sheet resistivity of the source/drain diffusion [Fig. 5 (b)]. This implies that effective volume for power dissipation for a given current stress (i.e., ESD current stress) is dramatically reduced as temperature increases. As a result of reduced power dissipation volume, temperature increases more rapidly, resulting in thermal failures.

Furthermore, it implies that devices with silicide diffusion could fail thermally at much lower current levels than predicted when ignoring thermal effects because the temperature dependence of the current localization through the reduction in $\rho_c$ is severe which in turn causes enhanced heating near the edge of silicided contact (i.e., near the spacer edge).

The damage site of silicided (NiSi) device under high current stress is shown in Fig. 6. The parameters $L_a$, $L_b$ and $L_c$ are indicated with the failure picture. It can be clearly observed that due to the localized heating effect the contact holes in the drain side and drain/source junction were damaged, leading to filaments mainly towards the source. As can be seen, all of the heating takes place in $L_a$ and $L_b$ but not in $L_c$. Therefore, the most damage sites are found within the regions $L_a$ and $L_b$, and which implies that under ESD conditions current flow becomes more concentrated underneath the region $L_a$ and $L_b$ with temperature rise.

However, when the stress level is further increased the filament could form symmetrically at both drain and source side. This is also observed for a multifinger structure as shown in Fig. 7. These symmetrical melt filaments are well known for silicided devices [30]. Using the proposed contact resistance model, this symmetrical behavior can also be predicted since under ESD conditions the current density is highest at the gate edges on both the source and drain sides due to the decrease in contact resistance, which in turn leads to the symmetrical heating within the region $L_a$.

As briefly mentioned earlier, the temperature dependent silicide contact resistance behavior is difficult to be reproduced with device simulation. Though it is not accurate enough, using the device simulation it can be demonstrated that the current flow under silicided contact system is a strong function of temperature.

Using the device simulator *MEDICI* [31], the silicide/silicon structure has been replicated as a heterojunction structure. In order to simply represent the property of silicide ($CoSi_2$), the major material parameters such as electron affinity and effective density of states are adjusted. As a result, the barrier height becomes 0.64eV and the Fermi level in silicide region aligns to the edge of conduction band as can be seen from the band diagram at equilibrium in Fig. 8. Since the silicide region is imitated with a semiconductor, the ideal metal cannot be made and small band bending occurs in the silicide region. In the simulation, the doping concentration of silicon region is $1\times10^{20}$ $cm^{-3}$ and the thickness of silicide and the depth of silicon are set to 10 nm and 30 nm, respectively.

Thermionic emission current and tunneling current can be considered in simulation [32]. However, it still has a limitation, that is, tunneling current from *n*+ silicon region to silicide is neglected in the simulation since built-in electric field in the potential barrier is not accelerating field for the electron from *n*+ region [31]. In Fig. 9, I-V characteristics for the composed structure are shown. In this simulation, the anode ($CoSi_2$) voltage is higher than that of n+ silicon region, therefore electrons are emitted from *n*+ silicon to silicide, which is the general case in drain contact of NMOS transistor. Though thermal effect has been observed from the simulation, it seems that despite the proper parameter adjustment, the simulation mainly reflects thermionic emission carrier transport mechanism, which is dominant current component for Schottky diode, and tunneling is not counted by the reason mentioned above. It further implies that to some extent, device simulator still have a constraint for predicting thermal effect involved in the field emission process and the thermionic field emission process. Therefore, accurate modeling of the resistance of silicide/silicon contact system should be done and in turn, it needs to be implemented in device simulators for building an accurate comprehension of silicided contact behavior, which is significant for ESD performance of advanced VLSI devices.

## CONCLUSIONS

Based on refinement of established analysis, a temperature dependent specific contact resistance model has been presented. The theoretically based temperature-dependent contact resistance model can generate silicide contact resistance values at high temperature and it is capable of predicting the high-current behavior of silicided deep submicron devices, which is useful for the analysis of ESD reliability.

It is shown that the specific contact resistance for $CoSi_2$-Silicon dramatically decreases with increased temperature depending on the doping concentration level in the diffusion, in agreement with previous experimental work. Also, it is shown that variation of the specific contact resistance values have significant implications for ESD reliability through localized heating due to current crowding effects, since the effective volume for power dissipation is reduced with the extent of the current localization under the source/drain area for a given ESD stress.

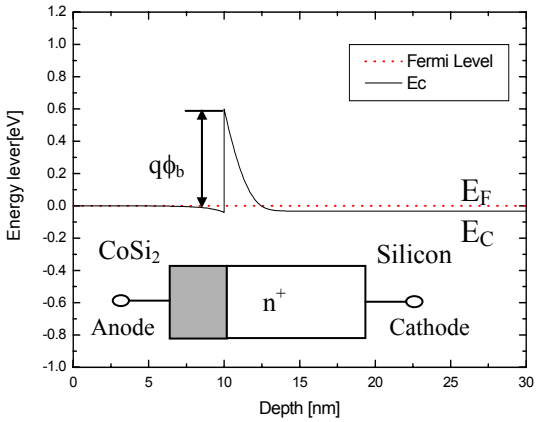


**Figure 8:** Band diagram for the $CoSi_2$/silicon structure using a heterojunction in *MEDICI*. Electron affinity and effective density of states in the semiconductor region are adjusted for representing the property of $CoSi_2$.

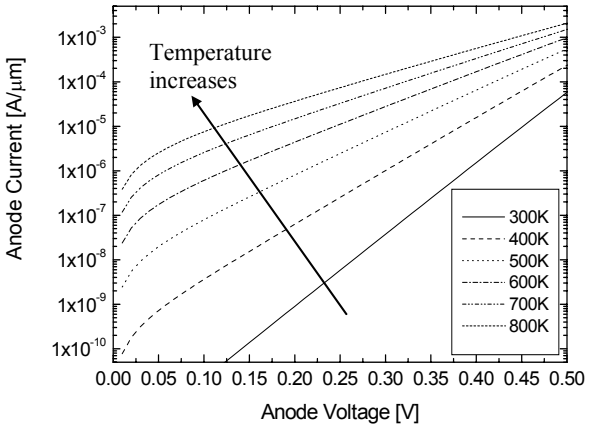


**Figure 9:** Current-Voltage characteristics for the $CoSi_2$/silicon structure using a heterojunction in *MEDICI*. However, it only shows Schottky barrier characteristics governed by thermionic emission.

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