Capacitance Reconstruction from Measured *C–V* in High Leakage, Nitride/Oxide MOS

Chang-Hoon Choi, *Student Member, IEEE*, Yider Wu, *Member, IEEE*, Jung-Suk Goo, *Student Member, IEEE*, Zhiping Yu, *Senior Member, IEEE*, and Robert W. Dutton, *Fellow, IEEE*

***Abstract*—A reconstruction technique of the gate capacitance from anomalous capacitance-voltage (*C–V*) curves in high leakage dielectric MOSFETs is presented. An RC network is used to accommodate the distributed nature of MOSFETs and an optimization technique is applied to extract the intrinsic gate capacitance. Applicability of the method is demonstrated for ultra-thin nitride/oxide (N/O $\sim$ 1.4 nm/0.7 nm) composite dielectric MOSFETs.**

***Index Terms*—Composite nitride/oxide gate dielectrics, C–V reconstruction, MOSFETs, tunneling.**

I. Introduction

ACCORDING to the latest CMOS technology roadmap (November 1999) by the Semiconductor Industry Association (SIA), CMOS with the gate lengths of 50 to 70 nm will need an oxide thickness of around 1.5 to 2.0 nm as early as 2001 [1]. With such thin oxide layers, direct tunneling results in an exponential increase in gate leakage current such that the series resistance in MOS capacitors becomes significant owing to the low impedance of the capacitor [2]. As a result, experimental capacitance–voltage (*C–V*) curves for ultrathin gate MOS devices show capacitance attenuation, both in the inversion and accumulation regions [3] and determination of an effective oxide thickness from the measured *C–V* curves has become problematic. Although recent studies have reported that the degradation of gate capacitance in MOSFETs can be suppressed by utilizing short channel lengths [4], this requires redesign of test patterns and more importantly, it may be difficult to extract pure, intrinsic gate capacitances due to the various parasitic effects in short channel devices. Since *C–V* measurement is a fundamental technique for MOSFET characterization and *C–V* curves are crucial in providing device information, a reconstruction technique of gate capacitance from measured *C–V* curves is needed for ultrathin gate dielectric MOSFETs.

This paper presents an extraction technique, using distorted *C–V* curves for high leakage gate dielectric MOSFETs, based on a distributed RC network approach. Modeling of gate capacitance and tunneling current along with validation of the distribute RC approach for ultrathin gate oxide MOSFETs, are described in Section II. The *C–V* reconstruction technique, based on measured *C–V* curves and its application to very thin nitride/oxide gate dielectric MOSFETs are discussed in Section III. Finally, conclusions are presented in Section IV.

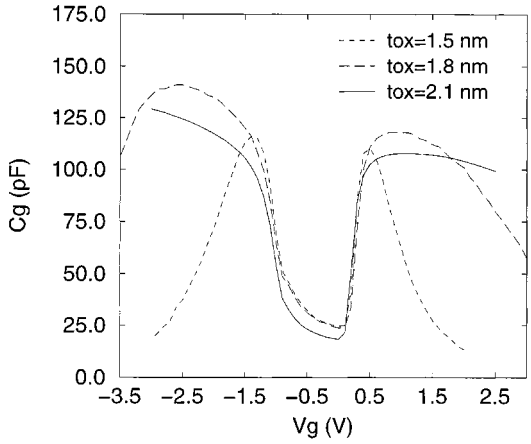


Fig. 1. Experimental *C–V* curves for thin gate oxide (t_{ox} = 1.5, 1.8, and 2.1 nm) n-MOSFETs.

II. Gate Capacitance Modeling

A. Anomalous C–V Behavior in Thin-Oxide MOS

Fig. 1 shows experimental *C–V* curves for gate oxide thicknesses of 1.5, 1.8, and 2.1 nm n-MOSFETs with an area of 100 μm $\times$100 μm, which were measured by the LCR capacitance meter using the RC parallel mode at a frequency of 100 kHz. Thickness extraction of the oxides was initially conducted using ellipsometry to a 122 Å oxide standard; high resolution TEM was then used to correct the shift between ellipsometry and TEM. In this figure, sharp decreases of gate capacitance appear for the oxide thicknesses of 1.5 and 1.8 nm, which is related to gate current and series resistance associated with the equivalent circuit in *C–V* measurement systems.

Fig. 2(a) shows the RC parallel circuit model of the LCR capacitance meters. G_m and C_m are the measured conductance and capacitance, respectively, which are determined from a single measurement of magnitude and impedance phase. Because this circuit model neglects the series resistance (R_s) associated with the bulk and contacts, it is most suitable for low series resistance devices. By contrast, a circuit model that more closely represents the real devices, including R_s, is shown in Fig. 2(b). G_t and C_t represent the tunneling conductance and

Manuscript received April 25, 2000. This work was supported by NSF under the Distributed Center for Advanced Electronics Simulations (DesCArtES). The review of this paper was arranged by Editor M. Lundstrom.

C.-H. Choi, J.-S. Goo, Z. Yu, and R. W. Dutton are with the Center for Integrated Systems, Stanford University, Stanford, CA 94305 USA (e-mail: chchoi@stanford.edu).

Y. Wu is with Advanced Micro Devices, Inc., Sunnyvale, CA 94088 USA.

Publisher Item Identifier S 0018-9383(00)07781-9.

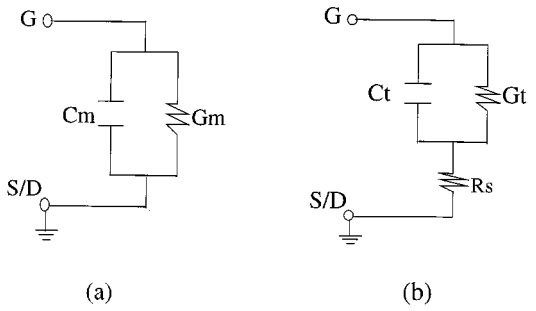


Fig. 2. Small-signal equivalent MOS capacitor models. (a) Single RC parallel circuit model of the measurement systems (LCR meters). (b) More accurate circuit model including series resistance (R_s).

the true, intrinsic capacitance, respectively. The relationship between C_m and C_t is expressed as [5]

$$C_m = \frac{C_t}{(G_t R_s + 1)^2 + \omega^2 C_t^2 R_s^2}. \tag{1}$$

Here, C_m and C_t are identical when R_s is very small, but the magnitude of C_m decreases to a value less than C_t when R_s increases.

In spite of these limitations, *C–V* measurements of thin oxides with large leakage currents are widely performed, often using the parallel RC circuit model in Fig. 2(a) [2]. The true capacitance (C_t) of the devices cannot be ascertained simply by the measurement of magnitude and impedance phase (i.e., G_m and C_m). Namely, when G_t becomes large, due to high leakage of thin dielectrics, R_s is amplified, leading to decreased capacitance (C_m) as the magnitude of gate bias increases [6]. As a result, determination of intrinsic gate capacitance and effective oxide thickness from *C–V* measurements becomes difficult in the presence of leaky, very-thin oxide MOSFETs.

B. Capacitance and Tunneling Current Models

For gate oxide thicknesses less than 3.0 nm, the oxide field reaches a maximum of 5 MV/cm such that the operation of deep-submicron MOSFETs enters a regime in which tunneling and charge confinement effects become noticeable. Classical inversion charge modeling is no longer sufficient for these device characteristics [7]. In the classical case, electron density has its maximum value at the Si–SiO_2 interface, while in the quantum mechanical case the electron density is diminished at the interface, increases to its maximum value and decreases with the distance from the silicon surface [8]. Hence, a quantum-mechanical (QM) model of the inversion charge profile peaks at around 10 Å below the silicon surface such that inversion charge is effectively reduced to that of an equivalent oxide which is a few angstroms thicker than the physical oxide. For the modeling of gate characteristics an empirical and hybrid model for the QM correction in MOS structures is proposed and implemented in a two-dimensional (2-D) device simulator, which combines both the van Dort [9] and Hansch models [10].

In order to model the carrier confinement, the density of conduction band states in the vicinity of the Si/SiO_2 interface is expressed as

$$N_C(z) = N_C \left[1 - e^{-(z+z_0)^2/\lambda_{th}^2}\right] \tag{2}$$

where N_C is the normal density of conduction band states, which is position-independent, and λ_{th} is a thermal wavelength determined by the carrier effective mass. The z-axis is perpendicular to the Si–SiO_2 interface and z_0 is introduced for the finite carrier concentration at the surface ($z = 0$).

The van Dort model employs bandgap broadening in the surface channel region to capture the dominant QM effects. The original form was proposed for the inversion region only. As a result, a singularity in the simulated *C–V* at the flatband voltage region was not carefully considered. While the QM effect is not a concern in this region, the discontinuous behavior of the model greatly limits its applications and causes numerical instabilities in multidimension device simulations. To eliminate the flatband singularity of the van Dort model, an alternative bandgap broadening expression is used in this work. The bandgap correction term with a 2/3 power-law dependence of the transverse surface electric field, F_S, was implemented in the van Dort model formalism as follows:

$$\Delta E_g(z) = \frac{\kappa\beta}{2k_B T} F_S^{2/3} \left[\frac{2e^{(z/L)^2}}{1 + e^{-2(z/L)^2}}\right] \tag{3}$$

where

β physical constant (see [9]);
κ fitting parameter with theoretical value of unity;
L characteristic decay length.

The singularity originates from the derivative of this quantity with respect to $F_S = 0$ in the gate capacitance computation. To eliminate the flatband singularity, the $F_S^{2/3}$ term in (3) is replaced with

$$(F_S^{2/3} \rightarrow) \frac{F_S^2}{a e^{-(F_S/\sigma)^2} + F_S^{4/3}} \tag{4}$$

where both a and σ are adjustable parameters. This expression preserves the asymptotic dependence of the bandgap correction on $F_S^{2/3}$ when $F_S \rightarrow \pm\infty$ while eliminating the flatband singularity.

Fig. 3 shows the comparison between experimentally measured and simulated *C–V* curves for 1.5- and 2.1-nm oxide n-MOSFET's with an area of $100\ \mu\text{m} \times 100\ \mu\text{m}$. For this analysis, the substrate doping profile is obtained using a process simulation that includes TED (transient enhanced diffusion) effects [11]. The *C–V* curve obtained by utilizing the QM-corrected behavior, based on device simulation, shows good agreement with experimental data for $t_{ox} = 2.1$ nm, as in Fig. 3(a). The reduction of gate capacitance in the accumulation region is related to the QM effect; the reduction in the inversion region is related to both the QM and poly depletion effects. However, as shown in Fig. 3(b), the simulation model cannot predict the characteristics of $t_{ox} = 1.5$ nm; discrepancies in the deep inversion and accumulation regions can be attributed to neglecting gate tunneling current effects. To model the anomalous *C–V* behavior for gate oxides thinner than 2.0 nm, tunneling current effects should be incorporated along with the QM capacitance model.

In this work, the tunneling current is calculated using a one-dimensional (1-D) Green's function simulator, NEMO [12], which is a Schrödinger equation solver. NEMO considers the injection from both quasibound states and continuum states;

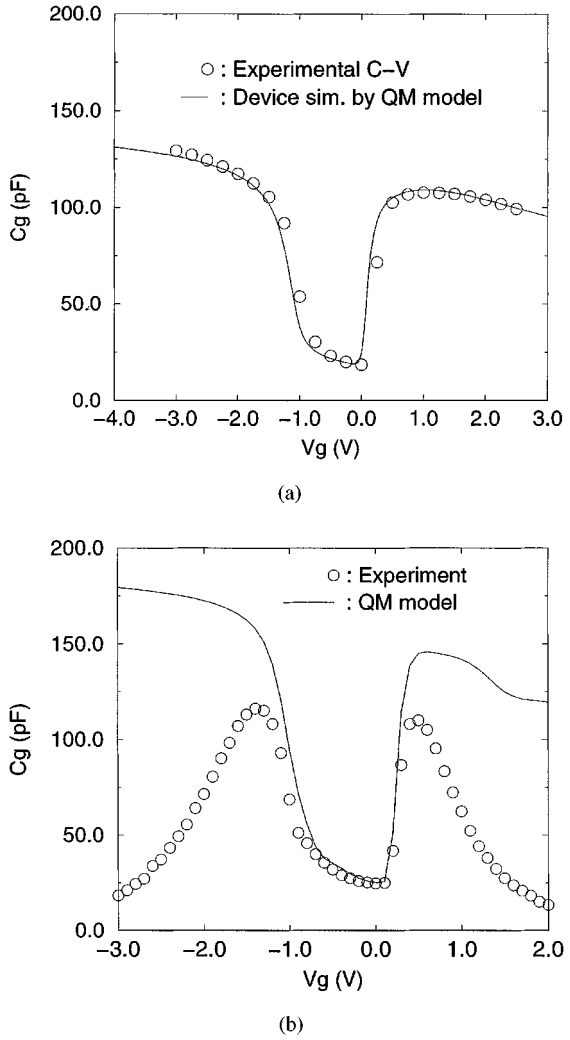


Fig. 3. Simulated and experimental *C–V* curves for n-MOSFET with t_{ox} = 1.5 and 2.1 nm, circles denote measurements and lines indicate QM device simulation results. (a) t_{ox} = 2.1 nm. (b) t_{ox} = 1.5 nm. Note that QM capacitance modeling without considering gate current cannot predict the distorted *C–V* curve for $t_{ox} < 2.0$ nm.

the carrier density is calculated quantum mechanically in the device. NEMO also considers multiple-scattering effects which are important for very thin SiO_2 layers [13]. Fig. 4 shows measured and simulated gate tunneling currents for three different gate oxide thicknesses—1.3, 1.5, and 1.8 nm. The substrate doping profile obtained from a calibrated process simulation was used; oxide thickness was the variable parameter (1.3 to 1.8 nm). However, these oxide thickness values were about 0.5 Å, greater than that of the measured values due to effects of vanishing electron wavefunctions at the oxide interface and the displacement of the electron peak toward the bulk which is common in quantum simulations [14]. The discrepancies between the measured and simulated current–voltages (*I–V*'s) are probably caused by surface roughness and uncertainty in determining the effective oxide thickness.

C. Equivalent Circuit Modeling

In order to model the decrease of gate capacitance in ultrathin gate MOS transistors, an equivalent RC network is used.

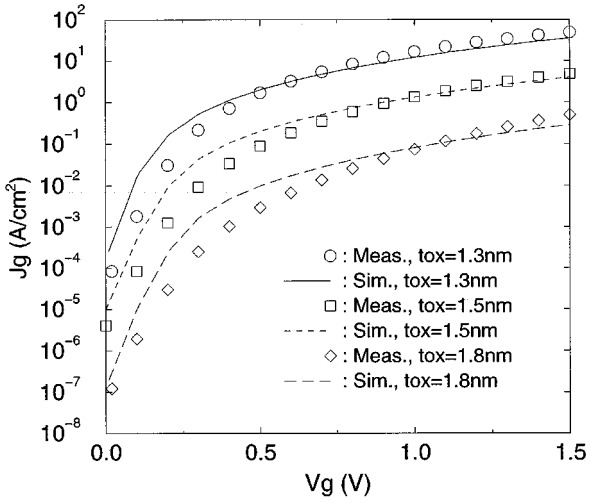


Fig. 4. Measured gate tunneling currents (*I–V*) compared to simulations using 1-D Green's function solver for t_{ox} = 1.3, 1.5, and 1.8 nm, respectively.

To model gate tunneling currents considering parasitic resistance, the silicon surface region is divided into small rectangular segments perpendicular to the channel-current flow in order to consider the series resistance (R_s), as shown in Fig. 5(a). The poly-Si area is vertically divided into small segments to reflect the polysilicon resistance effects (R_g). Typical sheet resistance of the polysilicon (R_g) is 4 to 5 $\Omega/\square$, which is much smaller than the series resistance ($R_s \sim$ 0.1–1 K$\Omega/\square$). Fig. 5(b) shows the equivalent circuit for the single vertical segment represented in Fig. 5(a). The equivalent circuit for the whole device structure is constructed by incorporating all the vertical segments. The tunneling current is modeled using a nonlinear, voltage-controlled current source ($i_g(V_g)$) derived from the gate current simulation discussed previously. The magnitude of current in each segment is then scaled according to the number of RC stages used. Also, the gate capacitance without the gate tunneling effects (or capacitance attenuation) is modeled using a nonlinear, voltage-controlled capacitance ($C_i(V_g)$). SPICE ac small-signal analysis is then performed to find the input admittance ($Y_{\text{in}} = G + j\omega C$) of the circuit at the given frequency (i.e., 100 kHz). The *C–V* data including gate tunneling effects is finally obtained by taking the imaginary component of Y_{in} (i.e., $C = \text{Im}(Y_{\text{in}})/\omega$).

Fig. 6 shows modeling results compared to the measurements for oxide thicknesses of 1.3, 1.5, and 1.8 nm, when the number of RC segments is 20. The sharp transition point in capacitance becomes lower as gate oxide thickness is reduced, which results from the increase in gate tunneling current with an exponential-like dependence between tunneling current and oxide thickness.

Contrary to the general concerns, Momese *et al.* [15] have demonstrated that the direct tunneling gate current does not adversely affect the MOSFET drain current down to 1.5 nm gate oxide devices with gate lengths less than 1 μm. The behavior of gate tunneling current strongly depends on the drain bias effects on MOSFET operation, especially in short channel MOSFETs, because the drain field easily penetrates into the channel region close to the source areas in the short-channel devices

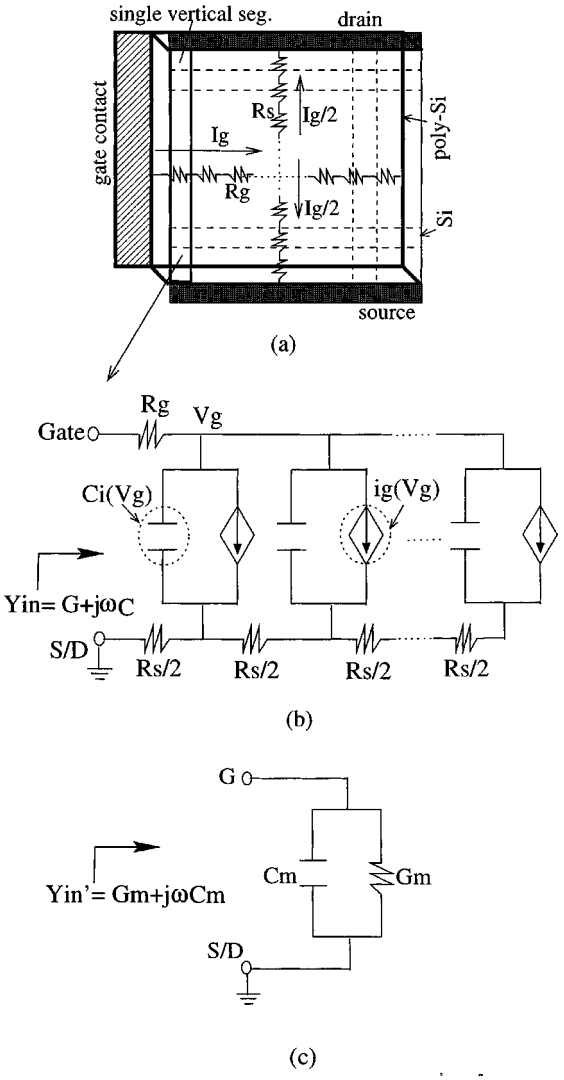


Fig. 5. Equivalent circuit approach for ultrathin gate oxide MOS with the source/drain grounded. (a) Top view of the MOS structure with gate current flows. (b) Distributed RC network used in this work. (c) RC circuit model used in capacitance measurements.

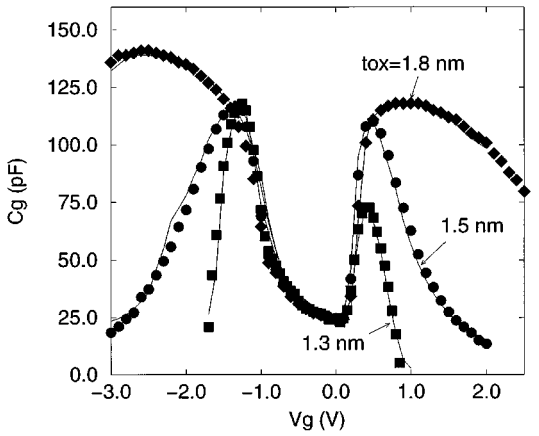


Fig. 6. Simulated anomalous C–V ($\mathrm{Im}(Y_{\mathrm{in}})$) curves obtained from the network analysis for the equivalent circuit (lines), symbols represent measured C–V's for $t_{ox} = 1.3$, 1.5, and 1.8 nm.

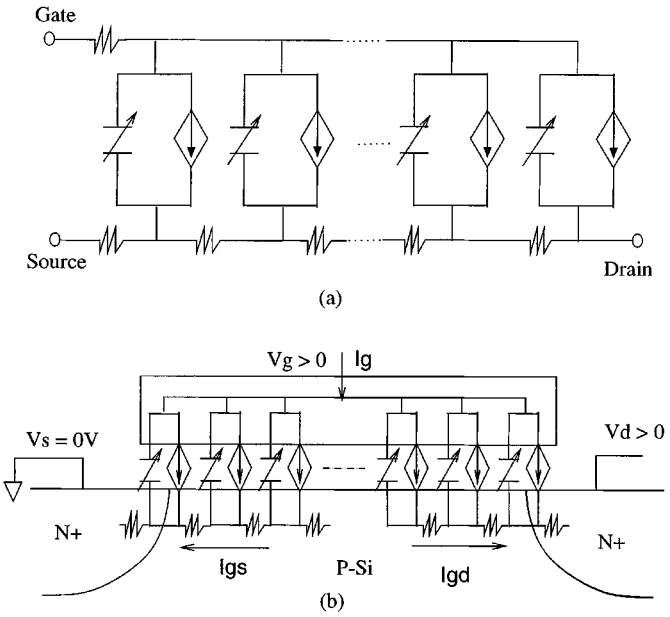
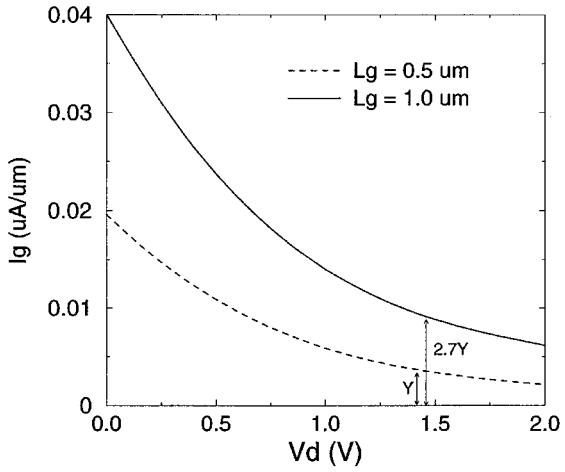


Fig. 7. Modeling of gate tunneling current considering the drain bias effects. (a) Equivalent circuit for n-MOSFETs when the drain bias is given. (b) Gate tunneling current ($I_g = I_{gs} + I_{gd}$).

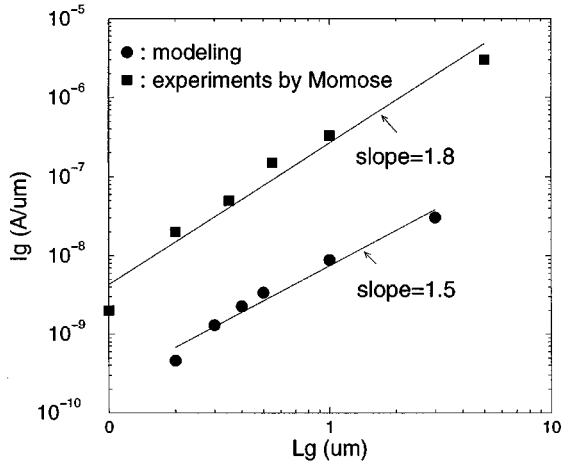
(i.e., drain-induced barrier lowering or DIBL). Gate tunneling current with respect to the drain bias (i.e., $V_d > 0$ V) is modeled using the equivalent circuit, as shown in Fig. 7. Here, the channel length dependence of the gate tunneling current (I_g) considering the short channel effects can be estimated due to the distributed channel resistance [16]. As a result, the simulated gate tunneling current is shown to decrease as the drain bias increases since the potential difference between the gate and the Si surface becomes smaller, as shown in Fig. 8(a). In addition, effects of gate tunneling current on the drain current become less serious as the channel length is reduced, owing to the exponentially decreasing gate current. Fig. 8(b) shows the simulated gate-channel dependence of I_g; I_g decreases in inverse proportion to $L_g^{1.5}$, which is comparable to the experiments by Momose *et al.* [15], [17], where the slopes were 1.8 and 1.5, respectively.

III. *C–V* Reconstruction Model

Recently, alternate insulating materials with a dielectric constant much larger than that of SiO_2 are under evaluation to replace the conventional SiO_2 gate dielectrics and thereby overcome gate tunneling problems [18]. In particular, nitride/oxide (N/O) composite layer gate dielectrics have emerged as a promising alternative to SiO_2 in CMOS devices [19]. The composite N/O gate prevents boron diffusion from polysilicon gates during thermal dopant activation anneals. In addition, carrier mobility is enhanced because the ultrathin buffer oxide of the composite layer improves the interface quality at the Si substrate. More important, lower tunneling currents can be obtained compared to pure oxide gates, due to the increased physical film thickness associated with the higher dielectric constant of the nitride layer ($\epsilon_{nitride} \sim 7.8$). It was reported that 1.6-nm oxide equivalent N/O dielectric MOSFETs showed more than a 100-fold reduction in tunneling current compared with 1.6-nm single layer oxide devices [19]. However, even though tunneling current is much reduced in N/O composite MOSFETs compared to SiO_2 dielectrics, the $C - V$ curves of



(a)



(b)

Fig. 8. Drain bias and gate channel length dependence of gate tunneling current for t_{ox} =1.5 nm. (a) I_g versus V_{ds} for L_g = 0.5 and 1.0 μm when V_{gs} =1.5 V, note that I_g of L_g = 1.0 μm is more than twice than that of L_g = 0.5 μm. (b) Experimental [15] and modeled I_g with respect to L_g's at the saturation region (V_{gs} = V_{ds} =1.5 V).

very-thin N/O MOSFETs still show capacitance attenuation, a reconstruction technique of gate capacitance from the distorted *C–V* is necessary to predict device performance.

A. Previous Reconstruction Method

The *C–V* reconstruction technique in the previously reported literature [2] is efficient and useful for small-area MOS devices with low leakage current, where the *C–V* curve is reconstructed from a derived equation, consisting of measured capacitance and conductance values obtained at two different ac frequencies (e.g., f_1 = 50 kHz, f_2 = 100 kHz or f_1 = 100 kHz, f_2 = 1 MHz). However, since the technique treats a large-area MOS device as a single RC circuit [see Fig. 2(b)], it has potential problems for large area devices with higher leakage currents. In practice, the gate current and capacitance in long-channel devices is not uniform along the channel direction due to the distributed gate and series resistance effects; a single-lumped RC model is not an adequate circuit representation for large MOS devices.

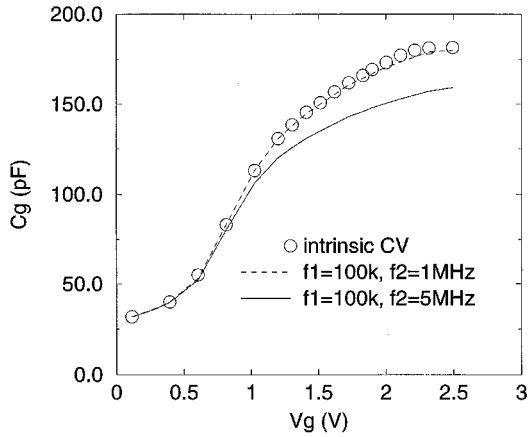


Fig. 9. Reconstructed *C–V* curves after the method in [2], circles represent the intrinsic *C–V*, and dotted and solid lines represent reconstructed *C–V*'s for the applied frequencies of 100 kHz–1 MHz and 100 kHz–5 MHz, respectively.

Also, choosing qualitatively dissimilar (measured) *C–V* curves may cause substantial error in the reconstruction process.

Fig. 9 shows simulated *C–V* curves for 100 μm $\times$100 μm p-MOSFETs after applying this method for reconstruction. Fairly large discrepancies are observed when reconstructing the *C–V* curve using (f_1 = 100 kHz, f_2 = 5 MHz). These *C–V* curves are qualitatively dissimilar because the frequency of 5 MHz is above the cutoff frequency (f_T) of the device, estimated to be [20]:

$$f_T = \frac{\mu_n (V_G - V_T)}{2\pi {L_g}^2} \simeq 1.5 \text{ MHz} \tag{5}$$

where L_g = 100 μm, V_G = 2 V, μ_n =600 cm^2/V$\cdot s$, and V_T = 0.4 V.

Thus, the single-lump RC small-signal model as in Fig. 2(b) is no longer accurate for the case of 5 MHz; the series resistance becomes significant due to the low impedance of capacitance at higher frequencies. On the other hand, a low frequency *C–V* measurement is not suitable for high leakage dielectric MOS capacitors since it causes considerable measurement error. The approximated instrumentation error for LCR meters is given as [6]

$$error(\%) = 0.1\sqrt{1 + \left(\frac{G_m}{2\pi f C_m}\right)^2} \tag{6}$$

where C_m and G_m are measured capacitance and conductance, respectively. For example, the instrumentation errors calculated using (6) are 12.7% and 1.2% for the applied frequency of 100 kHz and 1 MHz, respectively; the measured G_m and C_m are 1.0 mS and 13.4 pF for a 1.5-nm oxide thickness (n-MOSFET) at V_g =2.0 V. Hence, high frequency *C–V* measurements and the incorporation of a distributed RC model are desirable in modeling of large-area, high-leakage dielectric MOSFETs.

B. Optimization Technique

For capacitance reconstruction, the distributed RC network for high leakage dielectric MOSFETs [Fig. 5(b)] is used. The intrinsic gate capacitance, which is to be extracted, is modeled with a voltage-controlled capacitance ($C_i(V_g)$). The conductance is modeled using a voltage-controlled current source ($i_g(V_g)$), which has been determined based on measured gate current data.

Capacitance reconstruction consists of extraction of $C_i(V_g)$ from the distributed RC network such that the imaginary part and real part (C and G) of the simulated input admittance (Y_{in}) can be matched with the measured capacitance and measured conductance (C_m and G_m), shown in Fig. 5(b) and (c).

For the R_s extraction, sheet resistance (R_{sh}) of the device is calculated using conventional drift-diffusion theory of carrier transport [21]:

$$R_{sh}(x) = \frac{\frac{d}{dx}\phi_n(x)}{I_{ds}} \tag{7}$$

where x is the direction parallel to the Si surface and ϕ_n is the electron quasi-Fermi level obtained from 2-D device simulation. I_{ds} is independent of x due to current continuity; the sheet resistivity is simply proportional to the lateral gradient of $\phi_n(x)$. This expression is valid as long as the device is sufficiently wide and the current flow is dominantly parallel to the x-direction.

Using device simulation and (7), R_s was determined to be in the range between 60 and 70 Ω for a 100 μm $\times$100 μm P-MOSFET structure with a peak dopant concentration of 1.3×10^{18} cm^{-3}. R_g used in the extraction process was fixed at 5 $\Omega/\square$, which is a typical sheet resistance of the polysilicon gate.

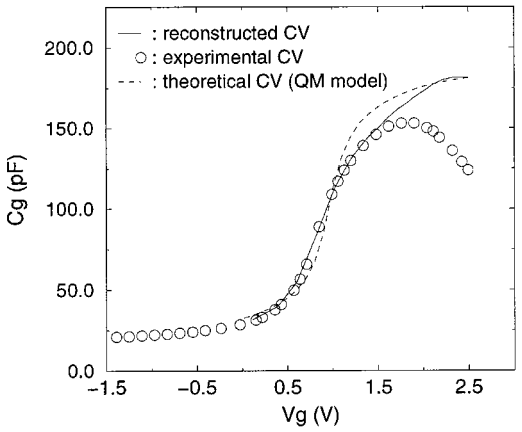
Given this set of parameters, the next step is to perform circuit optimization for the distributed RC network in order to extract the intrinsic capacitance ($C_i(V_g)$). A Levenberg–Marquadt algorithm implemented in HSPICE [22] is used which numerically combines the steepest-descent method with a Gauss–Newton approach to give the greatest stability for points far from the minimum while achieving rapid convergence for points near the minimum [23]. The quantity to be minimized is the norm of the error vector, $\boldsymbol{f}(\boldsymbol{p})$, given by

$$||\boldsymbol{f}(\boldsymbol{p})||^2 = \sum_k f_k(\boldsymbol{p})^2 = \sum_k \left[\frac{x_k(\boldsymbol{p}) - x_k^*}{\max(x_k^*, x_{\min})}\right]^2 \tag{8}$$

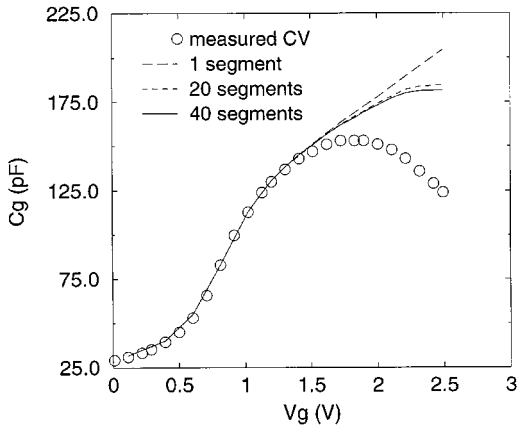
where $\boldsymbol{p}$ represents the vector of optimized parameters and the vector $\boldsymbol{f}(\boldsymbol{p})$ consists of the errors evaluated at each gate bias point. x_k and x_k^* are the calculated capacitance/conductance and measured capacitance/conductance, respectively, at the kth data point. For each iteration of the algorithm, the model is evaluated at each data point and the error vector $\boldsymbol{f}(\boldsymbol{p})$ is calculated; the parameter vector $\boldsymbol{p}$ is then adjusted to reduce $||\boldsymbol{f}(\boldsymbol{p})||^2$, the sum of the squares of the errors. For the $C_i(V_g)$ extraction, HSPICE ac small-signal analysis is performed, coupled with optimization to find the input admittance ($Y_{\text{in}} = G + j\omega C$) for the circuit.

C. Application Results

The N/O composite dielectric P-MOSFETs (N/O $\sim$ 1.4 nm/0.7 nm) with p$^+$-poly gates implanted by BF_2 (30 keV, 5×10^{15} cm^{-2}) were fabricated on 1.3×10^{18} cm^{-3} n-type Si $\langle 100 \rangle$ substrates. The bottom oxide layer was formed using N_2O remote-plasma oxide and the RPECVD nitride was then deposited using SiH_4 and N_2 as source gases to form the N/O structures. The nitride thickness is determined from the deposition rate and the oxide thickness was extracted using Auger electron spectroscopy [19]. *C–V* measurements for the nitride/oxide P-MOSFET (N/O $\sim$ 1.4 nm/0.7 nm) were performed using the RC parallel mode, as shown in Fig. 2(a). The device area is 100 μm $\times$100 μm and the applied small-signal frequency is 1 MHz. Measured *C–V* data are represented by circles in Fig. 10(a) and show a sharp decrease of the capacitance in the accumulation region for gate biases greater than 1.7 V. The solid line in the figure represents the reconstructed gate capacitance from the method described above. The reconstructed gate capacitance of the N/O composite MOS device in the deep accumulation region is 180.4 pF, which corresponds to the gate capacitance of an equivalent oxide thickness of 1.9 nm ($t_{ox,eq} = 1.9$ nm), assuming a classical charge model. Also, the capacitance corresponds to a gate capacitance with an equivalent oxide thickness of 1.4 nm ($t_{ox,eq-qm} = 1.4$ nm), assuming the QM model.



(a)



(b)

Fig. 10. *C–V* reconstruction results using the proposed technique. (a) measured (circles) and reconstructed (solid line) *C–V* curves by using the distributed RC network and optimization technique, dashed line indicates theoretical $C - V$ with QM device simulation. (b) comparison of extracted *C–V* curves with respect to the number of segments in the RC ladder network, circles denote the measured anomalous *C–V* and lines show the reconstructed intrinsic capacitance for the different number of segments—1, 20 and 40 segments.

Regarding validation of the reconstructed *C–V* curve, direct comparison with the experimentally reconstructed curves is the most desirable. For such a comparison, however, test structures

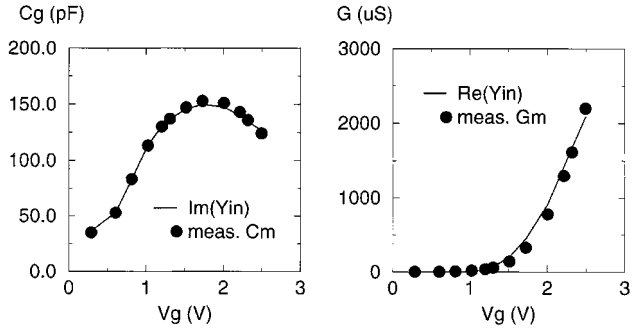


Fig. 11. Optimization results, measured C_m/G_m compared to final C/G ($\mathrm{Im}(Y_{\mathrm{in}})/\mathrm{Re}(Y_{\mathrm{in}})$) after the $C-V$ reconstruction.

with channel lengths of 1–10 μm are necessary to avoid capacitance attenuation, as reported in [4]. Instead, theoretical *C–V* calculations are used, where the QM model has been considered for N/O ($\sim$ 1.4 nm/0.7 nm) dielectric P-MOSFET. The objective of the theoretical calculation is to find a reasonable capacitance range for the layer thickness, not to produce a perfect fit. As a result, the reconstructed gate capacitance shows good correspondence to the theoretical one in deep accumulation, as shown in Fig. 10(a); discrepancies between the theoretical and reconstructed curves may be attributed to the uncertainties in the series resistance value and not having modeled interface state properties specifically [5].

Fig. 10(b) shows the reconstructed *C–V* curves with respect to the number of segments in the RC ladder network. The shape of the reconstructed *C–V* for a single segment case is unrealistic, while the reconstructed capacitance values in deep accumulation are almost identical for 20 and 40-segment cases compared to the theoretical calculations.

Fig. 11 shows comparison between the measured C_m/G_m and the simulated C/G ($=\mathrm{Im}(Y_{\mathbf{in}})/\mathrm{Re}(Y_{\mathbf{in}})$) when the final intrinsic capacitances have been extracted, the optimization error between the measured and the simulated capacitance/conductance is 2%.

IV. Conclusions

A reconstruction technique for *C–V* curves, based on distorted *C–V* curves in high leakage dielectric MOSFETs has been developed. Anomalous *C–V* behavior has been modeled using a distributed RC network to account for the QM effects as well as the distributed RC nature of MOSFETs; the intrinsic, pure gate capacitance is conversely extracted from the anomalous measured *C–V* curves. The reconstructed $C-V$ data is comparable to the theoretical QM calculations for very-thin nitride/oxide gate dielectric ($t_{ox,eq-qm} \sim$ 1.4 nm) MOSFETs.

References

[1] E. J. Lerner, "The end of the road for Moore's law," *IBM J. Res. Develop.*, pp. 6–11, 1999.
[2] K. J. Yang and C. Hu, "MOS capacitance measurements for high-leakage thin dielectrics," *IEEE Trans. Electron Devices*, vol. 46, pp. 1500–1501, July 1999.
[3] C.-H. Choi *et al.*, "MOS $C-V$ characterization of ultra-thin gate oxide thickness (1.3–1.8 nm)," *IEEE Electron Device Lett.*, vol. 20, pp. 292–294, June 1999.
[4] K. Ahmed *et al.*, "Impact of tunnel currents and channel resistance on the characterization of channel inversion layer charge and polysilicon-gate depletion of sub-20-Å gate oxide MOSFET's," *IEEE Trans. Electron Devices*, vol. 46, pp. 1650–1655, Aug. 1999.
[5] E. M. Vogel, W. K. Henson, C. A. Richter, and J. S. Suehle, "Limitations of Conductance to the measurement of the interface state density of MOS capacitors with tunneling gate dielectrics," *IEEE Trans. Electron Devices*, vol. 47, pp. 601–608, Mar. 2000.
[6] W. K. Henson *et al.*, "Estimating oxide thickness of tunnel oxides down to 1.4 nm using conventional capacitance-voltage measurements on MOS capacitors," *IEEE Electron Device Lett.*, vol. 20, pp. 179–181, Apr. 1999.
[7] S. H. Lo *et al.*, "Modeling and characterization of n^+ and p^+ polysilicon-gated ultra thin oxides (21–26 Å)," in *Proc. Symp. VLSI Technol.*, 1997, pp. 149–150.
[8] N. D. Arora, *MOSFET Model for VLSI Circuit Simulation*. Berlin, Germany: Springer-Verlag, 1993.
[9] M. J. van Dort, P. H. Woerlee, and A. J. Walker, "A simple model for quantization effects in heavily-doped silicon MOSFET's at inversion conditions," *Solid-State Electron.*, vol. 37, p. 411, 1994.
[10] W. Hänsch, T. Vogelsang, R. Kircher, and M. Orlowski, "Carrier transport near the Si/SiO_2 interface of a MOSFET," *Solid-State Electron.*, vol. 32, p. 839, 1989.
[11] P. Vande Voorde *et al.*, "Accurate doping profile determination using TED/QM models extensible to sub-quarter micron nMOSFETs," in *IEDM Tech. Dig.*, 1996, p. 811.
[12] C. Bowen *et al.*, "Physical oxide thickness extraction and verification using quantum mechanical simulation," in *IEDM Tech. Dig.*, 1997, pp. 869–872.
[13] S. Nagano, M. Tsukiji, E. Hasegawa, and A. Ishitani, "Mechanism of leakage current through the nano-scale SiO_2 layer," *J. Appl. Phys.*, vol. 75, p. 3530, 1994.
[14] C. S. Rafferty *et al.*, "Multi-dimensional quantum effect simulation using a density-gradient model and script-level programming techniques," in *Proc. Conf. Simulation Semiconductor Processes and Devices*, 1999, pp. 137–140.
[15] H. S. Momose *et al.*, "1.5 nm direct-tunneling gate oxide Si MOSFET's," *IEEE Trans. Electron Devices*, vol. 43, pp. 1233–1242, Aug. 1996.
[16] C.-H. Choi *et al.*, "$C-V$ and gate tunneling current characterization of ultra-thin gate oxide MOS (t_{ox} = 1.3–1.8 nm)," in *Proc. Symp. VLSI Technol.*, 1999, pp. 151–152.
[17] H. S. Momose *et al.*, "A study of flicker noise in N^- and P^- MOSFET's with ultra-thin gate oxide in the direct-tunneling regime," in *IEDM Tech. Dig.*, 1998, pp. 923–926.
[18] Y. Wu and G. Lucovsky, "Ultrathin nitride/oxide (N/O) gate dielectrics for p^+-polysilicon gated PMOSFET's prepared by a combined remote plasma enhanced CVD/thermal oxidation process," *IEEE Electron Device Lett.*, vol. 19, pp. 367–369, Oct. 1998.
[19] Y. Wu, Y.-M. Lee, and G. Lucovsky, "1.6 nm oxide equivalent gate dielectrics using nitride/oxide (N/O) composites prepared by RPECVD/oxidation process," *IEEE Electron Device Lett.*, vol. 21, pp. 116–118, Mar. 2000.
[20] K. Kano, *Semiconductor Devices*. Englewood Cliffs, NJ: Prentice-Hall, 1998.
[21] Y. Taur and T. Ning, *Fundamental of Modern VLSI Device*. Cambridge, U.K.: Cambridge Univ. Press, 1998.
[22] *HSPICE User's Manual*: AVANT! Corp., 1998.
[23] K. Doganis and D. L. Scharfetter, "General optimization and extraction of IC device model parameters," *IEEE Trans. Computer-Aided Design*, vol. 30, pp. 1219–1228, Sept. 1983.

Chang-Hoon Choi (S'97) received the B.S. and M.S. degrees in electronic engineering from Sogang University, Seoul, Korea, in 1988 and 1990, respectively. He is currently pursuing the Ph.D. degree at the Center for Integrated Systems, Stanford University, Stanford, CA.

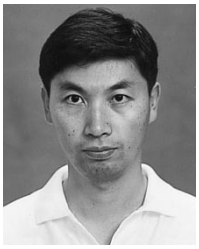
From January 1990 through May 1997, he was with Samsung Electronics Co., Ltd., Kyungki-Do, Korea, where he engaged in modeling and simulation on the IC circuits, devices, and TCAD. His research interests include characterization, modeling, and simulation of processes/devices for future CMOS generations.

Mr. Choi is a Member of the IEEE Electron Device Society and has served as a reviewer for IEEE TRANSACTIONS ON ELECTRON DEVICES. He is listed in *Who's Who in the World*.

Yider Wu (M'96) received the B.S. degree in physics from the National Tsing Hua University, Taiwan, R.O.C., in 1990, the M.S. degree in applied physics from the University of Massachusetts, Lowell, in 1994, and the Ph.D. degree in electrical and computer engineering from North Carolina State University in 1999. His dissertation focused on the formation, characterization, and modeling of remote PECVD ultrathin nitride/oxide composite layer gate dielectrics.

After a summer internship in the Strategic Technology Group in Advanced Micro Devices (AMD), Sunnyvale, CA, where he studied time dependent dielectric wearout of ultrathin gate dielectric, he returned to AMD in July 1999 as a Permanent Member. He is currently engaged in the integration issues of next generation flash memory technology within the Non-Volatile Memory Technology Directorate.

Dr. Wu is a Member of the American Vacuum Society and the Electrochemical Society.



Jung-Suk Goo (S'97) was born in Seoul, Korea, in 1966. He received the B.S.E.E degree from Yonsei University, Seoul, Korea, in 1988, and the M.S.E.E. degree from Stanford University, Stanford, CA, in 1997. He is currently working toward the Ph.D. degree at Stanford.

From 1988 to 1989, he was with GoldStar Semiconductor Company, Korea, involved in EPROM and 4 M DRAM projects. From 1898 to 1995, He was with LG Semicon Company, Korea. During this period, he was engaged in next-generation DRAM development such as 64 M and 256 M, and also was involved in a flash memory project. His primary research areas were DRAM process development, device evaluation, and reliability modeling especially the hot carrier effect. He has authored and co-authored approximately 20 journal and conference papers and holds six U.S. patents. His current research interests are CMOS low noise amplifier design and high-frequency MOSFET noise modeling.

Zhiping Yu (M'90–SM'90) received the B.S. degree from Tsinghua University, Beijing, China, in 1967, and the M.S. and Ph.D degrees from Stanford University, Stanford, CA, in 1980 and 1985, respectively.

He is currently a Senior Research Scientist in the Department of Electrical Engineering, Stanford University, and also holds a Full Professorship at Tsinghua University. His research interests focus on IC process, device, and circuit simulation, and in particular, the numerical techniques and modeling of RF and heterostructure devices. He has been involved in efforts to develop a simulation package for optoelectronic devices and 3-D solid modeling for ICs. Besides the full time university research, he is a Consultant to HP Computer System and Technology Lab, HP, developing advanced transport models for subquarter-micron CMOS technology, including quantum mechanical effects.

Dr. Yu is currently serves as the Associate Editor of IEEE TRANS. CAD OF IC AND SYSTEMS, responsible for TCAD-related fields.

Robert W. Dutton (S'67–M'70–SM'80–F'84) received the B.S., M.S., and Ph.D. degrees from the University of California, Berkeley, in 1966, 1967, and 1970, respectively.

He is Professor of Electrical Engineering at Stanford University and Director of Research in the Center for Integrated systems. He has held Summer staff positions at Fairchild, Bell Telephone Laboratories, Hewlett-Packard, IBM Research, and Matsushita during 1967, 1973, 1975, 1977, and 1988, respectively. His research interests focus on IC process, device, and circuit technologies—especially the use of CAD and parallel computational methods. He has published more than 200 journal articles and graduated more than four dozen doctorate students.

Dr. Dutton was Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN (1984–1986). He was awarded the 1987 IEEE J. J. Ebers Award, a 1988 Guggenheim Fellowship to study in Japan, was elected to the National Academy of Engineering in 1991, and received the Jack A Morton Award for 1996.