Direct Tunneling Current Model for Circuit Simulation

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Abstract

This paper presents a compact direct tunneling current model for circuit simulation to predict ultra-thin gate oxide ($<$ 2.0 nm) CMOS circuit performance by introducing an explicit surface potential model with quantum-mechanical corrections. It demonstrates good agreement with the results from the numerical solver and measured data for the very-thin gate oxide thicknesses ranging 1.3 – 1.8 nm.

Introduction

According to the SIA roadmap, CMOS with gate length of 50–70 nm needs an oxide thickness of around 1.5–2.0 nm, which corresponds to 2–3 layers of silicon atoms. With such a thin oxide, direct tunneling occurs, resulting in exponentially increasing gate leakage current. This gate leakage current increases power dissipation and deteriorates device performance and circuit stability for ULSI [1].

However, even though there were many reports concerning the effects of the gate leakage current to MOS transistor operations, fewer studies have been made regarding impact of the gate current on circuit operation due to absence of a circuit simulation model for gate tunneling current. Hence, a gate tunneling current model is needed to analyze circuit immunity against the gate leakage current including dependencies on architecture and operating conditions. In this paper, a compact direct tunneling model for very-thin gate oxide MOS transistors suitable for circuit simulation is presented.

Surface potential based tunneling model

Fig. 1 shows direct tunneling of electrons across gate oxide from the p-type Si substrate to n^+-poly Si gate. This direct tunneling current model is expressed as [2],

$$J_{DT} = C(V_{ox}/t_{ox})^2 e^{\frac{-B(1-(1-V_{ox}/\Phi_B)^{3/2})}{V_{ox}/t_{ox}}} \tag{1}$$

where B and C are physical parameters (see [2]).

In order to apply Eq. (1) to the calculation of gate tunneling current, it is necessary to relate the oxide voltage (V_{ox}) to the applied voltage (V_{gs}), since V_{ox} depends on V_{gs} as well as the surface potential (ψ_s) as follows:

$$V_{ox} = V_{gs} - V_{fb} - \psi_s \tag{2}$$

However, ψ_s can only be solved accurately using an iterative numerical approach, requiring expensive computations, which is not desirable for circuit simulation. In order to reduce computation time while retaining an accurate relationship between the surface potential and the terminal voltages, an explicit formulation of surface potential (ψ_s) [3] is used in this work.

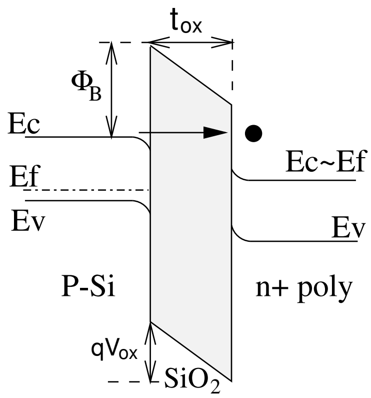


Fig. 1. Direct tunneling of electron in n^+-polysilicon / SiO_2 / p-Si MOS structure ($V_{ox} < \Phi_B$).

Under the assumptions of having a gradual channel and using the charge sheet approximation for an ideal n-type MOS transistor, the surface potential in the weak inversion region ($0 < \psi_s < 2\phi_f$) can be approximated as [4]:

$$\psi_{s,weak} = V_{gs} - V_{fb} + \frac{\gamma^2}{2} - \gamma\sqrt{V_{gs} - V_{fb} + \frac{\gamma^2}{4}} \tag{3}$$

where γ is the body factor defined by $\sqrt{2q\epsilon_{Si}N_a}/C_{ox}$.

In the strong inversion region ($\psi_s > 2\phi_f$) ψ_s becomes

$$\psi_{s,strong} = 2\phi_f + V \tag{4}$$

where V denotes the electron quasi-Fermi potential, ranging from V_{sb} at the source to V_{ds} at the drain side. The surface potential at the drain node ($\psi_{s,drain}$) is modeled to consider the drain bias (V_{ds}) effect as:

$$\psi_{s,drain} = \psi_s(V_{ds} + V_{sb}), \quad \psi_{s,source} = \psi_s(V_{sb}) \tag{5}$$

This enables reduction of gate tunneling current at the drain as the drain bias increases due to the decrease of the potential difference between the gate and drain (i.e. decrease of V_{ox} at the drain). In addition, ΔV_{gs} is introduced to consider the channel length dependence on gate current related to the drain-induced barrier lowering (DIBL) effect as:

$$\Delta V_{gs} = \delta_{DIBL}\sqrt{2\phi_f + V_{sb}} \cdot V_{ds} \tag{6}$$

where $\delta_{DIBL} = \delta_O(\frac{L}{L_R})^{n_{dibl}}$, L_R is the reference gate length and n_{dibl} is an exponent of the length dependence. This ΔV_{gs}

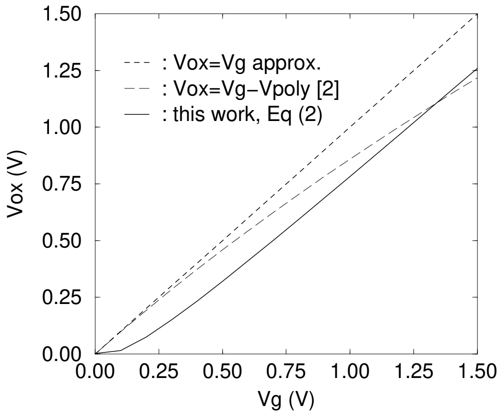


Fig. 2. Voltage drop at oxide (V_{ox}) with respect to the applied gate bias for t_{ox} = 1.5 nm. Comparisons between V_{ox} = V_g approximation, V_g - V_{poly}, and the surface potential based model.

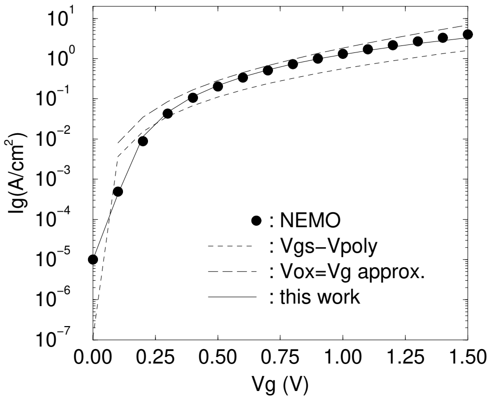


Fig. 3. Simulated gate current curves using V_g approximation, V_g - V_{poly}, and the surface potential based model, symbols are obtained from NEMO, an approximated Schrödinger equation solver (t_{ox} = 1.5 nm).

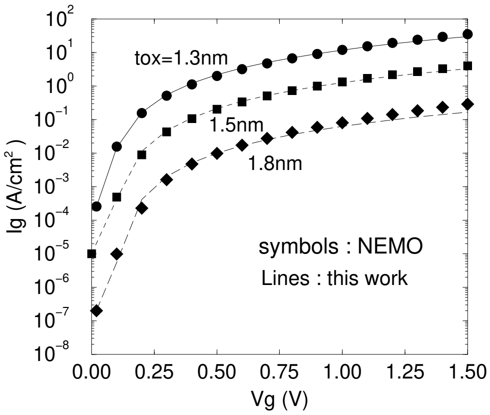


Fig. 4. Comparisons of simulated gate current using the compact model for different t_{ox}'s (1.3, 1.5, and 1.8 nm). Symbols denote gate current from NEMO.

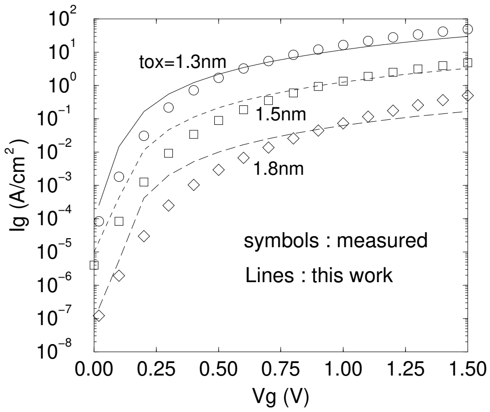


Fig. 5. Comparisons of simulated gate current using the compact model and measured data for different t_{ox}'s (1.3, 1.5, and 1.8 nm).

is added to V_{gs} in Eq. (3). As a result, effects of gate length dependence of gate tunneling current is taken into account because ψ_s is abruptly increased as the channel length is scaled down.

Quantum-Mechanical effects

For gate oxide thicknesses less than 2.0 nm, quantum-mechanical effects become dominant. In the classical case, the electron density has its maximum value at the Si-SiO$_2$ interface, while in the quantum mechanical case the electron density is diminished at the interface, increases to its maximum value and decreases with the distance from the surface [4]. Hence, in the quantum-mechanical model the inversion charge profile peaks at around 10 Å below the silicon surface such that inversion charge is effectively reduced to that of an equivalent oxide which is a few angstroms to nanometer thicker than the physical oxide.

For calculation of the surface potential considering the QM effects, the intrinsic carrier concentration, n_i, is evaluated by introducing a bandgap broadening mechanism which is an approximate manner of van Dort's bandgap broadening approach expressed as [5]:

$$\Delta E_g = \frac{\beta}{2kT} E_n^{2/3} \tag{7}$$

where E_n is the normal electric field at the Si-SiO$_2$ interface which is gate bias dependent determined by V_{ox} and t_{ox}, and β is a fact that can be determined experimentally. The value of ΔE_g is used to calculate new intrinsic carrier concentration (n_i) and Fermi potential (ϕ_f).

Results and discussions

Fig. 2 shows the simulated oxide voltages (V_{ox}) with respect to gate bias using V_{ox} = V_g approximation, V_{ox} = V_g - V_{poly} [2], and the surface potential based model. Fig. 3 shows simulated gate currents using the compact model, the conventional methods [2][6] and 1D Green's function solver, NEMO [7], that is an approximated Schrödinger equation solver. Gate tunneling current in the low gate bias regime obtained from the compact model agrees well with that from the numerical solver due to the surface potential model in the weak inversion region. Comparing NEMO and real measurements, simulated gate currents for different oxide thicknesses

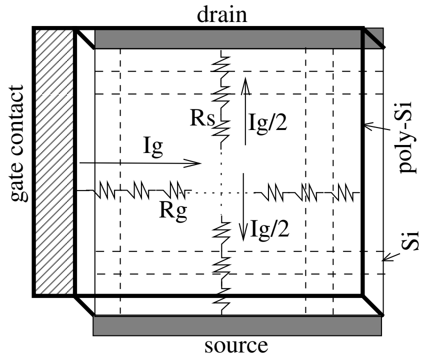


Fig. 6. Gate and series resistance (R_g and R_s) effects associated with gate current (I_g) in ultra-thin oxide, large area MOS transistor.

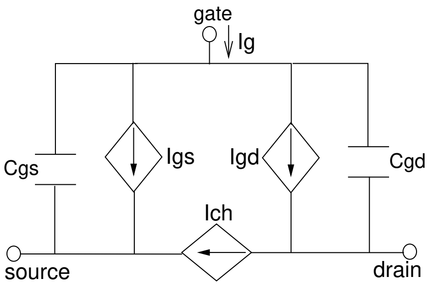


Fig. 7. Circuit model of gate tunneling current for circuit simulation (I_g = I_{gs} + I_{gd}).

are shown in Fig. 4 and 5. The simulated gate currents using the compact model agree well with those from NEMO for the oxide thicknesses of 1.3, 1.5, and 1.8 nm due to consideration of the surface potential as well as quantum mechanical effects. The discrepancies between the measured and simulated data in Fig. 5 are probably caused by surface roughness, uncertainty in determining the effective oxide thickness, and the IR drop at the poly gate and the channel due to the gate leakage current. In reality, the gate tunneling current behavior in MOS terminals is affected by the three-dimensional geometric effects associated with gate (R_g) and series resistance (R_s), as shown in Fig. 6 [5].

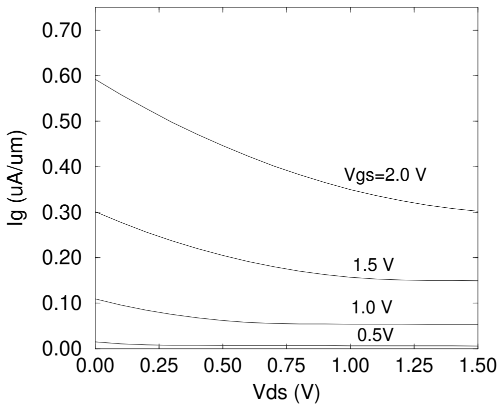


Fig. 8. Simulated gate tunneling current versus V_{ds} for different V_{gs}, L_g = 10 μm and t_{ox} = 1.5 nm.

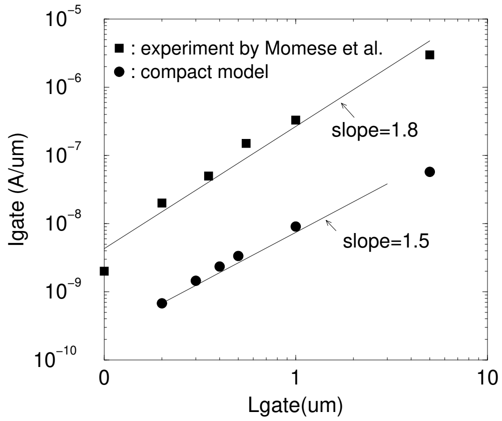
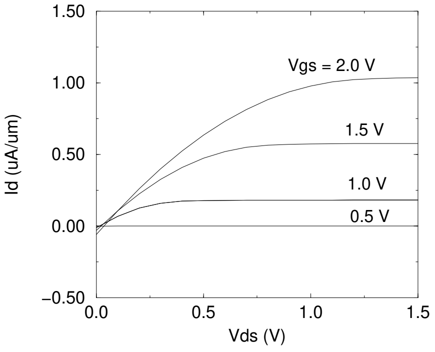


Fig. 9. Gate length dependence of gate tunneling current at V_{ds} = V_{gs} = 1.5 V for t_{ox} = 1.5 nm, the simulated slope is comparable with ref. [7] due to consideration of DIBL.

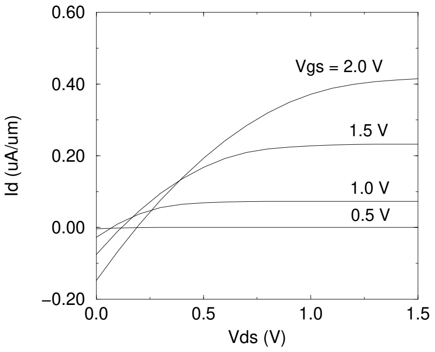
In order to consider drain bias effects ($V_d > 0$ V) an equivalent circuit is used as in Fig. 7, where gate current (I_g) is composed of gate-to-source current (I_{gs}) and and gate-to-drain current (I_{gd}). Gate current in the drain (I_{gd}) is determined by surface potential at the drain ($\psi_{s,drain}$) for the given drain bias. Namely, I_{gs} and I_{gd} are computed independently by considering the surface potential of gate-to-source ($\psi_{s,source}$) and gate-to-drain ($\psi_{s,drain}$) in Eq. (5). In this work, these voltage-controlled current sources, I_{gs} and I_{gd}, were described by utilizing the behavioral modeling in SPICE; the BSIM3 model was used as a channel current (I_{ch}) model. As a result, as shown in Fig. 8 the simulated gate current decreases as the drain bias increases due to the increase of surface potential at the drain, which leads to V_{ox} reduction. The direction of gate current near the drain region can even become reversed when the potential of the drain is higher than that of the gate. Hence, total gate tunneling current becomes lower as the drain bias moves from the linear to the saturation region operations; the gate current effect is dominant at high V_{gs} and low V_{ds} bias conditions.

Fig. 9 illustrates the simulated channel-length dependence on gate current at V_{ds} = V_{gs} = 1.5 V by consideration the DIBL effect; I_g decreases in inverse proportion to $L_g^{1.5}$, which is comparable to the slope of the experiment (= 1.8) by Momose $et\ al$ [8]. It is obvious that effects of gate tunneling current to the drain current become less problematic for the short channel MOSFETs because the channel current is much higher than gate current and gate current decreases exponentially as the channel length is reduced. However, even though the gate current for individual transistor with very small size is not significant, the total gate current for the entire chip will become a serious problem for battery applications [9].

Fig. 10 (a) and (b) show the simulated drain currents for L_g = 20 μm and L_g = 50 μm when gate tunneling effects are considered. In the long channel regime of L_g = 50 μm, anomalous electric characteristics are observed at very low V_{ds}, because the magnitude of gate current is comparable to the drain current in this bias range.

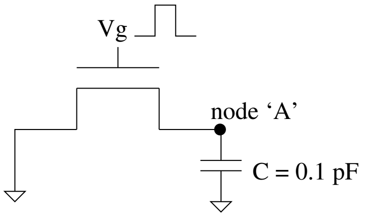


(a)

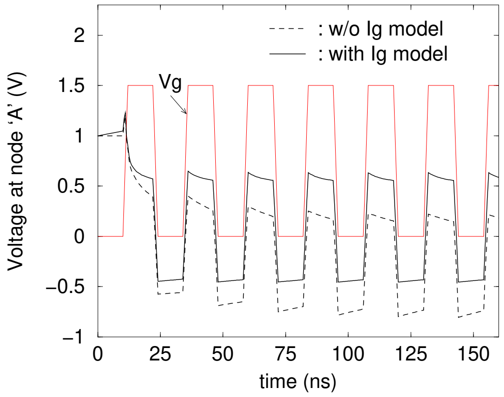


(b)

Fig. 10. Simulated drain current (I_d) versus V_d for t_{ox} = 1.5 nm, (a) L_g = 20 μm (b) L_g = 50 μm.



(a)



(b)

Fig. 11. Transient circuit simulation results with the gate current model, (a) test circuit with NMOS (W/L = 100 μm/20 μm and t_{ox} = 1.5 nm) and 0.1 pF capacitor, (b) simulated voltages at node 'A' with and without gate tunneling current models.

SPICE transient circuit simulation using the compact model is performed for the simple circuit as shown in Fig. 11, composed of a single NMOS transistor with a 0.1 pF capacitor. To observe the distinct effects of gate tunneling current during circuit operation, a large transistor (W/L = 100 μm/20 μm) is used. With the compact model, gate tunneling current effects are remarkable; the node 'A' remains at a steady voltage due to the current injection from the gate, while it gradually decreases as a function of time when the gate current is ignored.

Summary

An accurate direct tunneling model for circuit simulation is reported that incorporates an explicit surface potential model and quantum-mechanical corrections. Simulated gate currents from this model demonstrate good agreement with the results from a numerical solver and measured data for gate oxides ranging 1.3 – 1.8 nm.

Acknowledgment: The support from NSF through NCCE and DesCArtES projects is greatly appreciated.

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