A Fast 3D Modeling Approach to Parasitics Extraction of Bonding Wires for RF Circuits

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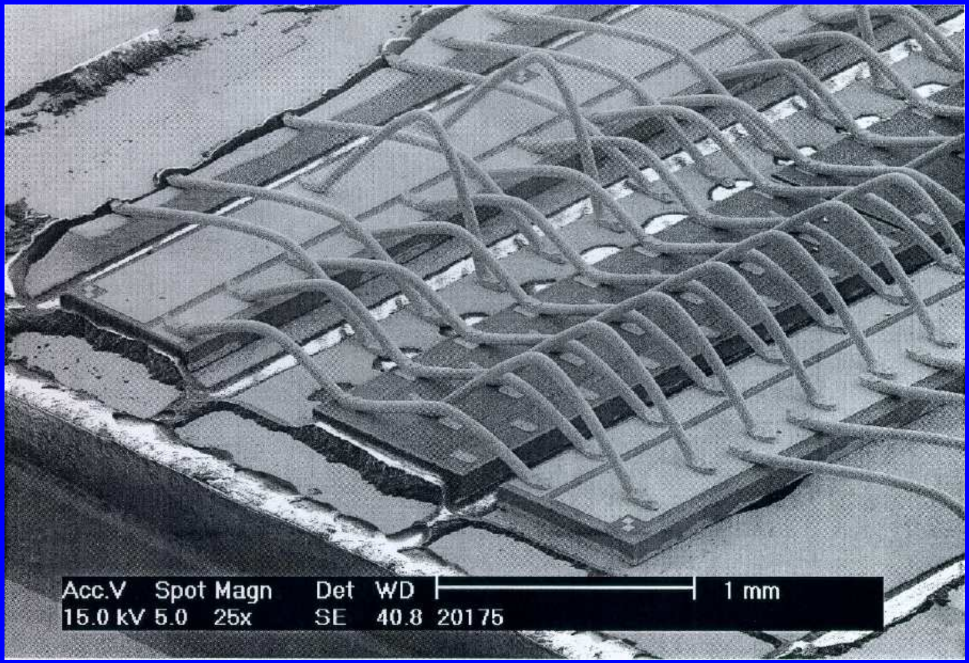
Outline

- Background and Motivation
- A New Geometry Extraction Method for Bonding Wires for RF Circuits
- Experiment and Simulation Results
- Summary and Future Works

Background and Motivation

- Bonding wires are used in IC packaging and RF circuits.
- At high frequency, parasitics of bonding wires impact performance.
- RF circuit designers use bonding wire as a circuit element.

Inside of Package



Inside of the package of a 55W bipolar transistor for 1.9 GHz PCS base stations

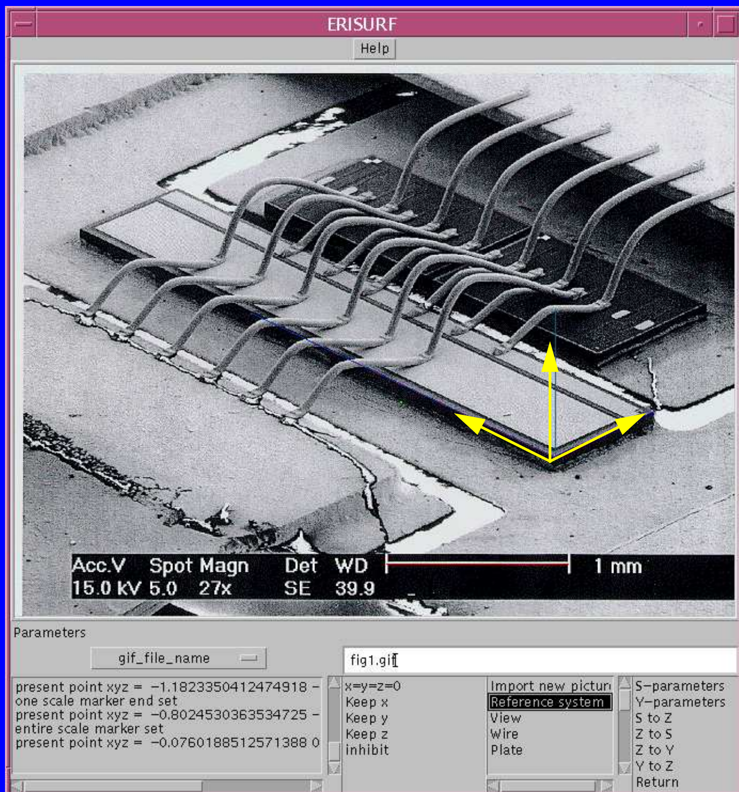
A New Geometry Extraction Method

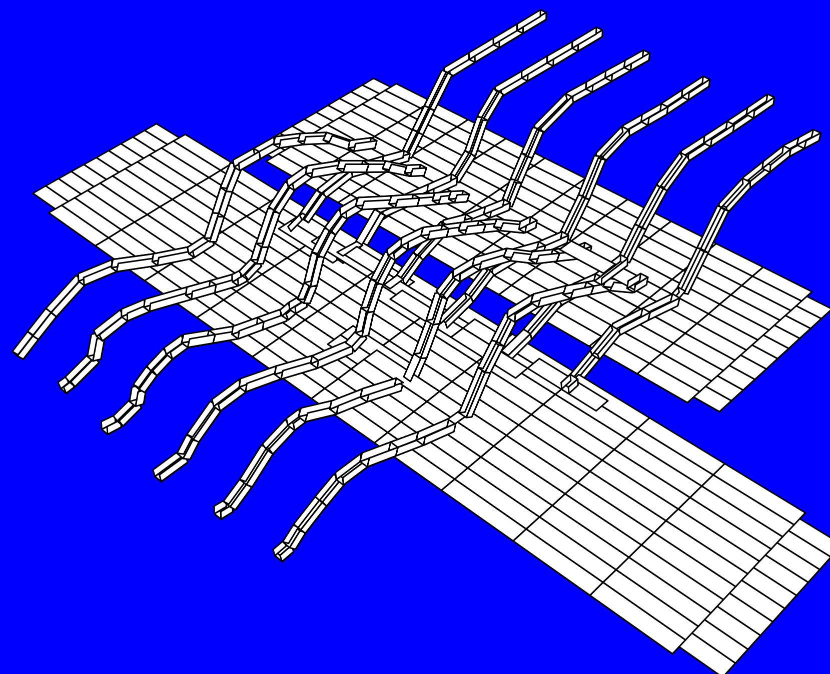
- Bonding wire’s curvature is very difficult to predict before it is fabricated.
- Accurate electrical modeling depends on good 3D geometry modeling.
- To obtain the geometry of the wires, SEM photos are used.

A New Geometry Extraction Method

- Use one properly positioned SEM photo
- Define a reference coordinate system
- Superimpose a drawing on the photo to emulate 3D movements, constructing a 3D geometry for field solvers
- Can be run across the Internet

A New Geometry Extraction Method





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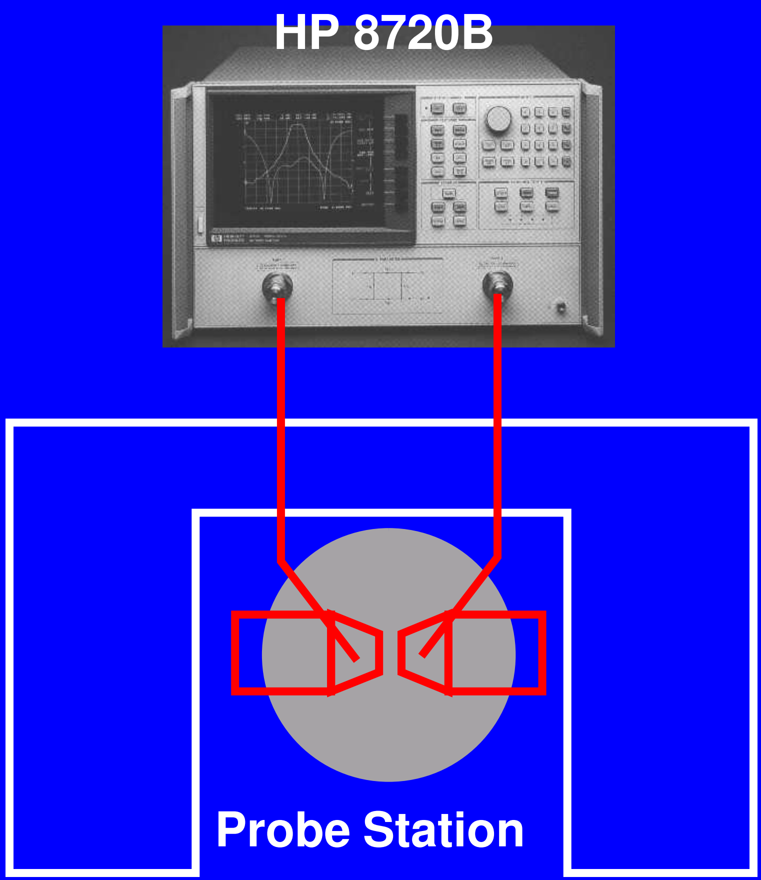
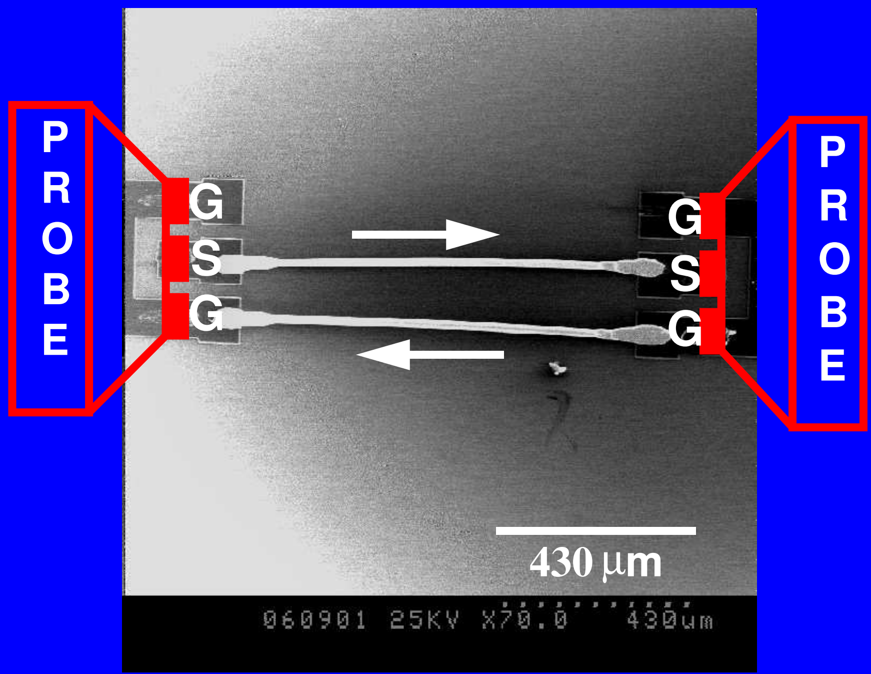
Experiments and Simulation

- Test structures are designed and fabricated.
- Two port S parameters were measured using network analyzer and coplanar ground-signal-ground probe.
- Simulation: ERISURF $\longrightarrow$ FASTHENRY $\longrightarrow$ Impedance $\rightarrow$ HSPICE/MDS $\rightarrow$ S-Parameters

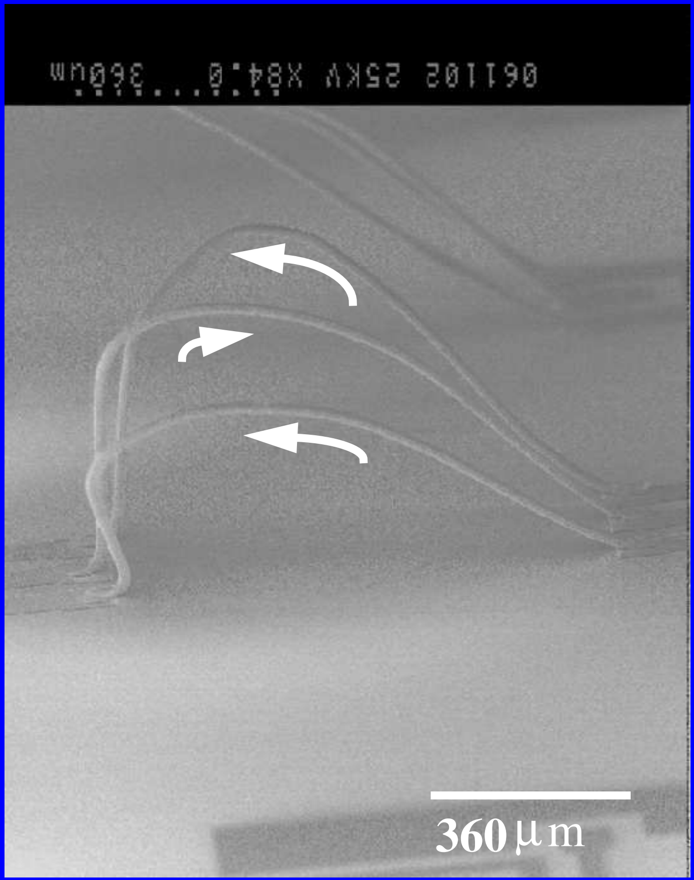
Testing Setup





Device Under Test

Test Structure Curv31



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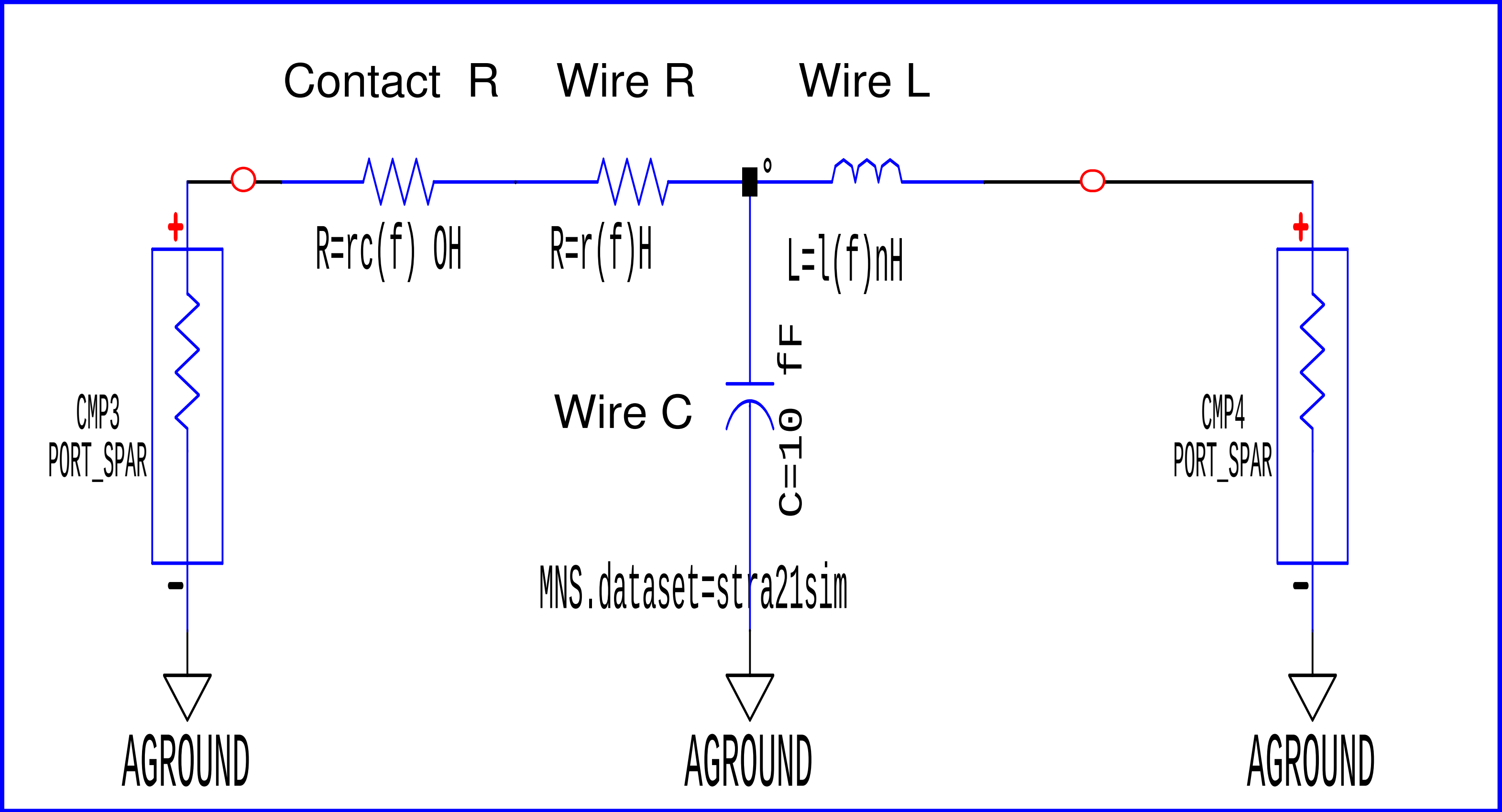
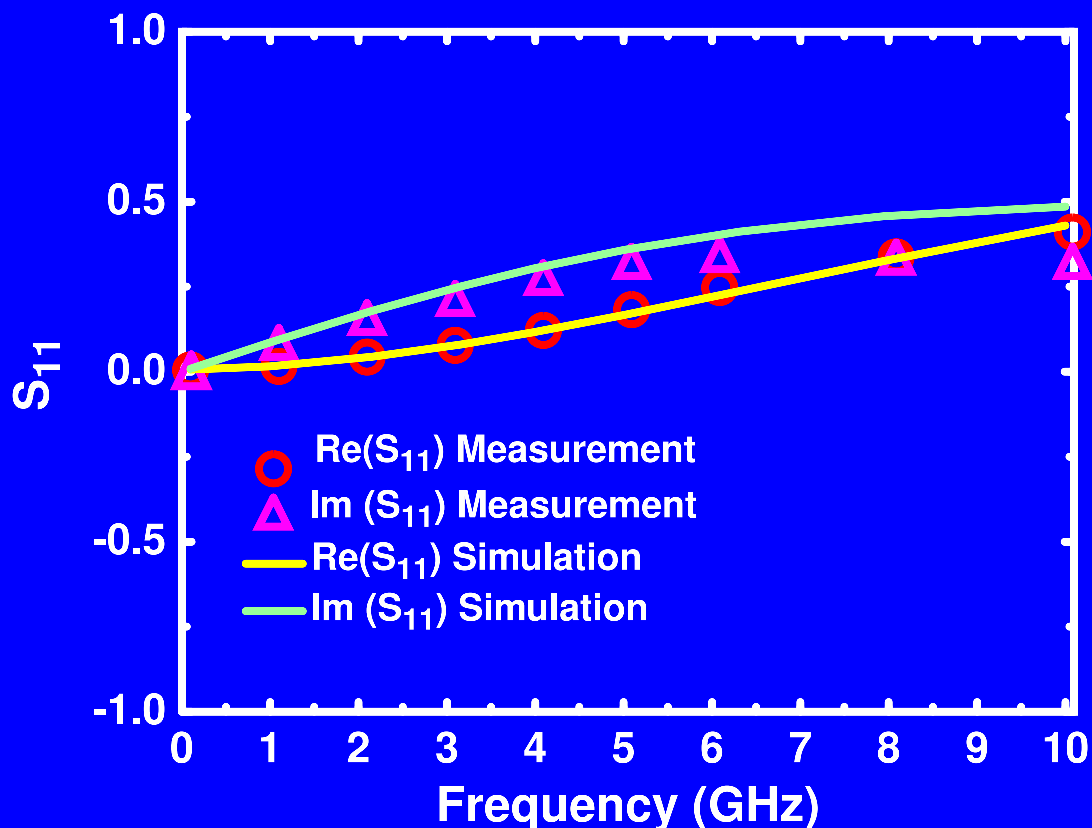
An Equivalent Circuit for Bonding Wires

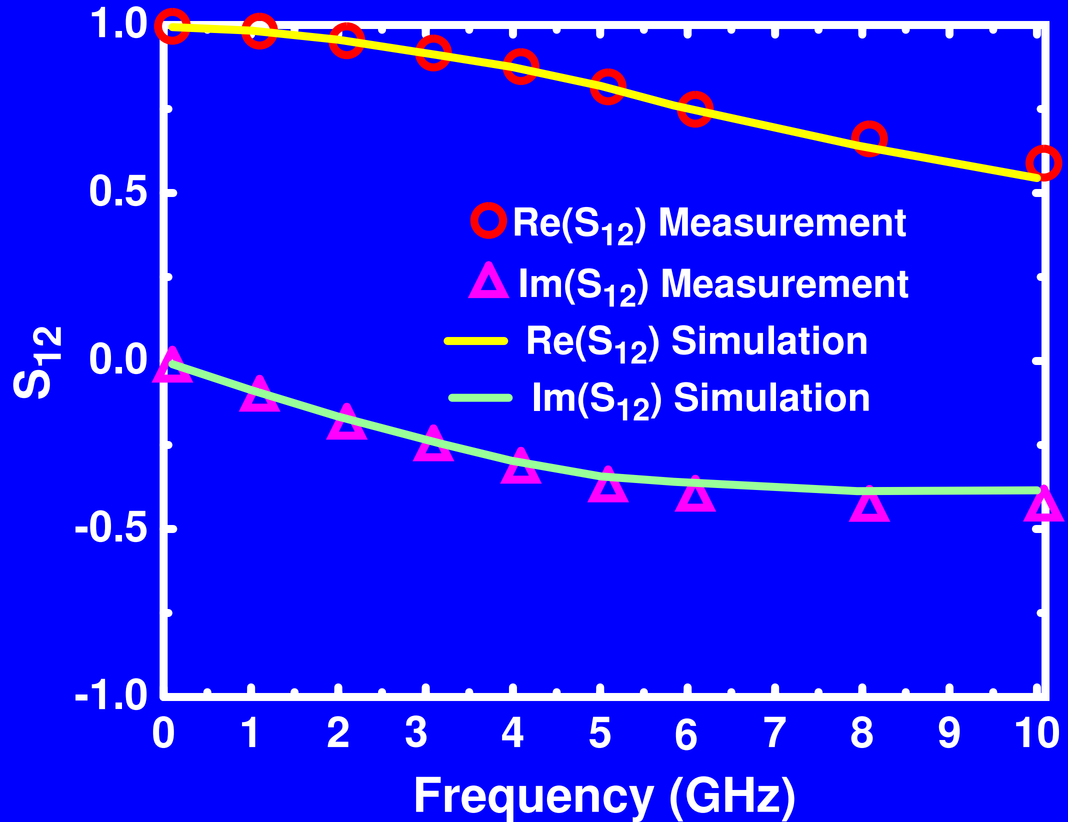


Measured and Simulated S Parameters for Straight Wires



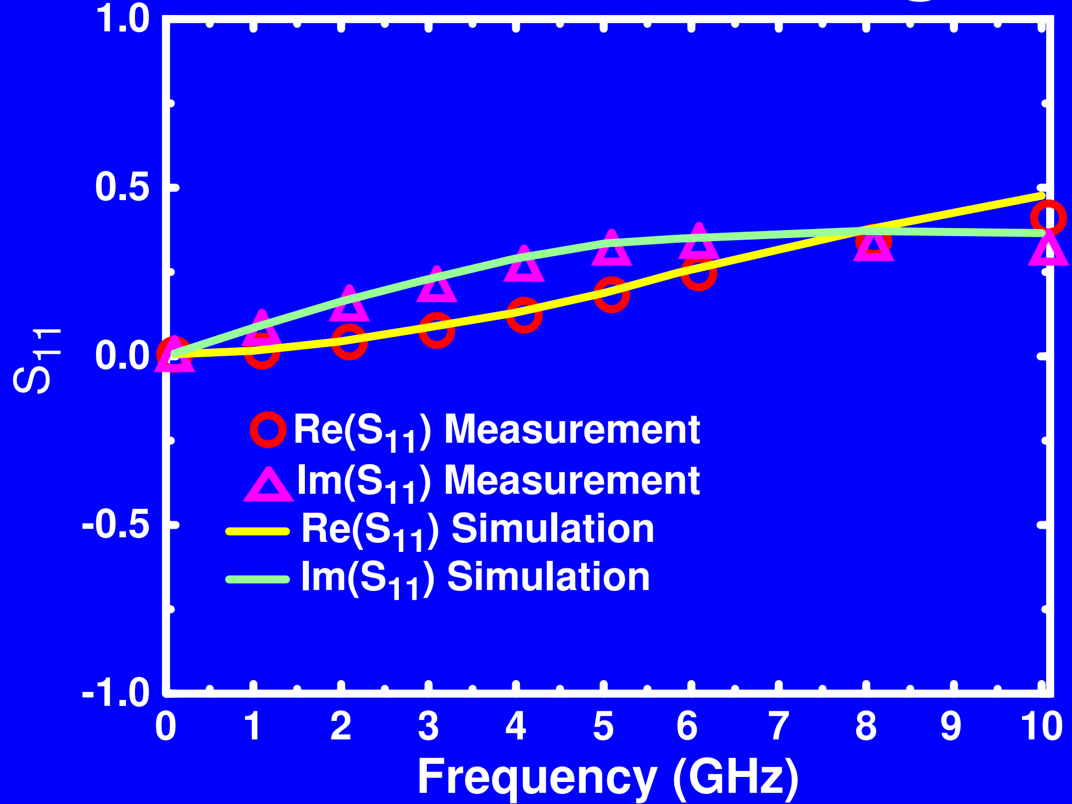
Stra21: two straight lines each of 1mm long without capacitance in model

Measured and Simulated S Parameters for Straight Wires



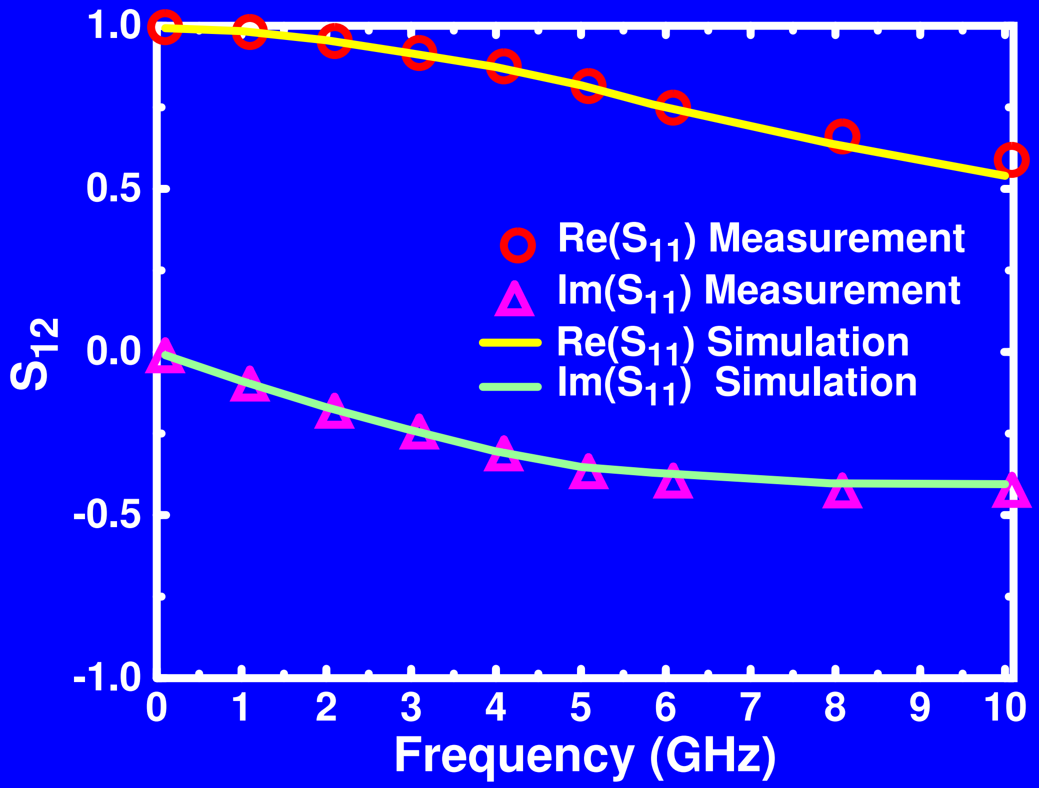
S12 of Stra21 without capacitance included.

Measured and Simulated S Parameters for Straight Wires



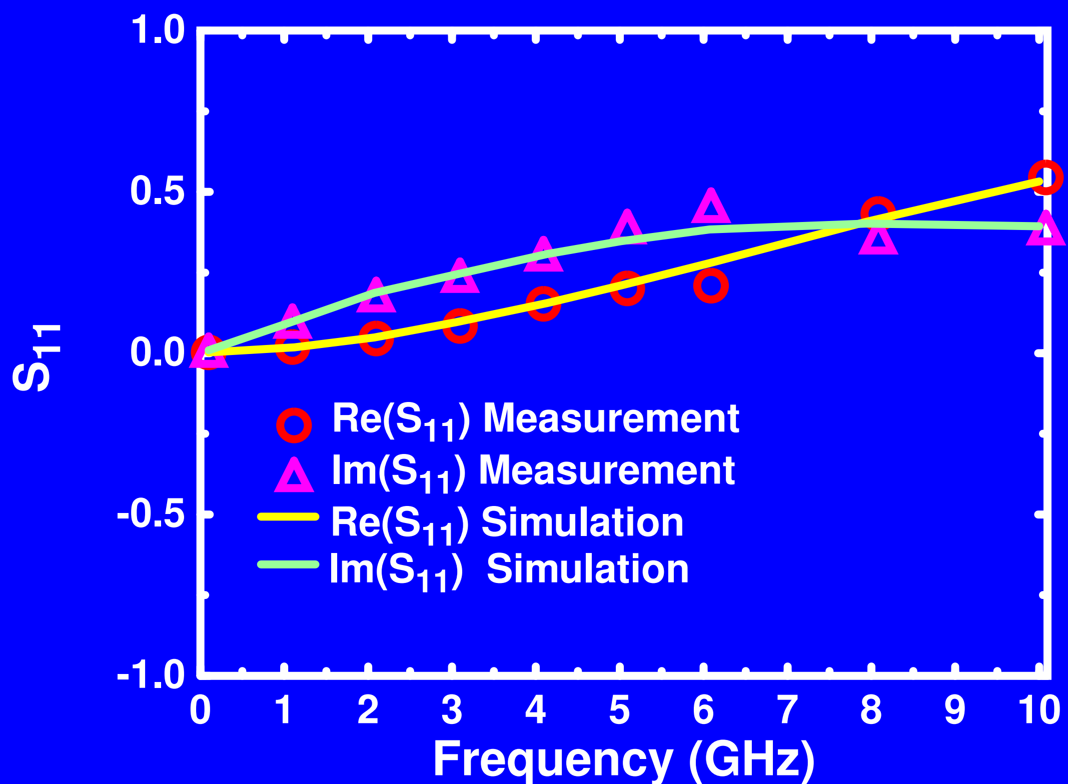
S_{11} of Stra21 with capacitance in model

Measured and Simulated S Parameters for Straight Wires



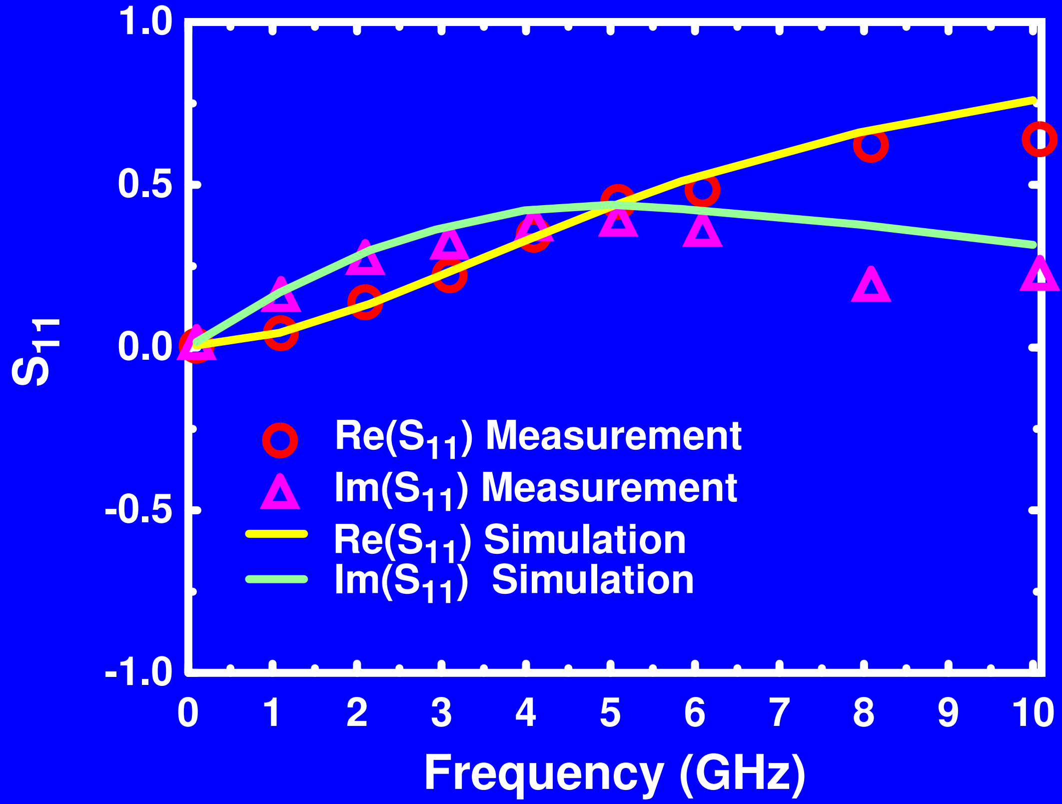
S_{12} of Stra21 with capacitance in model

Measured and Simulated S Parameters for Curved Wires (Curv31)



S_{11} for Curv31 with capacitance included

Measured and Simulated S Parameters for Curved Wires (Curv22)



S_{11} for Curv22 with capacitance included

Estimate by Analytical Formulation

$$L \approx \left[\frac{\mu_0 l}{2\pi}\right] \times \left[\ln\left(\frac{2l}{r}\right) - 0.75\right]$$

$$M \approx \frac{\mu_0 l}{2\pi} \times \left[\ln\left(\frac{2l}{D}\right) - 1 + \frac{D}{l}\right]$$

Comparison of Analytical Calculation, Simulation, and Measurement

Table 1: Inductance Comparison at 1.1 GHz (nH)

	Stra21	Curv22	Curv31
Measurement	1.377	2.802	1.546
Simulation	1.414	2.694	1.533
Sim. Error	2.69%	3.85%	0.84%
Calculation	1.233	N/A	N/A
Cal. Error	10.5%	N/A	N/A

Summary

- A 3D modeling approach to characterization of bonding wires is presented.
- Test structures were designed and fabricated. Extracted electrical parameters show very good agreement with measured data up to 10 GHz.

Future Work

- To model packaged RF power devices (BJT, LDMOS) to provide macro model for circuit simulation (SPICE, MDS).
- On-chip VLSI interconnect analysis including inductance, capacitance, and EMI.
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