Two-Dimensional Polysilicon Quantum-Mechanical Effects in Double-Gate SOI

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I. Introduction

Double-gated, fully depleted SOI is one promising candidate technology for sub-20nm devices. Recently, efforts have been devoted to Quantum-Mechanical (QM) treatments of the charge behavior not only for the silicon substrate, but also for the polysilicon gate due to significant polysilicon quantization effects for scaled devices [1][2]. Polysilicon quantization effects become significant for scaled devices with very-thin gate dielectrics since a deep quantum well is formed near the poly/oxide interface when an abrupt energy barrier exists due to high electric fields. As a result, carriers in the polysilicon are repelled from the interface for the depletion condition, leading to a negative voltage shift, which is the reverse of the QM quantization occurring in the silicon substrate [1]. To date, however, 2-dimensional QM charge behavior in poly-gate influenced by the drain bias has not been reported. In this work, device simulation results based on a density gradient (DG) quantum-mechanical model [3] are used to quantify 2-D polysilicon quantization effects in the presence of drain bias for double-gate SOI.

II. Polysilicon Quantization Effects

The schematic of a double-gate SOI NMOS is shown in Fig. 1. In this work, we assumed that L_g = 20 nm, t_{si} = 5 nm, t_{ox} = 1 nm, $N_d = 1.0\times10^{20}$ cm^{-3} and $N_a = 2.5\times10^{18}$ cm^{-3}, which are chosen based on the 35 nm technology in the reference [4]. Fig. 2 compares electron distributions in the vertical direction obtained from, (i) density gradient (DG) model applied to both polysilicon and silicon substrate – full DG, and (ii) DG model applied to silicon substrate only – partial DG. Bias conditions are V_{gs} = 1.0 V and $V_d = V_s$ = 0 V. Two different dopant concentrations in the poly-gate ($N_p = 5.0\times10^{19}$ and 2.0×10^{20} cm^{-3}) and two different oxide thicknesses (t_{ox} = 1 and 2 nm) are assumed. As a result, polysilicon quantization effects seem not to be critical for $N_p = 5.0\times10^{19}$ cm^{-3}; significant differences are not detectable in the electron distributions between the full and the partial DG models. In Fig. 3, electron "pile-up" due to the polysilicon quantization effect can be seen for higher gate dopant concentrations, $N_p > 1\times10^{20}$ cm^{-3}. This is because polysilicon depletion effects are much more dominant than the polysilicon quantization effect for the lower doping concentration. This implies that the use of full DG is not necessary for the lower N_p. Meanwhile, significant differences can be observed in comparing the full DG and the partial DG for $N_p = 2.0\times10^{20}$ cm^{-3}. For highly-doped polysilicon, electrons in the gate are pushed away from the poly/oxide interface in the presence of the abrupt energy barrier, leading to carrier "pile-up" at 2-3 nm away from the interface. As a result, the effective oxide thickness obtained from the full DG theory becomes a few Å thicker than the calculated values based on the classical approach.

For lower N_p values, however, classical polydepletion is dominant rather than the quantization effect; devices which suffer noticeably from polydepletion effects, depending on gate length and dopant profiles [5], are shown in Fig. 4. It should be noted that as the gate length is scaled down, the portion of the inversion capacitance decreases, while the potential drop (V_p) increases, implying that device performance deterioration from the polydepletion effect will be more significant as devices continue to scale. In addition, for a laterally convex dopant distribution, as shown in Fig. 5, more potential reduction occurs in the gate sidewalls, which is common when the gate dopant is boron (i.e. PMOS), since boron atoms in silicon have a tendency to diffuse towards adjacent oxide regions. On the contrary, for a concave dopant profile in which the dopant concentration has its peak at the sidewall, the potential in the edge is now higher than that of the inner poly region.

For higher N_p values, the polysilicon quantization effect can be significant; Fig. 6(a) shows the potential distribution in the lateral direction for $N_p = 2.0\times10^{20}$ cm^{-3}. Note the potential drops at the gate edges due to the fringing field between the poly-gate and the source/drain regions. Also, note the potential difference between the full DG and the partial DG models (i.e. 0.06 V), which results from the polysilicon quantization effect. Fig. 6(b) shows a potential "bump" near the poly/oxide interface owing to the QM effect in the poly-gate.

In order to estimate the impact of the polysilicon quantization on electrical properties of the device, gate capacitances are calculated using the full and the partial DG models. Calculated C–V curves are shown in Fig 7, implying that about 0.12 V higher threshold voltage as well as ∼20 % over-estimated gate capacitance are predicted without considering the QM effects for highly-doped polysilicon gates.

III. Drain Enhanced Poly Quantization Effects

Now, consider the drain bias effect to the polysilicon quantization effects. When bias is applied to the drain, the vertical field in the poly-gate near the drain region is reduced by the drain-induced lateral field. Thus, both the electron concentration in the silicon inversion and the depletion in the poly-gate near the drain are reduced, which leads to an abrupt rise in QM charge. Fig. 8 shows electron contours within the polysilicon region for $V_d = 0$ and 1 V ($V_{gs} = 1$ V); the carrier "pile-up" occurs at 2–3 nm away from the poly/oxide interface for $V_d = 0$ V. Note that the carrier pile-up is enhanced for $V_d = 1$ V; the electron peak is located at ∼2 nm away from the interface and the concentration is higher (i.e. 2.3×10^{20} cm^{-3}) than that for $V_d = 0$ V (i.e. 2.1×10^{20} cm^{-3}).

This 2-D charge behavior can be explained using an equivalent circuit approach, as shown in Fig. 9. The depletion width is reduced and the depletion capacitance (C_p) near the drain is increased for positive drain bias due to the rise of the channel potential near the drain, V_{cd}, which enhances the QM quantization effects near the interface. As a result, more electrons are pushed away from the interface, leading to a quantum mechanical potential rise (ΔV_{QM}), as shown in Fig. 9(b). ΔV_{QM} near the source region is also increased since the channel potential near the source, V_{cs} is pulled up by the drain field effect, especially for short channel devices. As a result, the effective gate voltage ($V_{gs,eff}$) near the source becomes greater in the presence of the drain bias because ΔV_{QM} increases due to the QM effects in poly-gate. This implies that the variation of threshold voltage with drain bias, the so called *drain-induced barrier lowering* (DIBL) effect, becomes severe due to polysilicon quantization effects.

Fig. 10 shows the electron and potential distributions in the vertical direction in the presence of drain bias, $V_d = 1$ V. The electron concentration in the substrate decreases when the bias is applied to the drain, while the electron concentration in the poly-gate increases, as shown in Fig. 10(a). The potential rise in the poly/oxide interface is about 0.1 V for $V_d = 1$ V in the center of the channel, as shown in Fig. 10(b). Electron and potential distributions along the lateral direction near the poly/oxide interface are position-dependent for the drain bias, as represented in Fig. 11.

The calculated drain currents show that the potential rise near the source contributes an increase of effective gate voltage ($V_{gs,eff}$) and negative shift of threshold voltage (V_T), as shown in Fig 12. This drain bias-enhanced polysilicon quantization effect is more significant for short gates, since the drain field can easily penetrate to the source end of the channel; in turn the potential change in the channel near the source affects the QM charge in the polysilicon. Hence, a rise of $V_{gs,eff}$ and negative shift of V_T by the drain field are more severe for the shorter gate devices. As shown in Fig. 13, the potential rise in the poly near the source is ∼0.1 V for $L_g = 20$ nm, while it is only 0.02 V for $L_g = 80$ nm.

This effect can be reduced in asymmetric double-gate SOI structures with n^+ and p^+ poly gates because electrons that pile up in n^+ poly-gate can be compensated by holes that pile up in the opposite p^+ poly-gate.

IV. Conclusions

Important quantum-mechanical poly quantization effects are demonstrated that reduce inversion capacitance and accentuate short-channel (DIBL) effects in fully depleted double gate SOI devices. Without considering the polysilicon quantization effects, ∼20 % over-estimated gate capacitance is predicted with $L_g = 20$ nm, $t_{si} =$ 5 nm and $t_{ox} = 1$ nm. The polysilicon quantization effect is shown to be enhanced by the drain bias, which implies that DIBL of double-gate SOI is significant due to these effects. The QM effects become worse with increased gate doping, implying ultimate limitations in using polysilicon gates for sub-20 nm DG/FD SOI. Even highly-doped polysilicon gates degrade device performance for sub-20 nm DG/FD SOI due to the polysilicon quantization effects, just as low-doped polysilicon gates degrade performance due to polydepletion effects.

Acknowledgment

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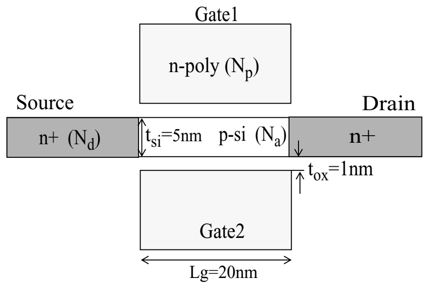


Fig. 1. Double-gate SOI cross section studied in this work.

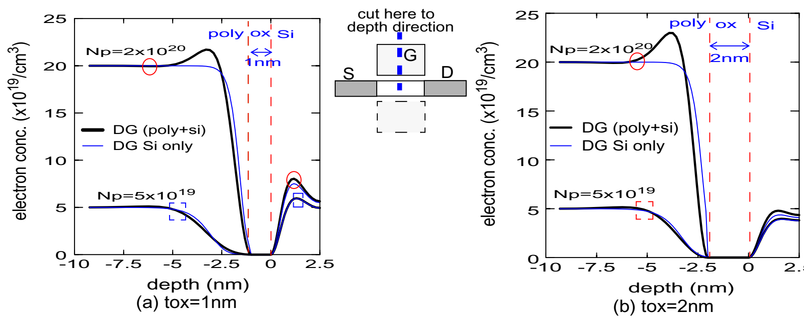


Fig. 2. Comparisons of electron distributions obtained from full (poly+si) and partial (si) DG models.

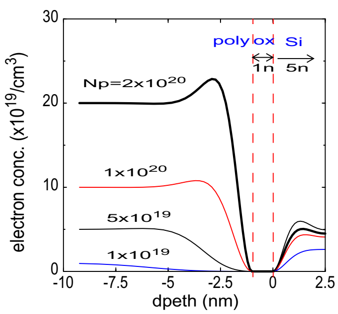


Fig. 3. Electron distributions in the vertical direction for different poly dopants (Np) obtained from full (poly+Si) DG model.

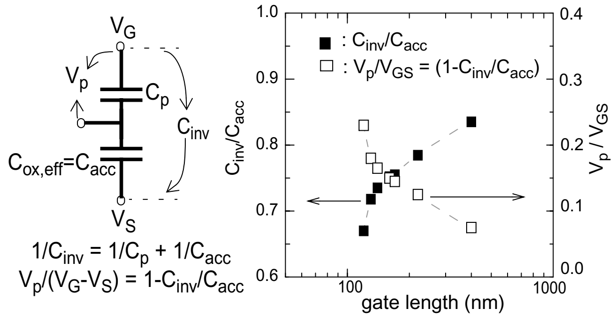


Fig. 4. Polydepletion effects for lower Np;measured C_{inv}/C_{acc} and V_p/V_{GS} for gate lengths (PMOS with t_{ox} = 1.6 nm).

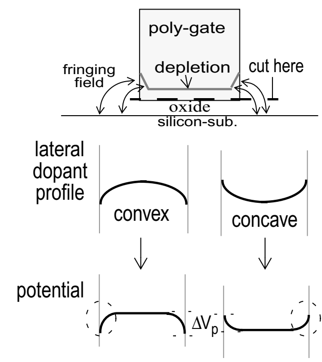


Fig. 5. Polydepletion effect due to non-uniform, lateral dopant profile.

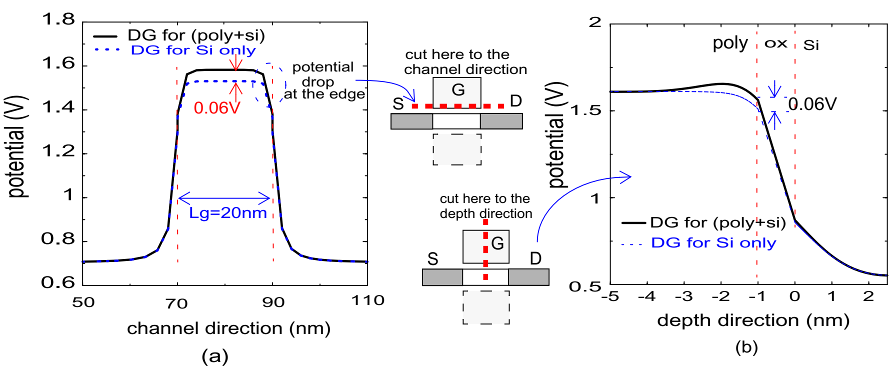


Fig. 6. Potential distributions in the lateral and the vertical directions for full (poly + Si) DG and partial (Si only) DG models (Vg = 1 V and Vs = Vd = 0 V).

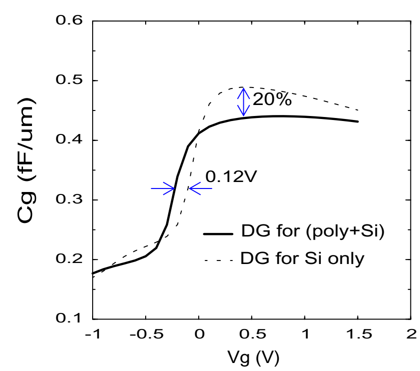
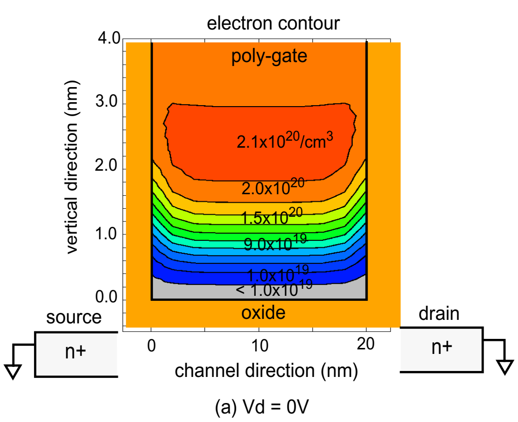


Fig. 7. Gate capacitance calculated by using full and partial DG models, Np = 2.0×10^{20} cm^{-3} and Vd = Vs = 0 V.



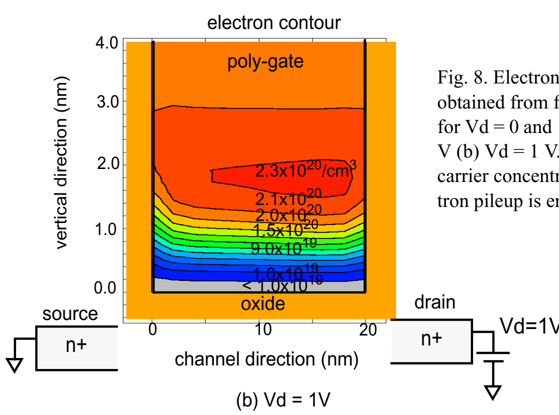


Fig. 8. Electron contours in poly-gate obtained from full DG theory for Vd = 0 and 1 V (Vg = 1 V) (a) Vd = 0 V (b) Vd = 1 V. Note the abrupt rise of carrier concentration for Vd = 1 V; electron pileup is enhanced by the drain bias

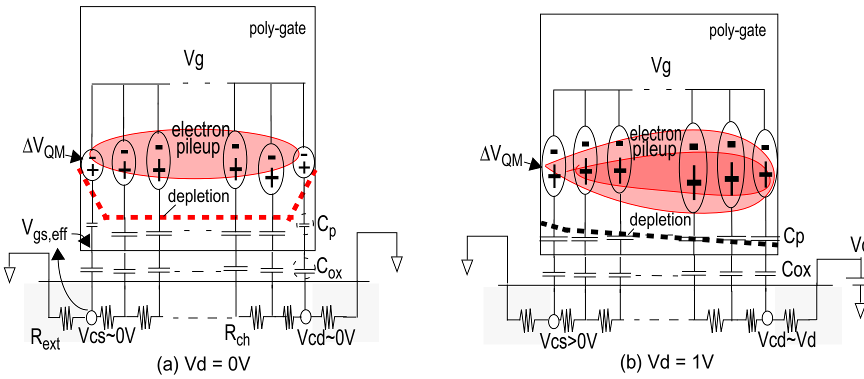


Fig. 9. Schematic of drain bias effects on ploysilicon quantization. $V_{gs,eff}$ is the effective gate voltage, ΔV_{QM} is the potential rise due to poly quantization, C_p is poly depletion capacitance and (V_{cs} and V_{cd}) are the channel potential near the source and drain regions, respectively, (a) Vd = 0 V (b) Vd = 1 V. Note that ΔV_{QM} becomes greater for Vd=1V due to poly-Si QM effects.

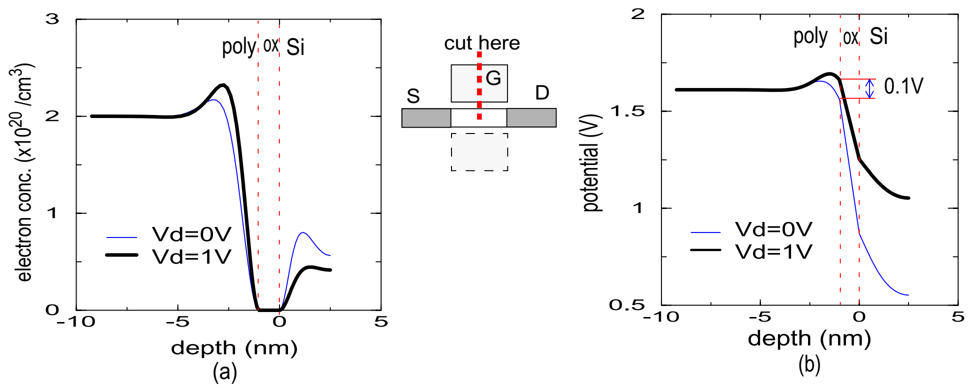


Fig. 10. Drain bias dependent electron and potential distributions in the vertical direction obtained by using the full DG model (Vg = 1 V), (a) electron (b) potential distribution.

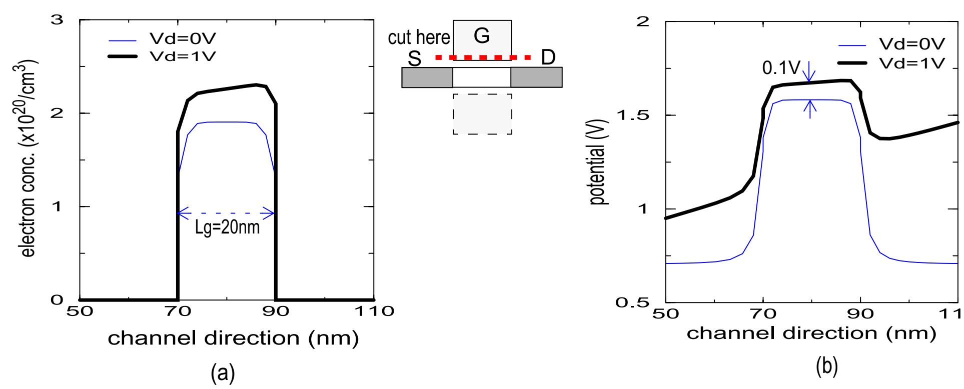


Fig. 11. Drain bias dependent electron and potential distributions in the lateral direction obtained by using the full DG model (Vg = 1 V), (a) electron (b) potential distribution.

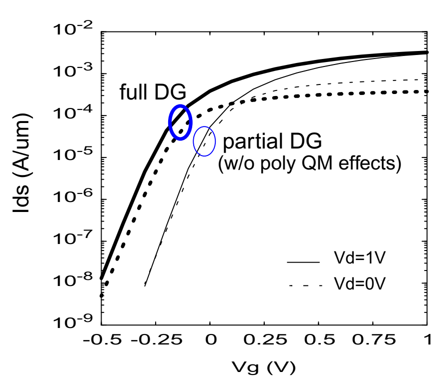


Fig. 12. Calculated drain currents between full and partial DG model; increase of effective gate bias and shift of threshold voltage are enhanced by the drain bias.

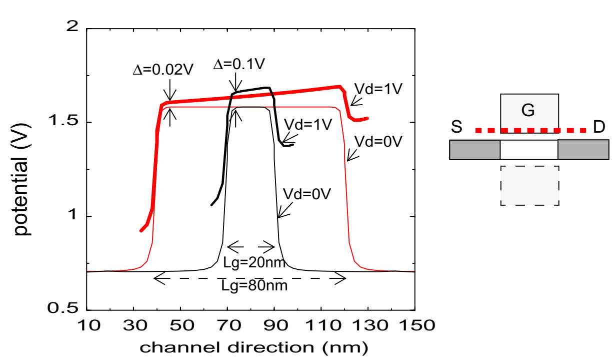


Fig. 13. Channel length dependent drain field effects on polysilicon quantization, potential distributions along the poly/oxide interface for Lg = 20 and 80 nm. Note that potential rise near the source is significant for Lg = 20 nm, implying worse short-channel effects (i.e. DIBL) for shorter gates due to polysilion quantization effects.