Gate Bias Induced Heating Effect and Implications for the Design of Deep Submicron ESD Protection

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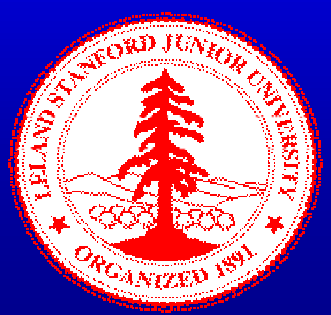


Stanford University

*** Texas Instruments**

Purpose

- To investigate the impact of gate bias on ESD protection:

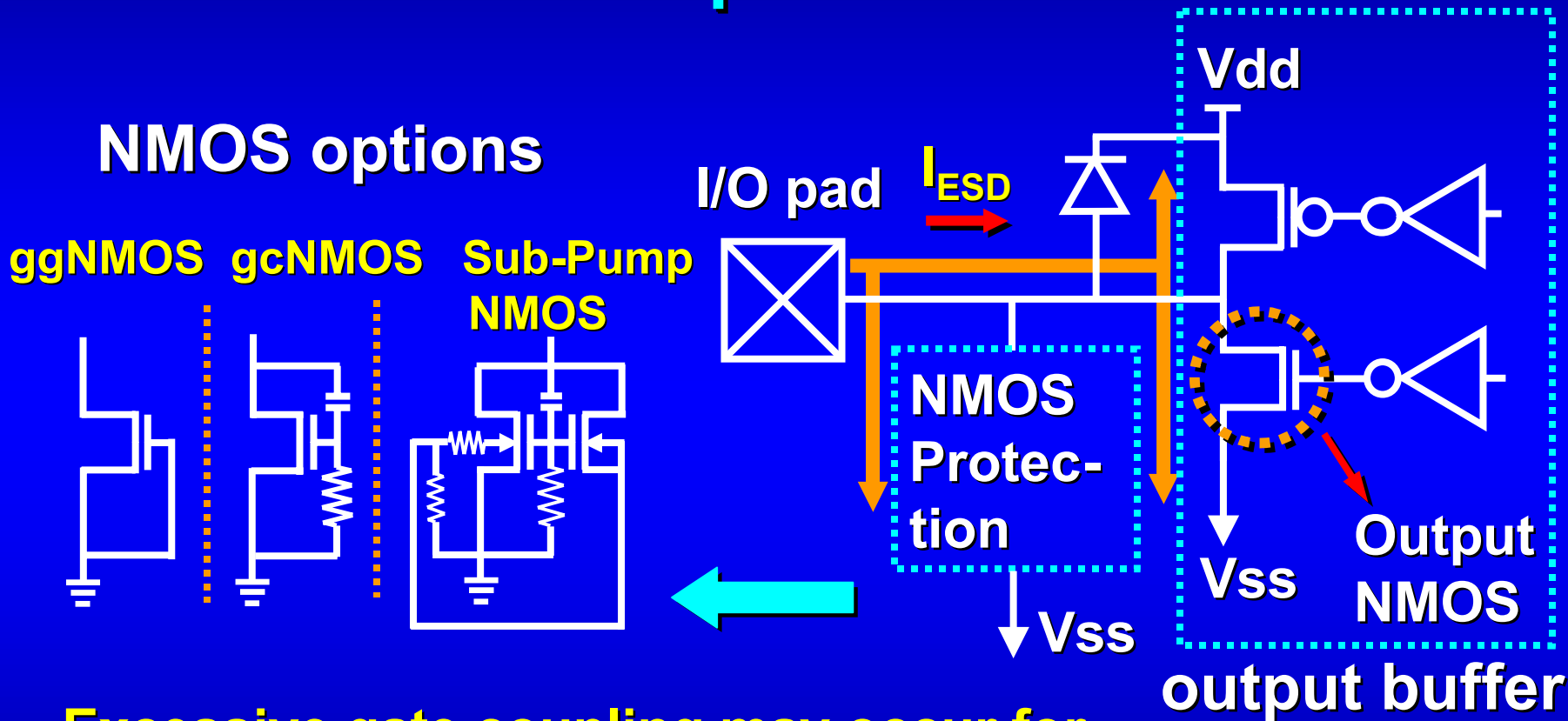
  Why does ESD performance degrade with high gate bias?

- To establish design guidelines that would be important for the ESD protection circuit designs

Outline

- Introduction
- Output NMOS Failure
- Experiments
- Simulations and Analysis
- Implications for ESD Protection
- Summary

Typical ESD protection design for Output Buffer



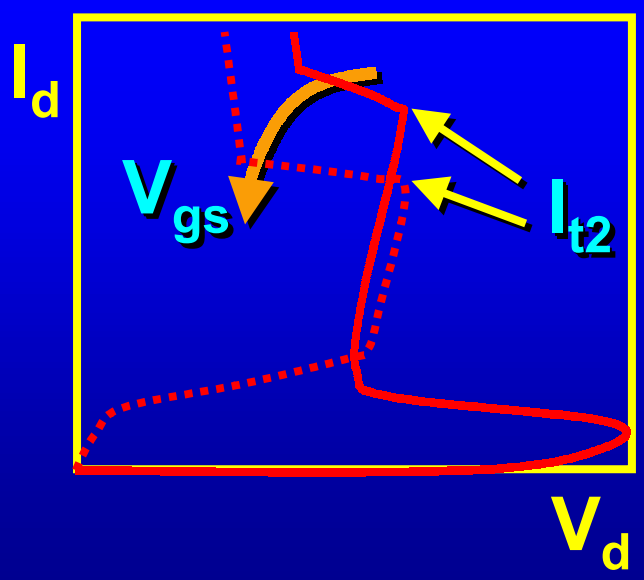
Excessive gate coupling may occur for output NMOS with Vdd charging through the diode

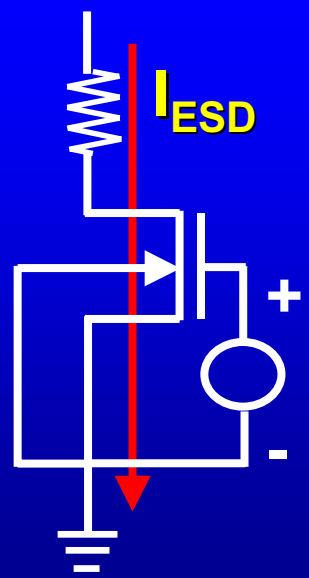
Introduction

- Under ESD conditions with high gate bias (excess gate coupling), the failure threshold current of the NMOS is known to degrade

  Polgreen et al., TED. 1992

  Chen et al., EOS/ESD Symp. 1997



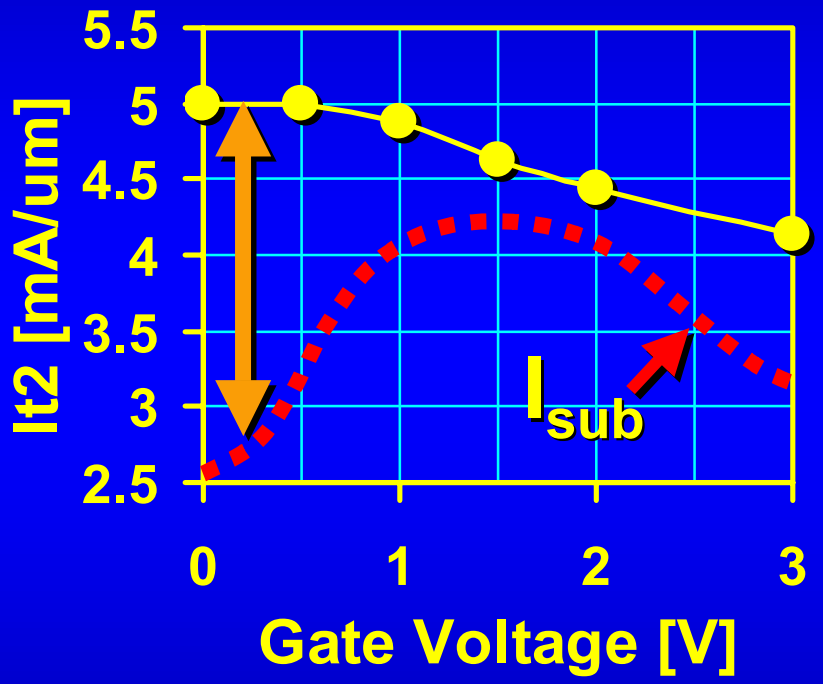


Introduction

- Degradation is technology dependent and its impact on protection designs have not been fully explored
- For advanced technologies, ESD strength degradation with high gate bias seems to depend on the finger width
- The finger width and substrate bias also determine the conduction uniformity and are important for overall protection design

  Oh et al., IRPS 2001

Second Breakdown Triggering Current (I_{t2}) with V_{gs} for silicided NMOS



Beyond 0.35μm tech.

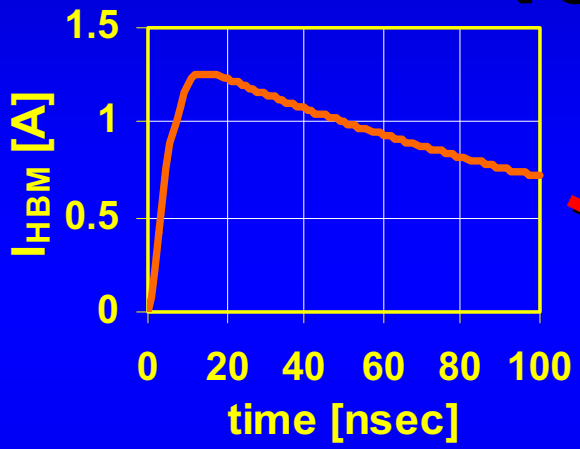
I_{t2} degradation doesn't follow the I_{sub} with low V_{gs}

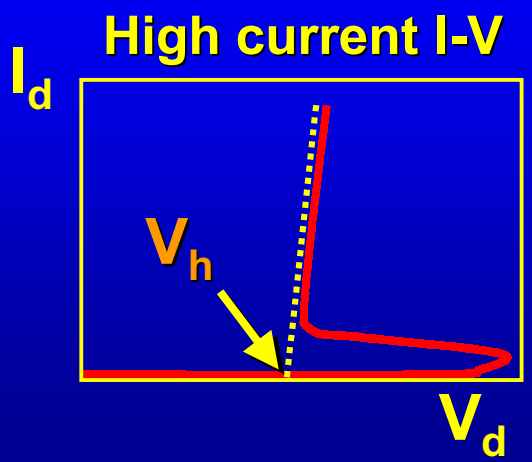
→Implying new physical mechanism

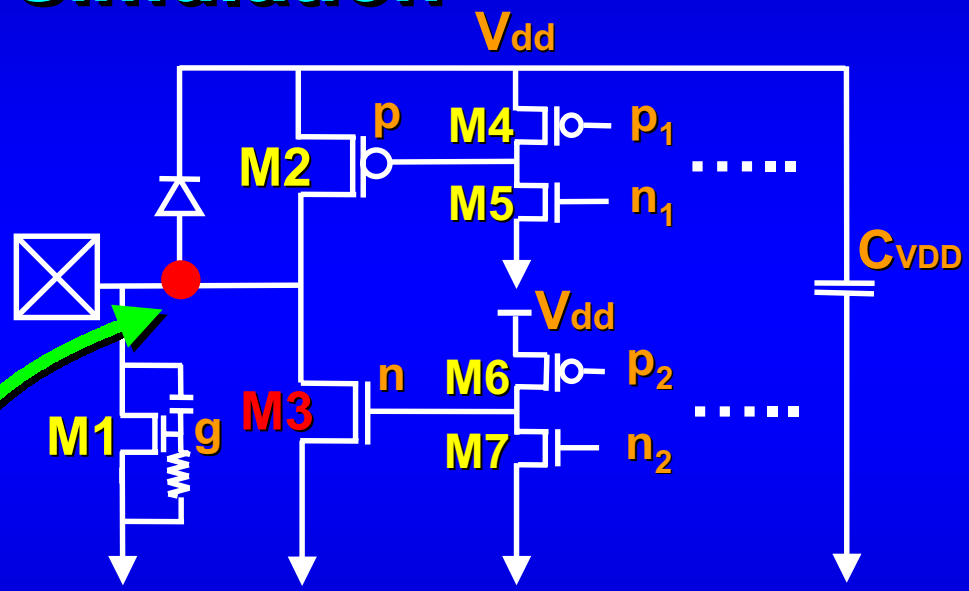
Need to identify main cause of this degradation for robust design of ESD protection

Output NMOS Failure

2KV Human Body Model (HBM) Test Simulation







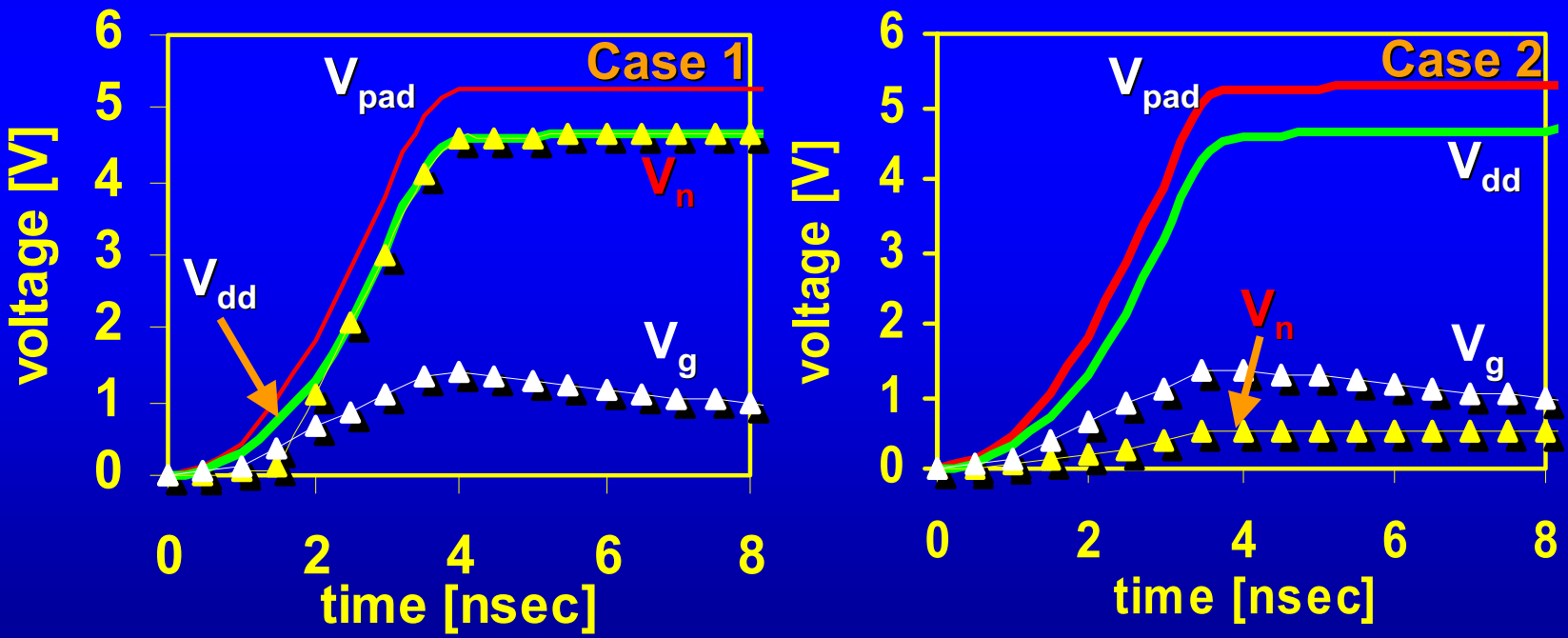
M1= 400/0.25
M3= 50/0.25
M5=M7=10/0.25

M2= 100/0.25
M4=M6=20/0.25

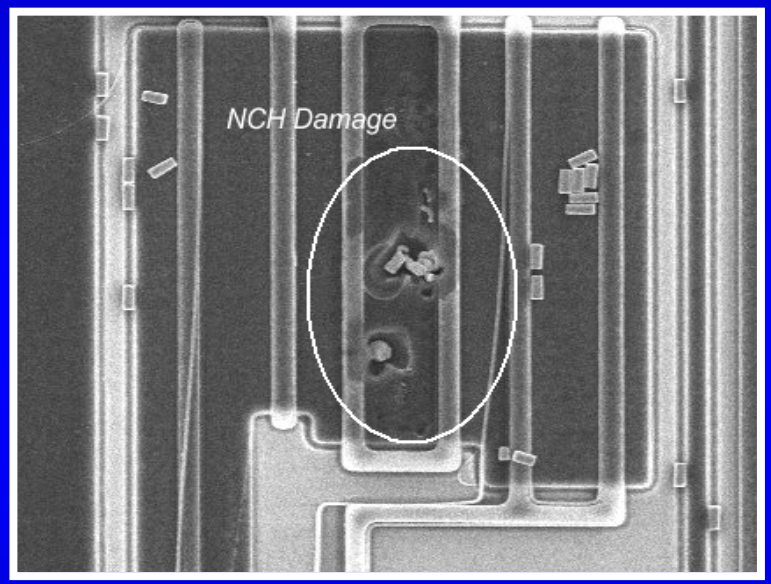
- Under HBM ESD stress, gate potential (V_n) of output NMOS may be higher than V_g, depending on the pre-drive circuit conditions

  → Output NMOS weaker than Protection NMOS

  - Case 1 : n_1, n_2, p_1, & p_2 → GND
  - Case 2 : n_1, n_2 → GND p_1, p_2 → V_{dd}



Failure of output NMOS due to excess gate coupling



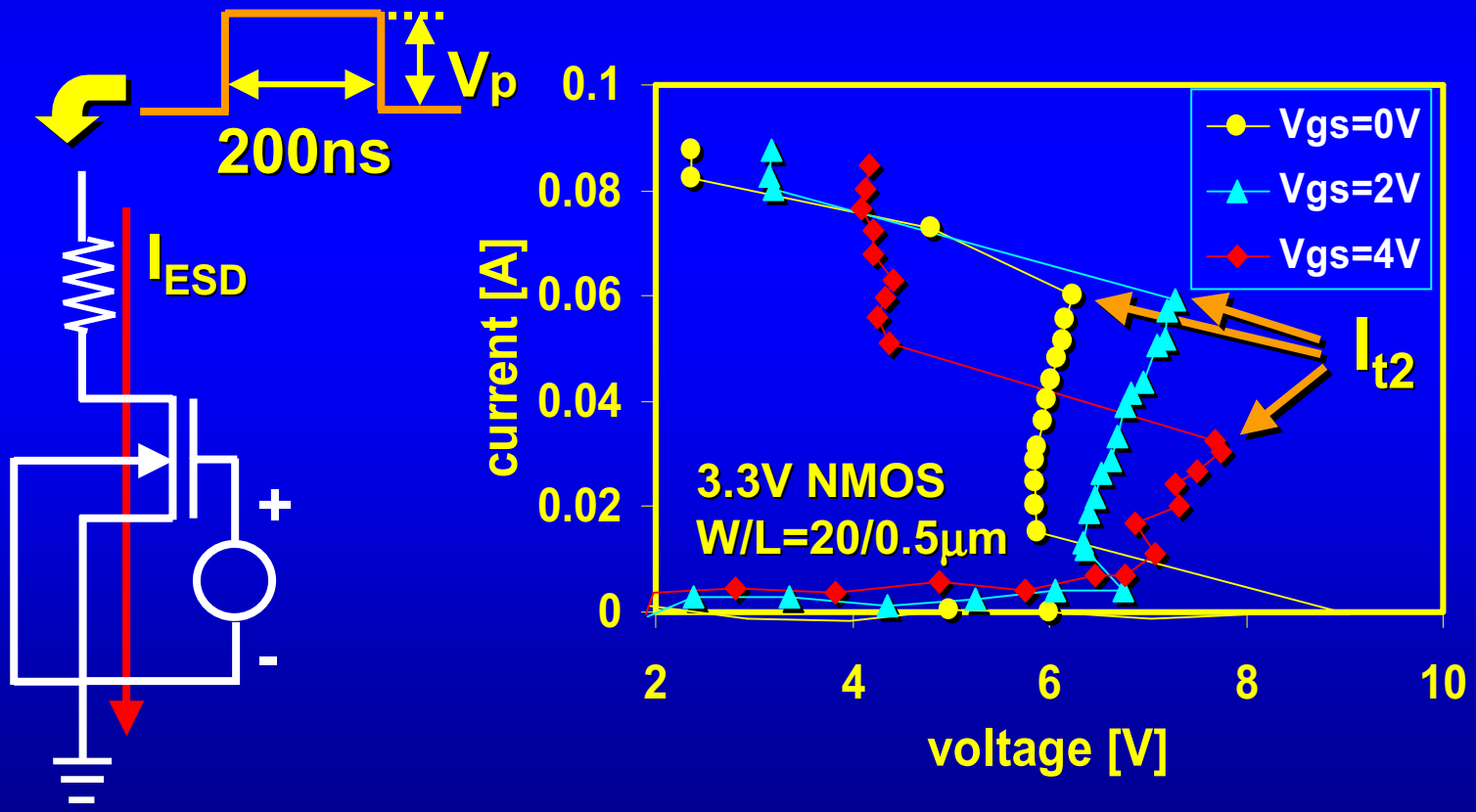
Failure of NMOS in HBM test

High gate coupling lowers ESD strength, output NMOS fails earlier than the protection device

Significantly reduces the effectiveness of the ESD protection design

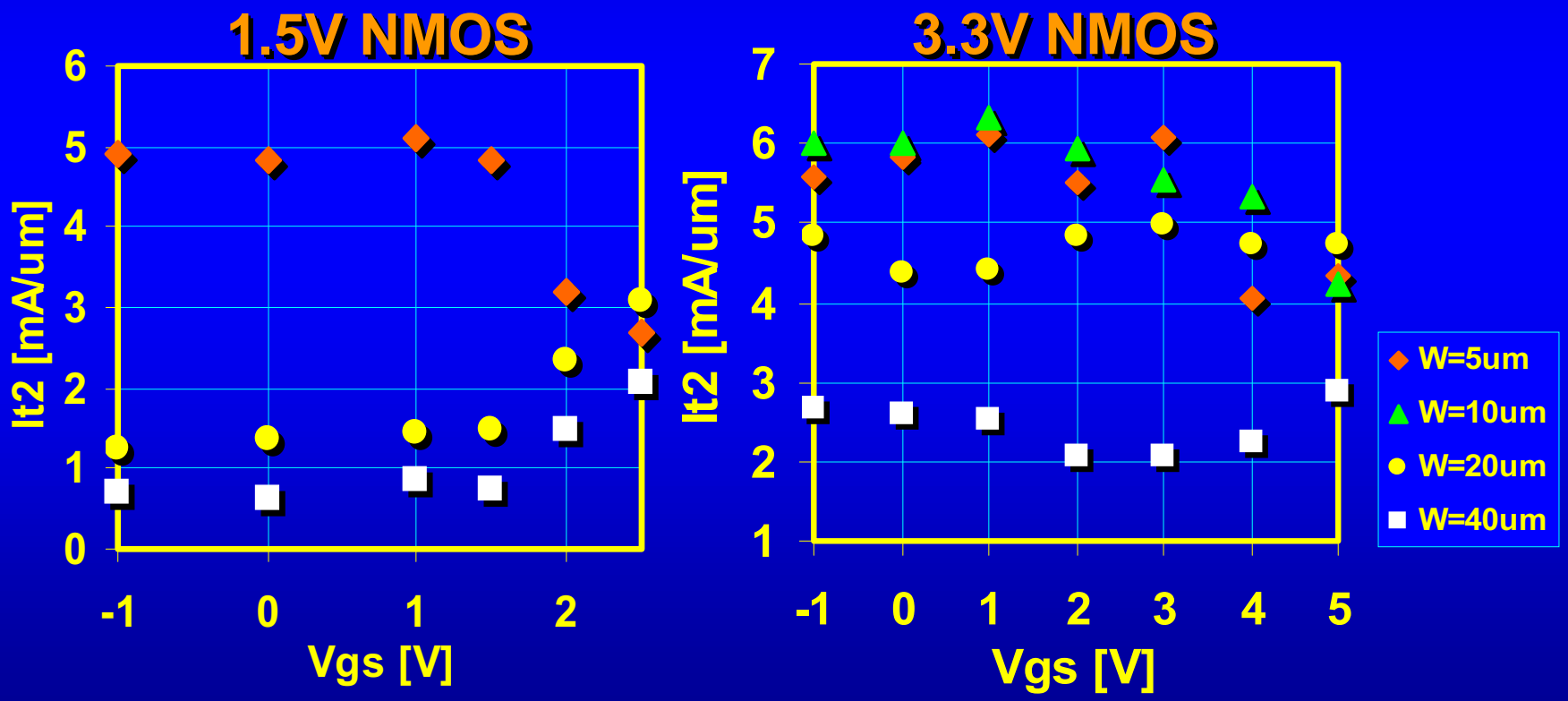
Experiments

Transmission Line Pulsing (TLP) Test for 1.5V & 3.3V NMOS for 0.13 μm tech.



I_{t2} with V_{gs}

- Impact of V_{gs} on I_{t2} depends on W_F despite different process and gate structures

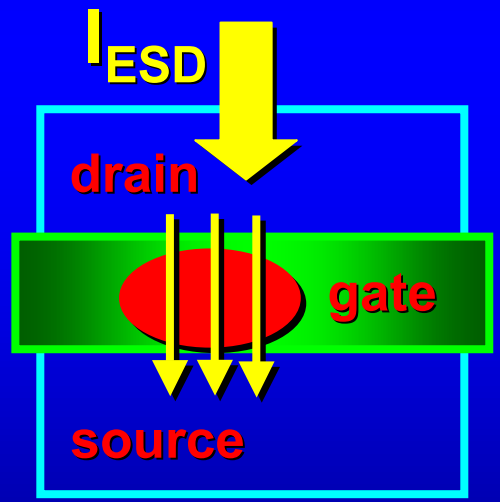


Width dependence of I_{t2} degradation

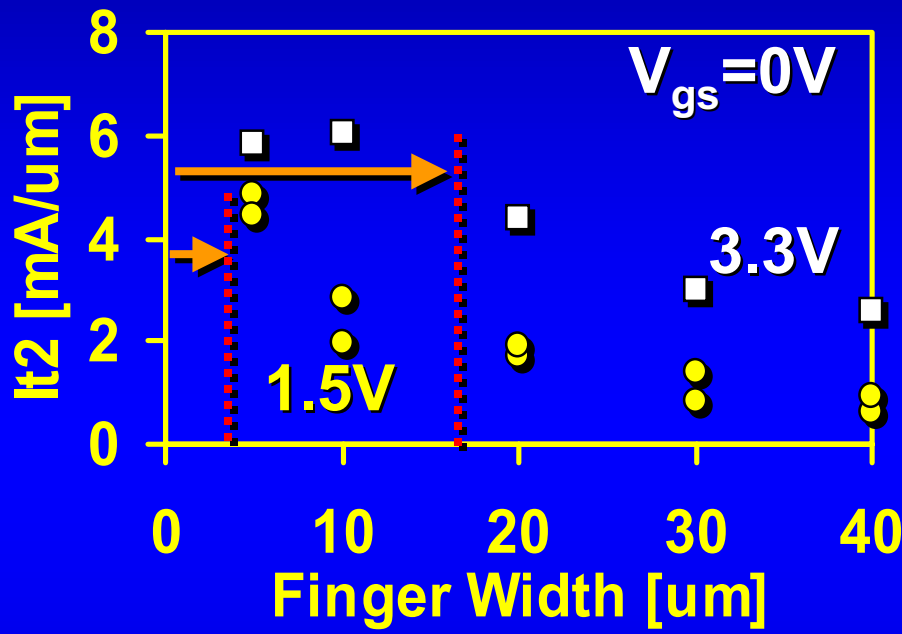
- I_{t2} improved for wide NMOS with V_{gs}
- I_{t2} reduced for narrow NMOS with V_{gs}
  → implying two competing mechanisms depending on W_F

- For advanced silicided wide finger width NMOS, I_{ESD} is non-uniform

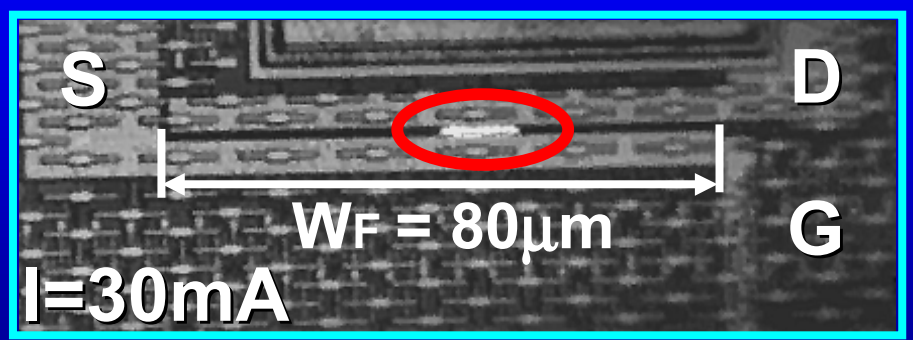
V_{gs} effects are influenced by the extent of lateral uniformity of I_{ESD}



Non-Uniform I_{ESD} Conduction



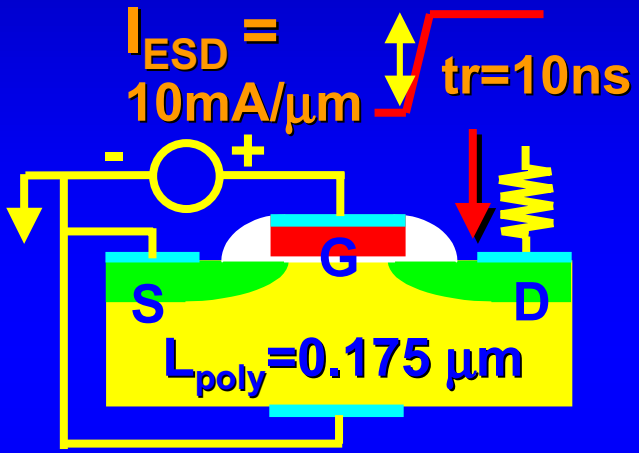
Non-uniform I_{ESD} conduction for the 0.13μm Technology

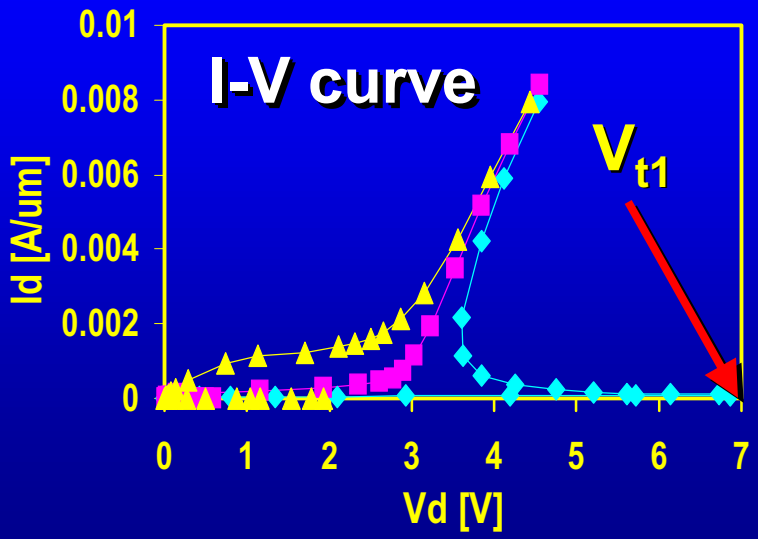


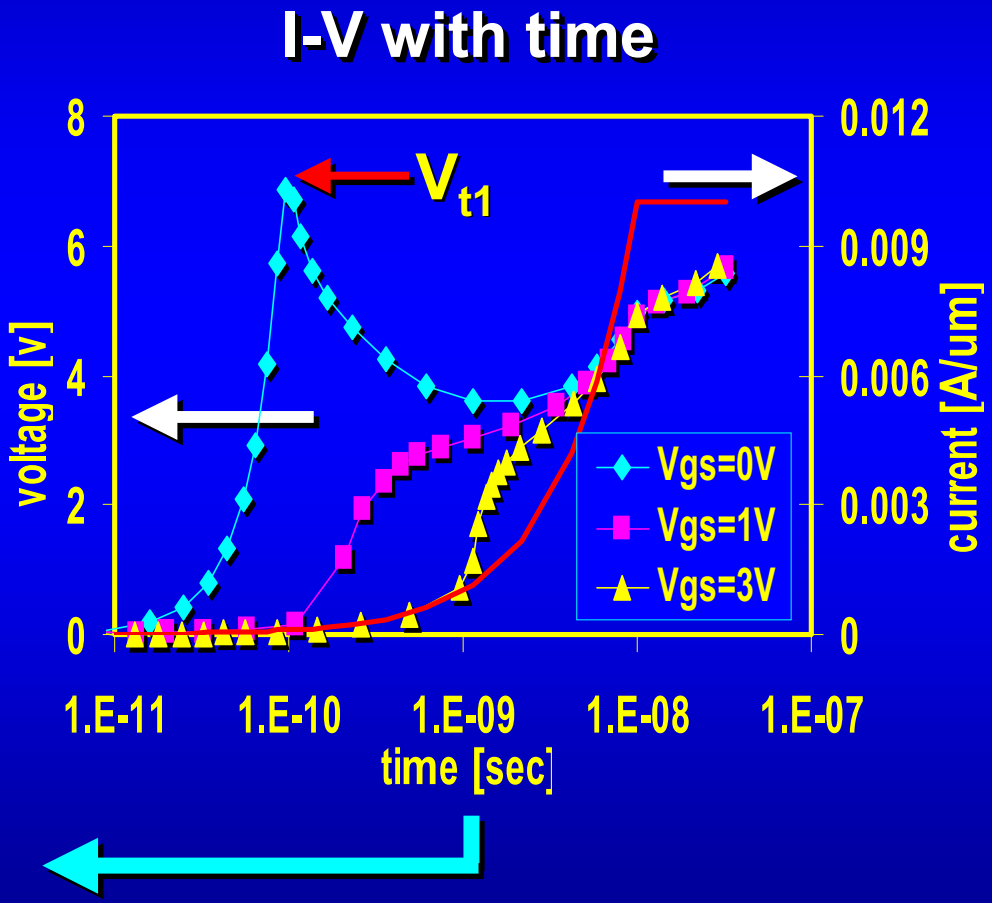
I_{ESD} distribution by EMMI (3.3V NMOS)

Simulations and Analysis

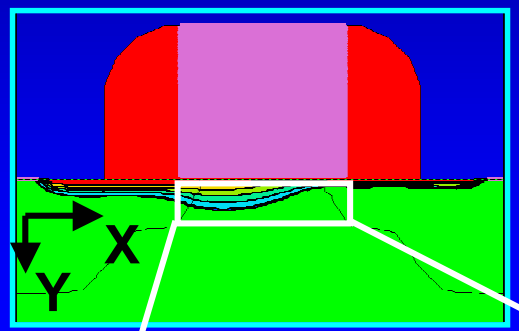
Mixed Mode Transient Simulation (@ t=10ns)

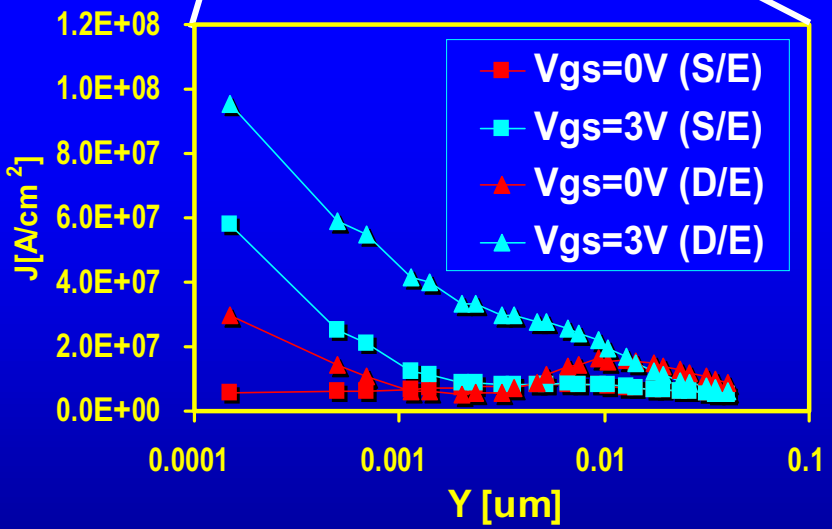


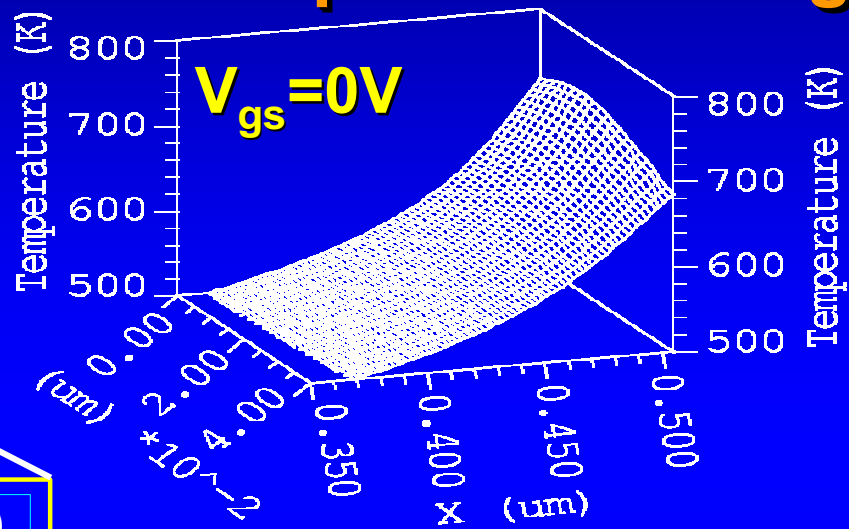


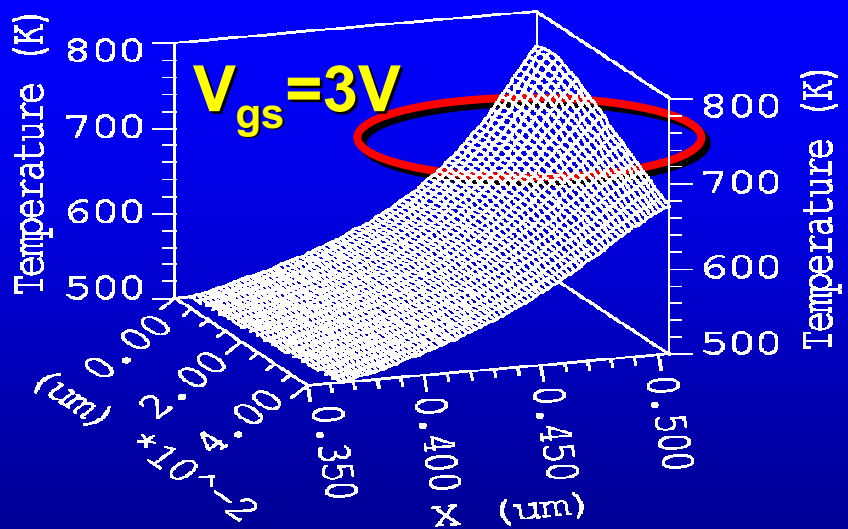


- Current density modulated by V_{gs} within channel area → **local temperature changes**

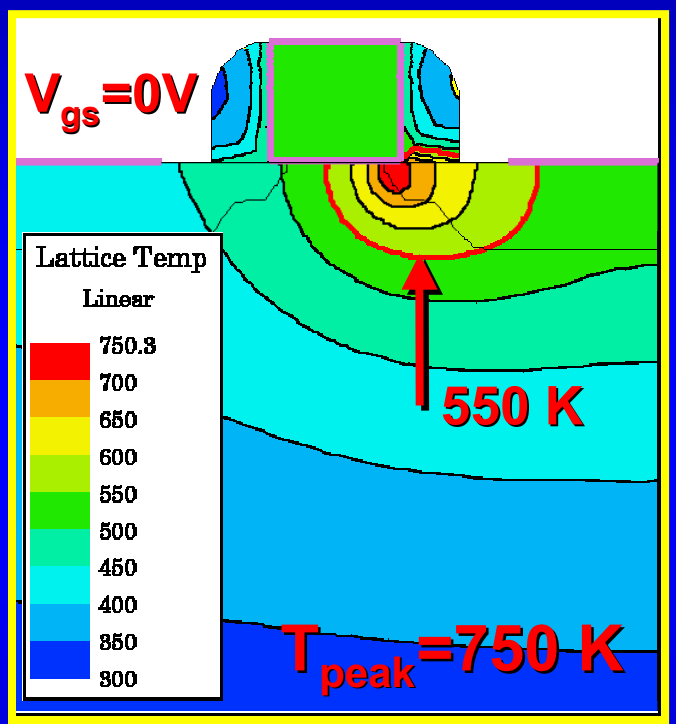


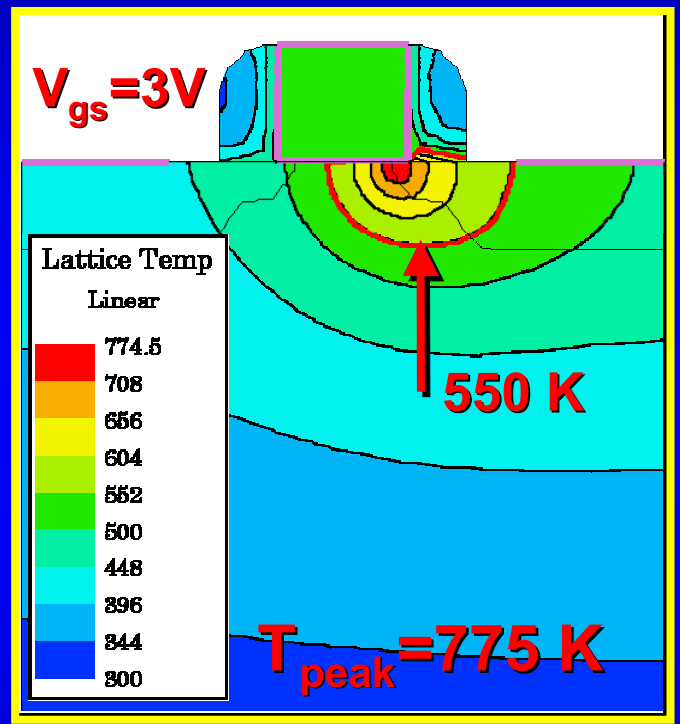


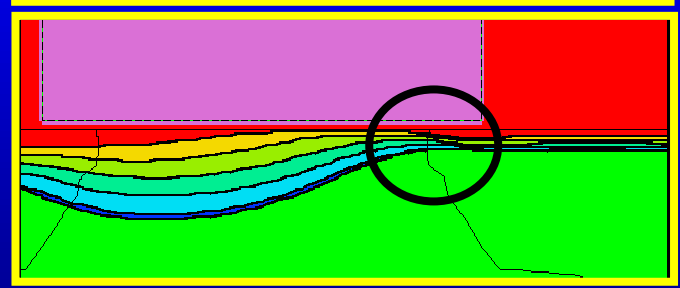




- As V_{gs} increases, temperature distribution more localized as well as T_{peak} gets higher

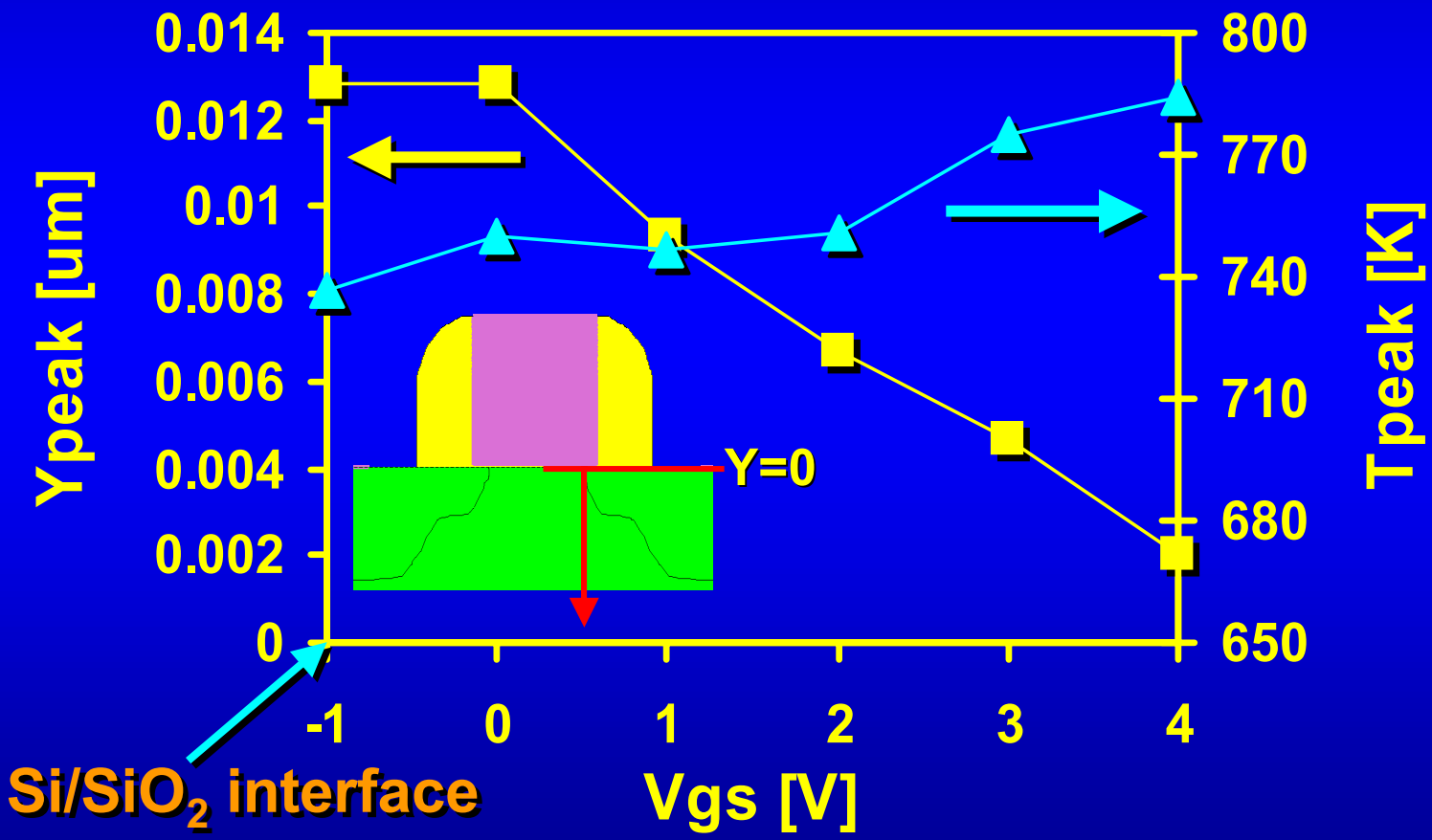






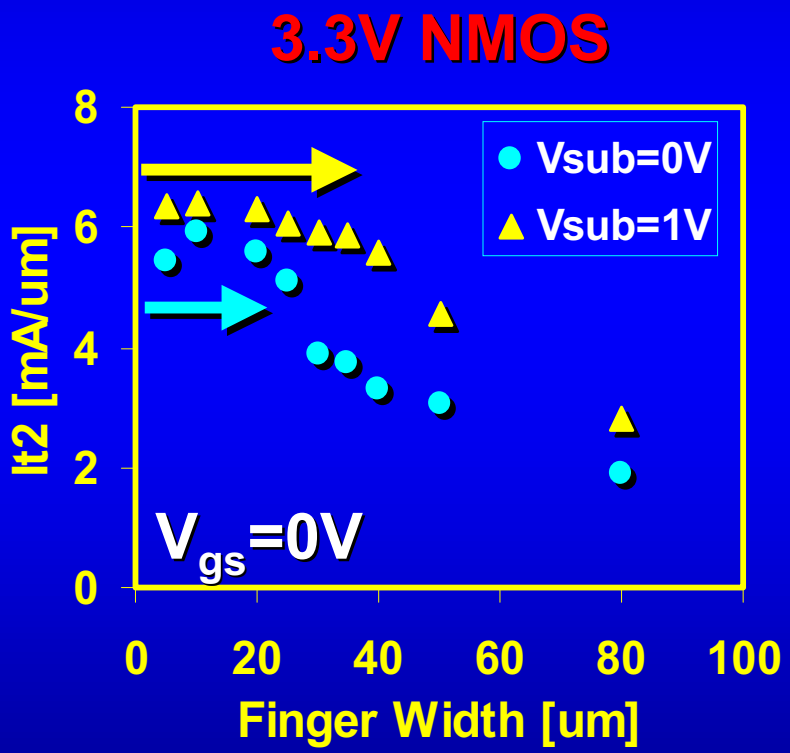
- In addition, location of T_{peak} moves closer to the surface with V_{gs}

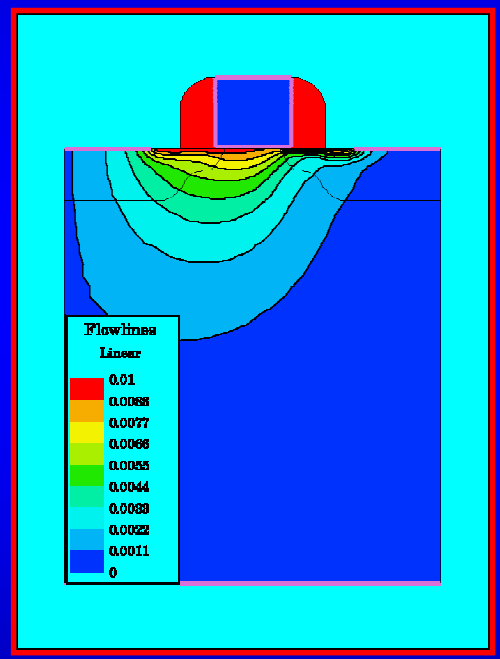
  → more vulnerable to surface damage



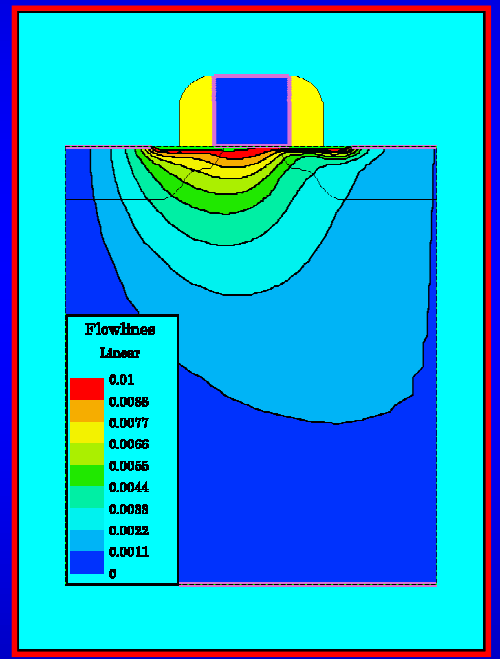
Impact of V_{sub}

- The turned on width increases with V_{sub} and I_{ESD} flows deeper into the substrate



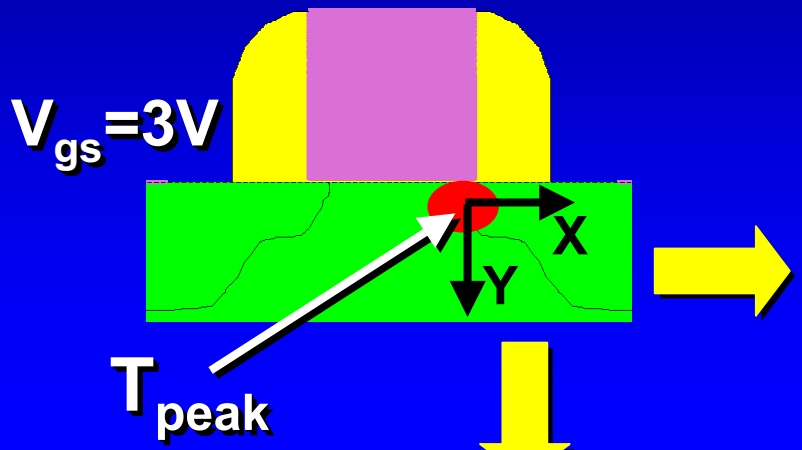


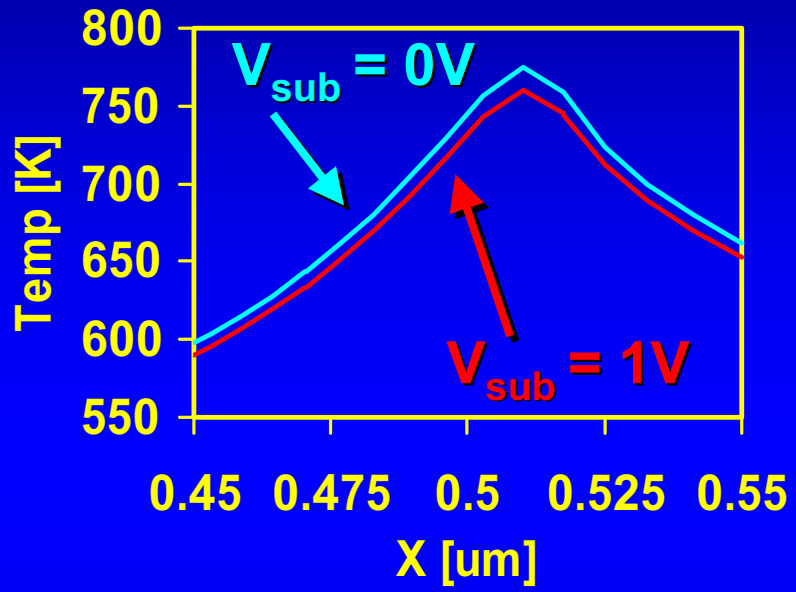
V_{gs} =3V
V_{sub}=0V

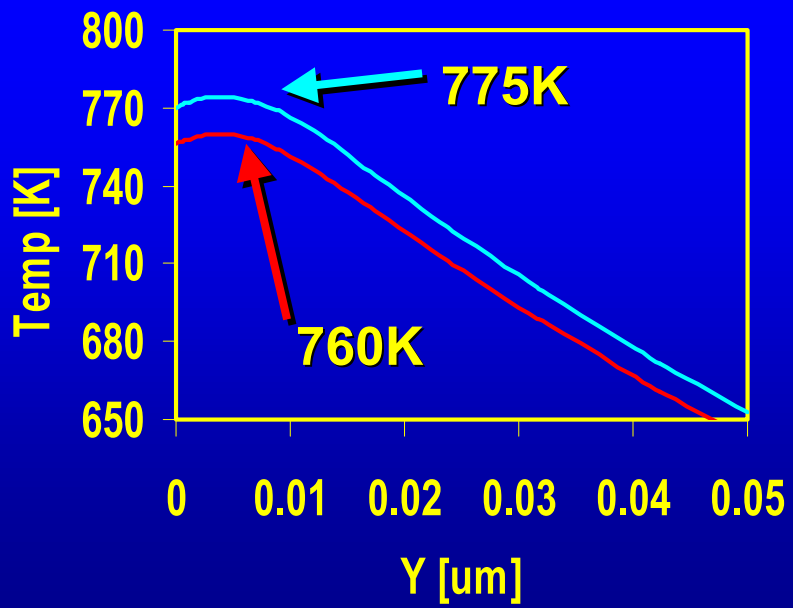


V_{gs} =3V
V_{sub}=1V

● Compensate for degradation of I_{t2} with V_{gs}





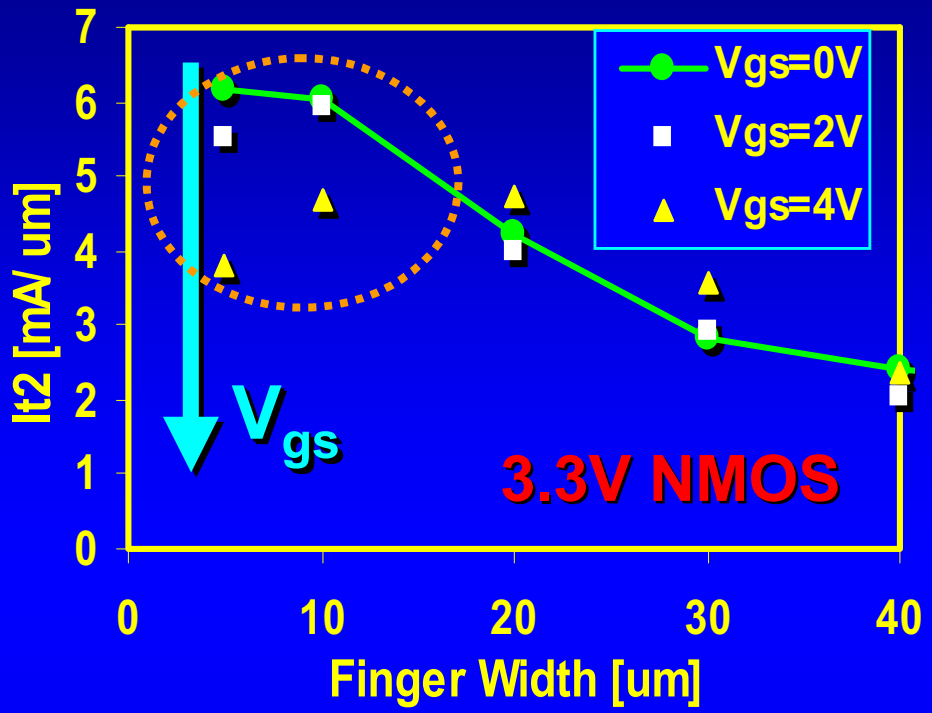


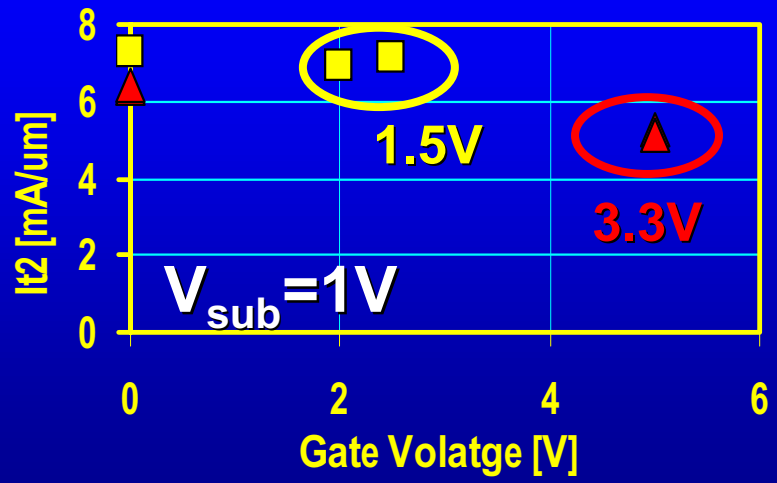
V_{gs} induced heating can be alleviated with V_{sub}

- Two competing mechanisms of gate bias effect depending on W_F

  For W_F where I_{ESD} is Uniform V_{gs} induced heating degrades I_{t2}

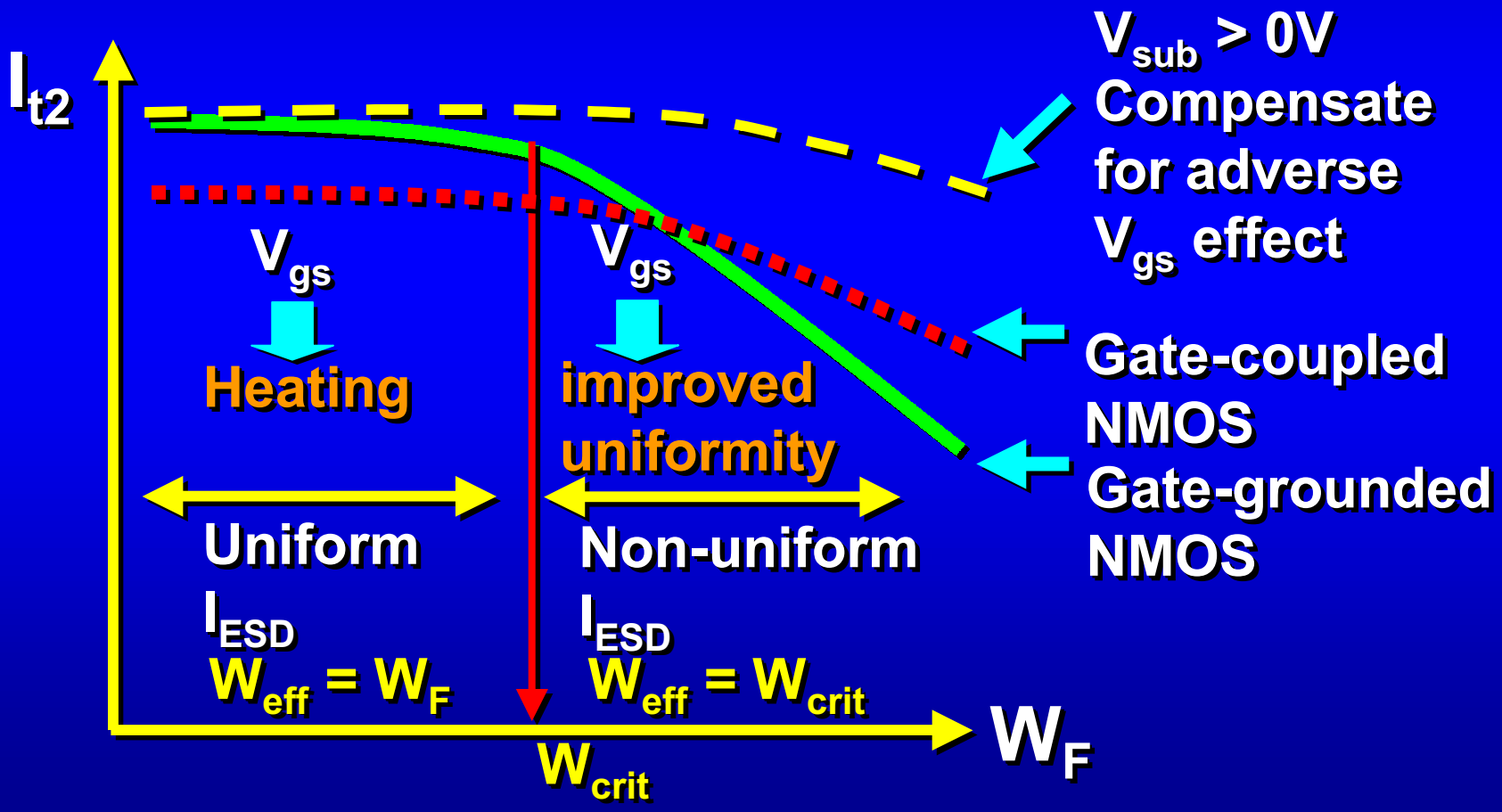
- Impact of V_{sub} on reduction of I_{t2} with V_{gs}





Implications for ESD Protection

Design Window for High Performance ESD Protection Devices



Design Consideration

- For the substrate trigger protection, ggNMOS can be used with V_{sub}
- For gcNMOS without V_{sub}, the gate should be designed with *R* & *C* to maintain gate bias below I_{t2} roll-off
- For the output NMOS, size should be carefully determined according to gate-coupling level (since no V_{sub} is available and gate-coupling is unpredictable)

Summary

- Investigated I_{t2} degradation with V_{gs} for advanced ESD protection design
- Gate bias induced heating effect is the root cause of I_{t2} reduction with V_{gs}
- Improved understanding and provided new insight into ESD protection
- Also, showed V_{sub} can compensate for the adverse V_{gs} effect
- Presented design windows for efficient and robust ESD protection