The Equivalence of van der Ziel and BSIM4 Models in Modeling the Induced Gate Noise of MOSFETs

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I. Introduction

The *de facto* industry standard model BSIM3 has not accounted for the induced gate noise. As CMOS is increasingly used for RF applications, it is apparent that the inclusion is necessary. The next generation model BSIM4 [1], [2] released for public use in March 2000, amends the shortcoming of BSIM3 by addressing the induced gate noise. The BSIM4 model shown in Fig. 1 (a), however, adopts a drastically different modeling strategy, in contrast to the van der Ziel model [3] shown in Fig. 1 (b), which is the well accepted model and has a solid physical basis. For examples, the gate current noise in the van der Ziel model is frequency dependent and correlated with the drain current noise. By contrast, the induced gate noise in BSIM4 is accounted for by a voltage noise source $\overline{v_{R_s}^2}$, which is frequency-independent, uncorrelated ($\overline{v_{R_s} i_{dp}^*} = 0$), and connected to the *source electrode* instead of the gate. Thus the BSIM4 approach has the advantage that it is easily implementable in typical SPICE simulators. However, it is important to validate whether the new approach is in fact equivalent to the van der Ziel model. This paper is the first independent study that identifies the physical relation between these two noise models and also compares their noise performance at the circuit level, with special emphasis on non-grounded source conditions, including four of the most common low noise amplifier architectures.

II. Physical Relation between the Two Models

Since the condition that $R_x \gg R_s$ is generally satisfied, this paper uses a simplified BSIM4 model shown in Fig. 1 (c), by assuming that the source resistance (R_s) can be neglected. To focus on the circuit equivalence issue, noise sources ($\overline{i_d^2}$, $\overline{i_g i_d^*}$, $\overline{i_g^2}$, $\overline{i_{dp}^2}$, $\overline{v_x^2}$) were simply considered as fitting variables, independent of bias or geometry effects described in Appendix I. Measured data is usually given in the form of *four noise parameters* [4], which describe the source-admittance dependence of the noise figure using four independent variables:

$$NF = NF_{min} + \frac{|Y_s - Y_{opt}|^2 R_n}{G_s} \quad (1)$$

where NF_{min} is the best performance that the circuit can achieve with the optimum source admittance condition ($Y_s = Y_{opt}$), and R_n determines the sensitivity of NF when Y_s differs from Y_{opt}. In conjunction with two-port network parameters, $NF_{min} - R_n - G_{opt} - B_{opt}$ is strictly equivalent to the intrinsic noise sources (see Appendix II).

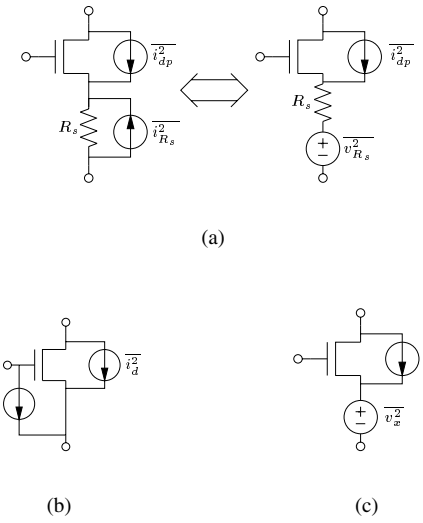


Fig. 1. MOSFET thermal noise models. (a) BSIM4 as implemented. (b) van der Ziel model. (c) Simplified BSIM4 (assuming R_s is negligible)

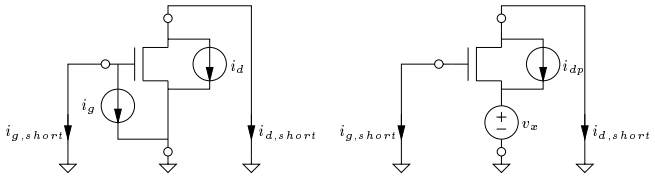
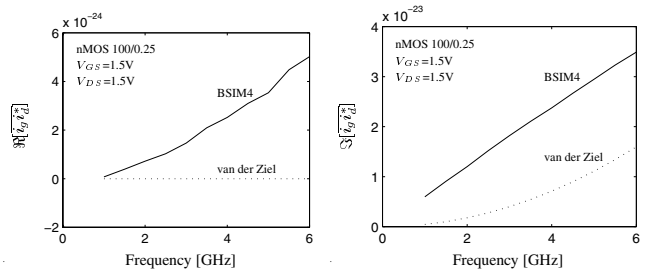


Fig. 2. Schematic for model comparison. (a) van der Ziel model (b) BSIM4.

In the case of MOSFETs, it is known that $\overline{i_g i_d^*}$ is almost purely imaginary; consequently NF_{min} becomes a dependent factor of R_n and G_{opt} [5]. Reducing the number of variables further, the BSIM4 formulation has assumed an additional relation[1] between noise sources. The underlying assumption of

[1]Pospieszalski has proposed another two-parameter noise model assuming $\overline{v_{in} i_{out}^*} = 0$ [6]. While it is well satisfied in GaAs devices [5], simple calculation shows that it is not applicable to MOSFETs.



(a) (b)

Fig. 3. Comparison for the correlated noise power spectrum. (a) real part (b) imaginary part.

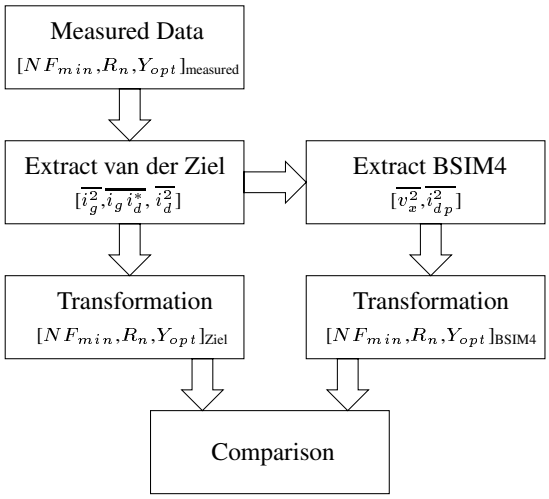


Fig. 4. Model comparison procedure.

the BSIM model can be identified by comparing the short-circuited noise current at two electrodes as shown in Fig. 2 (a) and (b):

$$i_{g,short} = -i_g = (Y_{11} + Y_{12})v_x \quad (2)$$

$$i_{d,short} = -i_d = (Y_{21} + Y_{22})v_x - i_{dp} \quad (3)$$

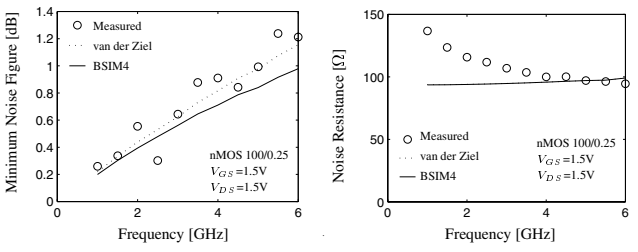
Thus the BSIM4 model replicates the frequency dependence and correlation of the induced gate noise as follows:

$$\overline{i_{g,BSIM4}^2} = |Y_{11} + Y_{12}|^2 \overline{v_x^2} \quad (4)$$
$$\approx \omega^2 C_{gs}^2 \overline{v_x^2}$$

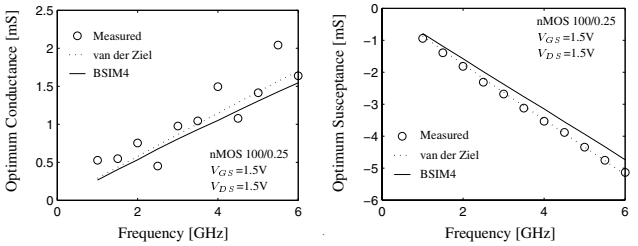
$$\overline{i_g i_{d,BSIM4}^*} = (Y_{11} + Y_{12})(Y_{21} + Y_{22})^* \overline{v_x^2} \quad (5)$$
$$\approx j g_m \omega C_{gs} \overline{v_x^2}$$

$$\overline{i_{d,BSIM4}^2} = |Y_{21} + Y_{22}|^2 \overline{v_x^2} + \overline{i_{dp}^2} \quad (6)$$
$$\approx g_m^2 \overline{v_x^2} + \overline{i_{dp}^2}$$

Equations (4) and (5) suggest that the BSIM4 model assumes



(a) (b)



(c) (d)

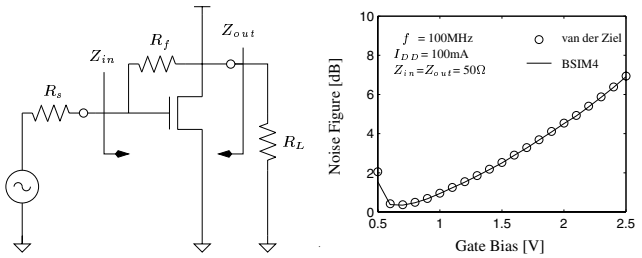
Fig. 5. Frequency dependence of four-noise parameters. Generated using noise sources extracted at 5GHz. (a) NF_{min} (b) R_n (c) G_{opt} (d) B_{opt}.

$\overline{i_g i_d^*} = \overline{i_g^2}(Y_{21} + Y_{22})^*/(Y_{11} + Y_{12})^*$, which usually causes errors in $\overline{i_g i_d^*}$ modeling as shown in Fig. 3.

III. Results and Discussion

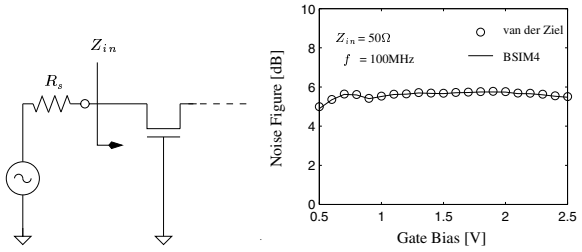
According to the two-port noise theory [7], the two models should yield exactly the same noise performance for various circuit topologies, as long as they reproduce the same four noise parameter sets. To examine the equivalence of the two models, measured four noise parameters are compared with ones that are reproduced by extracted noise sources. The procedure is illustrated in Fig. 4. First, noise sources for the van der Ziel model were extracted at 5GHz by directly converting the noise matrix. Second, noise sources of the BSIM4 model, the values of $\overline{v_x^2}$ of $\overline{i_{dp}^2}$, were chosen to fit $\overline{i_g^2}$ and $\overline{i_d^2}$ values, respectively. Then the extracted noise sources were extrapolated to other frequencies with measured s-parameters. For the van der Ziel model, $\overline{i_g^2}$ and $\overline{i_g i_d^*}$ were adjusted based on their frequency dependence. In Fig. 5, the frequency dependence of the four noise parameters are compared based on the noise sources extracted at 5GHz. These results demonstrate that the frequency independent noise source $\overline{v_x^2}$ reproduces the behavior of the frequency dependent noise $\overline{i_g^2}$ at the device level. Since R_n is determined by $\overline{i_d^2}$, both models should yield exactly the same value in Fig. 5 (b). The error in $\overline{i_g i_d^*}$ term leads to discrepancies in other parameters in Fig. 5 (a), (c), and (d) but the differences are acceptably small.

Next, turning to actual circuit applications, the noise fig-



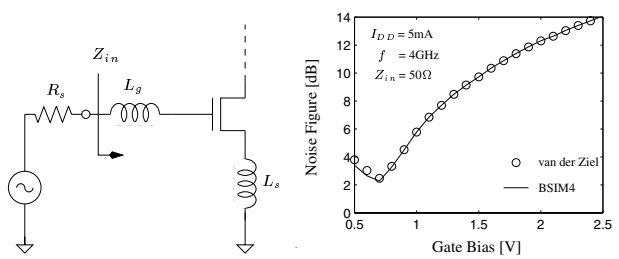
(a) (b)

Fig. 6. Shunt-series feedback broadband amplifier. (a) Architecture (b) Power-constrained noise performance.



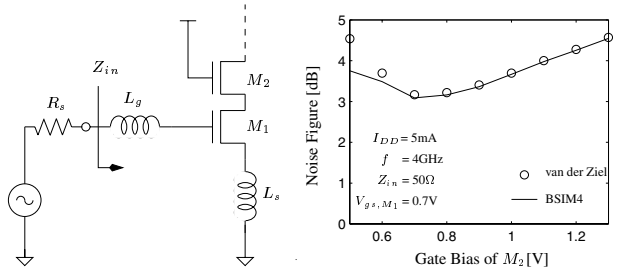
(a) (b)

Fig. 7. $1/g_m$ termination broadband amplifier. (a) Architecture (b) Noise performance.



(a) (b)

Fig. 8. Inductive degeneration tuned amplifier. (a) Architecture (b) Power-constrained noise performance.



(a) (b)

Fig. 9. Inductive degeneration tuned amplifier with cascode stage. (a) Architecture (b) Power-constrained noise performance.

ure is calculated for various circuit topologies using the noise analysis method for linear network described in Appendix II. Noise parameters are reproduced for the two models as described previously. Fig. 6 (a) shows a broadband amplifier with feedback (R_f) used to achieve impedance matching at input and output. In the case of van der Ziel model, the induced gate noise has negligible impact on the noise figure, up to moderately high frequencies. By contrast, the drain noise $\overline{i_{dp}^2}$ for BSIM4 is smaller by $g_m^2\overline{v_x^2}$ than $\overline{i_d^2}$ from van der Ziel model. However, the broadband contribution of $\overline{v_x^2}$ compensates for this difference. Thus both models yield the same overall noise performance. In other words, NF_{min} is close to zero in the frequency range below 1GHz; R_n is the same for both models; the key factor that differentiates the noise performance is Y_{opt}. In Fig. 6 (b), $Y_{opt} \ll 1/50$ except for the very low gate bias range, thus both models yield the same results.

Another broadband amplifier architecture, whose input impedance is adjusted by its g_m, is shown in Fig. 7 (a). BSIM4 again exhibits an identical noise figure in Fig. 7 (b), with the same physical differences as noted above. This case validates the non-grounded source condition of operation.

A good example that highlights the impact of induced gate noise is the power-constrained design of the tuned amplifier, illustrated in Fig. 8 (a). Usually this architecture exhibits valley-shaped noise characteristics for a power-constraint as shown in Fig. 8 (b); the drain noise is dominant as the gate bias becomes lower while the induced gate noise becomes dominant at high gate bias. The correlated term $\overline{i_g i_d^*}$ affects the noise performance at low gate bias but it is less significant than the drain noise [9]. Therefore the noise figure shows excellent agreement and again validates further the non-grounded source conditions in modeling noise. This can be also explained based on the four noise parameters. When the gate bias is high, the mismatch of Y_{opt} to Y_s is so large that the noise performance (1) can be approximated as:

$$NF \approx \frac{|Y_s|^2 R_n}{G_s} \tag{7}$$

As the gate bias becomes lower, Y_{opt} gets closer to Y_s so imperfect reproduction of noise parameters in Fig. 5 results in observable differences. These differences become more noticeable when the cascoded stage is taken into account as shown in Fig. 9. Nevertheless, the error is acceptably small.

IV. Conclusion

This paper is the first independent comparison between BSIM4 and the van der Ziel models for induced gate noise.

Despite the very different modeling strategies, BSIM4 successfully reproduces the classical van der Ziel model, introducing only small errors in the correlated noise term. In the case of practical circuits, noticeable errors usually arise for very low gate bias conditions yet the errors are acceptably small. Therefore, the two models can be considered as being equivalent to each other in most practical circuits, including non-grounded source conditions of operation.

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APPENDIX I : NOISE MODEL DESCRIPTIONS

A. van der Ziel Model

$$\overline{i_d^2} = 4\,k\,T\,\Delta f\,\gamma\,g_{d0} \quad (8)$$

$$\overline{i_g^2} = 4\,k\,T\,\Delta f\,\delta\,g_g \quad (9)$$

$$\overline{i_g i_d^*} = c\,\sqrt{\overline{i_g^2}\,\overline{i_d^2}} \quad (10)$$

B. BSIM4 Model [1], [2]

$$\overline{i_{dp}^2} = 4kT\Delta f\frac{V_{DS,eff}}{I_{DS}}(\beta g_m + \beta g_{mb} + g_d)^2 - 4kT\Delta f R_x(g_m + g_{mb} + g_d)^2 \quad (11)$$

$$\overline{v_{R_s}^2} = 4kT\Delta f(R_x + R_s) \quad (12)$$

$$R_x \triangleq \theta^2\frac{V_{DS,eff}}{I_{DS}} \quad (13)$$

$$\beta \triangleq 0.577\left[1 + \text{TNOIA}\ L_{eff}\left(\frac{V_{GST,eff}}{\mathcal{E}_{sat}L_{eff}}\right)^2\right] \quad (14)$$

$$\theta \triangleq 0.37\left[1 + \text{TNOIB}\ L_{eff}\left(\frac{V_{GST,eff}}{\mathcal{E}_{sat}L_{eff}}\right)^2\right] \quad (15)$$

APPENDIX II : NOISY TWO-PORT

It is known that any noisy two-port can be represented by a noiseless two-port and its corresponding two noise sources [7]. Depending on the type of noise sources, many representations can be derived but the following three representations are particularly useful: admittance for parallel, impedance for series, and ABCD for cascade connection [8].

$$\boldsymbol{C}_Y \triangleq 2kT\Re[Y] \quad (16)$$

$$\boldsymbol{C}_Y = \boldsymbol{C}_{Y_1} + \boldsymbol{C}_{Y_2} \quad (17)$$

$$\boldsymbol{C}_Z \triangleq 2kT\Re[Z] \quad (18)$$

$$\boldsymbol{C}_Z = \boldsymbol{C}_{Z_1} + \boldsymbol{C}_{Z_2} \quad (19)$$

$$\boldsymbol{C}_A \triangleq 2kT\begin{bmatrix} R_n & \frac{F_{min}-1}{2} - R_n Y_{opt}^* \\ \frac{F_{min}-1}{2} - R_n Y_{opt} & R_n|Y_{opt}|^2 \end{bmatrix} \quad (20)$$

$$\boldsymbol{C}_A = \boldsymbol{A}_1\boldsymbol{C}_{A_2}\boldsymbol{A}_1^\dagger + \boldsymbol{C}_{A_1} \quad (21)$$

where † denotes the transpose conjugate.

Each representation can be transformed into another by a matrix operation:

$$\boldsymbol{C}' = \boldsymbol{T}\boldsymbol{C}\boldsymbol{T}^\dagger \quad (22)$$

where $\boldsymbol{C}$ and $\boldsymbol{C}'$ are the noise correlation matrices of the original and resulting representations respectively, $\boldsymbol{T}$ is the transformation matrix given in the following table.

		Original Representation		
		Admittance	Impedance	ABCD
Resulting Representation	Admittance	$\begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix}$	$\begin{bmatrix}y_{11} & y_{12}\\ y_{21} & y_{22}\end{bmatrix}$	$\begin{bmatrix}-y_{11} & 1\\ -y_{21} & 0\end{bmatrix}$
	Impedance	$\begin{bmatrix}z_{11} & z_{12}\\ z_{21} & z_{22}\end{bmatrix}$	$\begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix}$	$\begin{bmatrix}1 & -z_{11}\\ 0 & -z_{21}\end{bmatrix}$
	ABCD	$\begin{bmatrix}0 & a_{12}\\ 1 & a_{22}\end{bmatrix}$	$\begin{bmatrix}1 & -a_{11}\\ 0 & -a_{21}\end{bmatrix}$	$\begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix}$

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