Hot Electron Transistors on Silicon Substrate (HESS)– A Computational Prototyping

Edwin C. Kan, Gyo-Young Jin and Robert W. Dutton
Center for Integrated Systems, Stanford University
AEL 201, Stanford University, Stanford, CA 94305

Abstract

Operational principles of hot electron transistors based on the real space transfer effect are examined. New device configurations on silicon substrate without use of heterojunctions are proposed. Design trade-offs for different operating conditions are briefly summarized. The new designs are computationally prototyped by a full-band Monte Carlo device simulator.

Introduction

Device operations based on hot electrons are promising for high-speed electronics. There are mainly two types of hot electron transistors. The first type is similar to a bipolar transistor. However, the carrier injection from emitter to base is not by a forward-bias p-n junction, but by hot carriers over a barrier through emission or tunneling [1, 2]. This type of hot electron transistors can be well modeled by 1-D analyses with detailed considerations on scattering rate [3]. In this paper, we will however focus on the other type of hot electron transistors based on the real space transfer effect [4], which is inherently two dimensional: heating of electrons in one direction, and a barrier in another orthogonal direction to sift hot electrons. In the first implementation by CHINT (CHarge INjection Transistor)[5], the electrons are initially confined by the potential well formed by AlGaAs/GaAs, InGaAs/InAlAs or SiGe/Si semiconductor heterojunctions, and some electrons heated by the channel electric field will overcome the perpendicular potential barrier and be collected by the substrate contact. The operating principles are very similar to those of vacuum tubes, but the electron gas can be heated or cooled much faster (subpicosecond range) than the lattice gas. In the following we will discuss other possible implementations, particularly on using only the silicon technology without heterojunctions. Since hot carriers far away from thermal equilibrium need to be accurately accounted for to model the basic transistor operations (in comparison, the hot carrier effects in MOSFET and BJT can be treated by modification or perturbation to the carriers still quite close to thermal equilibrium), DAMOLCES, a full-band Monte Carlo device simulators with detailed scattering rate calculations [7, 8], is used for computational prototyping.

Device Considerations

The ideal way to build the hot electron transistors is that the barrier will also serve to confine the carriers in the carrier hearter. This is what had been achieved in the CHINT implementation [5], where the wide bandgap material is virtually undoped (or selectively doped to control the input/output current ratio) and the narrow band gap material forms an nin structure. The spill-over free electrons pulled in by the built-in and applied fields will be confined in the narrow bandgap material close to the interface, even with a negative voltage applied to the wide bandgap substrate contact. Also, cold electrons will still encounter a significant barrier with positive substrate bias to minimize waste output current. III-V semiconductor systems have very good interface properties and the barrier height can be tuned easily from material composition. For CHINT, the hot electrons flow close to the barrier interface (however, the confining field is less effective to confine hot electrons) and hence minimizing the drift time of hot electrons over the barrier. In fact, the real space transfer is so effective in this design that large peak-to-valley ratio of negative differential resistance (NDR) is developed [6]. However, AlGaAs/GaAs technology is expensive and difficult for IC applications, and NDR is usually hard to control in digital design. Besides the implementation used in CHINT, where carrier heating is achieved through the space-charge-limited current and barrier through heterojunctions, there are other possibilities for carrier heaters and barriers. For heating, the reverse-bias current of p-n junctions is also very effective, although the current will be small before junction avalanche. Tunneling electrons from another barrier (such as in quantum yield measurement) can be of high energy, and this implementation will become similar to that used in the first type of hot electron transistors. Tunneling electrons in a Zener breakdown diode can be a very effective hot electron source. For barriers, semiconductor-insulator interface, semiconductor-metal Schottky interface and fully depleted p-n junction (similar to the camel barrier [2]) are other possible candidates. The semiconductor-insulator barrier is usually rather high (above 2.5eV) and requires a strong electron heater, while the Schottky barrier height is usually medium (from 0.5 to 0.9 eV), and most carrier heating mechanisms should be effective enough. Possible implementations of the Hot Electron on Silicon Substrate (HESS) transistors are summarized in Table 1. However, there are several nonideal features for these alternatives. The electrons will not be naturally confined to the interface if negative (and small positive) collector bias is applied. The Schottky barrier will further suffer from the leakage current, which will need even more careful control on the collector bias. These nonidealities will make the HESS transistor have smaller operating ranges. However, as shown in the next section, there are still windows for transistor functions.

Computational Prototyping

Device simulation of CHINT has been performed in [9]. The heterojunction transport is treated with self-consistent thermionic emission. The HESS transistors requires more flexible boundary conditions (the Schottky and semiconductor/insulator interface transport) and more accurate estimation of hot electrons with careful band and scattering calculations since the barrier is higher. The full-band Monte Carlo device simulator DAMOCLES [8] is chosen as the computational prototyping tool for the HESS transistors. The simulation structure is shown in Figs. 1 and 2, where we use an nin structure as the heater and a Schottky contact as the barrier. In this example, the operating range needs to be more carefully chosen. The conduction band contour is shown in Fig. 3. It can be clearly seen that the collector contact has formed a barrier. Fig. 4 is a cross-section at $y = 0$ in Fig. 3 together with the electrons (the kinetic energy is the distance between electrons and the conduction band) It can be seen that electrons will become hotter close to the drain n^+ region and may overcome the Schottky barrier. The electron concentration and energy are shown in Figs. 5 and 6, respectively. Figure 7 shows the distribution function in the vicinity of the collector contact.

Conclusions

Feasibility of the HESS transistor is demonstrated with the device Monte Carlo simulator. More work is necessary to characterize the transistor behavior. Other possible implementations of the HESS transistor is under investigation. Fabrication of test devices is planned in the future. The strategy for simulating the hot electron transistors is also briefly summarized.

Acknowledgement

This work has been supported through ARPA Contract # DABT63-94-C-0055 (Computational Prototyping of 21st Century Semiconductors). We also gratefully acknowledge the support of IBM in providing DAMOCLES for use in this research as well as in support of the National Center for Computational Electronics (NCCE–NSF Contract # ECS-9200560).

References

[1] S. M. Sze, *Physics of Semiconductor Devices, 2nd Ed.*, New York: John Wiley & Sons, 1981, p. 184.

[2] M. Heiblum, "Hot Electron Transistors, " *Proc. IEEE Conf. High-Speed Semiconductor Devices and Circuits (Cornell)*, 1985, pp. 24-34.

[3] D. C. Herbert, "Structured-base hot-electron transistors: I. Scattering rates, " *Semicond. Sci. Technol.*, vol. 3, pp. 101-110, 1988.

[4] K. Hess, *Advanced Theory of Semiconductor Devices,* New Jersey: Prentice Hall, 1988, Chap. 15.

[5] S. Suryi, A. Kastalsky, A. C. Gossard and R. H. Hendel, "Charge Injection Transistor Based on Real-Space Hot-Electron Transfer, " *IEEE Trans. Electron Dev.*, vol. ED-31, no. 6, pp. 832-839, June 1983.

[6] P. M. Mensz, P. A. Garbinski, A. Y. Cho, D. L. Sivco and S. Luryi, "High transconductance and large peak-to-valley ratio of negative differential conductance in three-terminal InGaAs/InAlAs real-space transfer devices, " Appl. Phys. Lett., vol. 57, p. 2558, 1990.

[7] M. V. Fischetti, "Monte Carlo simulation of transport in technologically significant semiconductors of the diamond and zinc-blende structures - Part I: homogeneous transport, " IEEE Trans. Electron Devices, vol. 38, pp. 634-649, 1991.

[8] S. E. Laux and M. V. Fischetti, *DAMOCLES 1.5 User's Guide*, IBM Research Division, 1994.

[9] M. R. Pinto and S. Luryi, "Simulation of multiply connected current-voltage characteristics in charge injection transistor, " *IEDM Tech. Dig.*, 1991, p. 507.

	Barrier			
Heater	heterojunction	pn junction (camel)	semicond./ins.	Schottky
nin	CHINT	$\surd$	X	$\surd$
pn (avalanche)	X	X	$\surd$	$\surd$
pn (Zener)	X	X	$\surd$	$\surd$

Table 1: Possible HESS transistor implementations.

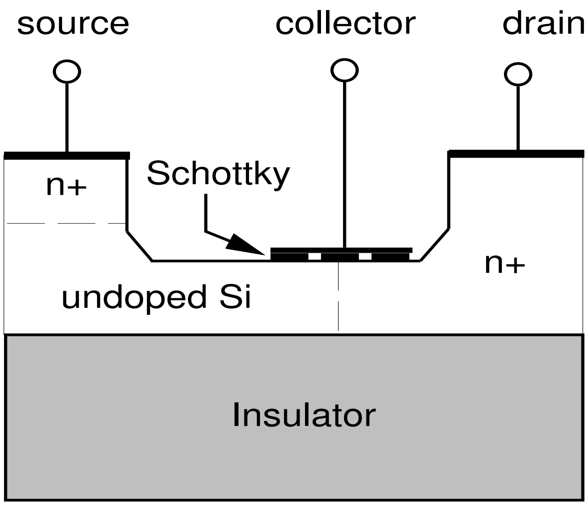

Fig. 1: Device 1 is a modified MESFET structure. Electrons are heated by the space-charge-limited current and the barrier is formed by the metal Schottky contact.

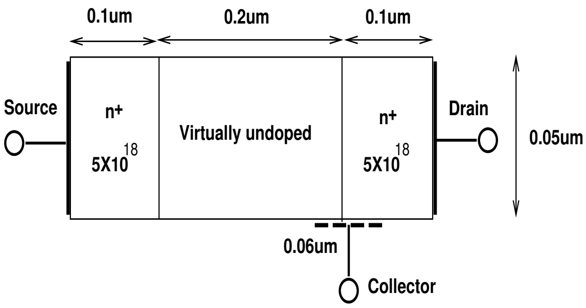

Fig. 2: The structure simulated by DAMOCLES. Simplification of geometry of the structure in Fig. 1 is made to shorten simulation time.

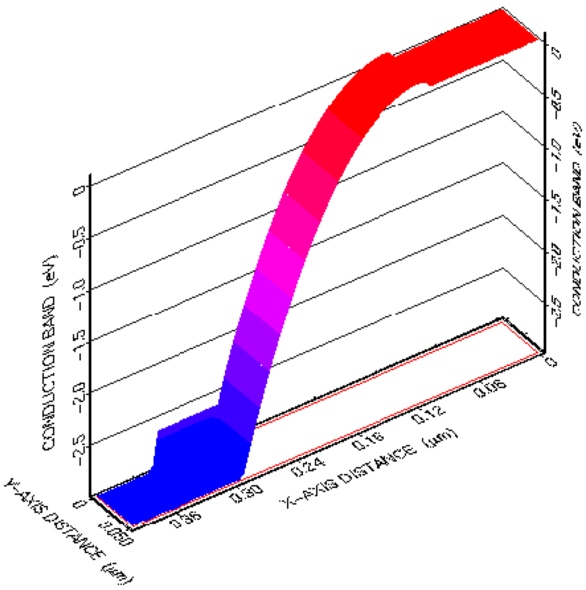

Fig. 3: Potential contours of the device in Fig. 2.

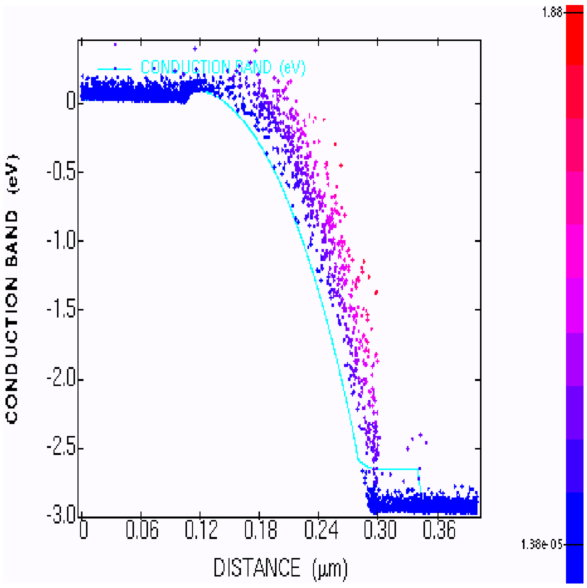

Fig. 4: Cross-section at $y = 0$ in Fig. 3. The electron kinetic energy is the distance between the electron and the conduction band.