Gate Length Dependent Polysilicon Depletion Effects

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***Abstract*—Degradation of MOS gate capacitance in the inversion region becomes worse as the gate length is scaled down, according to a new experiment. Namely, polysilicon depletion effect has gate length dependence. The origin of this gate length-dependent polydepletion effect has been modeled and verified by using device simulation. As a result, the gradient of dopant distribution resulting from ion implant is shown to be an additional potential drop in the polygate. In addition, the enlarged depletion width at the gate sidewall can worsen the polydepletion effect for very-small MOSFETs.**

***Index Terms*—Gate capacitance, gate length effect, impurity distribution effect, MOSFET, polydepletion, polysilicon depletion effect.**

I. Introduction

IN THE dual n^+-p^+ gate CMOS process in which the gates are doped by ion implantation, concerns arise when the polysilicon gate is not doped heavily enough. This so-called polysilicon depletion effect reduces inversion charge density and transconductance, especially for very-thin oxide MOS devices [1]. Nonuniform, graded doping profiles in the polygate are inevitable due to the implant and constrained annealing conditions to avoid impurity penetration through the gate oxide, while maintaining the required source/drain junction depths [2].

Fig. 1 shows experimentally measured inversion gate capacitance (C_{inv}) relative to accumulation gate capacitance (C_{acc}) for p-channel MOSFET with various gate lengths. C_{inv}/C_{acc} for each gate length has been corrected by considering the gate overlap capacitance (C_{ov}): $(C_{inv} - C_{ov})/(C_{acc} - C_{ov})$. Also, portion of potential drop (V_p) in polygate relative to the gate bias (V_G–V_S) can be extracted. It should be noted that the portion of the inversion capacitance decreases as the gate length is scaled from 0.4 μm down to 0.12 μm. In other words, the potential drop (V_p) increases as the gate length is scaled down, implying that device performance deterioration by the polydepletion effect will be more significant as devices continue to scaled down.

II. Graded Impurity Distribution Effects

The potential drop in the presence of nonuniform dopant distribution is shown in Fig. 2. When the gate is doped by ion implantation, the dopant distribution as a function of position from the top down to the gate oxide direction can be represented as

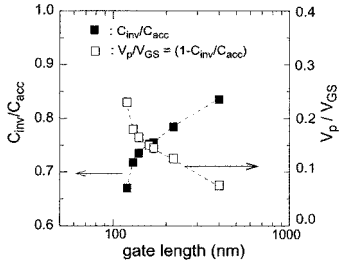

Fig. 1. Experimentally measured C_{inv}/C_{acc} and V_p/V_{GS} for PMOS, corrected for gate overlap capacitance (C_{ov}) [i.e., $(C_{inv} - C_{ov})/(C_{acc} - C_{ov})$], showing severe polydepletion effects in scaled devices. C_{acc} and C_{inv} are chosen at $V_{GS} = 2.0$ and -1.0 V, respectively, from measured CV.

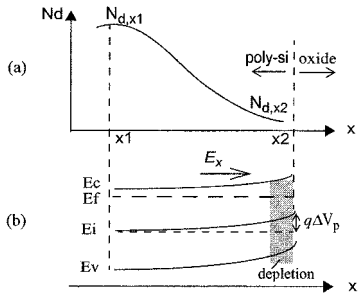

Fig. 2. Nonuniform, graded impurity distribution and corresponding band diagram, showing built-in electric field (E_x) and potential drop (ΔV_{p1}) in the polygate.

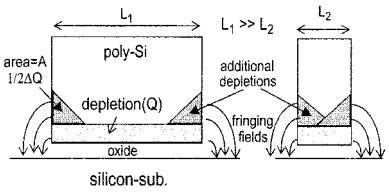

Fig. 3. Gate length effect on polydepletion, effective depletion width is wider for shorter gate, leading to an additional potential drop, ΔV_{p2}.

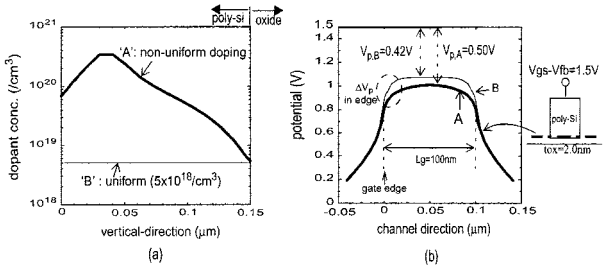

Fig. 4. Impact of nonuniform dopant distribution on polydepletion effects (ΔV_{p1}). (a) Comparison of nonuniform ("A") and uniform ("B") dopant distributions (b) potential drops between uniform and nonuniform profiles.

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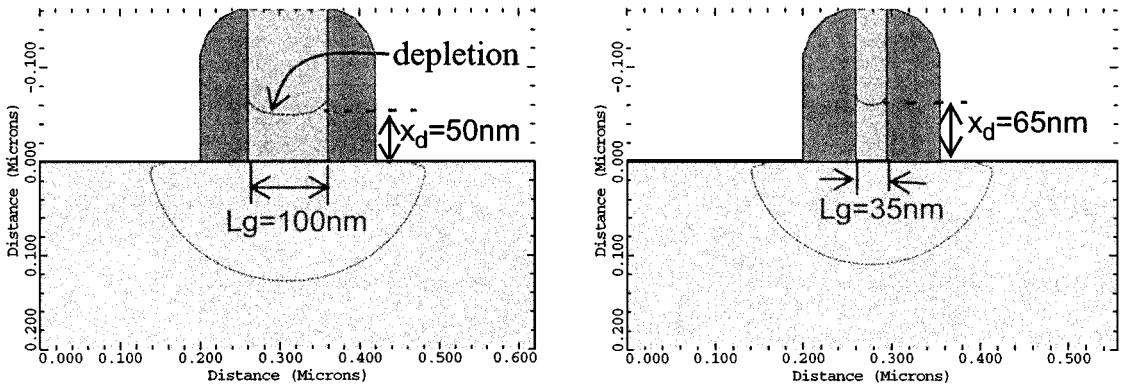

Fig. 5. Gate length-dependent polydepletion effect; depletion width (X_d) of $L_g = 35$ nm is wider than that of $L_g = 100$ nm due to the additional depletions in gate sidewall (ΔV_{p2}), $V_{gs} = 2.0$ V.

in Fig. 2(a). Since the dopant density and carrier concentration vary with position, a built-in electric field exists between $x1$ and $x2$, leading to built-in depletion, as shown in Fig. 2(b). Under thermal equilibrium there is no current flow; the built-in field, E_x, in an n-type polygate can be expressed as [3]

$$E_x = -\frac{d\phi}{dx} \approx -\frac{kT}{q}\frac{1}{N_d}\frac{dN_d}{dx} \quad d\phi \approx \frac{kT}{q}\frac{dN_d}{N_d} \tag{1}$$

where ϕ is the potential and N_d is the doping concentration in the position. A potential drop (ΔV_{p1}) is established at the interface due to the graded dopant distribution between x_1 and x_2 which can be approximated as

$$\Delta V_{p1} = \phi_{x1} - \phi_{x2} = \frac{kT}{q}\ln\frac{N_{d,\,x1}}{N_{d,\,x2}}. \tag{2}$$

When N_d changes from 10^{20} to 10^{18} cm^{-3}, the potential drop is about 0.12 V estimated from (1) even with no gate bias, which is on the order of the threshold voltage for sub-100 nm MOSFETs. This additional potential drop across the polysilicon gate (ΔV_{p1}) should be added to the voltage drop based on the uniform dopant concentration (V_p).

III. Gate Length Effects

Polysilicon depletion effects depending on the gate length are shown in Fig. 3; additional depletion effects at the gate sidewalls due to the fringing gate fields, result in additional potential drops. Similar to that of the narrow-width effect, the portion of the additional charge (ΔQ) in total charge (Q) becomes higher as the gate length is scaled down, resulting in wider depletion widths and additional potential drops for shorter gate lengths (i.e., L_2). Let "A" denote the triangular area of the additional charge ΔQ, then the additional potential drop (ΔV_{p2}) due to the sidewall depletion is approximated as [4]

$$\frac{1}{2}\Delta Q \approx qN_d\frac{A}{L}\,(C/\mathrm{cm}^2) \quad \Delta V_{p2} \approx \frac{\Delta Q}{C_d} = \frac{2qN_dA}{LC_d} \tag{3}$$

where L is the gate length and C_d is the depletion capacitance in the polysilicon gate. This implies that potential drop increases in inverse proportion to the L and ΔV_{p2} should be also added to V_p to reflect further polydepletion for very short gate lengths.

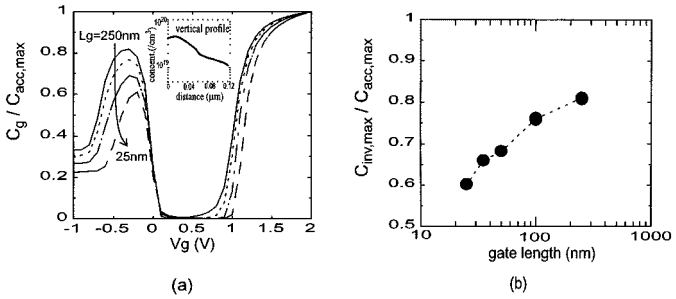

Fig. 6. Simulated gate capacitance of p-channel MOS for various gate lengths ($t_{ox} = 2.0$ nm and $t_{poly} = 0.12$ μm); (a) normalized gate capacitance corrected for gate overlap capacitance; $(C_g - C_{ov})/(C_{acc,\max} - C_{ov})$ for $L_g = 250$, 100, 50, and 25 nm, inset is the vertical dopant profile used in the simulation. (b) Ratio of maximum inversion capacitance ($C_{inv,\max}$) to maximum accumulation capacitance ($C_{acc,\max}$).

IV. Simulation and Analysis

Comparison of potential drops (V_p) has been made for nonuniform (A) and uniform doping (B) cases, as represented in Fig. 4(a). V_p values calculated by using a two-dimensional device simulator, MEDICI [5], are shown in Fig. 4(b). It is instructive to note that V_p for case B is less than that of A, in spite of its lower average doping concentration, which can be attributed to the graded impurity distribution effects, reflected by ΔV_{p1}, discussed previously.

Regarding the gate length dependence, device simulation results show that the depletion width of $L_g = 35$ nm is wider than that of $L_g = 100$ nm, resulting in ~0.1 V larger V_p (i.e., $V_{gs} = 2.0$ V) due to the ΔV_{p2} effect, as shown in Fig. 5. This effect becomes more serious when the gate dopant is Boron (i.e., p-channel MOS). Boron atoms in the gate have a tendency to diffuse toward adjacent oxides. This results in laterally more convex dopant profile along the gate, which further widens depletion widths in the gate sides.

Simulated gate capacitances of p-channel MOS capacitors show that a nonuniform gate dopant profile with the peak concentration of $\sim 4 \times 10^{19}$ cm^{-3} and the minimum concentration near the bottom of $\sim 1.5 \times 10^{19}$ cm^{-3} produces significant C_{inv} reductions, as shown in Fig. 6(a). In order to eliminate short-channel effects source/drain region has not been made in the PMOS structure.

The normalized gate capacitance corrected for overlap capacitance (C_{ov}), $(C_g - C_{ov})/(C_{acc,\max} - C_{ov})$, decreases with the gate length from $L_g = 250$ nm down to 25 nm. As a result, as shown in Fig. 6(b), the portion of simulated maximum inversion capacitance relative to accumulation capacitance, $C_{\max,inv}/C_{\max,acc}$, shows trends consistent with experiments previously shown in Fig. 1.

V. Conclusions

Impact of the nonuniform dopant distribution (ΔV_{p1}) and the short gate length (ΔV_{p2}) on the polydepletion effects has been modeled and verified. The reduced gate capacitance in the inversion region for short gate lengths can be attributed to the additional depletion at the gate sidewall due to the fringing gate fields. This additional potential drop in short gate lengths can worsen the polydepletion effects especially for nonuniformly doped, sub-100 nm poly gate devices. Achieving less steep dopant gradients can be a potential solution to overcome this problem.

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