Resonant Gate Tunneling Current in Double-Gate SOI: A Simulation Study

Chang-Hoon Choi, Zhiping Yu, and Robert W. Dutton

***Abstract*—Gate tunneling current in fully depleted, double-gate (DG) silicon-on-insulator (SOI) MOSFETs is characterized based on quantum-mechanical principles. The gate tunneling current for symmetrical DG SOI with ground-plane (t_{ox} =1.5 nm and T_{Si} =5 nm) is shown to be higher relative to single-gate (bulk) MOS structure. The tunneling is enhanced as the silicon layer becomes thinner since the thinner silicon layer acts a deep quantum well. The simulated I_G–V_G of DG SOI has negative differential resistance like that of the resonant tunnel diodes at the gate bias ~ 1.4 V.**

***Index Terms*—Asymmetrical DG (ADG), double-gate (DG) silicon-on-insulator (SOI), fully depleted (FD), gate tunneling current, quantum-mechanical theory, resonant tunneling diodes (RTD), symmetrical DG with ground-plane (SGP).**

I. Introduction

The fully depleted (FD) double-gate (DG) silicon-on-insulator (SOI) is known as a promising device for the ultimate stage of MOSFET scaling, where ~10–nm channel lengths are intimated, owing to its inherent suppression of short channel effects and almost ideal subthreshold slope. The target oxide thickness (t_{ox}) for the DG-SOI device is expected around 0.5 –1.5 nm for the gate length of 25 nm [1]. In such a thin gate oxide regime the gate direct tunneling current clearly appears, which can alter device characteristics significantly. To date, however, no study has been yet reported on the gate direct tunneling in FD/DG SOI MOSFETs. If the silicon layer thickness (T_{Si}) in DG SOI is ultrathin, the energy quantization effect becomes evident in the quantum well, which considerably affects the electron distribution in the silicon layer; this in turn affects electron tunneling significantly, since the current transmission through the potential barrier is influenced by the energy states in the silicon layer (ie., quantum well). Therefore, the mechanism of gate direct tunneling in very thin silicon layer DG SOI must be assessed based on a quantum-mechanical approach to determine the design parameters of future DG SOI. This article includes modeling and simulation of gate tunneling current for DG SOI based on a quantum-mechanical equation solver.

II. Tunneling in SDG and SGP Structures

Fully depleted, symmetrical double-gate (SDG) nMOSFET with two n-type poly-gates has an undesirable, negative threshold voltage [2], [3]. To overcome this, asymmetrical DG (ADG) with n^+/p^+ poly-gates and SDG with ground plane (SGP) have been proposed for adjustment threshold voltage by using a different gate work function or different back-gate bias. Schematics and band diagrams of DG SOI nMOSFETs are shown in Fig. 1[4]– SDG with gate bias applied to both n^+ gates (SDG) and SDG with back-gate grounded (SGP). Consider one-dimensional (1–D) device structures without considering the source and drain effects. As shown in the band diagram in Fig. 1(a), the same potential retains between the two gates for SDG structure. Thus, even though tunneling can locally occur between the front (back) gate and front (back) channel, the net current is zero, if the gate current flowing from the source/drain is not taken into account. Meanwhile, for SGP structure a potential difference exists between the two gates, when the bias is applied to the front gate ($V_{FG} > V_T$). Also, note that p-type silicon layer is inverted to n-type when the silicon layer thickness is thin enough. Thus, for very thin oxide thickness electrons can tunnel the oxide from the back gate to the front gate, such that positive gate current flows, as shown in Fig. 1(b).

In quantum-mechanical theory, an electron is treated as a wave-function, such that there is some probability that electrons can tunnel through the barrier even though the electron energy is below the barrier. In DG SOI structure with a thin silicon layer, a quantum-well forms in the silicon layer between the oxide barriers. Thus, the gate tunneling current with regard to the bias can be discontinuous in DG structure due to the resonant tunneling as a consequence of discrete energy states in the silicon layer (quantum-well).

III. Quantum-Mechanical Simulation

In this work, the tunneling current is calculated using a 1–D Greens function simulator, NEMO [5], which is a Schrödinger equation solver. For NEMO simulation, the multiple single band structure with Hartree self-consistency model is used. We assume that $T_{Si} = 5$–40 nm, $t_{ox} =$ 1.5 nm, $N_{p-sub} = 1.0 \times 10^{18}$ cm^{-3} and $N_{n-poly} = 2.0 \times 10^{20}$ cm^{-3}.

Fig. 2 compares the simulated direct tunneling currents of SGP structure for various silicon layer thicknesses (T_{Si} =5–40 nm); gate tunneling current is higher as the silicon layer becomes thinner. The silicon layer can act as a quantum well for very thin layer DG SOI, such that the silicon thickness (ie. quantum-well thickness) determines eigenenergies of the confined states.

Fig. 3(a) compares simulated band diagrams for $T_{Si} = 5$ and 40 nm when $V_{FG} = 1$ V and $V_{BG} = 0$ V. It is obvious that thinner silicon layer easily undergoes the *volume inversion*, in which the whole volume of the silicon layer is in the strong inversion state. As a result, the potential barrier in the silicon layer for $T_{Si} = 40$ nm is not favorable for electrons to tunnel from the back gate (left) to the top (right) gates. Thus, the electron tunneling from the back-gate to the front-gate through the double barrier becomes significant as the silicon layer is thinner.

Meanwhile, for the ADG structure without source and drain, there is less strong volume inversion in the p-type silicon layer due to the influence of p^+ poly-gate, as shown in Fig. 3(b). Thus, few electrons will be available in the poly-gate and the silicon layer. As a result, there is no conceivable tunneling current in the ADG.

Fig. 4 compares simulated gate tunneling currents between DG SOI ($T_{Si} = 5$ nm) and single-gate (bulk) MOS structure with $T_{Si} = 0.5$ μm. The gate current for DG structure is higher than for single-gate MOS due to the resonant tunneling effects in the DG. For zero bias there will be no tunneling current in the DG structure. As the front-gate bias increases the energy level of the cathode (back-gate) begins to align with the energy level of the silicon layer; electron tunneling current flows, reaching the peak current. As the bias increases further, the two energy levels become out of adjustment, removing the resonant condition. As a consequence, the electron density is much reduced compared to that for the peak current. This results in abrupt decrease of the tunneling current down to the valley current ~1.5 V. Then, the current increases

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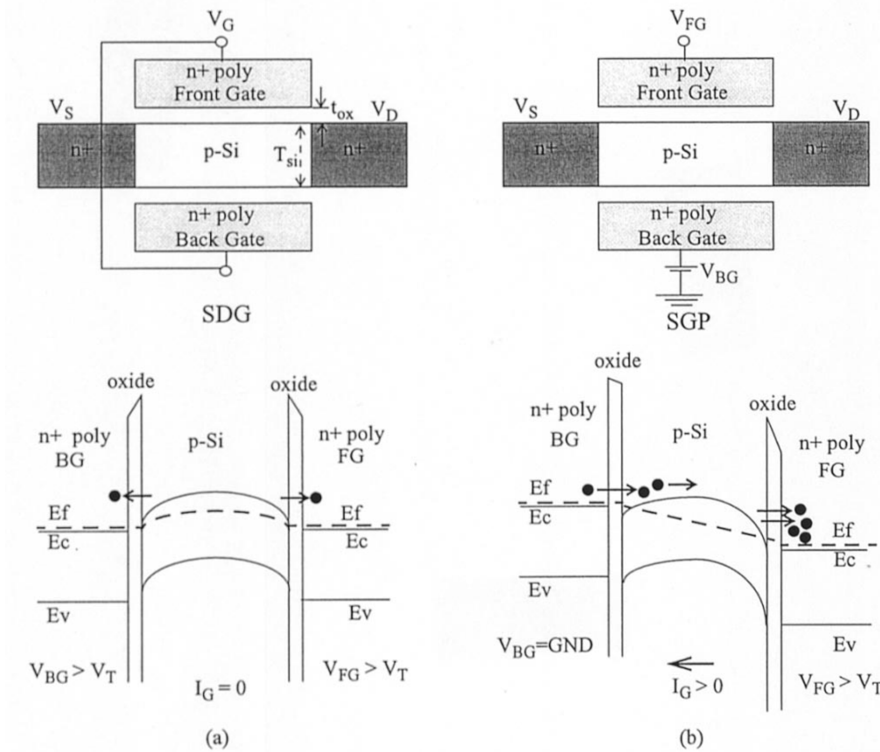

Fig. 1. DG structures and corresponding band diagrams without considering source/drain (2–D) effects. (a) SDG. (b) SGP. There is gate-tunneling current for SGP, but no gate current for SDG structure.

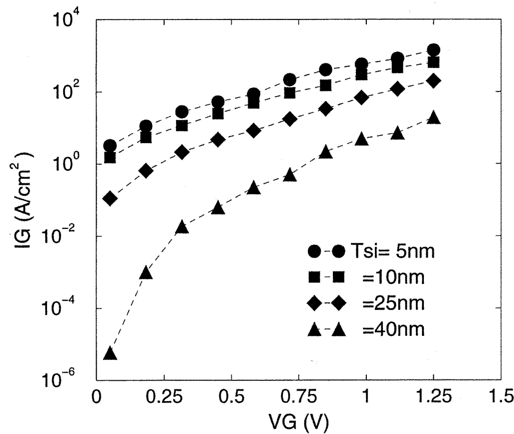

Fig. 2. Simulated gate tunneling $I_{\rm G}$–$V_{\rm G}$ of SGP structure for different silicon layer thicknesses.

again as the bias further increases due to either thermionic current or the second resonant tunneling condition.

As a result, this gate tunneling current of DG structure has a negative-differential resistance like that of the (heterostructure) resonant-tunneling diode (RTD), which has received considerable attention lately for digital/analog and memory circuit applications [6], [7].

IV. Conclusion

Gate direct tunneling current for FD/DG SOI is modeled and verified by using Schrödinger equation solver. Gate tunneling current of SGP devices is significant which is enhanced as the silicon layer becomes thinner. To overcome the gate current problem, use of ADG SOI can be a solution. However, since the gate current has a negative-differential resistance SGP structure may be used to realize RTDs.

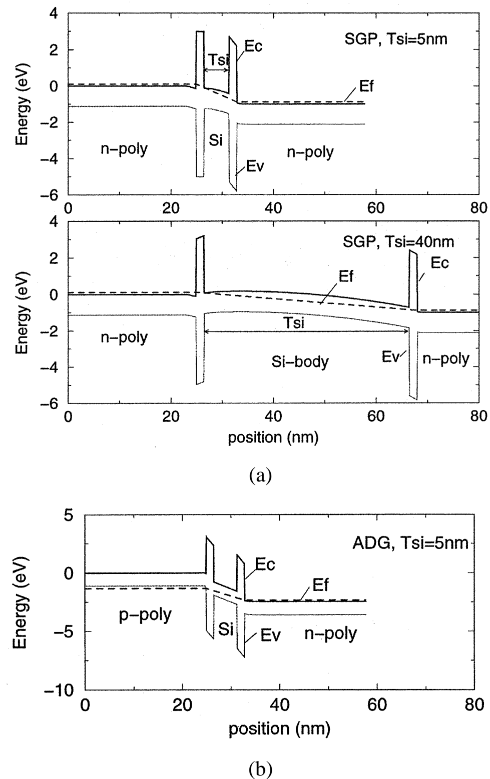

Fig. 3. Comparison of simulated band diagrams for SDG with SGP and ADG. (a) SGP for $T_{\rm Si} = 5$ and 40 nm; (b) ADG with n^{+}/p^{+} poly-gates, $T_{\rm Si} = 5$ nm.

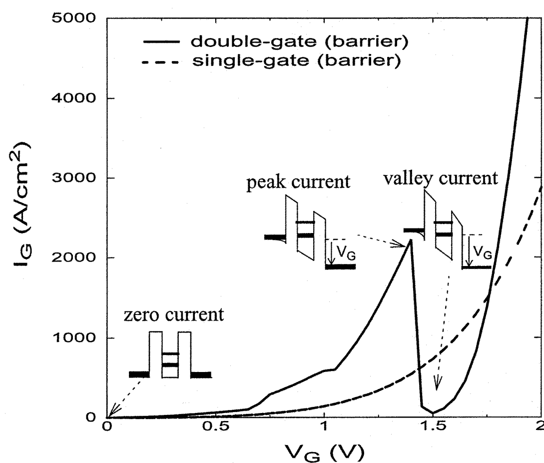

Fig. 4. Simulated gate tunneling currents for DG (barrier) structure (t_{ox} = 1.5 nm and T_{Si} = 5 nm) and single-gate MOS structure (t_{ox} = 1.5 nm and $T_{Si} = 0.5\ \mu$m). Note the resonant tunneling current for DG structure.

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Novel X- and Gamma-Ray Sensors Based on Bulk-Grown Silicon–Germanium

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***Abstract*—In this brief, preliminary experimental results and the theoretical assessment of various compositions of bulk-grown, single-crystal silicon-germanium (SiGe) for application in X- and gamma-ray sensors, are presented. It is shown that the absorption efficiency of $Si_{1-x}Ge_x$ sensors is significantly superior to that of silicon sensors, even for relatively low germanium concentrations, while the bandgap narrowing should be sufficiently small not to restrict the device operation to cryogenic temperatures, as in the case of pure germanium detectors. The experimental results obtained with PIN-like devices manufactured on $Si_{0.95}$ $Ge_{0.05}$ indicate suitable hole mobility, and superior detection efficiency for X-ray photons.**

***Index Terms*—Bulk SiGe, detectors, semiconductor, X-ray.**

I. INTRODUCTION

X- and gamma-ray sensors are key components in most X-ray imaging systems as well as in numerous scientific applications. In response to the varying requirements in detector performance from one application to another, a variety of detector types have been developed, ranging from the well-established X-ray-sensitive film and gas-filled counters to the most advanced, compound semiconductor sensors [1]–[3]. Particularly in the field of medical imaging, where high resolution and high absorption- and quantum-efficiencies, translate into doses and treatment quality, the search for new detectors is a top priority. Semiconductor detectors, which directly transform photons to electric signals, offer numerous advantages such as high atomic density (increasing absorption coefficients), small size, high energy, and lateral resolutions, etc. The detectors should be made of application-tailored materials, to provide sufficient absorption efficiency, charge collection, and other properties.

Due to the demands of the very large scale integration (VLSI) industry, silicon semiconductor is the most studied and "easiest" to process. However, the absorption coefficient of the midenergy X- and gamma-rays, is strongly dependent on the atomic number of the absorbing media [4]. Silicon, with an atomic number of only 14, has a serious drawback. The absorption coefficient of Ge, with an atomic number of 32 is significantly higher; however, its narrow band gap of 0.66 eV limits the operation of Ge detectors to cryogenic temperatures. It should be noted that sensors based on other materials, such as $Cd_{1-x}Zn_xTe$, HgI_2, are being studied and used for applications requiring high absorption efficiency for high-energy gamma-rays. While these semiconductors have high atomic numbers, some of their electrical properties, such as carrier lifetimes and mobilities should be improved [3], [5]–[7].

II. THEORETICAL CONSIDERATIONS

Primary photon absorption in the energy range (below ~1 MeV) mainly occurs through the photoelectric effect and the incoherent (Compton) scattering. The cross section for the photoelectric effect in silicon-germanium (SiGe), which is dominant for photons with energy up to 40–100 keV (depending on Ge concentration), is roughly proportional to Z^y, where Z is the atomic number and y is a

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