Impact of Poly-Gate Depletion on MOS RF Linearity

Chang-Hoon Choi, *Member, IEEE*, Zhiping Yu, *Senior Member, IEEE*, and Robert W. Dutton, *Fellow, IEEE*

***Abstract*—The distortion behavior for thin oxide MOS transistors can be degraded due to polysilicon-gate depletion effects. The nonlinear, bias-dependent gate capacitance for thin oxide MOSFET's results in significant 2nd-order derivatives in gate capacitance, $(\partial^2 C(V_{gs})/\partial V_{gs}^2)$, which in turn results in substantial 3rd-order derivative contributions to drain current, $(\partial^3 I_{ds}/\partial V_{gs}^3)$. This may restrict the use of very-thin oxide MOSFET's in RF applications.**

***Index Terms*—Distortion, gate capacitance, linearity, MOSFET, polydepletion, RF, thin oxide.**

I. Introduction

RECENTLY, the use of modern CMOS technologies have been extended not only to mixed analog-digital circuit design, but also to RF applications. In RF applications, miniaturization of gate length is an effective way to increase the cut-off frequency (f_T), because f_T increases in proportion to transconductance (g_m). The International Technological Roadmap for Semiconductor (ITRS) proposes an oxide thickness for NMOS RF devices, as indicated in Table I [1]. This oxide scaling is identical with that for high-performance logic devices, probably based on considerations of process compatibility. However, as oxide thickness is scaled down, MOSFET's increasingly suffer from various undesirable phenomena. In particular, polydepletion effects become important and can be inevitable for modern, thin oxide MOSFET's due to the serial connection of the reduced polydepletion capacitance with the enlarged oxide capacitance, leading to degradation of inversion gate capacitance and transconductance [2]. In experiments by *Langevelde* [3], the RF distortion is shown to be worse with decreasing oxide thickness. The impact of polydepletion effects on RF distortion behavior needs to be studied, in order to help project directions of future gate oxide scaling in MOS RF devices.

In analog MOS circuits, a purely sinusoidal input signal can produce a distorted output signal with higher-order harmonics due to the nonlinearity of MOS transistors [3]. These harmonics are mainly induced by higher-order derivatives of the current–voltage $(I$–$V)$ characteristics of the transistors. In particular, a lower limit on the distortion of MOS transistors is determined by the third-order derivative of the drain current (I_{ds}) with respect to gate bias (V_{gs}) $(g_{m3} = (\partial^3 I_{ds}/\partial V_{gs}^3))$ [4], [5]. Therefore, the amplitude of the third-order derivative of I_{ds} should be minimized for low-distortion applications [6].

Manuscript received January 2, 2003; revised February 12, 2003. This project is supported by Texas Instruments Inc., through a customized research under SRC Contract 2001-MJ-966.

C.-H. Choi and R. W. Dutton are with the Center for Integrated Systems, Stanford University, Stanford, CA 94305, USA (e-mail: chchoi@gloworm.stanford.edu).

Z. Yu is currently with Tsinghua University, Beijing, China.

Digital Object Identifier 10.1109/LED.2003.812549

TABLE I
ROADMAP FOR NMOS RF DEVICES (ITRS 2001 EDITION) [1]

year	2003	2004	2005	2006	2007	2010
gate length (nm)	65	53	45	40	35	18
f_T (GHz)	183	225	264	322	372	541
t_{ox} physical (nm)	1.1–1.6	0.9–1.4	0.8–1.3	0.7–1.2	0.6–1.1	0.5–0.8

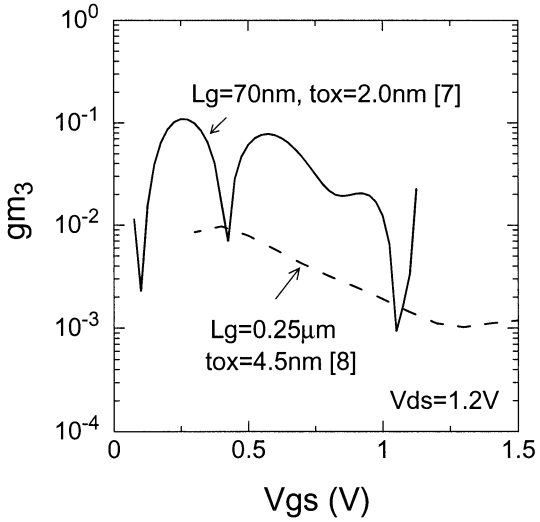

Fig. 1. Measured third-order derivative of drain current, $g_{m3}(= (\partial^3 I_{ds}/\partial V_{gs}^3))$, at $V_{ds} = 1.2$ V for $L_g = 70$ nm, $t_{ox} = 2.0$ nm and $L_g = 0.25$ μm, $t_{ox} = 4.4$ nm NMOSFET's. $W = 10$ μm for both cases.

Fig. 1 shows the third-order derivatives of I_{ds} at $V_{ds} = 1.2$ V, labeled g_{m3}, obtained from measured NMOS I–V curves for two different technologies; a 70 nm gate length (L_g) device with $t_{ox} = 2.0$ nm [7] and a 0.25 μm device with $t_{ox} = 4.4$ nm [8]. The gate width is 10 μm for both technologies. Data shows that the amplitude of g_{m3} for the device with $L_g = 70$ nm and $t_{ox} = 2.0$ nm is greater than that for 0.25 μm device with a thicker oxide. Also, there are multiple zero-crossing points in g_{m3} for the device with $L_g = 70$ nm and $t_{ox} = 2.0$ nm. These results imply that the linearity of MOS transistors can be worse for scaled devices with very-thin oxide thickness.

II. RF Linearity Due to Polydepletion

The basic expression for drain current in a MOSFET is:

$$I_{ds} = Qv \tag{1}$$

where Q is the channel charge density along the current direction and v is the velocity of the carriers.

For sufficiently high fields the carrier velocity, v, approaches a saturated value, v_{sat}. Thus we can rewrite (1) as:

$$I_{ds} \simeq Qv_{sat} \tag{2}$$

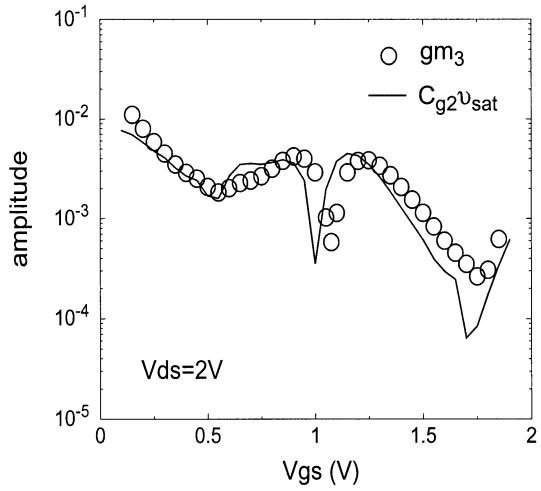

Fig. 2. Comparison between g_{m3} and $C_{g2}v_{sat}$ in (4) for an NMOS device with $L_g = 50$ nm and $t_{ox} = 1.5$ nm. I_{ds} and C_g were obtained by using device simulation for $V_{ds} = 2.0$ V and $v_{sat} = 1.0 \times 10^7$ cm/s.

where v_{sat} is the carrier saturation velocity in Si ($\sim 1 \times 10^7$ cm/s).

For the saturation drain current, the 1st-order derivative of I_{ds} with respect to the gate bias (V_{gs}), g_m, is given as:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \simeq \frac{\partial Q}{\partial V_{gs}} v_{sat} \simeq C(V_{gs}) v_{sat}. \tag{3}$$

In turn, the 3rd-order derivative, g_{m3}, can be expressed as:

$$g_{m3} = \frac{\partial^3 I_{ds}}{\partial V_{gs}^3} \simeq \frac{\partial^2 C(V_{gs})}{\partial V_{gs}^2} v_{sat} = C_{g2} v_{sat}. \tag{4}$$

Equation (4) implies that the 3rd-order derivative of I_{ds} that controls MOS distortion behavior is mainly determined by the 2nd-order derivative of the gate capacitance with respect to V_{gs} ($= (\partial^2 C(V_{gs})/\partial V_{gs}^2)$).

In order to validate the relationship in (4), device simulation by using MEDICI is applied to an NMOS device with $L_g = 50$ nm and $t_{ox} = 1.5$nm, to obtain drain current (I_{ds}) and the gate capacitance (C_g). The threshold voltage (V_{th}) of the device is about 0.02 V, which becomes a negative value for high drain bias due to short-channel effects. The dopant concentration of the poly-gate (N_p) is 2.5×10^{19} cm^{-3} and v_{sat} is assumed 1.0×10^7 cm/s in the simulation. As a result, reasonable agreement can be obtainable between g_{m3} and $C_{g2}v_{sat}$ at $V_{ds} = 2.0$ V, as shown in Fig. 2; the discrepancy between the two curves can be attributed to not having modeled the external source and drain resistance in the drain current formulation given by (2).

An ideal gate capacitance, in the strong inversion condition, should equal the total oxide capacitance, $C_{ox} = \epsilon_{ox}/t_{ox}$. However, the real gate capacitance in strong inversion is highly gate bias dependent, when the polydepletion effects are taken into account, which can be expressed as [9]:

$$C(V_{gs}) \simeq \frac{\epsilon_{ox}}{t_{ox} + t_{dp}(V_{gs})} \simeq \frac{\epsilon_{ox}}{\sqrt{t_{ox}^2 + \frac{2\epsilon_{Si}}{9qN_p}(V_{gs} - V_{fb} - \phi_s(V_{gs}))}} \tag{5}$$

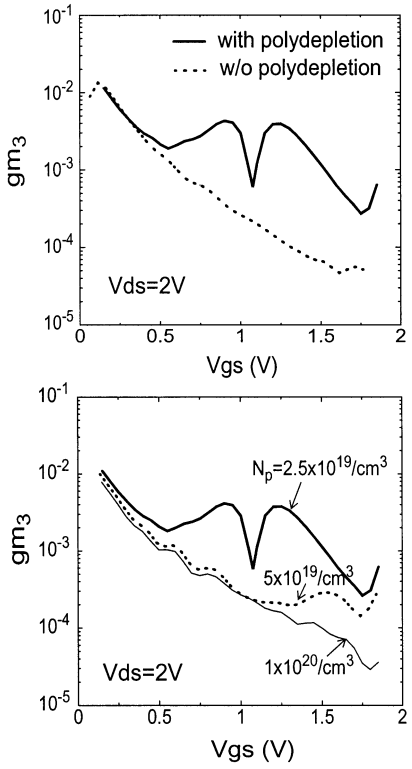

Fig. 3. Simulated g_{m3} amplitudes for an NMOS device with $L_g = 50$ nm and $t_{ox} = 1.5$ nm ($V_{ds} = 2.0$ V). (a) g_{m3} curve with polydepletion effects for $N_p = 2.5 \times 10^{19}$/cm^3 (solid line) and g_{m3} curve without polydepletion effects (dotted line). (b) g_{m3} curves for different N_p values.

where t_{dp} represents the depleted thickness in the poly-gate; N_p is the dopant concentration in the poly-gate; V_{fb} is the flat-band voltage; and ϕ_s is the surface potential in the channel.

Equation (5) shows a nonlinear relationship between the gate terminal voltage and the gate capacitance in the presence of the polydepletion effect. When the polydepletion effect is severe, MOSFET distortion behavior becomes worse, since the term $(\partial^2 C(V_{gs})/\partial V_{gs}^2)$ becomes substantial.

Fig. 3 shows simulated g_{m3} curves of an NMOS with $t_{ox} = 1.5$ nm and $L = 50$ μm for different process and device conditions. Here, the gate direct tunneling has not been considered. The solid line in Fig. 3(a) represents the g_{m3} curve in the presence of the polydepletion effects for $N_p = 2.5 \times 10^{19}$ cm^{-3}. The dotted line represents the g_{m3} curve when the polydepletion effects are not taken into account, in which the gate electrode is defined by a workfunction parameter. Note that there is no zero-crossing point and g_{m3} amplitude is reduced as the gate bias increases in the absence of polydepletion effects, because of nearly constant gate capacitance with respect to the gate bias. Also, overall g_{m3} at the higher gate bias is $\sim$10 times less relative to the case in the presence of the polydepletion effects. Fig. 3(b) shows g_{m3} curves for different N_p values; g_{m3} amplitude is reduced as the N_p value increases owing to the minimized polydepletion effects.

Simulation results imply that the RF distortion will be degraded in scaled MOS with ultra-thin oxides, which results from the nonlinear gate capacitance behavior under the influence of polydepletion effects, as expressed in (5).

III. Conclusions

Distortion behavior of scaled MOS transistors for RF applications can be degraded due to the nonlinear, bias-dependent gate capacitance resulting from polydepletion effects. The oxide thickness scaling scenario for NMOS RF devices proposed in the ITRS roadmap, which tracks the scaling for high-performance logic, may not be desirable in terms of degraded distortion behavior resulting from these effects, because system requirements on linearity become more stringent for future wideband RF applications.

Acknowledgment

The authors thank Dr. B. Yu of Advanced Micro Devices (AMD), Inc. for the 70 nm MOSFET data.

References

[1] International Technology Roadmap for Semiconductors, 2001 Edition. Semiconductor Industry Association. [Online]. Available: http://public.itrs.net/

[2] C.-H. Choi, P. R. Chidambaram, R. Khamankar, C. F. Machala, Z. Yu, and R. W. Dutton, "Gate length dependent polysilicon depletion effects," *IEEE Electron Device Lett.*, vol. 23, pp. 224–226, Apr. 2002.

[3] R. V. Langevelde, R. J. Havens, M. J. Knitel, P. H. Woerlee, and F. M. Klaassen, "RF-distortion in deep-submicron cmos technologies," in *IEDM Tech. Dig.*, 2000, pp. 807–810.

[4] G. Groenewold and W. J. Lubbers, "Systematic distortion analysis for MOSFET integrators with use of a new MOSFET model," *IEEE Trans. Circuits Syst.-II*, vol. 41, pp. 569–580, Sep 1994.

[5] A. O. Adan, T. Yoshimasu, S. Shitara, N. Tanbe, and M. Fukumi, "Linearity and low-noise performance of SOI MOSFET's for RF applications," *IEEE Trans. Electron Devices*, vol. 49, pp. 881–888, May 2002.

[6] R. V. Langevelde and F. M. Klaassen, "Effect of gate-field dependent mobility degradation on distortion analysis in MOSFET's," *IEEE Trans. Electron Devices*, vol. 44, pp. 2044–2052, Nov 1997.

[7] B. Yu, Y. Wang, H. Wang, Q. Xiang, C. Riccobene, S. Talwar, and M. R. Lin, "70 nm MOSFET with ultra-shallow, abrupt, and super-doped S/D extension implemented by laser thermal process (LTP)," in *IEDM Tech. Dig.*, 1999, pp. 509–512.

[8] C.-H. Choi, J.-S. Goo, Z. Yu, and R. W. Dutton, "Shallow source/drain extension effects on external resistance in sub-0.1 μm MOSFET's," *IEEE Trans. Electron Devices*, vol. 47, pp. 655–658, Mar 2000.

[9] E. Josse and T. Skotnicki, "2D analysis of gate polydepletion in ultra short MOSFET's," in *Proc. ESSDERC*, 2001, pp. 207–210.