Series Resistance Calculation for Source/Drain Extension Regions Using 2-D Device Simulation

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***Abstract*—Series resistance in the source/drain region is becoming a bottleneck for MOS device performance. A rigorous, simulation-based method for calculating resistance components that correctly accounts for current spreading is presented. Resistance calculation strategies used to project lateral abruptness requirements for future scaling, based on partitioning the device into vertical strips, are shown to cause substantial errors when current spreading occurs. This can result in an overestimate of the benefits of abrupt junctions. The physical resistances obtained from simulated devices are compared with the extracted resistances from the shift-and-ratio method. Discrepancies can be explained based on violation of the basic assumptions of the shift-and-ratio method: that series resistance is bias independent and the channel resistance is directly proportional to the channel length. A new extraction method that relaxes these assumptions is presented and used to provide deeper understanding in the application of the shift-and-ratio method to deep submicron devices.**

***Index Terms*—Error analysis, extraction methods, MOS device scaling, parameter estimation, resistance, semiconductor device modeling, series resistance.**

I. Introduction

SCALING of MOS devices is a major driving force of the semiconductor industry. However, for deep submicron devices, simple scaling alone will not suffice to improve performance. While the intrinsic channel resistance improves with scaling, parasitic resistances in the source/drain and contact regions do not scale well and have become a significant part of the total resistance. Understanding the factors controlling these resistances is therefore very important.

Three different methods for calculating physical resistances in an MOS device are examined in this paper: resistance calculations based on partitioning into vertical strips (Section II); a more rigorous method that correctly accounts for two-dimensional (2-D) current flow in the source/drain region (Section III); and the sheet resistivity equation as given in [3] (Section IV). In Section V, resistance calculations based on vertical strips, on which the ITRS [2] lateral extension abruptness requirements are based, are shown to introduce substantial errors in the spreading resistance. Finally, in Section VI, the physical resistances calculated using these numerical methods are compared with the extracted values from the shift-and-ratio method. A new extraction technique is presented and used to better understand the behavior of the shift-and-ratio method and to explain the observed discrepancies.

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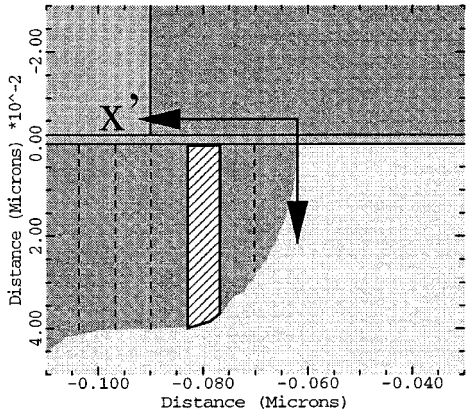


Fig. 1. Partitioning a device based on vertical strips.

II. Vertical Strip Calculation Method

A. Ng and Lynch's Analytical Model

Ng and Lynch [1] present an analytical treatment of the resistive components in the source/drain region. Analytical models can provide much qualitative insight into device behavior. However, the approximations needed to arrive at an analytical solution limit the achievable accuracy. Since the Ng and Lynch approach forms part of the basis for the International Technology Roadmap for Semiconductors (ITRS) [2] requirements for lateral source/drain abruptness, it is important to examine its assumptions carefully.

Ng and Lynch attempt to account for current spreading by partitioning the source/drain region into vertical strips as indicated in Fig. 1. Integrating along these strips and summing the resulting resistances in series gives[1]

$$R_{sp} = \int \frac{\rho(x')dx'}{(\tan 1)x'W} - \cdots \tag{1}$$

where W is the width of the device.

B. Limits of the Method

Resistance of the vertical strips can be calculated as in equation (1) only if both vertical side-walls of each strip lie on equipotential surfaces. Fig. 2 shows the equi-quasi-Fermi potential lines in a typical MOS device obtained from device

[1] x' is the distance from the edge of the channel along the Si/SiO_2 interface. Note that current spreading at an angle of 1 radian is assumed. The ellipsis in equation (1) represents a correction term resulting from the way R_{sp} is defined in Ng and Lynch, which we ignore.

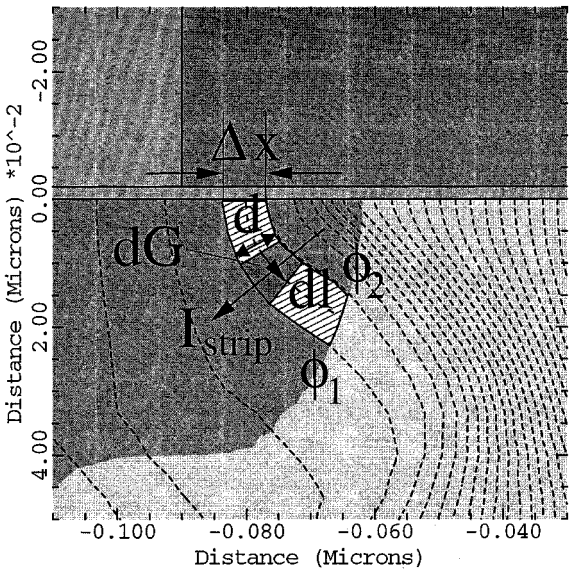


Fig. 2. Partitioning a device based on equipotential lines. Each resistive strip can be further decomposed into microscopic conductances of value $dG = (\sigma(\vec{x})/d(\vec{x}))\, d\vec{l}$ connected in parallel.

simulation. Due to current spreading in the source/drain regions, the equipotential lines are not vertical. As a result, resistance calculations based on vertical strips are subject to significant errors in these regions, as we shall see in Section V-A.

III. Calculation Based on Equipotential Lines

A method for calculating resistance components for arbitrary doping using device simulation is now developed. Local variations in carrier concentrations and mobility as well as the multidimensional nature of current flow are accurately accounted for.

A. Resistances in the Bulk

For multidimensional current flow, resistances must be combined in accordance with the equipotential lines. The region of interest is partitioned into thin resistive strips (striped area, Fig. 2) bounded by the equipotential lines. These strips are then partitioned into microscopic resistance elements (conductance dG in Fig. 2) connected in parallel. The resistance of the strip defined by the equipotential lines ϕ_1 and ϕ_2 can then be calculated as follows:

$$\frac{1}{R_{\phi_1,\phi_2}} = \int \frac{\sigma(\vec{x})}{d(\vec{x})}\, W \cdot d\vec{l} = \frac{W}{\phi_2 - \phi_1} \int \sigma(\vec{x}) \vec{\nabla}\phi(\vec{x}) \cdot d\vec{l} \tag{2}$$

where $\vec{x}$ is a point along the path integral,[2] $d(\vec{x})$ is the width of the strip at $\vec{x}$, and σ is the local conductivity.

The total resistance of the region can then be calculated by summing these resistances in series

$$R = \sum_{i=0}^{n-1} R_{\phi_i,\phi_{i+1}}. \tag{3}$$

[2]Since current flow in a MOS device is confined to a finite layer close to the surface, the limits of integration for each strip are bounded.

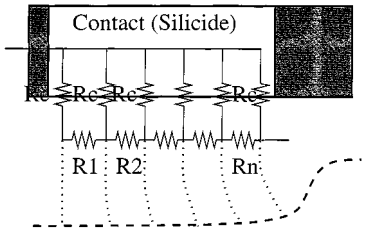


Fig. 3. Equivalent circuit for calculating the resistances of the source/drain contacts.

B. Contact Resistance

Fig. 3 shows a distributed resistive network for calculating the resistive contribution of the contact region. The total contact resistance is obtained by recursively applying

$$R_{\Sigma,1} = R_{c,1} + R_1 \tag{4}$$

$$R_{\Sigma,i} = \left(\frac{1}{R_{\Sigma,i-1}} + \frac{1}{R_{c,i}}\right)^{-1} + R_i \qquad i = 1 \cdots n \tag{5}$$

$$R_{co} = \left(\frac{1}{R_{\Sigma,n}} + \frac{1}{R_{c,n+1}}\right)^{-1} \tag{6}$$

where R_i is the resistance of the ith strip,[3] $R_{c,i} = \rho_c \cdot l_i \cdot W$ is the contact resistance associated with that strip, ρ_c is the contact resistivity between the silicide and the source/drain region, l_i is the distance spanned by the ith strip at the surface, and W is the width of the device.

IV. Calculation Using the Quasi-Fermi Level at the Surface

A third method for calculating resistances uses an incremental form of Ohm's law [3]–[5]. For an NMOS device

$$R_{sh}(x) = \frac{d\phi_n(x)}{dx} \Big/ \frac{I_{ds}}{W} \tag{7}$$

where x is the horizontal coordinate, ϕ_n is the electron quasi-Fermi level at the Si/SiO_2 interface, I_{ds} is the total current, and W is the width of the device.

Equation (7) involves only quantities at the Si/SiO_2 interface and may seem like a crude, one-dimensional (1-D) approximation. [3] suggests that it is valid only when the equipotential contours are perpendicular to the Si/SiO_2 interface.[4] It can in fact be shown that (7) is appropriate even where 2-D current flow is important.[5] Note that the more general expressions of (2) and (3) allow calculation of resistances for arbitrarily defined regions, which is not possible using (7).

[3]Calculated using (2).

[4]That is, when current flow is largely parallel to the x-direction.

[5]

$$R_{\phi_1,\phi_2} = \frac{\phi_2 - \phi_1}{I_{ds}} \equiv R_{\phi_1,\phi_2} = (\phi_2 - \phi_1) \Big/ \left(W \int \sigma(\vec{x}) \vec{\nabla}\phi(\vec{x}) \cdot d\vec{l}\right)$$

and

$$R_{sh} = \lim_{\Delta x \to 0} \frac{\phi_2 - \phi_1}{I_{ds}} \cdot \frac{1}{\Delta x}.$$

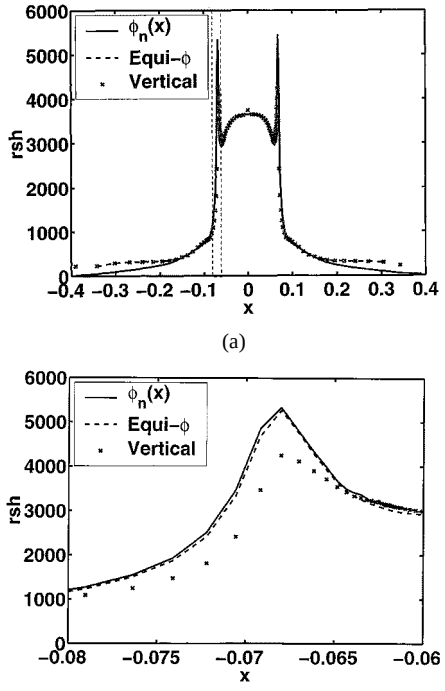


Fig. 4. (a) Comparison of R_{sh} calculated using quasi-Fermi level at Si/SiO_2 interface ($\phi_n(x)$); numerical integration based on equipotential lines (equi-ϕ); and numerical integration based on vertical strips (vertical). (b) Expanded plot showing the overlap region [dashed box in (a)].

V. Results

A. Comparison Between Resistance Calculation Methods

Fig. 4 compares the sheet resistance calculated with the three methods described in this paper: calculation based on quasi-Fermi levels at the Si/SiO_2 interface [$\phi_n(x)$, see Section IV]; numerical integration based on equipotential lines (equi-ϕ, see Section III); and numerical integration based on vertical strips (vertical, see Section II).

As discussed in Section IV, the R_{sh} calculated using the two quasi-Fermi level based methods match well, except in the contact regions.[6] It is also clear from Fig. 4(b) that the vertical strip method significantly underestimates the sheet resistivity in the extension region, where current spreading is important. An error of 27% in the calculated $R_{overlap}$ is seen in Table I. Note that the impact of the calculation method on the other resistive components are small, since current spreading is significant only in the overlap region.

Table II compares the $R_{overlap}$ calculated using the three methods for different lateral doping abruptness in the source/drain extension region. The error in calculations based on vertical strips increases with junction abruptness. For more abrupt junctions, current spreading occurs closer to the metallurgical junction and affects a larger fraction of the gate-extension overlap region. Therefore we conclude that resistance calculations based on vertical strips (such as Ng and Lynch [1]) overestimate the benefits of increasing lateral source/drain abruptness on series resistance.

[6]Equation (7) assumes a constant I_{ds} throughout the device, which is not true in the contact regions.

TABLE I
Resistive Components (in Ω/μm) Calculated Using the Three Methods Described in This Paper. Note the Error in $R_{overlap}$ for the Vertical Case

Method	R_{co}	R_{spacer}	$R_{overlap}$	R_{chan}
III $\phi_n(x)$	65.8	35	**62.1**	428
II Equi-ϕ	66.2	36.1	**61.7**	432
I Vertical	65.6	33.1	**44.4**	434

TABLE II
$R_{overlap}$ Calculated for Devices With Several Lateral Source/Drain Abruptnesses Using the Three Methods Described in This Paper. Units in Ω/μm

Abruptness (nm/dec) / Method	10.0	7.5	5.0	3.5	2.5
III $\phi_n(x)$	92.3	81.6	69.7	62.1	56.8
II Equi-ϕ	92.5	81.6	69.5	61.7	56.4
I Vertical	85.0	71.0	55.1	44.4	37.0
% diff between I and II	8.1%	13.0%	20.7%	28.0%	53.3%

B. Resistance Components and Lateral Abruptness

Table III shows the resistive components calculated using (7) for a different set of devices with various lateral source/drain extension abruptness. A 30% decrease in $R_{overlap}$ is observed as the lateral abruptness varies from 6.5 nm/dec to 1.9 nm/dec. The qualitative trend is consistent with the predictions of Ng and Lynch [1]. Note that $R_{overlap}$ is the only resistive component with a strong dependence on lateral source/drain extension abruptness.

C. Gate-Bias Dependence of Resistance Components

Fig. 5 shows the sheet resistance of a device with lateral source/drain extension abruptness of 1.9 nm/dec at various applied gate biases. The gate extends from -0.025 to 0.025 μm, while the metallurgical junctions lie at ± 0.011 μm. It is clear that the channel and extension resistances have strong gate-bias dependence, due to gate control of the inversion and accumulation layers.

Fig. 6(a) shows schematically the bias dependent parts of the equipotential resistive strips. The bias dependent part is defined as the region in which the resistivity varies by more than 1% as the gate bias varies from 0.4 V to V_{dd}. Using (2), the gate-bias dependent part of the conductance for each equipotential strip is

$$G_{\phi_1,\phi_2,dept} = \frac{W}{\phi_2 - \phi_1} \int_{\mathcal{L}_{dept}} \sigma(\vec{x}) \vec{\nabla}\phi(\vec{x}) \cdot d\vec{l} \qquad (8)$$

where $\mathcal{L}_{dept}$ is the gate bias dependent part of the strip. Fig. 6(b) shows the gate-bias dependent resistance as a fraction of the

TABLE III
COMPARING RESISTIVE COMPONENTS FOR DEVICES WITH DIFFERENT LATERAL DOPING ABRUPTNESS IN THE SOURCE/DRAIN EXTENSION REGION. UNITS IN Ω/μm

Abruptness	R_{co}	R_{spacer}	$R_{overlap}$	R_{chan}	V_{th}
1.9 nm/dec	135.1	26.86	63.86	198.5	0.3459
3.3 nm/dec	135.1	27.1	72.7	212.7	0.3750
4.5 nm/dec	135.1	27.5	80.62	220.2	0.3862
6.5 nm/dec	135.1	28.58	91.88	222.4	0.3865

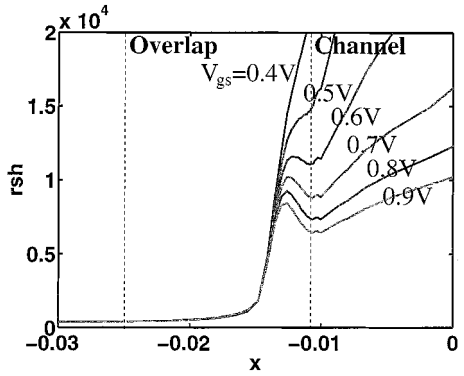


Fig. 5. Plot of sheet resistance along the channel for various V_{gs}. Lateral doping abruptness in the source/drain extension region is 1.9 nm/dec for this device. The gate extends from -0.025 to 0.025 μm. The metallurgical junctions lie at ± 0.011 μm, respectively.

total strip resistance. In the channel and part of the source/drain extension (close to the channel), the resistance of the entires trip depends on gate voltage.[7] Away from the channel, current spreading siphons current from the accumulation layer, causing the fraction of the strip under gate control to become smaller. Note that current spreading starts sooner for abrupt doping profiles.

VI. RESISTANCE CALCULATION VERSUS RESISTANCE EXTRACTION

While the resistance calculations described in Section III provide valuable insights it cannot be applied directly to actual devices.[8] To handle experimental data, extraction techniques such as the shift-and-ratio method [8], [9] are essential. Correlating the physical resistances [as calculated by (2) or (7)] with the values obtained by these extraction techniques is not straight forward, however.

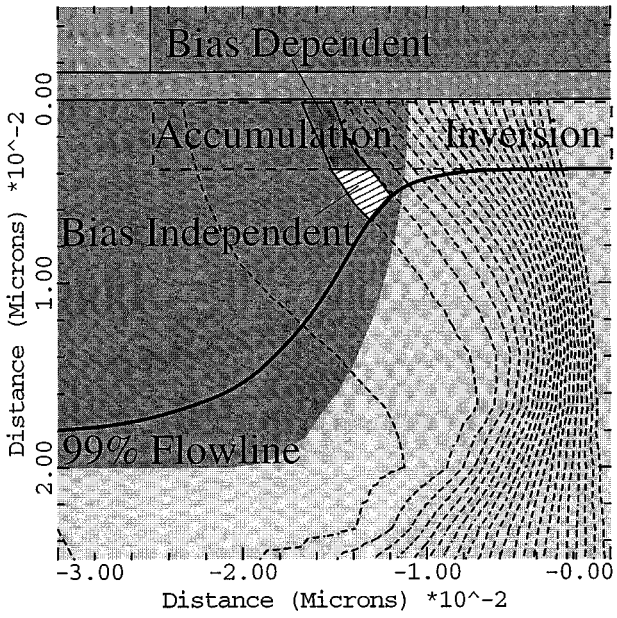
A. Shift-and-Ratio Method

The shift-and-ratio method is based on the following [9]

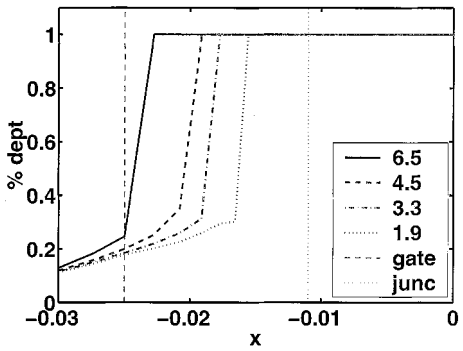
$$R^i_{tot}(V_g) = \hat{R}_{sd} + \hat{L}^i_{\text{eff}}\hat{f}_{ch}(V_g - V^0_t - \delta^i). \tag{9}$$

[7]This is consistent with Fig. 5.

[8]Spatial variation of quasifermi level cannot be measured directly.



(a)



(b)

Fig. 6. (a) Partitioning of resistive strips in to bias dependent and independent parts. (b) Plot of the contribution of the gate bias dependent part of the sheet conductance versus distance.

A major assumption of (9) is that the total device resistance can be partitioned into a gate-bias independent part ($\hat{R}_{sd}$), and a gate-bias dependent part that is directly proportional to channel length. The latter component is assumed to have the same basic functional V_g dependence for devices of all channel lengths.[9]

To obtain the threshold shift δ^i, the derivatives of the total resistance for the long channel and short channel devices are shifted with respect to one another until their ratio is approximately independent of gate bias. The effective channel length and source/drain resistance of the short channel device are then calculated from [8], [9]

$$\frac{\hat{L}^0_{\text{eff}}}{\hat{L}^i_{\text{eff}}} = r_{\delta\min} \equiv \frac{dR^0_{tot}(V_g)}{dV_g} \Big/ \frac{dR^i_{tot}(V_g - \delta^i)}{dV_g} \tag{10}$$

$$\hat{R}_{sd} = \frac{r_{\delta\min}R^i_{tot}(V_g - \delta^i) - R^0_{tot}(V_g)}{r_{\delta\min} - 1}. \tag{11}$$

Note that the gate bias range used in the extraction could have substantial influence on the extracted results [9].

[9]Threshold voltages are allowed to vary with channel lengths.

TABLE IV
EFFECTIVE CHANNEL LENGTHS AND SERIES RESISTANCES EXTRACTED USING THE SHIFT-AND-RATIO METHOD FOR DEVICES WITH GATE LENGTH OF 50 nm. V_{gs} EXTRACTION RANGE USED IN THE SHIFT-AND-RATIO METHOD IS FROM 0.8 V TO 1.5 V

Lat Abruptness	L_{eff} (nm)	R_{sd} (Ω)
1.9 nm/dec	20.9	153.9
3.3 nm/dec	21.6	164.1
4.5 nm/dec	21.9	176.0
6.5 nm/dec	22.5	178.5

B. Shift-and-Ratio Versus Physical Resistances

The $\hat{L}_{\text{eff}}$ and $\hat{R}_{sd}$ values extracted from the shift-and-ratio method, for devices with 50 nm gate length and various lateral source/drain abruptnesses, are shown in Table IV and Fig. 7. Compare $\hat{R}_{sd}$ with the gate-bias independent part[10] of the physical source/drain resistance R_0[11] shown in Fig. 7. While $\hat{R}_{sd}$ extracted using the shift-and-ratio method depends strongly on lateral source/drain abruptness, R_0 is essentially independent of lateral abruptness. Given that R_{ov} is the only resistive component with a strong dependence on lateral abruptness, it seems that $\hat{R}_{sd}$ actually incorporates a portion of R_{ov}, which is gate-bias dependent. This violates the assumptions of (9).

Note that while the previous implies that $\hat{R}_{sd}$ is supposed to be R_0 plus part of R_{ov}, R_0 is actually larger than the extracted $\hat{R}_{sd}$ for the 1.9 nm/dec case. Also, the extracted $\hat{L}_{\text{eff}}$ of devices with very abrupt junctions are smaller than the metallurgical channel length of 22 nm.[12] We shall return to these discrepancies in Section VI-D.

C. Extraction of Gate-Bias Dependent Source/Drain Resistance

A new extraction method that relaxes the assumption that the source/drain resistance be gate-bias independent is now presented. This will help in studying the behavior of the shift-and-ratio method in more detail.

Due to the accumulation layer, the resistance in the gate-extension overlap region is bias dependent. However this bias dependence is different from that of the channel due to differences in the conduction mechanisms.[13] Accordingly, (9) is modified to allow source/drain resistance to vary with gate bias

$$R^i_{tot}(V_g) = \tilde{R}_{sd}(V_g) + \tilde{L}^i_{\text{eff}}\tilde{f}_{ch}(V_g - V_t^0 - \delta^i). \tag{12}$$

The terms in (12) can be extracted by considering a long channel device and two other devices of different gate lengths.

[10]Resistances are assumed to be gate-bias independent where $r_{sh}(V_g = 0.4\text{ V})$ and $r_{sh}(V_g = V_{dd})$ differ by less than 1%.

[11]Calculated from the quasi-Fermi level.

[12]Devices with $\hat{L}_{\text{eff}}$ smaller than L_{met} are also observed in [9].

[13]Accumulation layer and current spreading in the overlap region versus inversion layer in the channel.

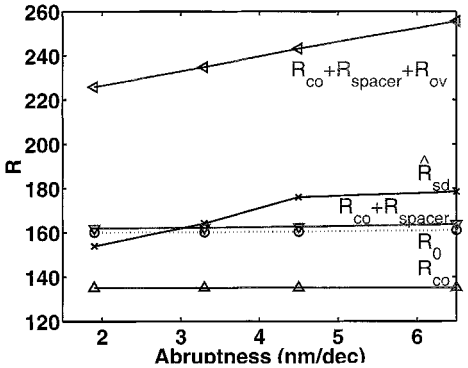


Fig. 7. Comparing $\hat{R}_{sd}$ extracted through shift-and-ratio with the physical resistances calculated using (7).

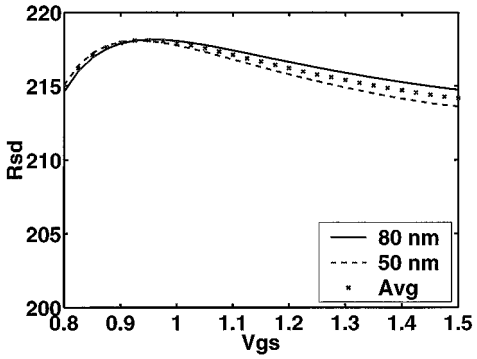


Fig. 8. Extracted $\widetilde{R_{sd}}$ term in Ω for the 50-nm device, the 80-nm device and their average. Note the difference between the three cases are less than 1%.

Assuming the former is dominated by channel resistance, the channel resistance per unit length is

$$\tilde{f}_{ch}(V_g - V_t^0) \approx \frac{R^0_{tot}(V_g)}{\tilde{L}^0_{\text{eff}}} \approx \frac{R^0_{tot}(V_g)}{L^0_{gate}}. \tag{13}$$

For the remaining devices, we can write

$$\tilde{R}^a_{sd}(V_g) = R^a_{tot}(V_g) - (L^a_{gate} - \Delta L)\cdot\tilde{f}_{ch}(V_g - V_t^0 - \delta V_t^a) \tag{14}$$

$$\tilde{R}^b_{sd}(V_g) = R^b_{tot}(V_g) - (L^b_{gate} - \Delta L)\cdot\tilde{f}_{ch}(V_g - V_t^0 - \delta V_t^b). \tag{15}$$

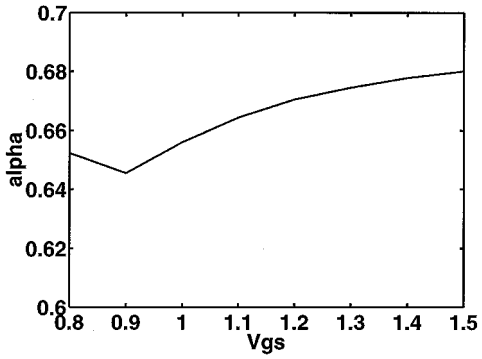
Now $\tilde{R}^a_{sd}(V_g)$ should equal $\tilde{R}^b_{sd}(V_g)$. Hence, ΔL, δV_t^a, and δV_t^b can be extracted by minimizing[14]

$$E = \sum_i \left(\tilde{R}^a_{sd}(V_g^i) - \tilde{R}^b_{sd}(V_g^i)\right)^2. \tag{16}$$

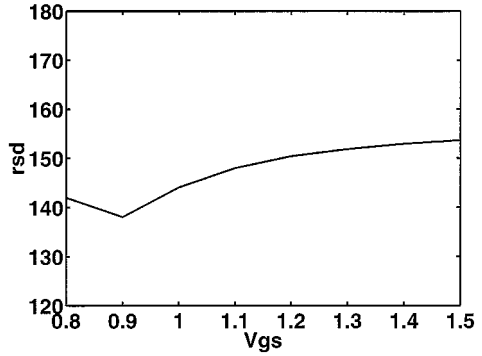
D. Limits of the Shift-and-Ratio Method

We can now examine the impact of the assumptions of the shift-and-ratio method on the extracted results. We begin by fitting the model represented by (12) to the simulated data.

[14]For instance, through simulated annealing.



(a)



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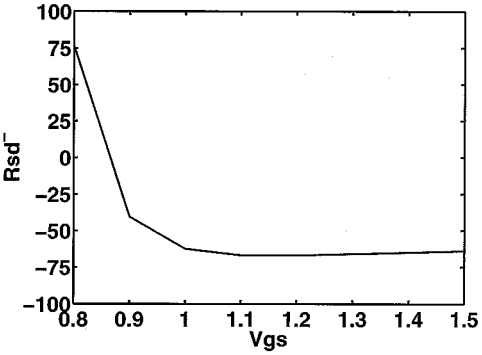

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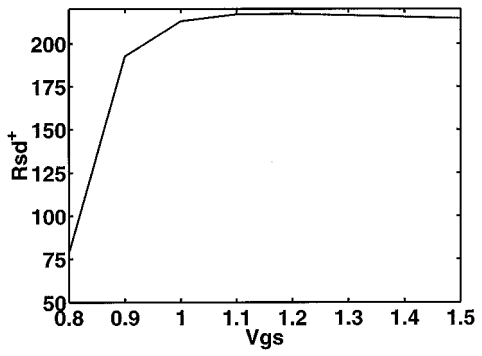

(d)

Fig. 9. Shift-and-ratio method applied to (12), with terms fitted to simulated devices with lateral extension abruptness of 1.9 nm/dec. (a) α factor. (b) Extracted R_{sd} from shift-and-ratio method. (c) R_{sd}^{-} from (18). (d) R_{sd}^{+} from (18). All resistance in Ohms.

Applying the procedure described in Section VI-C to simulated devices with gate lengths of 5 μm, 80 nm, and 50 nm yields an optimal fit at $\Delta L = 0.0356$, $\delta V_t^a = 0.131$ and $\delta V_t^b = 0.036$. The extracted R_{sd} versus gate bias is shown in Fig. 8. The extracted R_{sd} for the 50 nm and the 80 nm devices differ by less than 1%, suggesting that (12) is a good model in this case.

Consider applying the shift-and-ratio method to this model. Equation (10) becomes

$$r_{\delta\,\min} = \frac{L^0}{\tilde{L}^i}\,\frac{\frac{\tilde{R}'_{sd}(V_g)}{L^0} + f'_{ch}(V_g - V_t^0)}{\frac{\tilde{R}'_{sd}(V_g-\delta)}{\tilde{L}^i} + f'_{ch}(V_g - V_t^i - \delta)} = \left(\frac{L^0}{L^i}\right)\cdot\alpha. \tag{17}$$

Meanwhile, equation (11) becomes

$$\hat{R}_{sd} = \hat{R}_{sd}^{+} + \hat{R}_{sd}^{-} \tag{18}$$

where

$$\hat{R}_{sd}^{+} = \frac{\frac{\tilde{L}^0}{\tilde{L}^i}\,\alpha\,\frac{\tilde{R}_{sd}(V_g-\delta)}{\tilde{R}_{sd}(V_g)} - 1}{\frac{\tilde{L}^0}{\tilde{L}^i}\,\alpha - 1}\,\tilde{R}_{sd}(V_g) \tag{19}$$

$$\hat{R}_{sd}^{-} = \frac{\alpha - 1}{\frac{\tilde{L}^0}{\tilde{L}^i}\,\alpha - 1}\,\tilde{L}^0\tilde{f}_{ch}(V_g - V_t^0). \tag{20}$$

There are the constituent components of $\hat{R}_{sd}$.

Fig. 9 shows (17), (19) and (20) for the current example. $\hat{R}_{sd}^{+}$ [Fig. 9(d)] approximately equals the total physical resistance ($R_{co} + R_{spacer} + R_{ov}$). $\hat{R}_{sd}$ as extracted by the shift-and-ratio method [Fig. 9(b)] does not, contrary to desired. This is because the extension is influenced by the gate and α can be smaller than unity

$$\alpha \approx \frac{1}{1 + \frac{R_{sd1}f'_{sd}(V_g-\delta)}{L^i f'_{ch}(V_g - V_t^i - \delta)}} \tag{21}$$

which can then cause $\hat{R}_{sd}^{-}$ to become negative [Fig. 9(c)]. In fact, the value of this negative term is sufficiently large to cause the extracted R_{sd} to be smaller than R_0, as observed in Section VI-A. Note that the negative resistance component is a result of violating the assumptions of the extraction method, and has no physical meaning.

A couple of comments on the extracted L_{eff} is in order. First, (17) reduces to L^0/L^i when $V_t^0 = V_t^i + \delta$ and either the extension resistance is small or substantially less gate bias dependent than the channel resistance. When the extension is measurably influenced by the gate (e.g., in gradual junctions), α can be smaller than unity. Hence L_{eff}^i increases for gradual junctions, as in Table IV.

Second, in Section VI-A, it was observed that the extracted L_{eff} can be smaller than L_{met} for devices with abrupt junctions. The key to note is that the difference between the two terms in (12) lies in the fact that the latter is proportional to L. Due to counter-doping and short channel effects,[15] the edge of the channel behaves differently from the center, and is not scaled with channel length. The extraction routine cannot distinguish between this and the source/drain resistance, thus it lumps the former with the latter. The "base" channel length L as defined by (12) is thus shorter than L_{met}: it is 14 nm for the 50-nm device

[15]The following applies also in the presence of halo and reverse short channel effects.

in Section VI-C, smaller than the metallurgical channel length of 22 nm. At the same time, a small α factor of 0.67 is obtained [Fig. 9(a)]. The $L_{\rm eff}$, extracted using the shift-and-ratio method, of 20.9 nm in Table IV result from dividing 14 nm by the factor 0.67.

E. Discussion

Extraction results obtained when the assumptions of the extraction method are violated will lose physical meaning. Violation of these assumptions for deep sub-micron devices become more likely due to the complexity of the device physics. This does not by any means invalidate shift-and-ratio and other extraction methods. However, conclusions about the physical device, such as the metallurgical channel length and lateral doping profile [10], obtained from these extraction methods have to treated with caution [11]. All major assumptions of the methods have to be examined for their impact, and relaxed if necessary.[16] Alternatively, one can treat the extraction method as the *definition* of electrical quantities, to be used only in a context that is consistent with the extraction method [14], and rely instead on physical techniques such as those described in [15]–[17] for obtaining physical quantities.

The extraction procedure described in Section VI-C relaxes the assumption that the source/drain resistance be gate-bias independent.[17] However, the requirement for measurement of devices with three different channel lengths may make it vulnerable to statistical process variations [18].[18] The presentation and use of (12) in this paper is intended solely as a vehicle for error analysis and interpretation of the observed trends.

VII. Conclusions

A rigorous method for calculating bulk and contact resistances using device simulation that properly accounts for the 2-D nature of current flow in scaled MOS devices is presented. This is compared with two other resistance calculation strategies. Resistance calculations based on partitioning the device into vertical strips are shown to yield substantial errors where current spreading is important, and can result in an overestimation of the benefits of abrupt junctions. The sheet resistance equation based on the quasi-Fermi level at the Si/SiO_2 interface is shown to be identical to a special case of the generalized method.

The shift-and-ratio method is applied to simulated data and the results are correlated with the physical resistances of the device calculated using the methods described in this paper. Two of the assumptions of the shift-and-ratio method are violated for deep submicron devices: that 1) the source/drain resistance is gate-bias independent, and 2) the channel resistance is directly proportional to channel length. As a result, the effective channel length can be shorter than the metallurgical channel length and the extracted source/drain resistance can be smaller than the physical values. A new extraction method that relaxes some of these assumptions is presented.

[16]For example, the extraction method described in Section VI-C. Alternatively, inverse modeling techniques [12], [13], with proper choice of physical models, may be used.

[17]Imposed by the shift-and-ratio method.

[18]This is not a concern for simulated data and for understanding the operation of the shift-and-ratio method.

Ultimately, the extracted value from the shift-and-ratio method makes sense only within the context of the assumptions on which the method is based. It may be best to treat the extracted quantities as electrical values that may be useful even if they do not correlate fully with the physical quantities, and rely more on physical techniques for extracting physical parameters such as the lateral doping profile and metallurgical channel length.

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