# Dopant Profile and Gate Geometric Effects on Polysilicon Gate Depletion in Scaled MOS

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***Abstract*—Polysilicon depletion effects show a strong gate length dependence according to experimental p-channel MOS capacitance–voltage ($C$–$V$) data. The effect can be influenced not only by gate geometries, but also by dopant profiles in poly-gates. These effects have been modeled and verified using device simulation. Nonuniform dopant distributions in the vertical and lateral direction in the poly-gate cause additional potential drops. The potential drop in the poly-gate becomes critical as the gate geometry is scaled down due to edge and corner depletions resulting from fringing electric fields.**

***Index Terms*—Capacitance–voltage ($C$–$V$), dopant profile, gate geometry, polydepletion, polysilicon depletion, scaled MOS.**

## I. Introduction

INSUFFICIENTLY high doping in polysilicon gates becomes inevitable in modern CMOS processes due to conflicting requirements for low-energy ion implantation and constrained annealing conditions to achieve ultra-shallow source and drain junctions. This results in polydepletion effects for ultra-thin oxide MOSFETs due to the serial connection of the reduced polydepletion capacitance ($C_p$) with the enlarged oxide capacitance ($C_{ox,\,eff}$), leading to degradation of inversion gate capacitance and transconductance [1], [2].

Fig. 1 shows the measured inversion gate capacitance ($C_{inv}$) relative to accumulation gate capacitance ($C_{acc}$) for p-channel MOSFET with various gate lengths [3]. The oxide thickness is 1.6 nm, and the channel width is 1000 $\mu$m of the p-channel MOSFET. $C_{inv}/C_{acc}$ for each gate length has been corrected by considering the gate overlap capacitance ($C_{ov}$) $(C_{inv} - C_{ov})/(C_{acc} - C_{ov})$. The portion of potential drop ($V_p$) in poly-gate relative to the potential difference between the gate and the channel ($V_{GS} = V_G - V_S$) can be extracted based on the voltage division. It should be noted that as the gate length is scaled down, the portion of the inversion capacitance decreases, while the potential drop ($V_p$) increases, implying that device performance deterioration from the polydepletion effect will be more significant as devices continue to scale.

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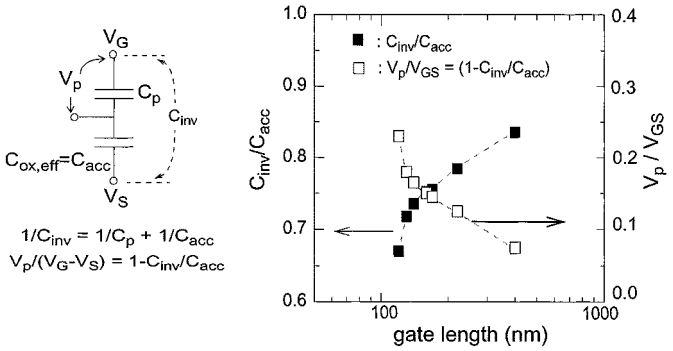


Fig. 1. Experimentally measured $C_{inv}/C_{acc}$ and $V_p/V_{GS}$ for PMOS, corrected for gate overlap capacitance ($C_{ov}$) [i.e., $(C_{inv} - C_{ov})/(C_{acc} - C_{ov})$], showing severe polydepletion effects in scaled devices. $C_{acc}$ and $C_{inv}$ are chosen at $V_{GS} = 2.0$ and $-1.0$ V, respectively, from the measured $CV$ curves.

This article discusses the impact of gate geometry and dopant distributions on polydepletion effects based on two and three-dimensional (3-D) device simulations.

## II. Dopant Profile Effects on Polydepletion

### A. Vertical Dopant Profile

Nonuniform, graded doping profiles of poly-gates can be attributed to the ion implant and constrained annealing conditions to avoid impurity penetration through the gate oxide, while maintaining shallow junction depths. The energy-band diagram in the presence of a nonuniform dopant distribution is shown in Fig. 2. When the gate is doped by ion implantation, the dopant distribution as a function of position from the top down to the gate oxide direction can be represented as shown in Fig. 2(a). Since the dopant density and carrier concentration vary with position, a built-in electric field exists between $x_1$ and $x_2$, leading to built-in potential, as shown in Fig. 2(b). Under thermal equilibrium there is no current flow; the built-in field, $E_x$, in an n-type poly-gate can be expressed as [4]

$$E_x = -\frac{d\phi}{dx} \approx -\frac{kT}{q}\,\frac{1}{N_d}\,\frac{dN_d}{dx} \qquad d\phi \approx \frac{kT}{q}\,\frac{dN_d}{N_d} \tag{1}$$

where $\phi$ is the potential, and $N_d$ is the position-dependent doping concentration. A potential drop ($\Delta V_p$) is established at the interface due to the graded dopant distribution between $x_1$ and $x_2$, which can be expressed as

$$\Delta V_p = \phi_{x1} - \phi_{x2} = \frac{kT}{q}\,\ln\frac{N_{d,x1}}{N_{d,x2}}. \tag{2}$$

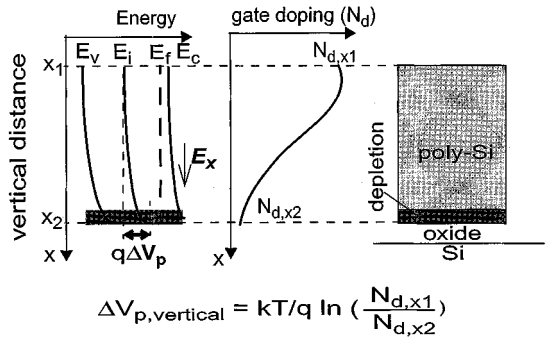


Fig. 2. Nonuniform, graded impurity distribution and corresponding band diagram, showing built-in electric field ($E_x$) and potential drop in the poly-gate region.

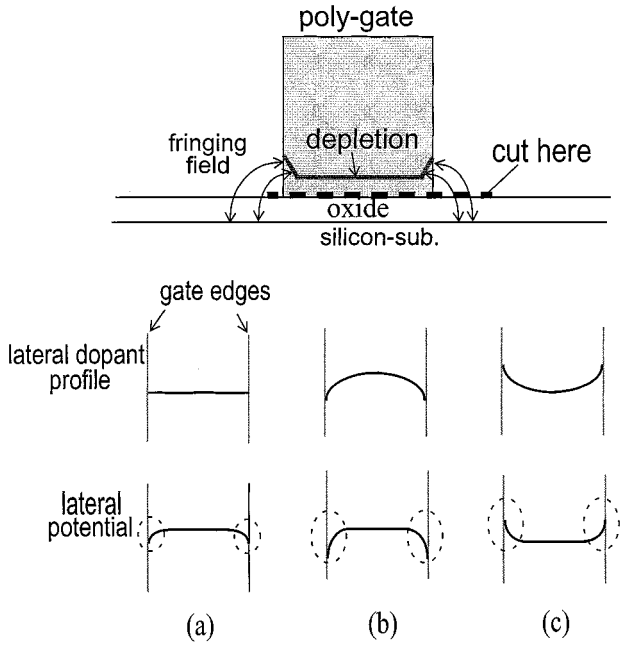


Fig. 3. Potential distributions along the bottom-gate for different lateral dopant distributions: (a) uniform, (b) convex, and (c) concave dopant profiles.

For example, when $N_d$ changes from $10^{20}$ to $10^{18}$ cm$^{-3}$, the potential drop is about 0.12 V estimated from (2) even with no gate bias, which is on the order of the threshold voltage for sub-100 nm MOSFETs. This additional potential drop across the polysilicon gate should be added to the voltage drop based on the uniform dopant concentration.

### B. Lateral Dopant Profile

Unless the polysilicon gate is completely degenerate, there is an enhanced potential drop at the gate edges caused by the fringing gate fields that terminate on the depletion boundary inside the gate sidewall, as depicted in Fig. 3. Even for the case of uniform doping, as shown in Fig. 3(a), the reduction of potential at the gate edge is shown to be about 13% based on two-dimensional (2-D) Poisson's equation solutions [5]. For a laterally convex dopant distribution, as shown in Fig. 3(b), more potential reduction occurs in the gate sidewalls, compared to that for the uniform doping case. This is caused by the lower dopant concentration in the gate sidewalls which further widens the depletion width, leading to additional potential drops. This is common when the gate dopant is Boron (i.e., p-channel MOS), since Boron atoms in silicon have a tendency to diffuse toward adjacent oxide regions. On the contrary, for a concave dopant profile in which the dopant concentration has its peak at the sidewall, the potential in the edge is now higher than that of the inner poly region, as shown in Fig. 3(c).

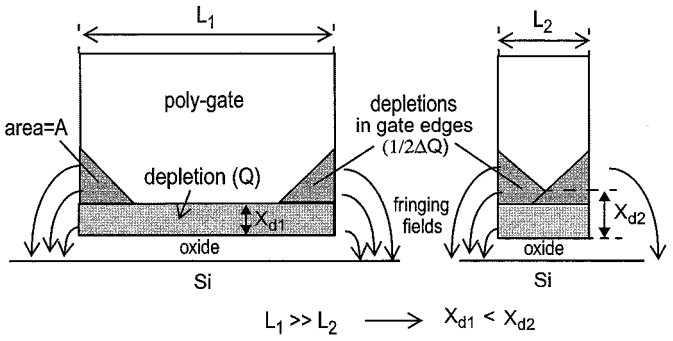


Fig. 4. Gate length effect on polydepletion, showing that an effective depletion width is wider for the shorter gate length, leading to an additional potential drop.

## III. Gate Geometric Effects on Polydepletion

### A. Gate Length Effects

A simple model of the polydepletion effect which depends on gate length is shown in Fig. 4. Similar to the well-known narrow-width effect, the portion of the additional charge ($\Delta Q$) to the total charge ($Q+\Delta Q$) becomes higher as the gate length is scaled down, resulting in wider depletion widths and additional potential drops for scaled gate lengths. Let $A$ denote the triangular area of the additional charge $\Delta Q$, then the additional potential drop ($\Delta V_p$) due to the sidewall depletion is approximated as [6]

$$\frac{1}{2}\Delta Q \approx qN_d \frac{A}{L}\,(\mathrm{C/cm^2}) \tag{3}$$

$$\Delta V_p \approx \frac{\Delta Q}{C_d} = \frac{2qN_dA}{LC_d} \tag{4}$$

where $L$ is the gate length and $C_d$ is the depletion capacitance in the sidewalls. Equation (4) implies that $\Delta V_p$ increases in inverse proportion to the gate length ($L$). This $\Delta V_p$ should be taken into account to reflect further polydepletion for very short gate lengths.

### B. Gate Width Effects

Consider the polydepletion effect for small-geometry devices. Fig. 5 shows a graphical interpretation of 3-D geometric effects for polydepletion when shallow trench isolation (STI) [7] is not considered. Notice the edge and corner depletion effects along the gate sidewalls in Fig. 5(b). The top views are for the gate plane slightly above the depletion region, as represented in Fig. 5(a). The corner depletion represented by the triangular region denotes the cross-over region, in which the width and length-direction depletions encounter each other. This geometrical effect of the polydepletion is problematic

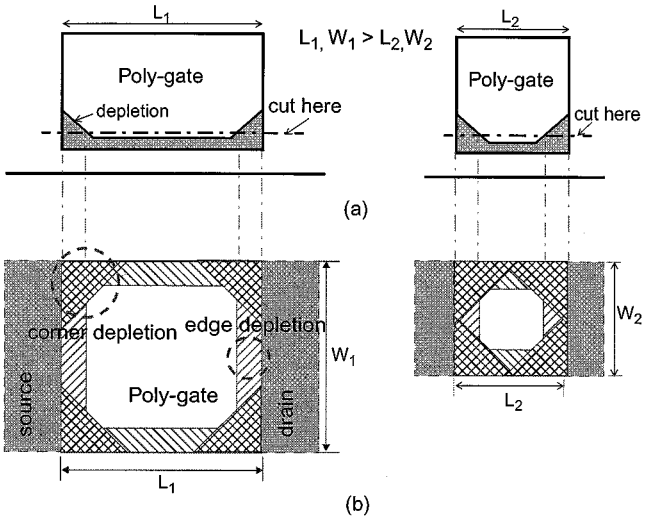


Fig. 5. Polydepletion effect for small-geometry devices. (a) Cross section for different gate sizes and (b) top view of corner and edge depletions on the gate plane represented in (a).

for small-geometry devices since this region cannot be scaled down even though the device dimensions continue to decrease. By comparing two different gate geometries, it is obvious that the portion of the edge and corner depletions relative to the whole gate area is greater for the small gate. Thus, additional potential is dropped across the poly-gate in small-geometry devices. Moreover, the charge shared due to the cross-over is shown to be larger than the simple sum of the charge resulting from the width and length-direction depletions [5]; an additional coupling effect exists in the cross-over region and the mutual modulation by this effect widens the depletion width for small-geometry devices.

## IV. Simulation and Analysis

### A. Dopant Profile Effects

Comparison of potential drops ($V_p$) has been made for nonuniform ("$A$") and uniform doping ("$B$") cases, as represented in Fig. 6(a). Potential distributions along the bottom gate interface obtained by using the 2-D device simulator, MEDICI [8], are shown in Fig. 6(b). It is instructive that the potential drop in the gate region for case "$B$" ($V_{p,B}$) is less than that for case "$A$" ($V_{p,A}$), in spite of its lower average doping concentration, which can be attributed to the graded impurity distribution effects, discussed previously.

Consider a p-channel MOS with p-type doped poly-gate. The thickness of the poly-gate and gate oxide are 0.12 $\mu$m and 2.0 nm, respectively. Fig. 7 shows simulated potential distributions for different lateral dopant profiles and gate lengths. For three cases, the vertical dopant profile is assumed to be identical with a peak concentration of $\sim 4.5 \times 10^{19}$ cm$^{-3}$ and minimum concentration of $\sim 1.0 \times 10^{19}$ cm$^{-3}$, as represented in Fig. 7(a). For a uniform dopant profile in Fig. 7(a), the overall potential for $L_g = 35$ nm is lower than that for $L_g = 100$ nm due to potential reduction at the gate edges. The potential drop in the edge is enhanced for a laterally convex dopant profile, as shown in Fig. 7(b), such that the overall potential is further reduced for the shorter gate length. Consider a concave dopant profile as

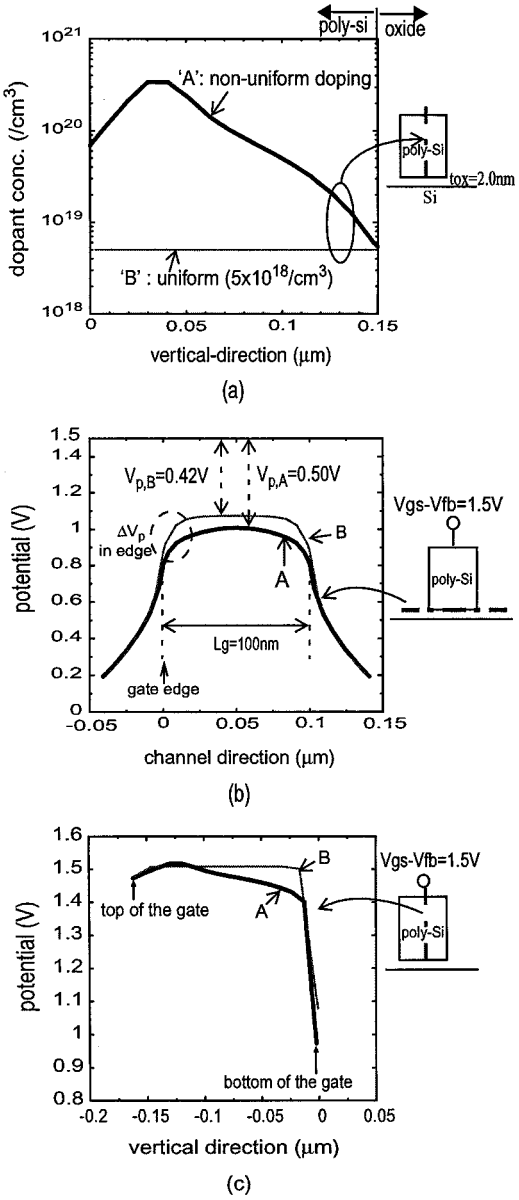


Fig. 6. Impact of vertically nonuniform dopant distribution on polydepletion: (a) dopant distributions in the vertical direction for nonuniform ("$A$") and uniform ("$B$") cases, (b) comparison of potential drops in the lateral direction, and (c) comparison of potential drops in the vertical direction.

shown in Fig. 7(c), which is not a common profile; the dopant profile has its peak in the edges and decreases toward inside down to $\sim 1.0 \times 10^{19}$ cm$^{-3}$. Contrary to the previous cases, less potential drop occurs in the edge regions compared to that in the middle of the gate. As a result, the average potential for $L_g = 35$ nm is higher than that of $L_g = 100$ nm.

### B. Gate Geometric Effects

Simulated gate capacitances of p-channel MOS devices show that a nonuniform gate dopant profile with the peak concentration of $\sim 4.5 \times 10^{19}$ cm$^{-3}$ and the minimum concentration near the poly-gate/oxide interface of $\sim 1.0 \times 10^{19}$ cm$^{-3}$ produces significant $C_{inv}$ reductions, as shown in Fig. 8(a). A convex dopant profile in the lateral direction is used in this work. In order to eliminate possible short-channel effects, the

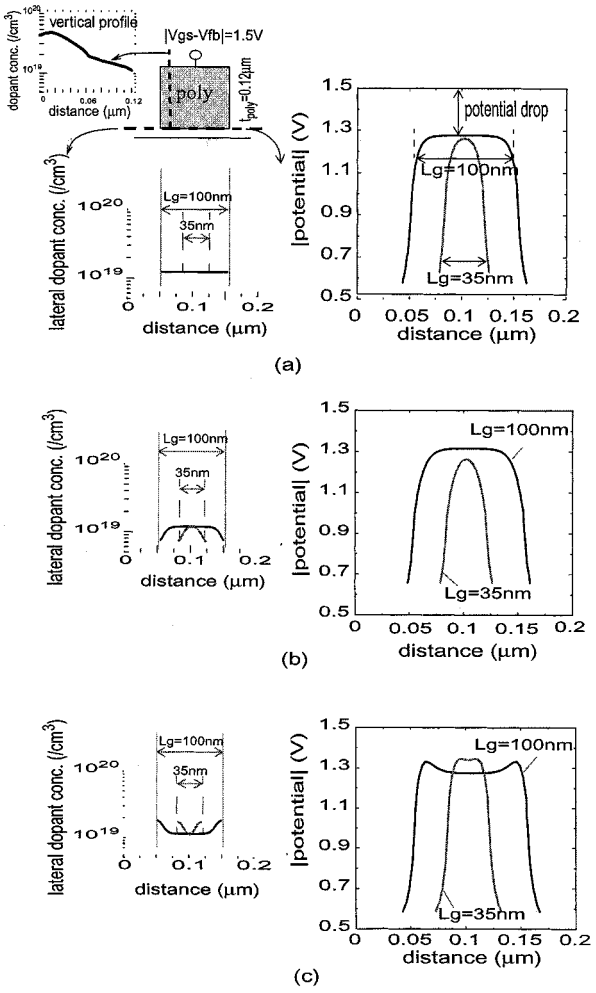


Fig. 7. Gate length-dependent potential distributions for different lateral dopant profiles (MOS devices for $t_{ox} = 2.0$ nm and $t_{poly} = 0.12$ $\mu$m): (a) uniform, (b) convex, and (c) concave dopant profile.

source/drain regions have not been included in the simulated structure.

The normalized gate capacitance corrected for overlap capacitance ($C_{ov}$), $(C_g - C_{ov})/(C_{acc,\max} - C_{ov})$, decreases with the gate length from $L_g = 250$ nm down to $L_g = 25$ nm. As a result, as shown in Fig. 8(b), the portion of simulated maximum inversion capacitance relative to accumulation capacitance, $C_{\max,inv}/C_{\max,acc}$, shows trends consistent with experiments previously presented in Fig. 1.

In order to observe the gate geometric effect of polydepletion, 3-D device simulations [9] are performed for two different gate sizes $W/L = 100$ nm/100 nm and $W/L = 35$ nm/35 nm. Shallow trench isolations (STIs) and $p^+$ source/drain regions are included in the structures. A laterally uniform and vertically graded gate dopant profile, as shown in the inset of Fig. 8(a), is used in this work. Simulated potential contours within the poly-gate are shown in Fig. 9. The absolute potential value on the top of the gate (i.e., $|V_{gs} - V_{fb}|$) is 2.5 V, while it reduces to 2.2–2.3 V near the depletion region of the gate. Note that the portion of the reduced potential area in the edge and corner regions relative to the whole gate area is higher for the smaller gate. The average potential value of the $W/L = 35$ nm/35 nm is less than that for $W/L = 100$ nm/100 nm.

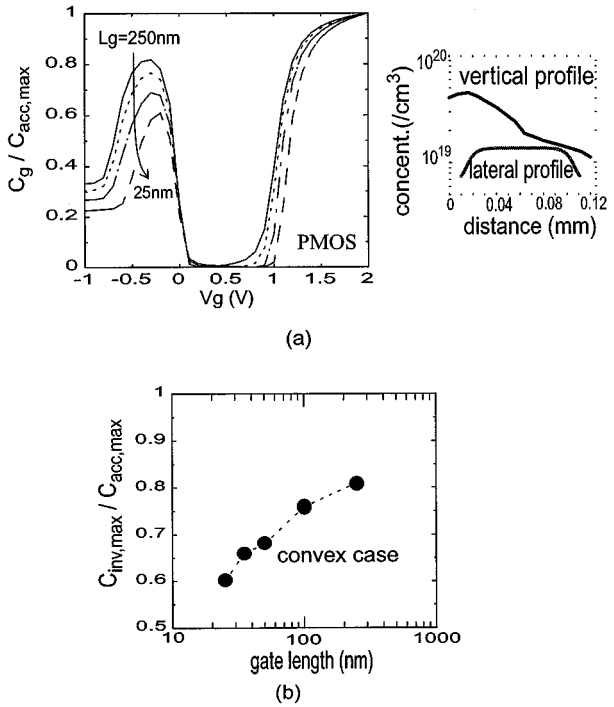


Fig. 8. Simulated gate capacitance of p-channel MOS for various gate lengths ($t_{ox} = 2.0$ nm and $t_{poly} = 0.12$ $\mu$m). (a) Normalized gate capacitance corrected for gate overlap capacitance; $(C_g - C_{ov})/(C_{acc,\max} - C_{ov})$ for $L_g = 250$, 100, 50, and 25 nm. Vertical and lateral dopant profiles (i.e., $L_g = 100$ nm) used in the simulation are also shown. (b) Ratio of maximum inversion capacitance ($C_{inv,\max}$) to maximum accumulation capacitance ($C_{acc,\max}$).

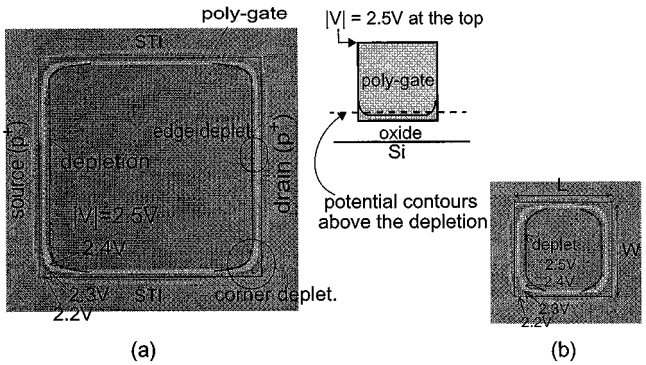


Fig. 9. Potential contours obtained from 3-D device simulation. Potential contours are taken along the depletion of the poly-gate, which is ~10 nm above the gate/oxide interface: (a) $W/L = 100$ nm/100 nm and (b) $W/L = 35$ nm/35 nm.

## V. Conclusions

Impact of nonuniform dopant distributions and gate geometry to polydepletion effects is reported based on a study using device simulation. Vertically nonuniform and steep dopant profiles in poly-gate result in built-in electric field effects and potential drops in the gate region. Laterally uniform and convex dopant profiles in the poly-gate cause substantial edge potential drops for short gate lengths, mainly due to fringing fields. Polydepletion effects will become more severe with continued scaling of MOSFETs due to the significance of corner and edge effects. Achieving highly doped gates with less dopant gradient in the poly-gate can be the most appropriate solution to overcome these problems.

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## REFERENCES

[1] R. Rios, N. D. Arora, and C.-L. Huang, "An analytic polysilicon depletion effect model for MOSFETs," *IEEE Electron Device Lett.*, vol. 15, pp. 129–131, Apr. 1994.
[2] N. D. Arora, R. Rios, and C.-L. Huang, "Modeling the polysilicon depletion effect and its impact on submicrometer CMOS circuit performance," *IEEE Trans. Electron Devices*, vol. 42, pp. 935–943, May 1995.
[3] C.-H. Choi, P. R. Chidambaram, R. Khamankar, C. F. Machala, Z. Yu, and R. W. Dutton, "Gate length dependent polysilicon depletion effects," *IEEE Electron Device Lett.*, vol. 23, pp. 224–226, Apr. 2002.
[4] R. Muller and T. Kamins, *Device Electronics for Integrated Circuits*. New York: Wiley, 1986.
[5] K. K. Hsueh, J. J. Sanchez, T. A. Demassa, and L. A. Akers, "Inverse-narrow-width effects and small-geometry MOSFET threshold model," *IEEE Trans. Electron Devices*, vol. 35, pp. 325–338, Mar. 1988.
[6] N. Arora, *MOSFET Models for VLSI Circuit Simulation*. New York: Springer-Verlag, 1993.
[7] T. Oishi, K. Shiozawa, A. Furukawa, and Y. Tokuda, "Isolation edge effect depending on gate length of MOSFETs with various isolation structures," *IEEE Trans. Electron Devices*, vol. 47, pp. 822–827, Apr. 2000.
[8] *MEDICI User's Manual*. Fremont, CA: Avant! Corp., 2000.
[9] *DAVINCI User's Manual*. Fremont, CA: Avant! Corp., 2000.

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