On-Chip Inductance Modeling and RLC Extraction of VLSI Interconnects for Circuit Simulation

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Abstract - On-Chip inductance modeling of VLSI interconnects is presented which captures 3D geometry from layout design and process technology information. Analytical formulae are derived for quick and accurate inductance estimation which can be used in circuit simulations and whole chip extraction screening process. Circuit simulations show critical global wire inductive effects as well as power and ground inductive noise.

I. INTRODUCTION

With high clock frequencies and faster transistor rise/fall time in modern VLSI circuits, long signal wires exhibit transmission line effects. Because of the use of wider wire and Cu interconnects for critical signals such as clock trees, inductance of the interconnect can no longer be ignored compared with its resistive component. Due to on-chip inductance effects, signal ringing is observed, cross talk is increased and power/ground bounce (noise) becomes worse. In high clock frequency microprocessor and ASIC designs, clock trees and power/ground grid need to be designed carefully to avoid large clock skew, signal inductive coupling and ground bounce [1][2].

To accurately model on-chip inductance, 3D geometry modeling which is based on 2D geometry layout information and process technology information is required. Electromagnetic field solvers are typically used to extract inductance based on these 3D geometry modeling. The values are often used as golden results of inductance extraction. Since it is computational expensive to use field solvers for the whole chip extraction, analytical formulae are desired to quickly and accurately calculate on-chip inductance. This is particularly important in the extraction screening process to identify inductively critical nets for further detailed analysis.

In this paper, we present a fast and accurate 3D geometry modeling tool based on Arcadia [3] data base. Fasthenry [4] is used as field solver to extract on-chip inductance. Analytical formulae are derived for self and mutual inductance estimation. Accurate self inductances of wires are also calculated based on the self inductances and their mutual inductances of the cascaded segments. Very good agreement of the calculation results from formulae with field solver simulation has been achieved. Circuit simulations of global wires with inductance extraction demonstrate inductive ringing effects and power/ground inductive noise.

II. 3D GEOMETRY MODELING AND INDUCTANCE EXTRACTION USING FIELD SOLVER

3D geometry modeling and inductance extraction have been developed based on layout design and process information. Fig. 1 shows the program flow chart. Layout design and technology file are used to generate Arcadia data base which essentially represents the layout with trapezoids. In addition to the geometry setting which is needed for capacitance extraction, inductance extraction requires user to select ports for each net in field solvers. The user will first choose the net for inductance extraction and identify the ports. Combined with process technology information, such as layer thickness and layer separation from to the substrate, 3D geometries of these nets which are suitable for inductance field solver, e.g. Fasthenry, are constructed from the Arcadia data base.

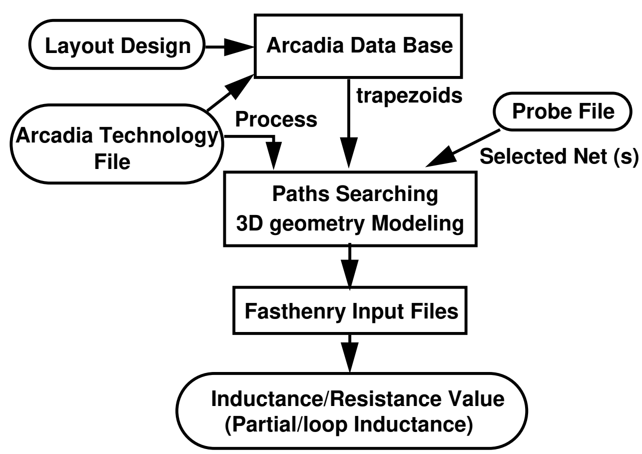

Fig. 1 Program Flow Chart

A. Path Searching in 3D Geometry Modeling

Geometry data consist of numerous trapezoids for each selected net. Electrical connection information, i.e., vias/contacts and equipotential edges, is also stored in the data. Automatic path searching is required to construct 3D geometries of the selected nets since each net usually includes many branches. The data structure is designed to facilitate the searching process which is a depth-first searching. Fig. 2 shows a search process to find a net which has ports of segment 1 and segment 10. Algorithm identifies the trapezoids where they are located. Then it starts with segment 1, and does depth-first search and constructs a tree as shown in Fig. 2. If the segment is the destination port of the net, the program stops; otherwise, it continues searching on another branch. This process continues until the second port is found. To build the whole path, algorithm traces back (dashed arrows) to complete the path construction.

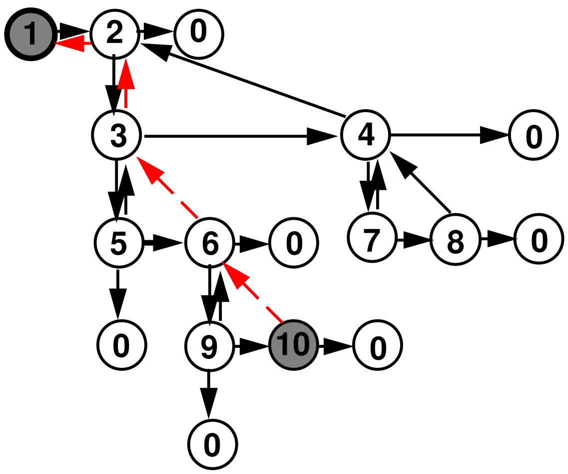

Fig. 2 Path searching in 3D geometry modeling.

Multi-nets/ports can be processed together in order to find the mutual inductances of different nets.

B. Inductance Extraction

The program generates input files for field solvers such as Fasthenry for inductance extraction. Because of proximity effects in high frequencies, a window enclosing the extracted nets can be defined which is bounded by nearest power/ground lines. Current returns of the nets are assumed to be through these power/ground lines. Therefore, loop inductance as well as partial inductance can be extracted. For example, a wire of length of about 2.82 mm and width of 1.2 µm in a commercial chip has partial inductance 4.67 nH and loop inductance 5.7 nH (ground line width of 8 µm). The mutual inductance (loop) with one of its neighbor line is 2.26 nH.

III. ANALYTICAL FORMULAE FOR INDUCTANCE ESTIMATION

Field solver extraction of inductance has high accuracy but it is time and memory expensive. It might not be practical for a whole chip inductance extraction. However, the extracted inductance value can be used as golden data for quick inductance estimation. To quickly calculate on-chip inductance for design guidance as well as for screening inductive important nets in the whole chip, analytical formulae are desired. In this section, self inductance as well as mutual inductance formulae are investigated and derived. Simulation results and analytical formulae estimations are in very good agreement.

A. Self Inductance Formula and Mutual Inductance Formula for Two Parallel Wire with Equal Length

Self inductance of a wire with rectangular cross section can be derived using electromagnetic field theory and geometry mean distance (G.M.D.)[5]. Equation (1) is for the self inductance when $l \gg (w+t)$ where l is the length of the wires. w and t are the width and thickness of the rectangular cross section, respectively. Equation (2) is for the mutual inductance of two parallel wires of distance d and equal length l when $l > d$,

$$L_{self} = \frac{\mu_0}{2\pi}\left[l \ln\left(\frac{2l}{w+t}\right) + \frac{l}{2} + 0.2235(w+t)\right] \quad (1)$$

$$M = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{d}\right) - 1 + \frac{d}{l}\right] \quad (2)$$

The self inductance is a nonlinear function of l which means it is non-scalable with respect to length. It is superlinear when $l > (w+t)$.

To consider skin effect, special frequency dependent term needs to be added. This term can be represented by Bessel function [5] which is curve fitted as shown in Fig. 3 where δ is the skin depth at a particular frequency. Fig. 4 plots the comparison between the simulation and formulae with and without skin effect. The revised formula accurately captures the skin effect though the frequency dependency is not large.

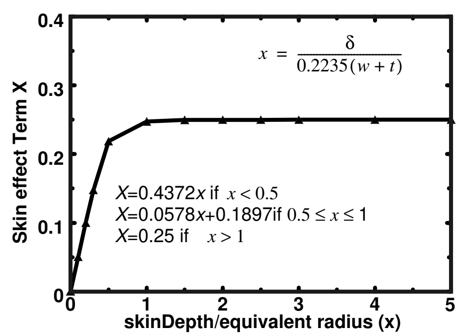

Fig. 3 Skin effect term. δ is the skin depth.

$$L_{self} = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{0.2235(w+t)}{l} - \mu_r(0.25 - X)\right]$$

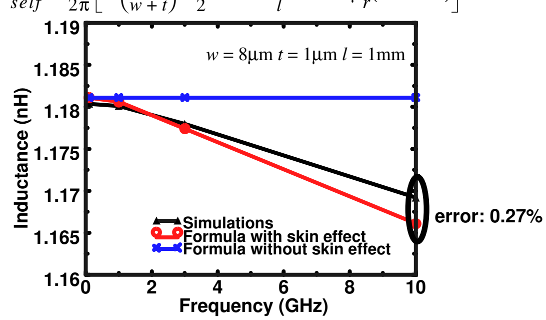

Fig. 4 Revised formula with the skin effect term.

B. Mutual Inductance of Two Parallel Wires with Unequal Length.

To calculate wire inductance in a complex wire environment or self inductance consisting of several cascaded segments in sequence, mutual inductance formulae of two parallel wires with unequal length are derived. There are six different positions of two parallel wires which result in six mutual inductance formulae. Fig. 5 illustrates the six different cases. *l, m, p, q* and *s* represent the wire lengths and some wire overlap lengths. *d* is the wires distance.

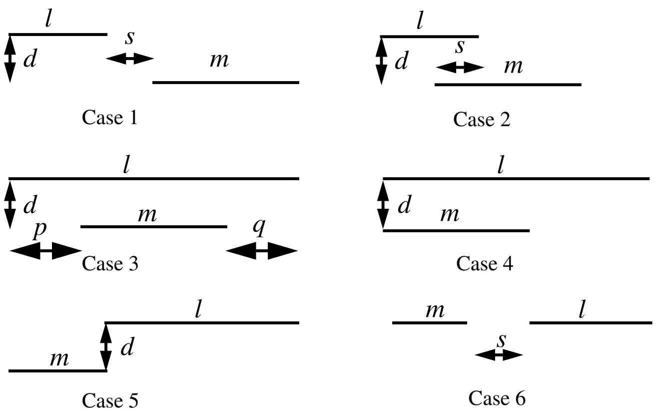

Fig. 5 Six relative positions for mutual inductance.

If the wave length of the signal at frequencies of interest is much larger than the dimension of the wire, the magnetic induction at every point of the field is in phase with the current. The induced electromotive forces are at all points in phase. The magnetic flux linked with a wire may be considered as the resultant of the fluxes (which is in phase under quasi-stationary condition) contributed by the separate elements of the inducing circuit. That is, the mutual inductance of a wire with the inducing wires is the algebraic sum of the mutual inductances of the separate elements of the inducing wires. For example, the mutual inductance of the two wires in the case 3 can be calculated as,

$$M = \frac{1}{2}[(M_{m+p} + M_{m+q}) - (M_p + M_q)] \quad (3)$$

where M_{m+p} represents the mutual inductance of the two parallel wires with $m+p$ equal length and separation of d. So are the other mutual terms.

Six formulae like (3) can be obtained and six formulae can be derived based on (2). For example, for Case 4, it can be shown as,

$$M = \frac{1}{2}\frac{\mu_0}{2\pi}\left[l\ln\left(\frac{l}{l-m}\right) + m\ln\left(\frac{4m(l-m)}{d^2}\right) - 2m + d\right] \quad (4)$$

where l, m and d are as indicated in Fig. 5.

Fig. 6 shows the comparison of the model based on (4) with the field solver simulations. As seen, the formula gives accurate estimations for reasonable distance. When distance become comparable to wire length, analytical formulae will underestimate the mutual inductance. For on-chip interconnects, wires usually are thin and long compared to their separation in the simulation window. Therefore, it does not result in appreciable errors. Case 1 and Case 6 share same formula and their mutual inductances usually are negligible because the magnetic flux linked each other in each case is very small.

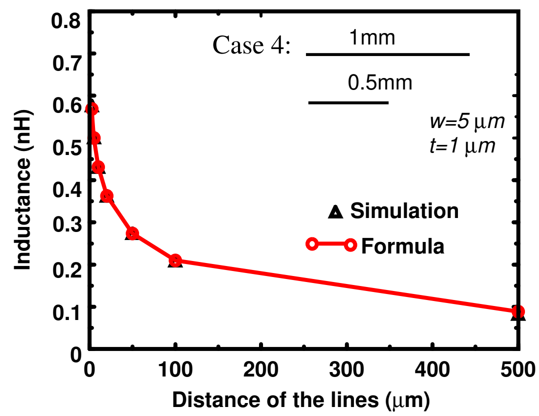

Fig. 6 Formula and simulation comparison.

Case 2:

$$M = \frac{u_0}{4\pi}\left[(l-s)\ln\left(\frac{l+m-s}{l-s}\right) + m\ln\frac{(l+m-s)}{m-s} + s\ln\left(\frac{4s(m-s)}{d^2}\right) - 2s\right]$$

Case 3:

$$M = \frac{u_0}{4\pi}\left[m\ln\frac{4(m+p)(m+q)}{d^2} + p\ln\frac{(m+p)}{p} + q\ln\frac{(m+q)}{q} - 2m\right]$$

Case 5:

$$M = \frac{u_0}{4\pi}\left[l\ln\left(\frac{l+m}{l}\right) + m\ln\frac{(l+m)}{m} - d\right]$$

Case 1 & 6:

$$M = \frac{u_0}{4\pi}\left[(l+s)\ln\left(\frac{l+m+s}{l+s}\right) + m\ln\frac{(l+m+s)}{m+s} + s\ln\left(\frac{s}{m+s}\right)\right]$$

Fig. 7 Other mutual inductance formulae.

C. Calculation of self Inductance of a Whole Wire

As indicated in section *A*, if a wire consists of several segments of which self inductances are known, the whole wire's self inductance does not equal to the sum of all the self inductances of all the segments because of the existence of mutual inductances. Instead, all segments' self inductances as well as mutual inductances between these segments are required to compute the whole wire's self inductance. It can be shown, using circuit theory, that the self inductance of a whole wire constructed by cascaded segments is as,

$$L_{self} = \sum_{i=1}^{N} l_i + \sum_{i=1}^{N}\sum_{j=i+1}^{N} 2k_{ij}M_{ij} \quad (5)$$

where N is the number of segments. l_i is the self inductance of segment i. $M_{i,j}$ is the mutual inductance between segment i and j of the whole wire. $k_{ij} = 0$ when segment i and j are orthogonal; $k_{ij} = 1$ when i and j have same current direction; $k_{ij} = -1$ when i and j have opposite current direction. Table 1 shows three typical wire structures' inductance calculation and their field solver simulations results.

TABLE I**Simulation and calculation of self inductance.** (nH)

Wire1: 3 segments and 3 turns (1.8 mm)			Wire2: 4 segments and 4 turns (2.1 mm)			Wire3: 5 segments and 5 turns (4mm)		
Sim.	Cal.	Error	Sim.	Cal.	Error	Sim.	Cal.	Error
2.27	2.26	0.4%	2.93	2.86	2.3%	5.35	5.17	3.4%

IV. APPLICATION OF INDUCTANCE CALCULATION IN CIRCUIT SIMULATION

For on-chip long thin wires, self inductance of a wire is solely determined by wire geometry, and mutual inductance of two wires is solely determined by geometries of the two wires and their spacing [6]. Therefore, the formulae developed above can be used to calculate self/mutual inductance for RLC interconnect modeling and circuit simulations to investigate inductive effects as well as power/ground noise. Self inductance of global wires, power line and ground line and mutual inductance between these lines can be calculated using the derived formulae. Capacitance and resistance can also be quickly calculated. Fig.8 shows one global wire (4 mm long and 5 µm wide) and two nearest power/ground lines (10 µm wide) within a selected window. Fig. 9 shows the simulation of the signal at the output of the receiver of the global wire. The overshoots are clearly observed with inductance effect included. Fig.10 shows the power noise and ground bounce when power/ground inductive effects are included in circuit simulation. Measures must be taken to avoid circuit failure, such as moving global wire closer to ground/power lines and using C4 bumps for power/ground lines.

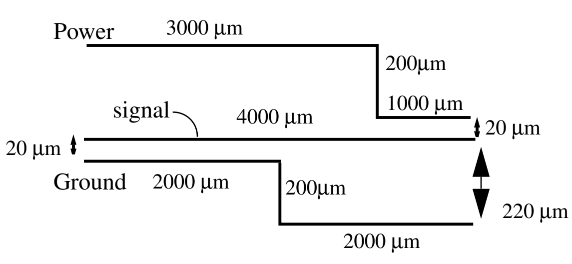

Fig. 8 One global line and two power/ground lines.

V. CONCULSIONS

On-chip inductance modeling of interconnects is presented which is based on accurate automatic 3D geometry generation. Analytical formulae derived for self and mutual inductance estimation are benchmarked with simulations, suitable for quick inductance extraction. Extracted RLC used in circuit simulation shows impact of on-chip inductance on signal integrity and power/ground noise.

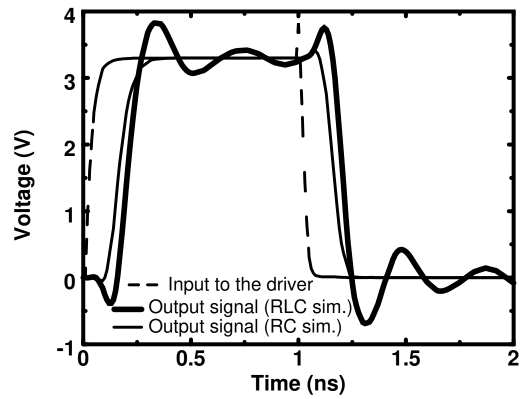

Fig. 9 Signal wave forms at the output of receiver: ringing effects with RLC simulation.

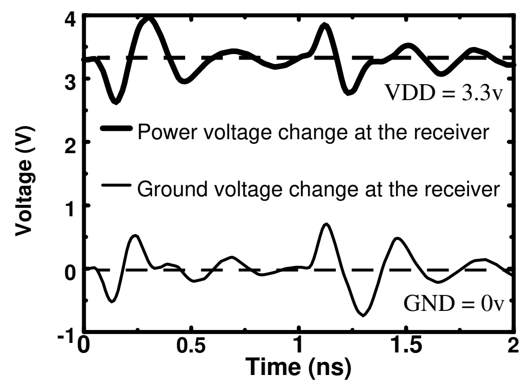

Fig. 10 Power and ground noise observed with RLC simulation.

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