A Fast Analytical Technique for Estimating the Bounds of On-Chip Clock Wire Inductance

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Abstract - Accurate integrity assessment of on-chip clock lines is difficult without any *a priori* knowledge about their inductance at an early stage in the clock design process. This paper introduces an efficient approach to estimate the bounds of on-chip clock wire inductance at the very beginning of the design stages. With this information, more accurate waveforms along the clock distribution networks can be obtained thus greatly reducing the overall length of design cycles.

I. Introduction

As VLSI technology evolves, a significant portion of the delay is caused by global interconnects. With higher clocking rate, increasing interconnect lengths, and decreasing rise times, inductance effects are more evident than ever. This is especially true for the clock distribution networks, where the delay and the slope of clock waveforms are critical to overall system performance. In the past, several different approaches have been proposed to extract the inductance values [1][2]. Though there are many techniques to accelerate the speed of the electromagnetic field solvers, they are still impractical to be included in the early design phase. This is because it is nearly impossible to obtain the exact current return paths at the very beginning of the design cycle, which are layout dependent. Hence, precise inductance values cannot be calculated without the details of physical information, such as locations of the clock lines and neighboring wires. To address this problem, a geometry-independent model has been developed, in the first part of the paper, which can estimate the bounds of possible on-chip clock wire inductance values at early design stages. The inductance information computed by the model can be incorporated into the delay/slope calculations to reduce several iterations between physical design (layout) and logic synthesis, thus shortening the design cycles. In the second half of the paper, the inductance values extracted by the proposed method have been used to quantify their impacts on various design metrics.

II. Background and Theory

Let us denote a routing plane, S, and points of clock source, C_s, and sinks, $P=\{P_1,P_2,.....P_n\}$. Let t(x,y) denote the delay between any point x and y. The clock routing problem is to minimize the delay(D) and skew(S). Where

$D = \max t(C_s, P_i)$ and

$S = \max | t(C_s, P_i)-t(C_s, P_j)|$.

In the past decade, the overall delay was modeled as Elmore delay [3], which accounted for the delay caused by the RC elements only and provided good estimation. The buffer insertion and wire sizing issues were also based on this Elmore delay model. However, for Deep Submicron (DSM) techniques, inductance effects are significant. Hence in order to accurately assess the integrity of clock wires, inductance must be considered.

For the analysis presented in this paper, it is instructive to note that: 1) Clock distribution networks are usually designed in a three-wire (ground-clock-ground) system. The ground wires aside the clock wire function as shieldings, as shown in Fig. 1(a). 2) The metal wires in the adjacent metal layers, which are orthogonal, have no significant impact on the inductance, since the magnetic flux linkages are small because of the direction of the current flow in those wires, as illustrated in Fig. 1(b). 3) The clock wires lying parallel on the same metal level are less likely to serve as return paths due to large separation. From [4], there are 580 clock sinks on a 17*17 mm^2 die. Assuming that the pins are uniformly distributed, the nearest distance between each pins would be around 700 microns. Thus it is justified to assume that they are not efficient return paths, as illustrated in Fig. 1(c). 4) The total clock wire inductance can be obtained by the cascade method [5], as shown in Fig. 1(d). 5) No skin depth effects are considered, because the heights of the global clock wires (as per [6]) are smaller than the skin depth even at several GHz, as shown in Table 1.

TABLE I

Frequency	0.5GHz	1.0GHz	2.0GHz	5.0GHz
Skin Depth (Cu metal)	2.96um	2.09um	1.48um	0.93um

From [7], the partial self inductance (L) of a on-chip clock wire segment is given by,

$$L = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{w+t}\right)+\frac{0.2235(w+t)}{l}+\frac{1}{2}\right] \quad (1)$$

where w, t, and l are the width, thickness, and length of the clock segment respectively. μ_o is the permeability. And, similarly, the mutual inductance (M) between two equal length (l) wires is given by,

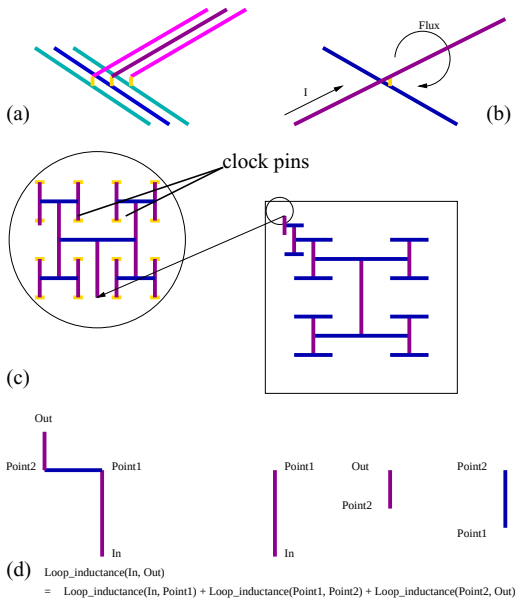

Fig. 1. (a) Three-wire (sandwich styled) clock system. (b) Adjacent layers have small magnetic flux linkages because of the direction of the current. (c) The clock sinks are at least several hundred microns away from each other. (Ground shieldings are not shown in the figure) (d) Cascade method can be used to estimate the loop inductance value.

$$M = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{s}\right) - 1 + \frac{s}{l}\right] \tag{2}$$

where s is the distance between the two metal wires.

Using (1) and (2), we can calculate the self and mutual inductance values, which can be used to construct an equivalent RLC circuit model of the sandwich style clock distribution system, as shown in Fig 2(a). However, the setup is too complicated for the estimation of the bounds. Thus the loop inductance method has been applied. In the loop inductance model, the impedance associated with the two neighboring ground wires are combined into an effective value, and the equivalent circuit is further simplified from Figure 2(a) to Figure 2(b) without losing informations on the clock net. The loop inductance (L_{loop}) can be described as,

$$L_{loop} = L_{ss} + 2\alpha_l M_{sl} + 2\alpha_r M_{sr} + 2\alpha_l\alpha_r M_{rl} + \alpha_l^2 L_{ll} + \alpha_r^2 L_{rr} \tag{3}$$

$$\alpha_i = \frac{-Z_{gnd}}{Z_i} \tag{4}$$

$$Z_{gnd}^{-1} = \left(\sum_{i=1}^{n} Z_i^{-1}\right) \tag{5}$$

In (3),(4), and (5) listed above, L_{ss}, L_{ll}, and L_{rr} are the self partial inductances of the clock and two ground wires, respectively. M_{sl}, M_{sr}, and M_{rl} are the mutual inductances between clock-ground1, clock-ground2, and ground1-ground2, respectively. α_r and α_l are the percentage coefficients of the returning currents. Z_i is the impedance of the return path i. Z_{gnd} is the total impedance of all the parallel return paths.

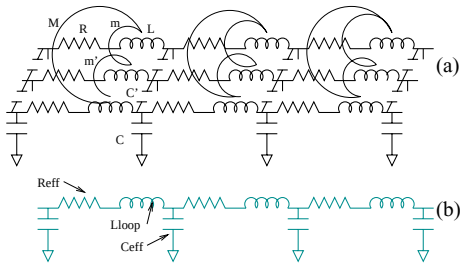

Fig. 2. (a) Distributed RLC model of a ground-clock-ground wire configuration. (b) Loop inductance model is used to simplify the circuit in (a).

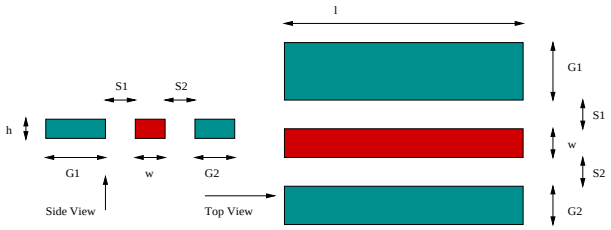

Fig. 3. Top view and side view of a three-wire system shown in Fig. 2 (a)

III. BOUND ESTIMATION METHODOLOGY

In Fig. 3, the cross sections and dimensions of a three-wire system are shown. From (1), (2), and (3), the loop inductance (L_{loop}) for a clock wire with given width and length, is a multi-variable function which can be expressed as $L_{loop}(G_1, G_2, S_1, S_2)$. Note that since the height h is fixed for a given technology, it is not included in the optimization process.

A. Lower Bound of the On-Chip Clock Wire Inductance

To calculate the lower bound of the on-chip clock wire inductance, the problem can be written as

min $\{L_{loop}\}$

subject to $S_1 \geq s_{min}$, $S_2 \geq s_{min}$, $G_1 \geq W_{min}$, $G_2 \geq W_{min}$ where s_{min} and W_{min} are the minimum spacing and wire width for a certain technology. Since the objective function is multi-variable, it can be solved by the Lagrange Method [8].

The Lagrangian function is,

$$\Lambda(S_1, S_2, G_1, G_2) = L_{loop} - \lambda_1(S_1 - s_{min}) - \lambda_2(S_2 - s_{min}) - \lambda_3(G_1 - W_{min}) - \lambda_4(G_2 - W_{min}) \tag{6}$$

If we assume that the ground wires are symmetric (S_1=S_2, G_1=G_2), the function can be further simplified as

$$\Lambda(S, G) = L_{loop} - \lambda_1(S - s_{min}) - \lambda_2(G - W_{min}) \tag{7}$$

The first-order optimality conditions can be stated as,

$$\nabla\Lambda(S, G) = \begin{bmatrix} \frac{\partial L_{loop}}{\partial S} - \lambda_1 \\ \frac{\partial L_{loop}}{\partial G} - \lambda_2 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{8}$$

and $\lambda_1(S\text{-}s_{min})=0$ (9)

$$\lambda_2(G-W_{min})=0 \tag{10}$$

where,

$$\frac{\partial L_{loop}}{\partial S} = \frac{\mu_0}{2\pi}\left[-1+\frac{3l}{G+w+2S}\right] \tag{11}$$

$$\frac{\partial L_{loop}}{\partial G} = \frac{\mu_0}{2\pi}\left[\frac{-l}{2(G+h)}+\frac{1.5l}{G+w+2S}-0.38825\right] \tag{12}$$

Solving (8), (9), (10), (11), (12), the lower bound will occur at:

$$S = s_{min} \tag{13}$$

$$G = \frac{(-a_1)-\sqrt{a_1^2-4a_2}}{2} \tag{14}$$

$$a_1 = h+w+2S-\frac{2l}{0.7765} \tag{15}$$

$$a_2 = h(w+2S)+\frac{l(w+2S-3h)}{0.7765} \tag{16}$$

Note that for situations where more than two ground wires exist, the value of loop inductance will be greater than the lower bound case we calculated. An "equivalent" wire, EW, can always be found to replace the set of several ground wires. The equivalent distance of the EW from the clock line will always be greater than the minimal spacing s_{min} . Hence it will always have a higher loop inductance value. The explanation is similar for the case where the ground paths are in the different metal layers, say two layers away. In that case, the distance is again larger than the s_{min} , and consequently, the lower bound calculated using proposed methodology is valid for both cases.

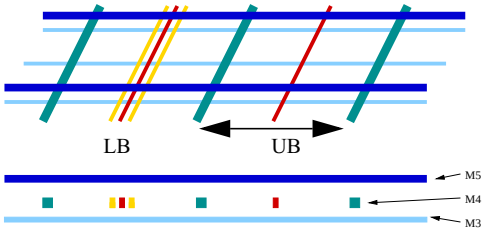

Fig. 4. Lower bound (LB) and upper bound (UB) configurations.

B. Upper Bound of On-Chip Clock Wire Inductance

The absolute upper bound will be $L_{loop}=L_{ss}$, i.e. there are no return paths, all the currents return at infinity. However, in real VLSI design, there are power rails/grids distributed uniformly over the chip, which provide the worst case current return path. If these wires are located at a distance D away from each other, the distance between the clock net and the return paths will be smaller than $D/2$.

Consequently, the upper bound problem can be expressed as

min $\{-L_{loop}\}$

subject to $-0.5 > \alpha_1 > -1$

and $(D-G-w)/2 > d > s_{min}$

Where D is the distance between the power rails, d is the distance between the clock wire and ground rail 1, and α_1 is the current returning coefficient of ground rail 1. In this case $\alpha_1+\alpha_2= -1$.

The Lagrange function can be written as,

$$\Lambda(\alpha_1, d) = -L_{loop}-\lambda_1(\alpha_1+1)-\lambda_2\left((-\alpha_1)-\frac{1}{2}\right) -\lambda_3(-2d+D-G-w)-\lambda_4(d-s_{min}) \tag{17}$$

The first-order optimal conditions should be

$$\nabla\Lambda(\alpha_1, d) = \begin{bmatrix} -\frac{\partial L_{loop}}{\partial \alpha_1}-\lambda_1+\lambda_2 \\ -\frac{\partial L_{loop}}{\partial d}+2\lambda_3-\lambda_4 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{18}$$

and $\lambda_1(\alpha_1+1)=0,$ (19)

$\lambda_2(-\alpha_1-0.5)=0,$ (20)

$\lambda_3(-2d+D-G-w)=0,$ (21)

$\lambda_4(d-s_{min})=0,$ (22)

where,

$$\frac{\partial L_{loop}}{\partial \alpha_1} = [(4\alpha_1+2)L_{11}-(4\alpha_1+2)M_{12}+2M_{1s}-2M_{2s}] \tag{23}$$

$$\frac{\partial L_{loop}}{\partial d} = -\frac{\mu_0 l}{2\pi}\left[\frac{4\alpha_1}{G+W+2d}+\frac{4\alpha_2}{2D-G-w-2d}+\frac{2}{l}\right] \tag{24}$$

Solving (17)-(24) gives the upper bound at:

$$\alpha_1 = -1 \tag{25}$$

$$d = \frac{D-G-w}{2} \tag{26}$$

IV. IMPULSE RESPONSE OF AN RLC CLOCK LINE

The Elmore delay, which is the first moment of the impulse response, is an upper bound for the RC delay [9]. However, as mentioned earlier, it does not include inductance effects. Consequently, the higher order model should be used when routing clock networks. The central moments based on probability theory proposed in [10] can be used as design metrics. The core concepts of central moments are summarized below and the simulation demonstrates the importance of including the inductance values in the delay calculation.

The moment of an impulse response, $h(t)$, is defined as,

$$m_i = \frac{(-1)^i}{i!}\int_0^\infty t^i h(t)dt \tag{27}$$

The Laplace Transform of $h(t)$, $H(s)$, can be expressed as,

$$H(s) = mo+m_1 s+m_2 s^2+m_3 s^3+HigherOrderTerm \tag{28}$$

And the second and third central moments used in the delay calculation are,

$$\mu_2 = 2m_2 - m_1^2 \quad (29)$$

$$\mu_3 = -6m_3 + 6m_1m_2 - 2m_1^3 \quad (30)$$

Where μ_2, and μ_3 are the variance, and measure of skewness of the impulse response function, *h(t)*. For an RC tree, these central moments are always positive. For the case of RLC trees, μ_2 and μ_3 will provide useful information about overshooting. They will decrease monotonically as inductance increases. When μ_2 and μ_3 become negative, a severe inductance effect will be observed.

V. RESULTS

Table II lists a comparison between the results obtained using the analytical method and FASTHENRY[2]. The minimum dimensions assigned in Table II are based on the UMC 0.18 µm technology. The first and the fourth columns are the lower (LB) and upper (UB) bounds of on-chip clock wire inductances. It can be observed that the LB and the UB inductances obtained using the analytical method are in excellent agreement with those from FASTHENRY simulations.

TABLE II

Wire Config.	(LB) l=1mm h=0.58um w=4um G=1.64um s=0.5um	l=1mm h=0.58um w=4um G=1.64um s=1um	l=1mm h=0.58um w=4um G=4um s=4um	(UB) l=1mm h=0.58um w=4um G=4um s=20um
Analytical Method	0.35nH	0.40nH	0.55nH	1.25nH
FASTHENRY	0.32nH	0.37nH	0.54nH	1.25nH

In order to quantify the impact of inductance on clock signal integrity metrics, the Asymptotic Waveform Evaluation (AWE) [11] technique was employed. The wire resistance and wire capacitance were extracted to be 0.065 ohm per square and 0.24 fF/µm, respectively, for a 0.18 µm technology file. The waveforms simulated (in Fig. 5) using AWE show the effects caused by inductances for the values listed in TABLE II. The figure also shows that the bounds of the inductances provide a good window for both delay and slope calculations.

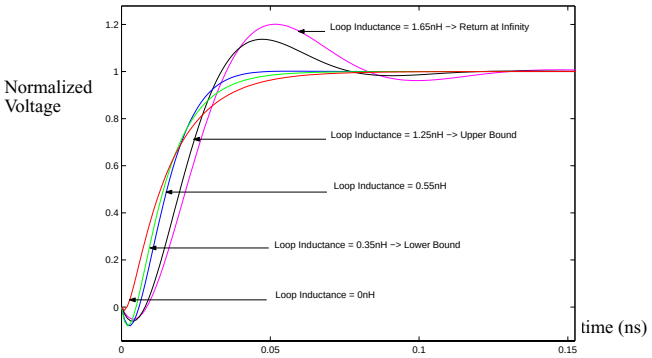

Fig. 5. Output waveform of an RLC interconnect.

Table III shows the delay, the second (μ_2), and the third (μ_3) central moments. It can be observed that different inductance value gives different delay numbers. Furthermore, the negative values of μ_2 and μ_3 imply overshooting. Thus μ_2 and μ_3 can be used as design metrics for clock routing problems.

TABLE III

L_{loop} (nH/mm)	0	(LB) 0.35	0.55	(UB) 1.25	1.61
µ2	2.02e-4	1.09e-4	5.55e-5	-1.31e-4	-2.26e-4
µ3	5.29e-6	4.55e-7	-2.31e-6	-1.20e-5	-1.69e-5
delay (ns)	0.0132	0.0141	0.0152	0.0196	0.0217

VI. CONCLUSION

In this paper, an analytical model using the Lagrange Method for estimating upper and lower bounds of on-chip clock wire loop inductance is demonstrated. Without any details of layout information, the approach efficiently estimates the possible range of the clock wire loop inductance. The ratio between the maximum and minimum possible value is within 4 for a 0.18 µm technology, which indicates that the bounds provide reasonably tight windows. Using these inductance bounds, the second and third central moments can be easily calculated from simulations, which provide an insight into the behavior of the clock output waveforms in time domain. These moments can be used as design metrics to ensure the integrity of the clock signal at an early design phase.

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