Perspectives on Technology and Technology-Driven CAD

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***Abstract*—Computer-aided design (CAD) techniques are absolutely essential to harness the ever-increasing complexity of the microsystem design. Similarly, the technology CAD (TCAD) tools played a key role in the development of new technology generations. Although there is a common belief that the TCAD tools have been trailing the technology development, the situation has been changing very significantly especially over the last decade. For the deep submicrometer (DSM) devices, these tools provide a better insight than any measurement techniques and they have become indispensable in the new device creation. Moreover, these tools after calibration to a relatively small number of experiments, exhibit very impressive predictive power, which is utilized to speed up the technology integration and transfer to volume manufacturing. This results in very manufacturable high-yielding products that can be ramped up much faster than in the past decade, which is absolutely necessary given the huge costs of integrated circuit fabrication lines, short product lifecycles and penalties for being late to the market place. In this paper, we will present our perspective on the semiconductor technology development, and highlight the rapid growth of TCAD and its strategic use in semiconductor industry.**

***Index Terms*—CMOS scaling, Concurrent design, design, design for manufacturing, manufacturing, simulation, TCAD, yield.**

I. INTRODUCTION

THE development of integrated circuit (IC) technology over the past several decades has had a profound impact on society, paving the way to the information revolution that is having a greater impact than its predecessor, the industrial revolution. Once a commodity industry for the larger electronics systems business, the semiconductor business has grown at a faster rate than its parent industry as more of the value of the final system can be attributed to the ICs in the system. The driving forces for the IC revolution and technological innovations are: miniaturization, manufacturing and microsystem architectures. Over the last 30 years, the minimum feature size of the IC device has scaled down by fortyfold and the functional density of chips has increased from dozens of devices to the Gigabit DRAM.

The challenges and rewards of designing and manufacturing leading edge integrated circuits have scaled as the complexities of the chip functionality increases. Today, the IC business is a \$150 B industry, which supports the \$750 B electronics industry. A question arises now how much longer can Moore's Law be maintained. Although the short range future looks quite optimistic, there are several key challenges that must be met, ranging from the new materials and innovative manufacturing processes to the new approaches to microsystem design and verification that would result in manufacturable and profitable products.

Computer-aided design (CAD) techniques are absolutely essential to harness the ever-increasing complexity of the microsystem design. The CAD tools developed over the last decades enabled the creation of highly complex systems. Similarly, the technology CAD (TCAD) tools played a key role in the development of new technology generations. Although there is a common belief that the TCAD tools have been trailing the technology development, the situation has been changing very significantly especially over the last decade. For the deep submicrometer (DSM) devices, these tools provide a better insight than any measurement techniques and they have become indispensable in the new device creation. Moreover, these tools after calibration to a relatively small number of experiments, exhibit very impressive predictive power, which is utilized to speed up the technology integration and transfer to volume manufacturing. This results in very manufacturable high-yielding products that can be ramped up much faster than in the past decade, which is absolutely necessary given the huge costs of IC fabrication lines, short product lifecycles and penalties for being late to the market place.

In this paper we present our perspective on the semiconductor technology development, and highlight the rapid growth of TCAD and its strategic use in industry. We will start by demonstrating, in Section II, TCAD applications to the technology scaling from the early 1970s until late 1990s. Then we will present a hierarchy of TCAD simulation tools ranging from the atomistic level to the equipment and manufacturing simulation levels. In Section IV, we then describe the role of TCAD in the overall IC design flow, focusing on the design-manufacturing interface. The yield modeling and improvement strategies utilizing TCAD will be presented in Section V. Next, we will present challenges in future transistor design and manufacturing. We will conclude with the modeling strategies needed to meet these challenges.

II. TECHNOLOGY SCALING AND EVOLUTION OF TCAD

TCAD modeling is the art of abstracting IC electrical behavior, supported by critical analysis and detailed understanding based on computer simulations, spanning the disciplines of: circuit design, device engineering, process development and integration into manufacturing. Computer simulations help in quantifying the details of behavioral models for ICs at the

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transistor and circuit levels and show the physical limitations at the process and manufacturing levels.

This section traces the evolution of IC processing and the TCAD modeling used in support of process design and manufacturing. Generations of MOS technology scaling have systematically: 1) leveraged existing TCAD tools, 2) challenged their capabilities at the next higher levels and 3) motivated research (and development) that continues to push the frontiers in support of IC applications. This section highlights several generations of technology scaling based on the use of TCAD, emphasizing the coupled roles of process and device simulation. The most recent generations of technology (and TCAD) clearly show transitions toward:

1) heterogeneous device requirements that complement the core digital technology base,
2) atomic-scale limits both in the devices and processing that shift the emphasis to consideration of the complete manufacturing process.

One-dimensional (1-D) simulations of IC processes and devices were dominant and generally sufficient for technologies of the mid-1970s with junction depths in the range of fractions of micrometers and channel lengths of several micrometers. It was possible to extrapolate from sets of 1-D profiles in creating the quasi-two-dimensional (2-D) technology files. For example, channel and field threshold adjustments involving ion implantation, diffusion and oxidation supported design optimizations of the then dominant enhancement/depletion (E/D) NMOS technology [1]. While sheet resistances and minority carrier effects could not be predictively evaluated, TCAD still played a highly productive role in the design of bipolar transistors (BJTs) and first-generation laterally doped (LD) MOS, providing means to understand the process trade-offs and parameter interdependencies [2], [3]. The need for calibration of TCAD was quickly realized as essential in augmenting the physically based models. Techniques such as spreading resistance probes (SRP), C-V and a variety of on-chip test patterns provided key support [1].

The 1980s witnessed the onset of aggressive MOS scaling and the rise of CMOS as the long-term winning very large scale integration (VLSI) technology choice, especially as power consumption and reduced voltage supply issues became critical. With dimensions moving below the level of 2 μm gate lengths (and commensurate junction and gate oxide scaling) TCAD assumed a critical role in MOS scaling. Two-dimensional modeling of effects such as: local oxide isolation (LOCOS) [4], channel doping threshold effects [5] and numerous substrate parasitics such as latchup [6] all required coordinated process and device modeling. Moreover, the physical effects such as enhanced dopant diffusion, due to point defects generated during oxidation and ion implantation, required new models and extensive characterization.

The challenges of relentless scaling mandated by Moore's Law, pushed lithography (and topography) issues to the forefront of TCAD challenges [7], [8]. The capital equipment budgets for new IC fabrication facilities strongly reflect this trend (now and for the indefinite future) and technologists struggle to realize tools and means to control processes for printing device features. The Mega-scale of integration was reached in the 1980s. Out of these processing issues, coupled with the growing complexity of the "ever shrinking transistor," the specialization and application of TCAD in manufacturing became essential. The complexity of process variables, especially in coupled fabrication steps and for complex processes such as plasma etching, quickly outran exhaustive experimentation; design of experiments (DOE) became a critical complement to the in-depth process/device simulation [9].

The late 1980s and continuing into the 1990s witnessed several transitions for both MOS scaling and the role of TCAD. The scaling of junctions and isolation both reached inflection points:

1) isolation moved from LOCOS to shallow trench isolation (STI);
2) increasingly complex "drain engineering" became necessary.

The physical models and growing dependence on multilayer etching and deposition steps shifted the modeling away from thick- to thin-film kinetics with requirements for additional (new) parameters to model multilayer stress and surface reaction kinetics. In general, this period marked the entry of atomic-scale physics into the practical challenges of the ongoing scaling. Shallow junction scaling and modeling also continued to become more complex. Details of physical models for implantation and point-defect assisted diffusion continue to be pushed to their limits for each technology generation-not unlike the challenges of optical lithography for patterning. Moreover, metrology for 2-D profile characterization is an open issue with no definitive solution. Progress in both the modeling and measurements of shallow junctions, while encouraging [10]–[12], is still far from routine or sufficient to fully support the ongoing experimental challenges of scaling.

During the late 1990s, the importance of electrical effects other than those of the intrinsic devices and gate delays, especially the role of interconnect and substrate parasitics, became a major concern. Earlier generation reliability issues for CMOS have shifted to the role of electro-static discharge (ESD) and its interrelationship with I/O circuit scaling [13]. These parasitic effects require characterization of both electrical and thermal behavior. Moreover, passive elements now pose major challenges to circuit and system designers. Materials and processing issues are critical; the modeling is also intertwined with systems issues such as chip-scale layout. Just as there was a transition from the gate-dominated delays toward [resistance-capacitance (*RC*)] interconnect-dominated delay limitations, now the importance of on-chip inductance brings still greater complexity to modeling and verification [14]–[16].

Substrate noise is another parasitic effect that couples both capacitively and resistively through the bulk regions and is of grave concern to analog designers, especially when both analog and digital blocks are included on the same chip [17], [18]. While many of the technology implications of substrate noise and modeling issues are now understood, the circuit layout and extraction problems are difficult—the phenomena are inherently three-dimensional (3-D) and distributed. The problem of cross talk in interconnects is another major challenge and, much like substrate noise, its distributed nature over extended regions make extraction and simulation difficult. Simplified extraction tools and methodology are essential from a verification point of

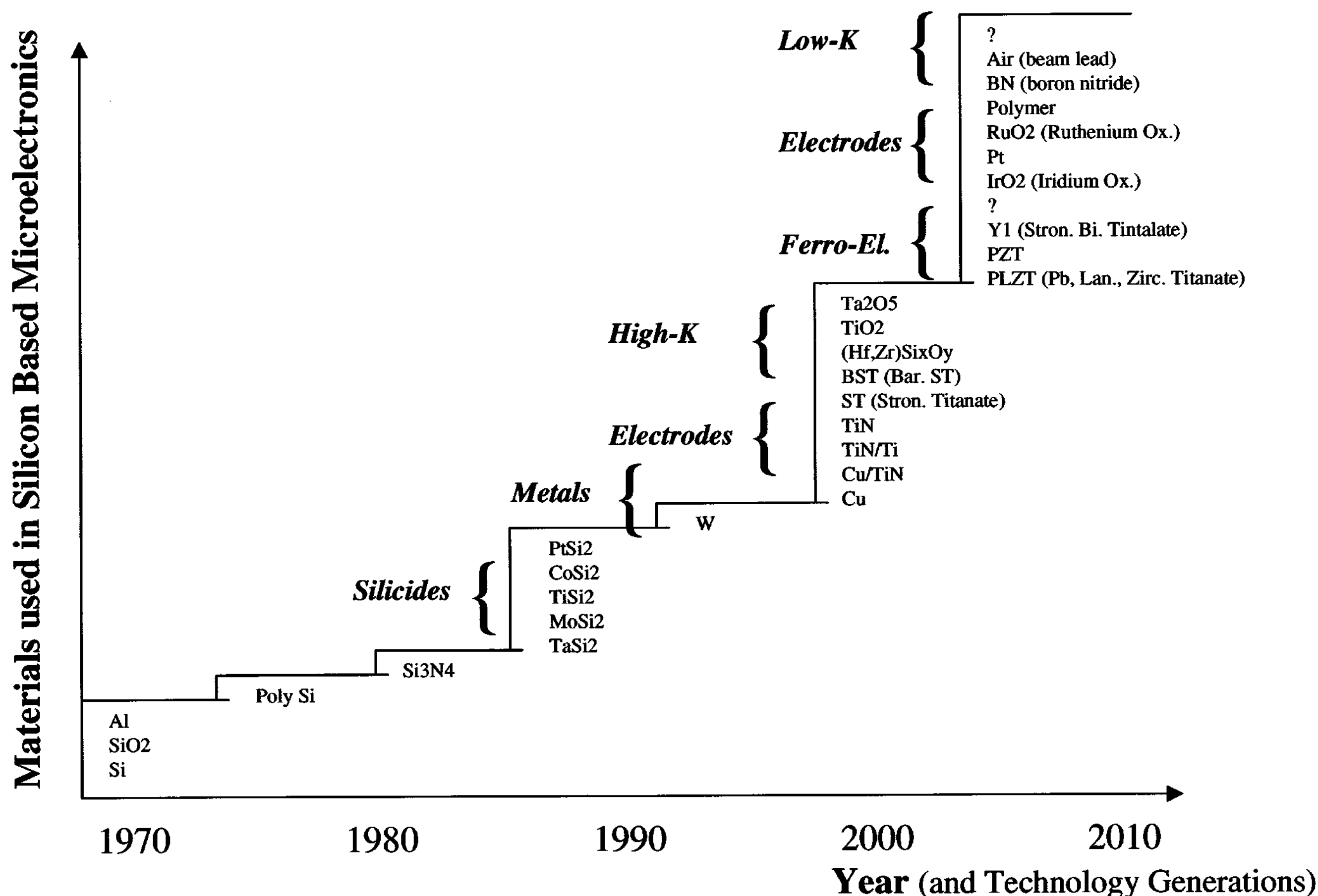


Fig. 1. Quantum leaps in new materials.

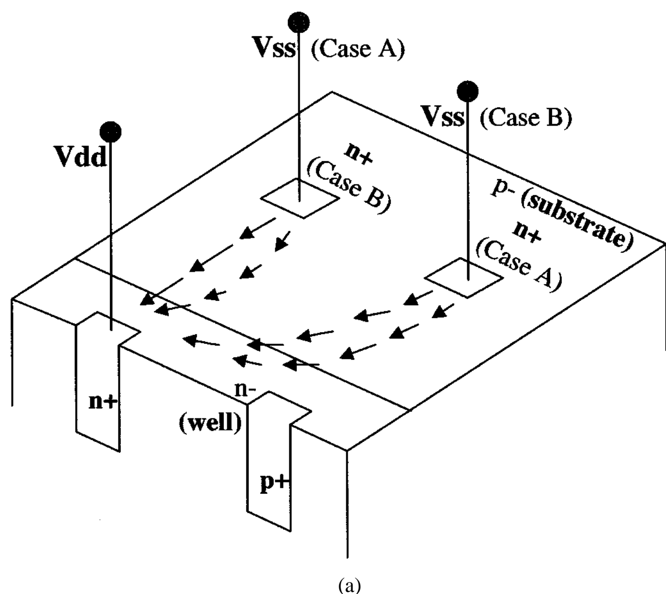
view [19]; scaling challenges of feature printability, including use of optical proximity correction (OPC) [20], require detailed modeling as discussed in the next section.

The TCAD analysis of multilayer interconnects is still in early stages of development. Fig. 1 illustrates a major physical challenge for both modeling and manufacturing, driven largely by performance constraints of both the intrinsic device and interconnect layers of ICs. This figure shows both the history and prospects of candidate materials that may be used in future advanced IC processes. Clearly, the projections push faster and into more new areas than have been explored (or well characterized) to date. Turning to high-level extraction and performance verification tools, modeling to date based on lumped elements or distributed delays lines, has become burdensome due to the inadequacy of both extraction methodology and analysis tools themselves. While the electrostatic and even time-dependent analyses using accelerated numerical methods are relatively mature, there are still major challenges to be faced, especially from the technology perspective as illustrated above in Fig. 1. The ever-increasing operating frequencies, combined with multilayered materials used for interconnects, are putting new demands on both technology and modeling.

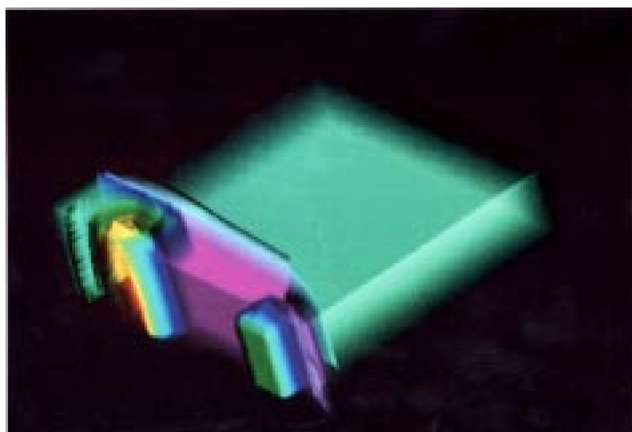
Over and above the 2-D modeling and measurement challenges, the need for 3-D modeling continues to grow, driven to a major degree by parasitic device effects such as ESD, substrate noise and other multidevice interactions (i.e., latchup) as discussed above and most certainly the 3-D interconnect problems. There have been impressive demonstrations of 3-D TCAD use in technology development, dating to the early 1990s [21]. At the same time, it is specifically the complex and distributed nature of structures that requires extensive gridding and more robust numerical analysis techniques in order to handle the computational complexity. Progress in high-performance computation (HPC) has moved from the exotic parallel computers in the early 1990s [22] into a regime where sustainable bandwidth and computational power of clusters of workstations is now outrunning the robustness (and scalability) of the application tools.

Fig. 2 gives a sample problem, solved in the early 1990s using parallel computation [22], for CMOS latchup. Fig. 2(a) shows schematically the test configurations: Case A has the $n+$ injecting node opposite the $p+$ source/drain node; Case B has the $n+$ injecting node directly opposite the $n+$ node (representing the $V_{\rm dd}$ and well contact point). For each case, the $V_{\rm ss}$ node (which is a $p+$ contact to the substrate) is at the opposite location from the $n+$ injector. Fig. 2(b) and (c) shows the electrostatic potential contours around the $n+$ $(V_{\rm dd})$ region under the respective injecting conditions of Case A and Case B. It is clear that Case B has more potential contours and hence is more robust (i.e., has a higher latchup trigger current by nearly twice that for Case A [22].

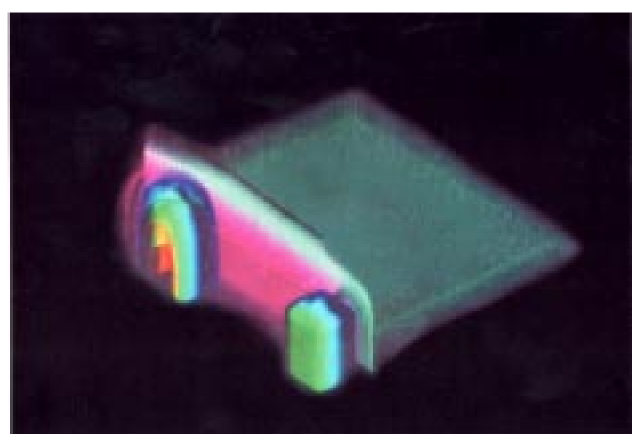
From a future TCAD perspective, these results based on then state-of-the-art parallel computing (i.e., Intel iPSC2) and visual-



(a)



(b)



(c)

Fig. 2. Latchup simulations in 3-D based on parallel computing $[x + 17]$. (a) Terminal test configurations showing $V_{\rm dd}$ (fixed) and two test cases where $V_{\rm ss}$ location is opposite to $n+$ injector. (b) Contour plot of electrostatic potential around $V_{\rm dd}$ $(n+)$ node for Case A. (c) Contour plot of electrostatic potential around $V_{\rm dd}$ $(n+)$ node for Case B.

ization should now (and even more so in the future) be achievable with networked computing. Many of the parasitic effects discussed above [13], [19] involve complex operating regimes with multipath, coupled phenomena. Multidevice computations and immersion-like visualization as depicted in Fig. 2(b) and (c) could be of major benefit in both technology development and generation of better simplified behavioral models.

The introduction to this section suggested two themes to consider in future generations of technology (and TCAD): heterogeneous device requirements and atomic scale limits as they impact considerations in manufacturing. While threads of these themes have appeared above, in looking to the future and in order to more deeply appreciate the issues raised in Sections IV and V, the following discussion gives a more detailed account of key issues.

Core CMOS technology, driven by transistors optimized for digital (CPU, memory and DSP) applications will continue to evolve and it is doubtful that materials other than silicon or devices fundamentally different from FETs will displace it. Quite to the contrary, CMOS continues to challenge higher frequency applications in wireless and exciting integrated, single-chip solutions that include RF functionality are becoming common. While silicon is not suitable for optical (light emitting) devices per se, the rapid progress in MEMS-based optical components that can be realized on silicon substrates now spans applications from displays to optical routers [23]. Even farther afield from electronics as we know it, IC micro-fabrication technology, including use of integrated electronics, is rapidly making progress in the biological sciences, predominantly in the areas of genetic research and drug discovery. These three widely different domains: wireless, optics and bio-tech are illustrative of what can be broadly classified as heterogeneous device (as well as circuit and system) applications that exploit the technology base of ICs.

Given this exceptional promise and leverage, the question them becomes: “what (single-chip) applications will emerge and at what cost in volume production?” The opportunity to integrate single-chip solutions that have: digital CMOS, analog (CMOS or SiGe HBT), RF (including all the passives needed), as well as still more exotic opto- or micro-electro-mechanical options is at present a wild dream (if not a nightmare). Nonetheless, the promise of future CAD systems, including process synthesis discussed in Section IV, is to have quantified and encapsulated (via tools and methodology) the necessary processing and manufacturing information sufficient for future integrated systems designers to make choices and trade-offs across heterogeneous technologies of the future.

III. Simulation Tool Hierarchy

Atomic-scale limits to device design and manufacturing present a key challenge for future technology generations. The above mention of research efforts on future devices (i.e., single electron structures, nanotubes etc.) has hinted both at the atomic-scale effects and the bottom-line challenges that ultimately must be faced if they are to become VLSI-scale contenders. Aside from this broad and uncertain landscape of future devices, there is a very real set of challenges already facing IC scaling at the atomic levels. Fig. 1 has set the stage for considering integration of alternate materials in manufacturing.

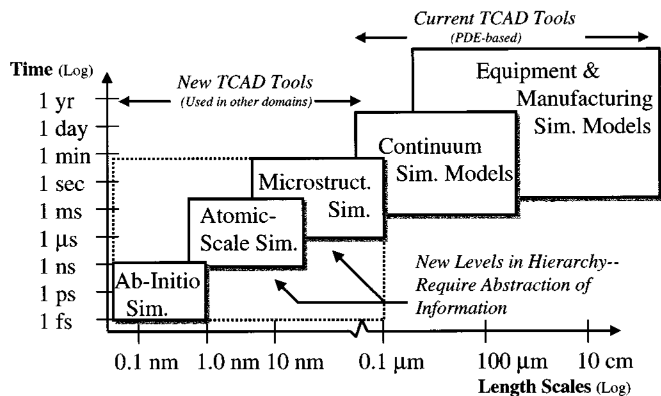


Fig. 3. Simulation tool hierarchy.

Fig. 3 looks broadly at the time and space axes of fabrication processes: at the highest levels are the equipment models (discussed next) and at the lowest levels are ab-initio, quantum modeling. In contrast to the well-known hierarchical chip design process, the crossing of boundaries between the hierarchy shown in Fig. 3 is still very much a research challenge, let alone able to be automated. Considering a rather specific example of plasma processing, the equipment level might involve: bulk plasma simulations, gas flow and thermal modeling, all at the macro-scales (mm, cm and meter scales). At the same time, the wafer, die and structure levels of modeling move progressively in the other direction (down to the nanometer scale) and finally the surface chemistry, for example, inside a trench for DRAM or STI, will deal with atomic-scale surface chemistry. The catch is that the ions on the trench surface are injected across a millimeter-scale plasma sheath but their distributions at the nanometer-scale features of the trench (or other patterned structure) directly affect critical dimensions (CDs) and, hence, performance of the devices.

The above example, while simply representative, illustrates a broad range of multiscale physical effects that are critical to understanding and control of manufacturing at the atomic-scale. TCAD tools at both the equipment and continuum levels are well established and broadly used. The lower-level tools are broadly used in their respective research communities (not necessarily a unified community in itself), but the usability and hierarchical integrability (in the sense that electronic design automation would deal with transistors, gates, etc.) is still an open research challenge. A specific example relates to dielectric constants (either electronic or optical), which are well-known and broadly used by device designers. At the same time, determining how to extract such data directly from quantum mechanical or molecular dynamic materials simulations is by no means straightforward or well understood. Multiscale effects, for example extended defect structures that are important for understanding leakage currents in devices and isolation structures, have even more complexity to them, both because of size and crossing boundaries in the hierarchy.

Equipment and topography modeling and simulation tools have become truly essential to reduce the technology development time and, therefore, cost. There are several unit process areas that have been tackled: chemical mechanical polishing (CMP), chemical vapor deposition (CVD), physical vapor deposition (PVD), and etch and thermal processing including rapid thermal processing (RTP). The sophistication of models used in the equipment simulators vary greatly from the simple experimentally derived response surface models (RSMs) for CMP [24], [25] to the computationally intensive more physically based etching/deposition models, such as in SPEEDIE [26]. The atomistic modeling approaches based on molecular dynamics, Monte Carlo and quantum chemistry have been also pursued quite vigorously in the last decade [27], [28].

In general, although these models are becoming more predictive, validation of simulation results is still an issue. For example, in the plasma enhanced CVD processes there are so many possible chemical reactions, that obtaining the reaction rates for the dominant ones, is an extremely difficult task [29]. These reactor scale equipment simulations must be combined with the feature scale simulations to predict the sensitivity of the film topography and composition to the spatial variations in such parameters as flux or temperature [29], [30].

In order to predict the profile evolution with enough accuracy to represent the very small structures such as trenches, contacts or vias, 3-D approaches to topography modeling have been recently developed [31], [32]. The full spectrum of these topography models covers lithography, etching and deposition modules. In the lithography area, the quantitative resist modeling is still the bottleneck and, therefore, the macroscopic models of Dill [33] and Mack [34] dominate. The modeling of image formation has received a lot of attention mostly because of the Optical Proximity Correction needs. There are numerous software tools for aerial imaging that result in good engineering approximations [20], [35], [36]. However, even these tools are not sufficient to handle the most recent lithography systems with large numerical apertures (NA), off-axis illumination and pupil filtering.

The situation is even more complicated in the prediction of light scattering from wafer topography and in the substrate, where the true 3-D Maxwell-equation based modeling approaches are necessary [37], [38]. These modeling programs must also include the photoresist development and postbaking to properly predict the 3-D profile for the new chemically amplified (CA) photoresist. Figs 4(a) and 3(d) show how these combined 3-D models for aerial imaging, photoresist exposure, development and postbake implemented in METROPOLE-3-D have produced an accurate representation of the photoresist notching in metal lithography. These simulation results have been successfully applied to the optimization of the anti-reflective coating in the commercial manufacturing process [38]. These 3-D lithography models have been also successfully combined with the efficient 3-D surface evolution models based on the level set methods [39]. Especially, the fast marching level set method [40] has been implemented is several topography modeling software tools.

In summary, the above discussion of both heterogeneous technology and atomic-scale issues in manufacturing reflects challenges that will affect, if not reshape, the future developments of integrated systems in the context of IC manufacturing. The next two sections consider in detail the manufacturing issues.

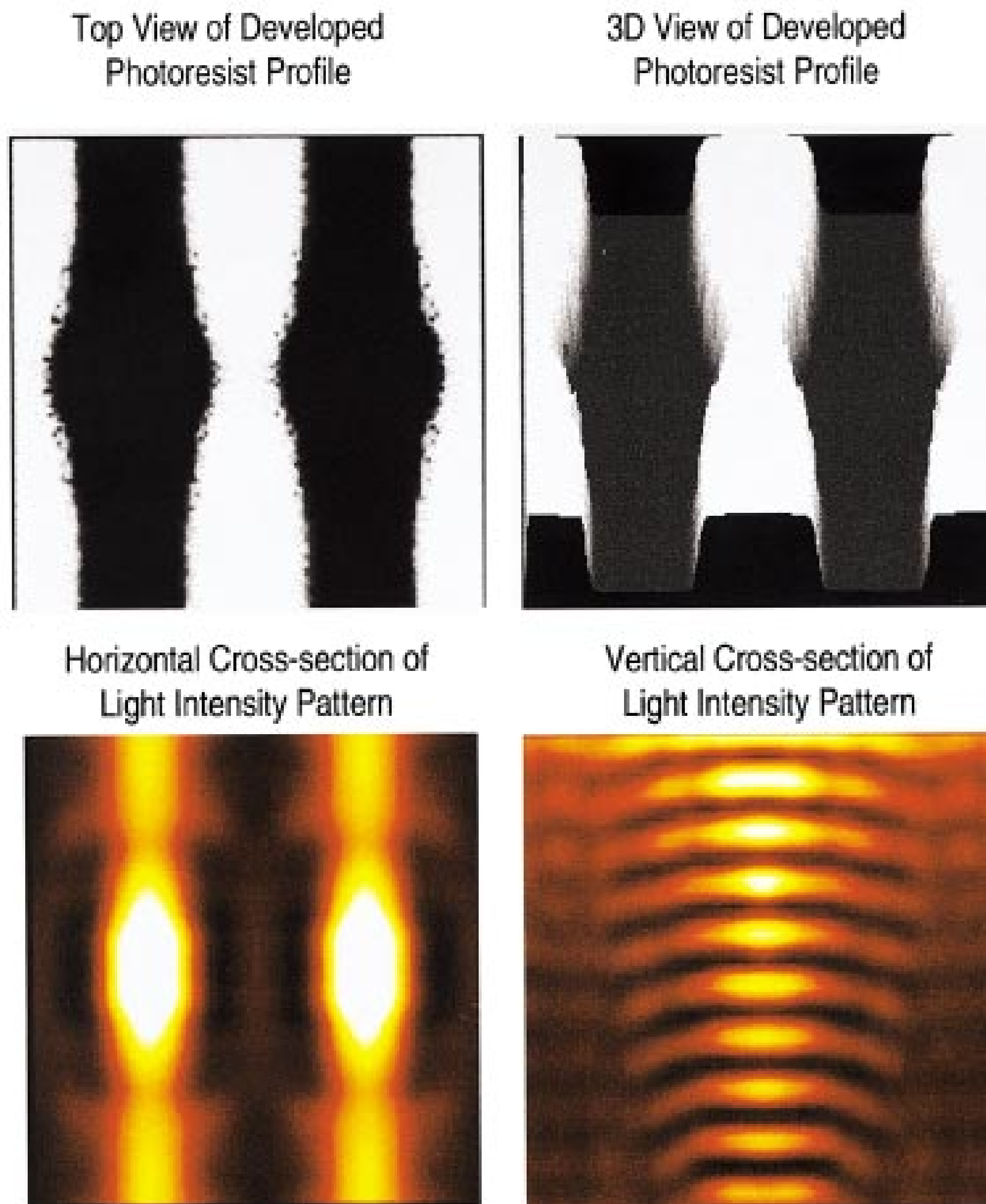


Fig. 4. Simulation results of metal line structure, reflective notching is observed.

IV. TCAD-Based Design-Manufacturing Interface

To develop an IC product, there are number of engineers involved from the unit process development to the system level specification. Typically, the technology development has been split into two basic regimes: product design and fabrication process development. There are three aspects of technology and product development that are relevant.

1) A single process is usually applied to many products.
2) Process and product developments are often undertaken at separate divisions of integrated device manufacturers (IDMs) or, especially in the last decade, different companies (fabless/foundry model).
3) Product performance variability and yield are determined by the sensitivity to the inherent variability in the process.

As a result, while a product functionality is statically defined during the design synthesis, the process will vary during manufacturing. In the early 1980s, the advent of VLSI created the need to formalize the interface between the design and manufacturing. To simplify the boundary between the product and process development regimes, semiconductor companies standardized on a basic interface of SPICE model cards, and LPE/DRC technology files. The layers of IC development in such an interface are shown in Fig. 5 [41]. The advantage of this type of interface is that the product and process design can be decoupled, and even performed concurrently. There are two disadvantages of this type of interface.

1) Unidirectional flow of information from the process developer to the product designer which is assumed to be static, i.e., it is assumed that the choices the designer

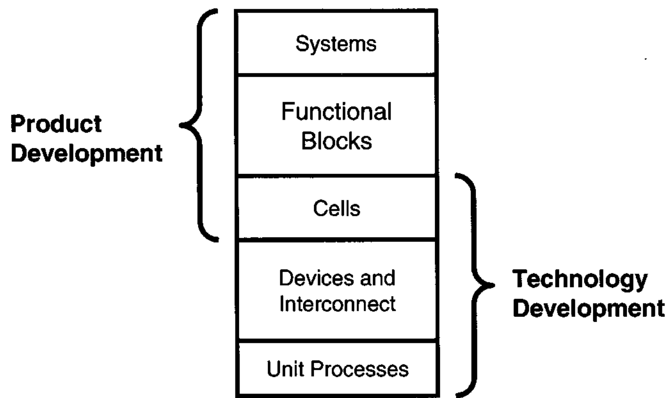


Fig. 5. Layers of IC development.

makes do not affect the electrical performance of the fundamental elements (e.g., transistors and interconnect structures) used in the design.

2) Conservative specifications of the process are provided to the product designers, the so-called worst-case SPICE files. This results in losing much of the value of the new process technology in performance due to gaurdbanding [42].

These two negatives have long been outweighed by the value of disaggregating the technology development from the product development for most product segments. This has begun to change due to the evolution of process technology. The changes are going to require re-defining the interface between the product and process designers. However, it is still crucial to maintain a clean interface, which will allow for the disaggregation of design and production. It will create opportunities in the mixed signal and memory area because it will be possible to obtain more realistic optimal designs, while providing the logic designers with an ability to take a full advantage of the technology capability [43].

The new interface needs to provide the following information to the IC designer.

- The intrinsic electrical variability of the circuit elements such as transistors and interconnect structures due to process variations.
- The sensitivity of the circuit elements electrical characteristics based on choices the designers make (e.g., the impact of layout configuration on electrical performance of interconnect).
- Post design manufacturability assessment and post design printability improvement.

Such an interface is depicted in Fig. 6 [41]. TCAD can play a key role in building the parameterization of the manufacturing capability.

A. Challenges and Solutions for the New Interface

As we pointed out above, there is a need to preserve a clean interface between the designers and the manufacturers while allowing for the parameterization of a new technology. Besides the accuracy of the parameterization of new technologies and designs, there are the following two conditions that must be met.

1) It must be possible to characterize the process early in the lifetime of the new technology.
2) It must be possible to characterize the effects of small perturbations.

To meet these two conditions, TCAD has been recently expanding from the software tools mostly used for technology development to the software that is also used to build a bridge between the designers and manufacturing. This interface includes many technologies where TCAD is of key importance, such as the post layout printing correction and interconnect characterization.

A key component of the design-manufacturing interface is the employment of statistical process/device simulation [3] to predict the distributions of electrical test values and SPICE parameters based on the distributions of equipment controls. The ability to use deterministic algorithms when extracting SPICE parameters is also a key part of the statistical characterization process. It is shown in [44] that it is possible to use the information available from TCAD process simulations (such as actual dopant profiles) to extract the SPICE parameters in ways which cannot be typically accomplished from I-V characterization. Fig. 7 gives a more detailed view of the several pieces of data and simulations required to achieve TCAD-based I-V characterization [45]. The use of process and device simulations, the forte of TCAD, is combined with other key data extraction, either direct metrology or other stand-alone modeling such as needed for C-V, to systematically calibrate and achieve a unified I-V data set. This methodology provides reliable data as well as support for relating physical effects back to controlling parameters that relate directly to either process recipe or even processing equipment dependencies. This approach was initially demonstrated with 0.25-μm technology [45] with excellent agreement, one parameter set fits all, across devices from 20-μm down to 0.25-μm channel lengths. Current trends in terms of SOC requirements for both analog and digital functions in the same process flow make such scalability of even greater importance in future process integration.

The new paradigm will be a parameterization of the interface, which will provide both sides with an understanding of how choices they make affect the overall chip performance, reliability, and yield. For this new vision to materialize, new applications for TCAD will (and are) emerging. This changing interface creates a number of new opportunities, such as:

- parameterization of within chip variations of interconnect variability;
- post layout printability evaluation and correction/enhancement of full chips (OPC and PSM);
- enhancement of design systems to exploit the abstracted view of process capabilities;
- exploitation of circuit/process co-design.

Recently, the process development was modularized and process integration has become a more structured process. Based upon the technology constraints and the target device performance, processes have been developed and the device performance has been abstracted for the product designers (see Fig. 8). Although the full blown product/process co-design has not been accomplished yet, there have been several approaches to synthesize the process to meet the desired device performance

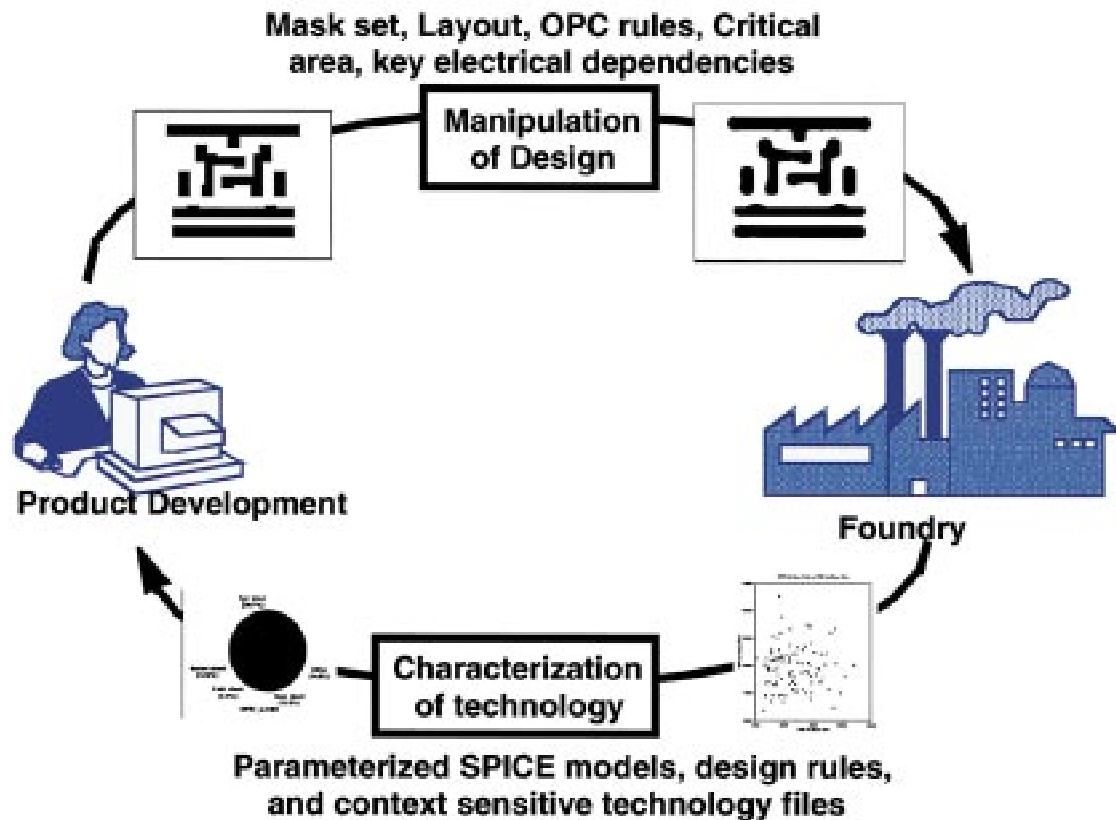


Fig. 6. Design-manufacturing interface.

objectives. An example of such process synthesis is given in [46] and is illustrated in Fig. 9. In this case, the objective function was the maximization of the NMOS transistor drive current (maximizing speed), while the constraints consisted of leakage current, threshold voltage and the peak substrate current (reliability metric). The recipe was optimized for modules source-drain, salicide and channel process modules. The results of first silicon were within 5% of the model predictions. Another approach of concurrent process technology development and circuit design is presented in [47]. In this method, a calibrated BSIM3 model was used to generate optimized device structures that met the target specs in first silicon. The latest example of circuit performance oriented device optimization was presented by Miyama and Kamohara [48]. In this approach, the pre-silicon BSIM3 model parameters are generated by changing process recipe, which results in very significant improvements in both power and speed of a microprocessor.

The ultimate challenge in process technology development is presented by the system-on-a-chip (SOC) in which microprocessor and analog cores must be implemented is a single chip with several types of memory (SRAM, DRAM, or Flash). The modular process development strategy has been proven effective in reducing process development time while satisfying the SOC process specs [49]. Two extremely ambitious approaches to the SOC technology development to satisfy the product requirements have been proposed very recently in the keynote addresses. In a keynote talk at 1999 IEDM by Kohyama [50], calibrated TCAD tools are applied to generate an optimized process recipe. The keynote presentation at ISSCC 2000 by Pinto [51] presents an extremely impressive integration of several technologies in a mix-and-match manner.

V. Yield Modeling and Improvement

In this age of multibillion dollar semiconductor fabrication facilities and increased time-to-market pressures, rapid yield learning is essential to achieve profitable production of integrated circuits. To be competitive, the cost per die must be minimized while quickly ramping the manufacturing yield to an economically acceptable level. Increasing the initial yield and rate of the yield ramp are the biggest drivers of product profitability making final product yield significantly less important than in the past.

Yield loss mechanisms in an IC can be classified into two types: global and local disturbances [52] (see Fig. 10). Global disturbances are those that affect all the devices on a chip or even a wafer at the same time. These variations can occur both within a die and across the wafer resulting in yield loss or a shift away from the nominal performance for each manufactured IC. Global variations usually affect the performance of ICs causing some ICs to miss design specifications. When the fabrication process is newly defined and is being tuned to achieve the necessary process and device parameters, the yield loss is typically due mainly to global disturbances.

In contrast to global disturbances, local disturbances introduce a deformation of a small local area of an IC die. These

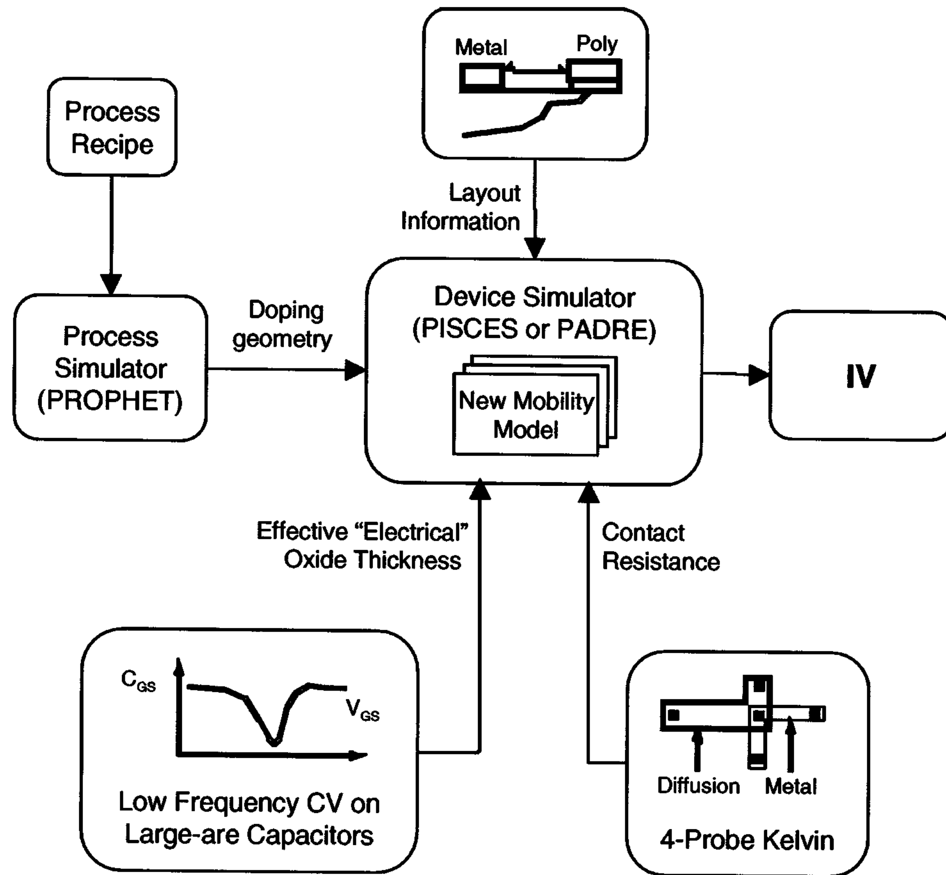


Fig. 7. TCAD-based IV characterization.

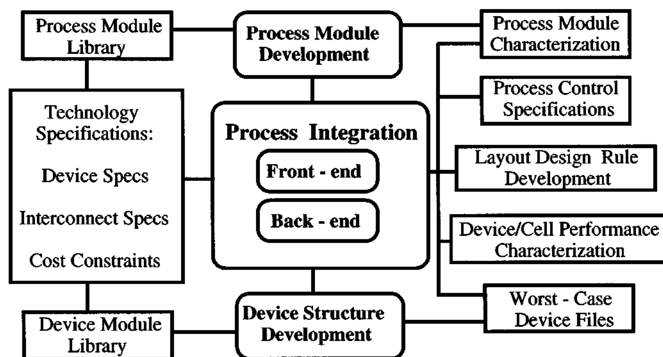


Fig. 8. Process synthesis.

deformations are usually referred to as random defects [53]. Random defects forming at a certain location on IC could cause the topography of the circuit to change. Local disturbances which lead to random defects arise mainly from some contamination affecting the wafer during fabrication process (see Fig. 11). In high-volume production, random defects caused by particulate contamination are typically the dominant reason for yield losses. Contamination defects that result in possible yield loss can be introduced at any one of hundreds of the process steps. The size of these defects that cause yield loss may be smaller than the design rule and the sensitivity limit of metrology equipment. This fact poses a challenge to modern deep submicrometer VLSI manufacturing technologies: how to accurately evaluate the yield impact of these particles. It has been seen that defects may propagate and grow throughout the process flow, and as a result cause faults in the final product. In recent studies, it was found that there are two major defect propagation mechanisms; namely, interlayer and intralayer defect propagation [54].

In addition, yield learning is becoming more difficult due to the increased complexity of the products, the processes, and their often-subtle interactions. Various new emerging process technologies have induced new problems, especially during the yield ramping process. For example, the CD of the active device has been scaled down below the wavelength used in photolithography process. This has introduced printability problems such as Lpoly variation and reflective notching effect. While within chip variation is typically due to effects such as micro-loading in the etch, variations in photo resist thickness, optical proximity effects, and stepper within field aberrations, the reflective notching is caused by the optical interaction between exposing light, resist and substrate structures. Fig. 4 in Section III shows the simulation result of a reflective notching effect caused by the reflective substrate [55].

Another example of intradie variation is the CMP process that is used to planarize the interlayer dielectric. The amount of material removed is highly dependent on the pattern density of the underlying layer [56]. As a result, the dielectric thickness variation within a chip can be thousands of angstroms and can be larger than the within wafer variation. Like the poly CD variation, most of the within chip variation in not purely random but

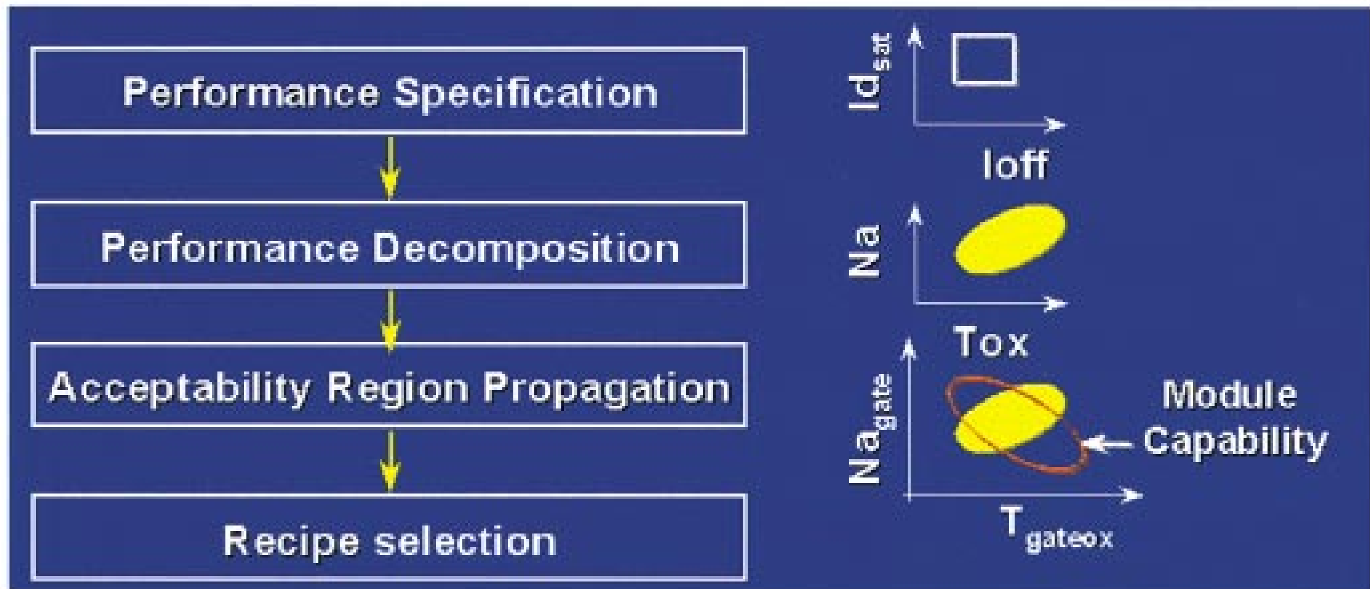


Fig. 9. Process synthesis flow.

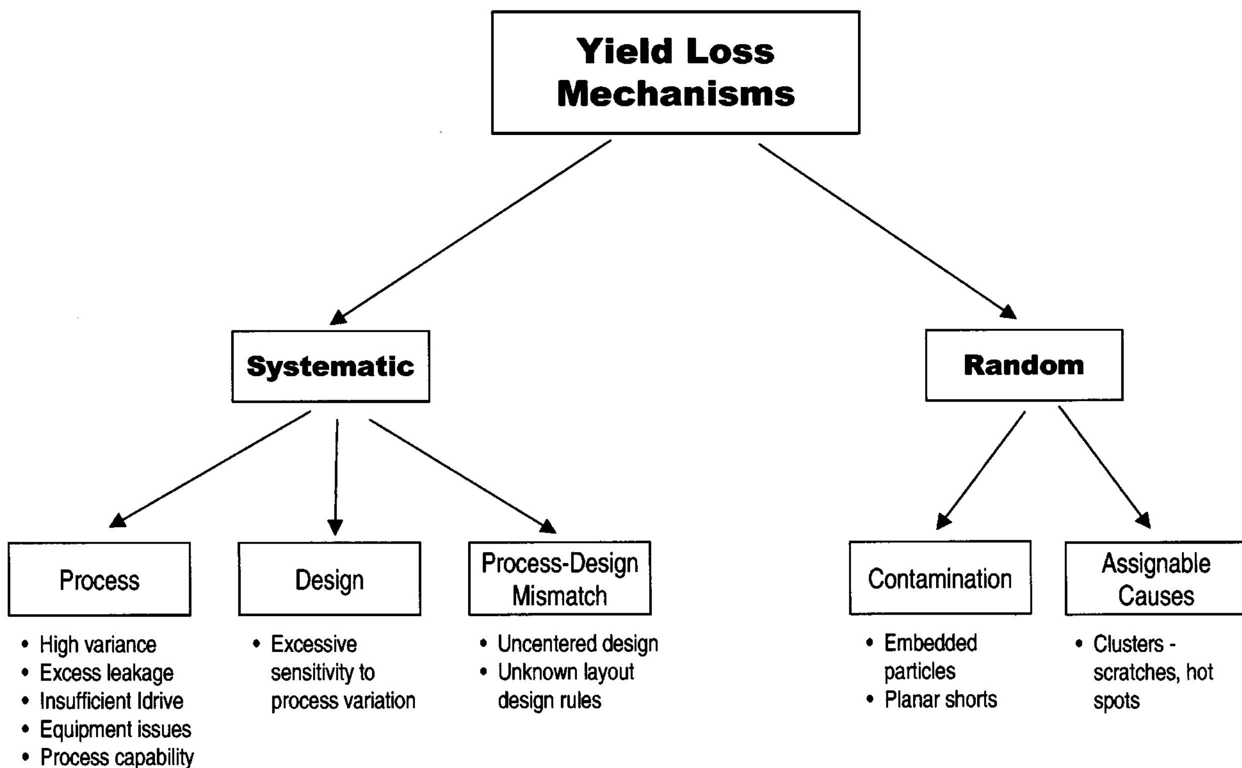


Fig. 10. Yield loss mechanisms.

depends on the layout, CMP pad material, slurry chemistry, rotation rate, and down force applied. Fig. 12 shows an example of intrawafer and intradie ILD thickness variation.

As the device size shrunk below quarter micrometer range, the device characteristics became a more important yield and circuit performance issue. Statistical fluctuations of the dopant concentration have become an increasingly significant source of active device variability. With decreasing device dimensions, the number of dopant atoms in the active volume is dropping into a range where the variability is becoming quite substantial. For example, in a MOSFET with the effective channel length of 0.1 μm, the statistical fluctuations of the threshold voltage and the drain current are almost 5%. This variability is in the range of gate length variability (Poly CD variation), which is typically as large as 10%.

During high-volume production, defect problems are typically addressed by optically inspecting wafer surfaces during production. Making a connection between an observed defect

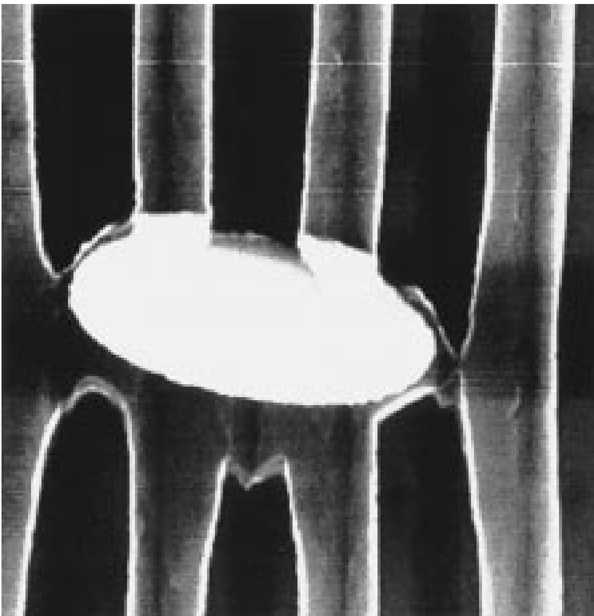


Fig. 11. Example of local defect: pattern deformation.

and an electrical fault is not automated. Early in the production life cycle, design/manufacturing interplay and defect problems are addressed by manipulating design rules, resizing transistors, and using more conservative cells.

Yield improvement in the fab often refers just to the reduction in contamination caused yield loss. However, the most important factor is the final package yield which also includes parametric (e.g., speed loss, high power consumption) and functional yield loss mechanisms. Parametric and functional yield loss mechanisms can both be due to random and systematic causes. Identifying and eliminating systematic yield loss mechanisms is a key to improving the yield ramp rate and increased profitability.

By leveraging simulation and hypothesis-driven statistical analysis, the diagnosis efficiency can be increased quite dramatically. A combination of yield and performance prediction techniques as well as statistically based data analysis can be applied to isolate the actual reason for yield loss. After the yield loss mechanism is isolated, solutions are rapidly proposed and evaluated via simulation until an optimal engineering solution is found to maximize yield while achieving performance targets. Simulation enables multiple solutions for each problem to be examined concurrently in a timely manner, reducing the time and expense of relying solely on lot split experiments (see Fig. 13) [43].

The five components of the analysis streams are as follows: defect monitoring, design analysis, data analysis, process/device parametric analysis and layout/circuit parametric analysis. The design and process/device analyses support the yield prediction while the data analysis isolates the exact signatures of the yield loss mechanisms that affect the product.

Predictive yield modeling is an indispensable capability during the yield ramp phase. This is especially true when multiple yield loss mechanisms may be present including such diverse failure mechanisms as random defects, pattern-dependent effects, within-die process variation and parametric process mis-centering. To help disaggregate the effects of individual root causes on final product yield, we have developed a methodology in which limited-yield prediction is used to provide microscopic observability of physical failure mechanisms. Furthermore, application of this methodology during technology or product development allows designers to anticipate certain types of yield loss and employ appropriate design optimizations.

VI. Future Transistor Design and Manufacturing Challenges

The above discussion has emphasized Moore's Law scaling of intrinsic devices as well as extrinsic and parasitic device scaling issues. Submicrometer device design over the past decade, has illustrated the essential and strategic use of TCAD. However, within the last several years the refinement of the national (US) and now the international technology roadmaps have reached "the red zone" (using a US football term), where future gains are facing greater fundamental challenges in continuing to follow Moore's Law as we know it-planar technology with only one layer of active devices. As device dimensions move below the 0.10 μm (or 100 nm) range with oxides below 25 A, the modeling challenges have changed dramatically. While alternative dielectric materials are under consideration for RAM technology, the integrity of the Si/SiO_2 interface is still the preeminent choice for VLSI. Generally, the scaling of gate dielectrics below 20 A poses fundamental problems in terms of leakage due to direct tunneling.

Challenges in creating shallow junctions and controlling thresholds, compound the problem of gate stack scaling. New degrees of freedom, such as spacers, multilayer (elevated) source/drains, sheet and contact resistance are among the issues to be addressed. Moreover, statistics of dopant distributions resulting from conventional methods of junction formation such as ion implantation are under growing pressure due to constraints of channeling tails and effects of damage. At the same time, alternative doping methods and technologies for junction formation are relatively immature. Similarly, the opportunities for epitaxial and other "atomically layered" structures for doping the channel region or controlling device properties using heterojunctions raise issues of cost in volume manufacturability, vis-a-vis ion implantation.

In spite of these many challenges in the scaling of conventional MOS devices, a number of technology options (primarily as additions to the baseline process) are finding both customers and manufacturers willing to address the process integration issues. Without giving detailed technology or application oriented discussions, it is worth noting SOI-based structures (predominantly for speed/power) and SiGe, based on MOS-compatible bipolar devices (predominantly for wireless), as two prominent examples. It is important to note that potential improvements in some system-level performance parameter are ultimately to be weighed in the context of manufacturability and total product cost.

Opportunities for creating truly atomic scale devices have become increasingly visible over the past decade. In fact, the above discussion of sub-100-nm conventional MOS device

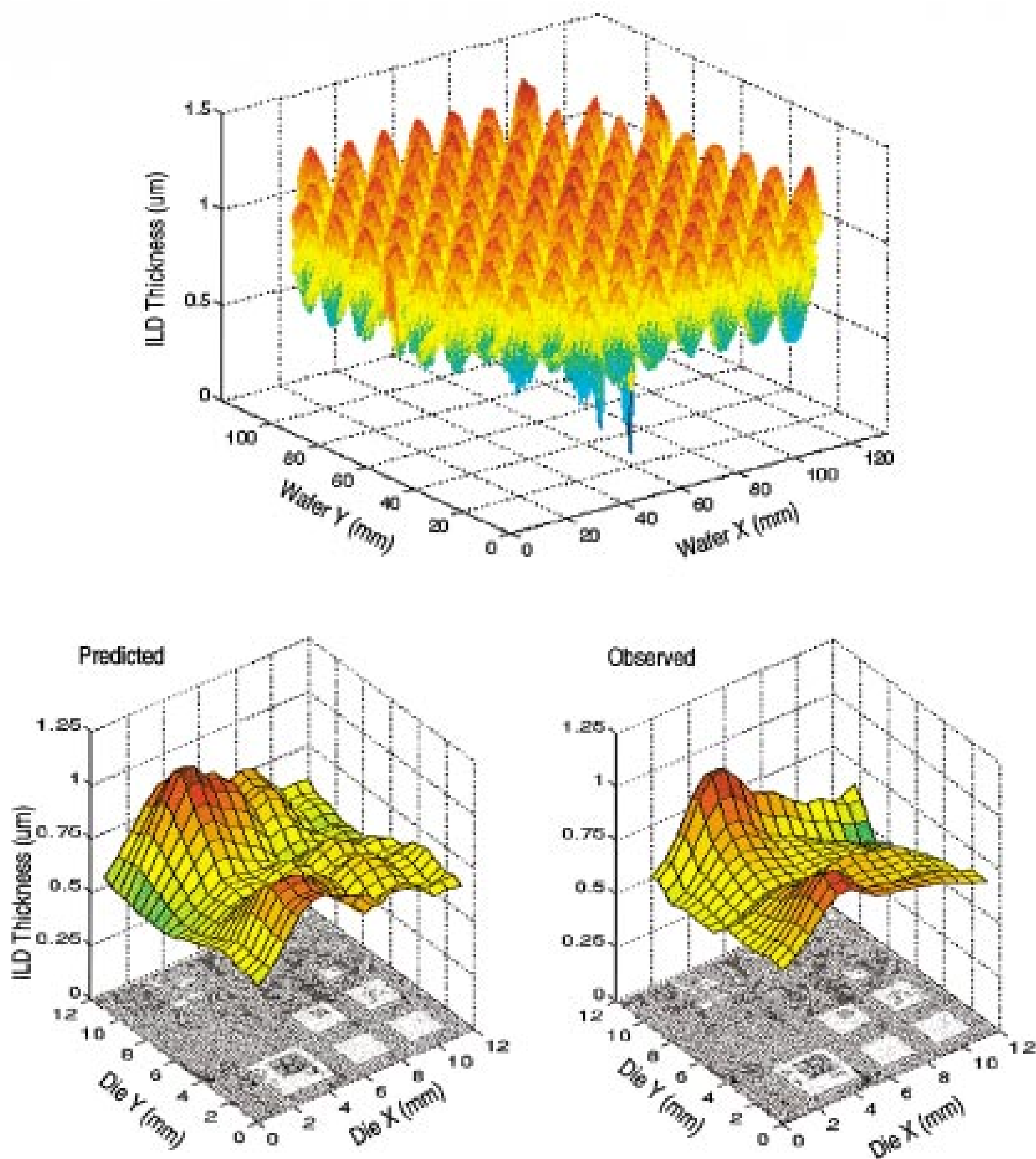


Fig. 12. ILD thickness variations due to CMP.

scaling issues, ultra-shallow junctions and ultra-thin gate stacks already have exposed "the tip of the iceberg." There is a host of competing alternative structures, ranging from atomic-scale dots and nanotubes, to the more conventional pillar type devices, either vertical or in-plane structures. In addition, several interesting options for single electron devices have been demonstrated based on modifications of either channel or dielectric interface properties. These polycrystalline channel structures and atomic scale dielectric effects depend critically on processing conditions of the materials. Again, in looking at this broad spectrum of devices with potential, ultimately the most basic challenges will be manufacturability in concert with the system leverage added by these new components versus the conventional devices that are displaced.

VII. Future of TCAD

The previous sections have discussed the strategic role of TCAD in technology development, both past and future, and a variety of manufacturing challenges that are of preeminent concern in scaling below the 100-nm gate length regime. This section considers tools and technical approaches, methodology in execution as well as supporting research, that are needed to sustain both scaling and SOC integration of heterogeneous technologies. The challenges presented earlier in terms of new materials and their scaling to atomic dimensions move outside the domain where incremental improvements, either in the technology or tools, are likely to be sufficient. There is a growing and critical concern that fundamentally new developments are needed.

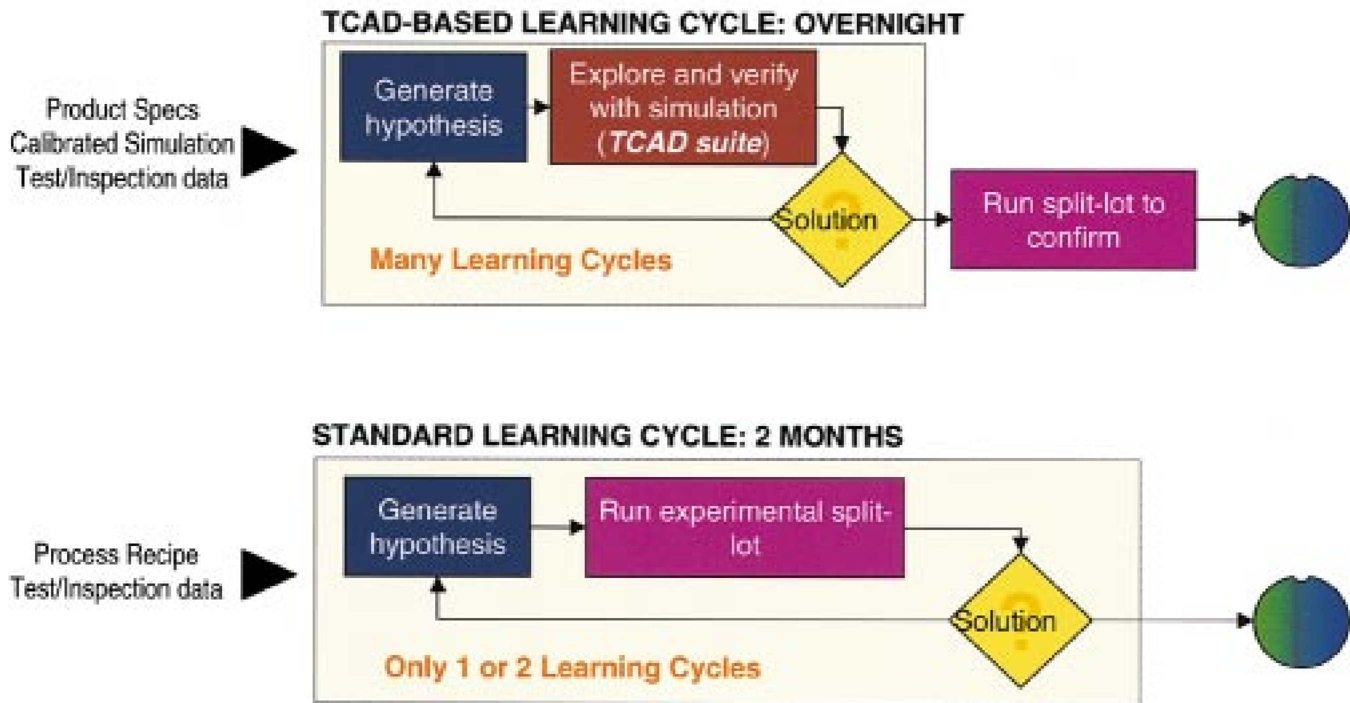


Fig. 13. TCAD-based yield learning cycle.

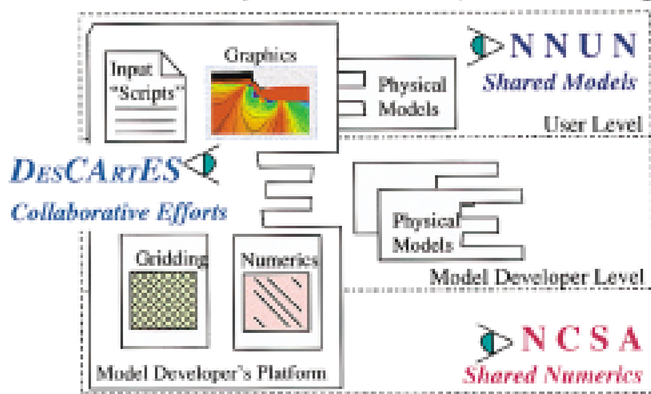


Fig. 14. Collaborative strategy for TCAD development.

In that sense, the need for research and critical (as well as open) discussion is essential. Fig. 14 illustrates one example of both a tool strategy for PDE-based TCAD and distributed, collaborative research efforts that can help sustain technology scaling.

PDE-based models, either for process or device simulation, continue to represent the "work horse" for technology design and scaling. Nonetheless, the numbers of equations needed to represent complex kinetic effects, for example transient enhanced diffusion of dopants or similar multiphysics device effect, can easily reach a dozen or more numerically stiff and highly nonlinear PDEs [57], [58]. There are exciting examples of "dial-an-operator" model developer's platforms, both academic and commercial [59]–[61]. In contrast to the "turn-key" TCAD tools, at present these new environments require still more expert developers, both because of the PDE programming effort and the fact that there is frequently new physics that requires extensive model validation (numerical and experimental). While these requirements pose major challenges, there are exciting examples of where rapid prototyping of fundamentally new models have been achieved and with turn-around times of weeks rather than years (as has been presented as a "roadblock" in the SIA NTRS 97 report about TCAD) [62], [63].

The second aspect of Fig. 14 relates to the collaborative, distributed sets of researchers that are needed to address future generations of TCAD models. Shown in the figure are three levels of modelers/developers: end users (and experimentalists), physical model developers and platform developers (including numerical analysis and computational experts). The acronyms (i.e., DesCArtES, NNUN, and NCSA) represent examples of communities of researchers with interests and activities specifically in each of the respective levels and working on topics that support the broadest venue for future development and application of TCAD [64]–[66].

Fig. 14 emphasizes the challenges of PDE-based modeling; the dominant examples to date have come from the TCAD domains on the scale of a few devices. In fact, the growing challenge is to address technology problems that reach to the die and wafer levels. Earlier discussion of manufacturing challenges such as CMP and etching/deposition have shown such requirements from one point of view. Problems such as signal integrity coming from inductive cross-talk give still another example where analysis complexity poses new challenges for TCAD in the future.

As the device density and operating frequencies increase with each generation of ICs, problems of power dissipation continue to pose both technology- and system-level challenges.

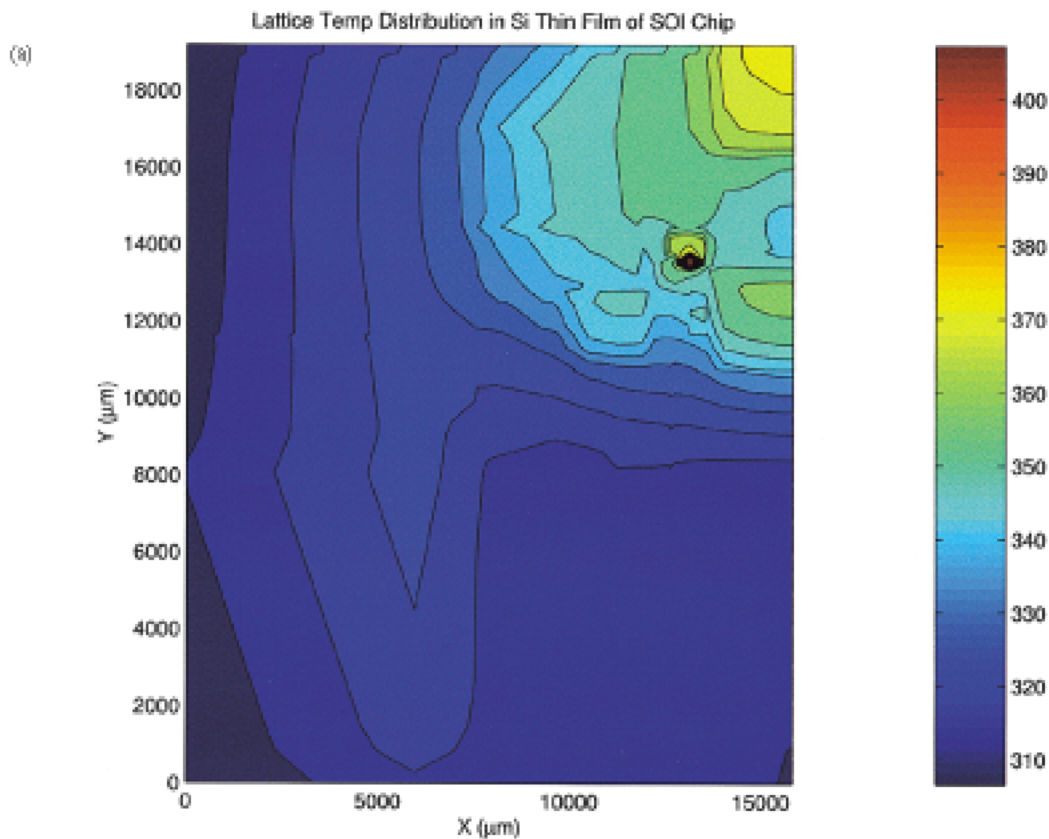


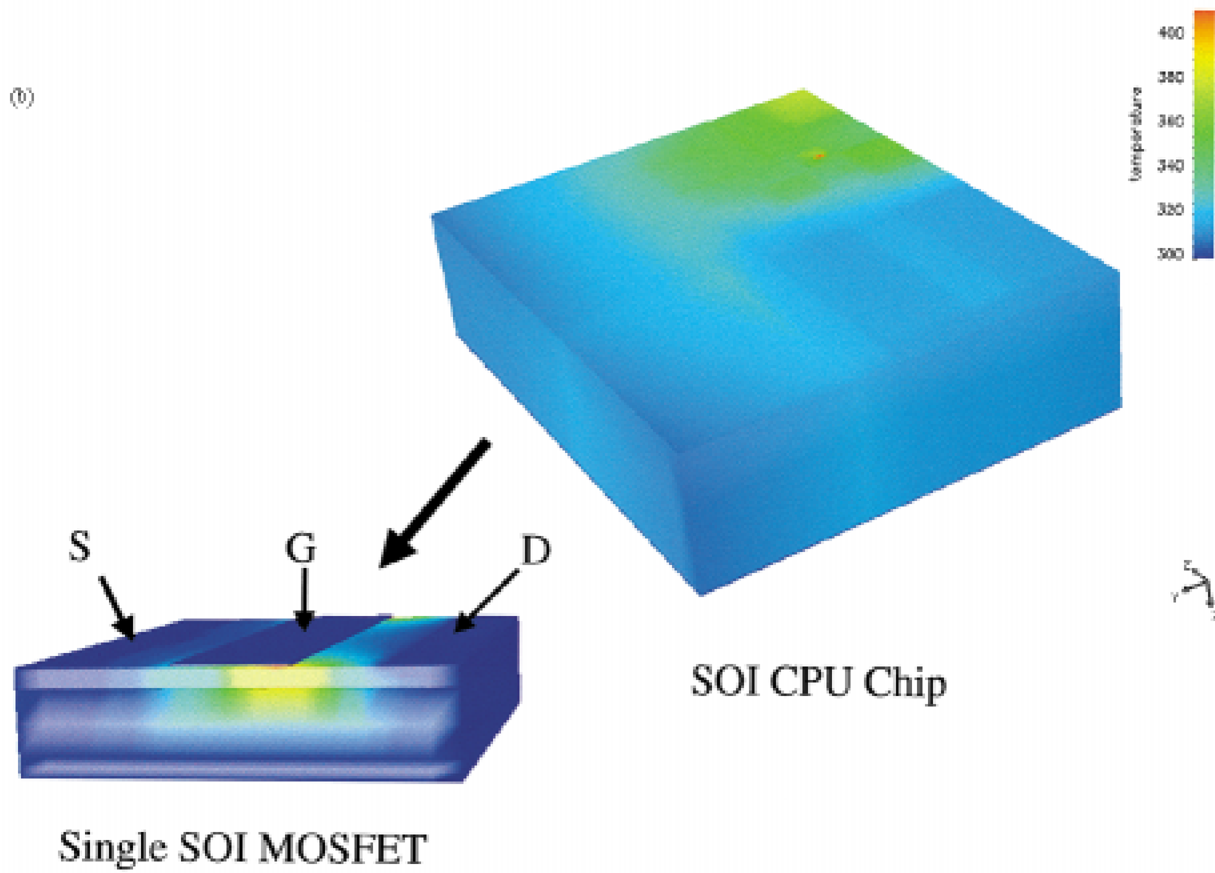
Fig. 15 (a) Simulation of thermal effects.

Fig. 15 shows new simulation results of thermal effects both at the full-chip level as well as at the device level [67]. Fig. 15(a) shows the temperature distribution across a processor-scale block where the heat generation coming from the various cell-level components is coupled with analysis of heat flow (Fourier's Law) in both the interconnect layers and substrate. This in itself represents standard thermal analysis with distributed source terms and their time-dependent coupling to the functional blocks. Fig. 15(b) shows a device-level view of thermal analysis where the electrical analysis (and heat generation) are fully coupled with the thermal analysis. In this case, the device structure involves SOI devices, a technology of growing interest for high-speed applications, where thermal properties in the layers can involve transport properties that deviate from Fourier's Law behavior and require fundamentally new modeling formalism to account for transient and anisotropic effects.

The PDE-based modeling capabilities used to generate both the chip- and device-level results shown in Fig. 15 represent a demonstration of next-generation plug-and-play TCAD tools [61]. The key points to emphasize are: the need for rapid prototyping of complex structures with material-dependent boundary conditions, new physical models that deviate from classical analysis, hence they require a new look at the analysis approach and model extraction for higher level system design. For example, while the emphasis of discussion in this paper has centered on SoC, the integrated solutions at a system level continue to push the frontiers of MCMs, flip-chip bonding and other multichip options. In that context, the requirements for TCAD that crosses the boundaries of both scale- and material-discontinuities in such heterogeneous technologies will only accelerate the challenges and need for further progress along the directions suggested in Fig. 15.

VIII. Conclusion

This paper has presented a vision for technology development, based on projections of new and emerging TCAD tools and methodologies, that offers exciting opportunities in realizing new paradigms for the design-manufacturing interface. The evolution of both TCAD and Moore's Law scaling have a tight relationship; many critical process steps and ability to optimize performance have been strategically leveraged by use of TCAD. Consideration is given to the issues of: what's next in TCAD?; what's next in transistors? and thoughts about re-defining the interface between process and product designers. The new paradigm will be based on a parameterization of the interface which will provide both sides with an understanding of how choices they make effect the overall chip performance, reliability, and yield. As this new interface is created and explored, TCAD tools will find a new relevance in the IC design community. This will create new opportunities for innovation for TCAD research and development engineers. While there are many challenges to overcome in reaching this new level of process co-design (in parallel and concert with product design), solid foundations



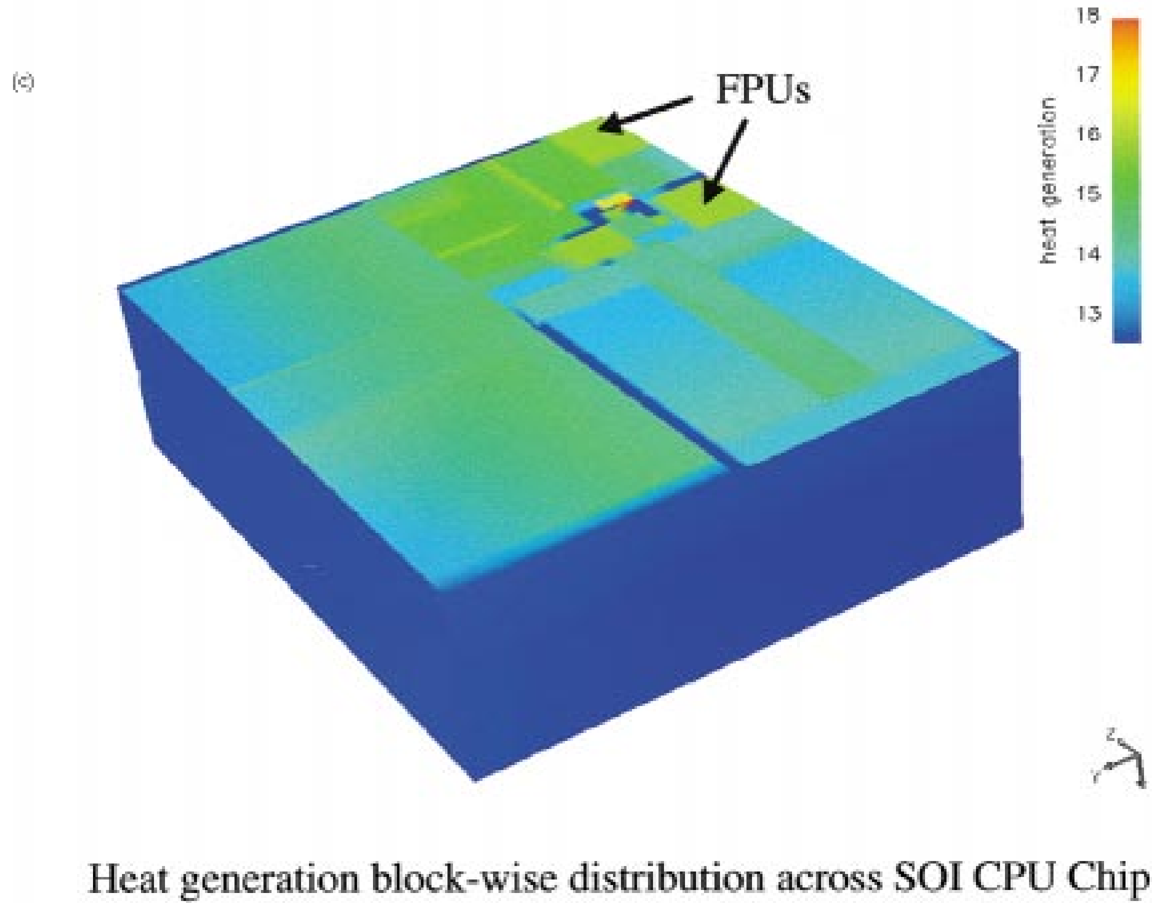


Fig. 15. (*Continued*.) (b) Simulation of thermal effects. (c) Simulation of thermal effects: Heat generation block-wise distribution across SOI CPU Chip.

and evolution of TCAD over the past two decades suggest that such a paradigm shift is achievable. Possibly of equal importance is the application pull requirements for new classes of SoC where heterogeneous technologies are required and the strategic importance of achieving design for manufacturing.

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